Mixed Tunnel-FET/MOSFET Level Shifters: a new proposal to extend the Tunnel-FET application domain

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***Abstract*— In this work, we identify the level shifter for voltage up-conversion from the ultralow voltage regime as a key application domain of tunnel field-effect transistors. We propose a mixed TFET-MOSFET level shifter design methodology, which exploits the complementary characteristics of TFET and MOSFET devices. Simulation results show that the hybrid level shifter exhibits superior dynamic performance at the same static power consumption compared to conventional MOSFET and pure TFET solutions. The advantage of the mixed design with respect to the conventional MOSFET approach is emphasized when lower voltage signals have to be up-converted, reaching an improvement of the energy delay product up to 3 decades. When compared to the full MOSFET design, the mixed TFET-MOSFET solution appears to be less sensitive towards threshold voltage variations in terms of dynamic figures of merit, at the expense of higher leakage variability. Similar results are obtained for four different level shifter topologies, thus indicating that the hybrid TFET-MOSFET approach offers intrinsic advantages in the design of level shifter for voltage up-conversion from the ultralow voltage regime compared to conventional MOSFET and pure TFET solutions.**

***Index Terms*— Tunnel field-effect transistor (TFET), level shifter (LS), technology computer aided design (TCAD).**

I. Introduction

With the growing interest in low energy-budget electronic applications, the tunnel field-effect transistor (TFET) is playing a major role as a new device concept, featuring a better performance/leakage tradeoff than conventional MOSFET at scaled power supply voltage (V_{DD}) levels. Differently from MOSFETs, where the minimum sub-threshold swing (SS) is theoretically constrained to the 60 mV/decade limit at room temperature, TFETs can offer steeper turn-on characteristics due to Band-To-Band Tunneling (BtBT) current [1]. Several mixed device-circuit studies as well as device-circuit co-design strategies have investigated the potentialities of such device concept at both device and circuit levels [2-13].

In today complex system on chips (SoCs), the multi-supply voltage domain (MSVD) technique [14] is emerging as an effective approach to improve energy efficiency. The MSVD technique consists of partitioning the design into separate voltage domains (or "voltage islands"), each operating at a proper supply voltage level depending on its timing requirements. Time-critical domains run at higher power supply voltage (V_{DDH}) to maximize the speed, whereas noncritical sections work at lower supply voltage (V_{DDL}) to optimize energy consumption, thus effectively managing tasks that require substantially different performances. Minimizing the delay and energy overhead of level conversion between different voltage domains is a key challenge in the design of effective multi-supply SoCs, becoming particularly critical when the number of power domains and/or the data width in the SoC increase [15]. Within this context, several level shifter (LS) circuit topologies were recently proposed for speed- and energy-efficient wide-range conversion from the deep sub-threshold regime up to the nominal supply voltage level [16-21].

In this work, we propose a mixed TFET-MOSFET LS design methodology, which exploits the complementary characteristics of TFETs and MOSFETs for voltage up-conversion. Among several mixed device/circuit works, only few of them have proposed and investigated mixed TFET-MOSFET solutions (e.g. hybrid SRAM cells [10,11]). Our work hinges in this context with the aim of identifying an additional area of application where the mixed TFET-MOSFET design can be an added value.

The remainder of the paper is organized as follows. Section II discusses the design and the main characteristics of the devices considered in this work. Section III introduces the analyzed LS circuit topologies alongside with the adopted simulation methodology. Comparative simulation results are discussed in Section IV. Finally, Section V concludes the paper.

Manuscript received July 31, 2015. This work was supported in part by the European Community's Seventh Framework Program under Grant Agreement 619509 (Project E2SWITCH).

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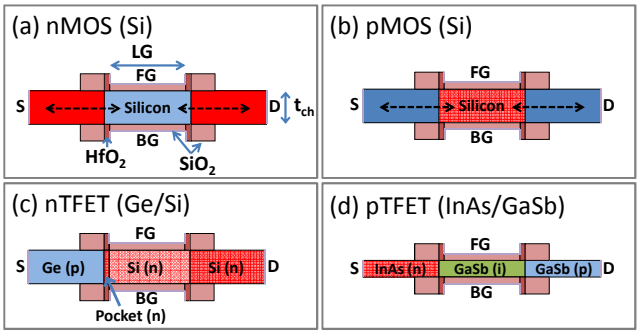

Fig.1. Structures of n-type MOSFET (a), p-type MOSFET (b), n-type TFET (c) and p-type TFET (d). Doping levels: MOSFETs: $N_{Source/Drain} = 10^{20}$ cm^{-3}, $N_{Channel} = 10^{17}$ cm^{-3}. nTFET: $N_{Source} = 2{\cdot}10^{19}$ cm^{-3}, $N_{Pocket} = 5{\cdot}10^{18}$ cm^{-3}, $N_{Channel} = 10^{17}$ cm^{-3}, $N_{Drain} = 10^{19}$ cm^{-3}. pTFET: $N_{Source} = 2{\cdot}10^{18}$ cm^{-3}, intrinsic channel, $N_{Drain} = 10^{19}$ cm^{-3}. Dimensions: L_G = 30 nm. t_{Ch}=10 nm (except t_{Ch} = 5 nm for the InAs/GaSb pTFET).

II. Device Design and Device Level Models

Ideal double-gate SOI geometries designed in [8] are used in this work as a reference for the conventional MOSFET devices, featuring a SS close to the 60 mV/dec theoretical limit. As a counterpart, hetero-junction TFETs featuring a SS below the 60 mV/dec have been designed. The same structure of MOSFETs (double-gate SOI with L_G = 30 nm and EOT = 1.1 nm) was taken as a base in the definition of complementary TFETs, while the choice of the hetero-structure materials and channel thickness was driven by some constraints imposed by the particular circuit application, as will be shortly discussed in the following.

It is well known that TFETs can outperform MOSFETs only at very low V_{DD} (V_{DD} < 0.4 V) [6-12], that is in circuit applications where they can take advantage of their steep transition from the off- to the on-state. Recent works [7,9,12], based on device simulations with a more accurate description of the device physics with respect to the TCAD modeling level, claimed that III-V materials provide the opportunity to achieve both steep turn-on operation and on-current comparable with MOSFET up to a V_{DD} of 400 mV. GaSb/InAs hetero-structure, in the presence of a suitable amount of transverse quantization (e.g. quantum wells with thickness ~ 5÷7 nm), has been proposed to implement both n- and p-type TFET devices [12,13], possibly with a slight Al concentration in the GaSb (e.g. $Al_{0.05}Ga_{0.95}Sb$) [7].

In the p-type TFET implementation, InAs is used for the source region, whereas (Al)GaSb is employed in the channel and drain regions. Although the complementary hetero-structure could be used to implement also the n-type TFET, due to relatively low band-gap of the InAs (~ 0.5 eV [4], including quantization effects), it features a strong ambipolar leakage as the V_{DS} is increased [12,13]. Being a V_{DS} up to 1V a key requirement of the LSs here discussed, InAs/GaSb hetero-junction has been used only to implement the pTFET. For the nTFET, germanium (Ge) / silicon (Si) hetero-junction is proposed. The low band-gap Ge is used in the source region to ensure large BtBT rates, whereas Si is employed in the

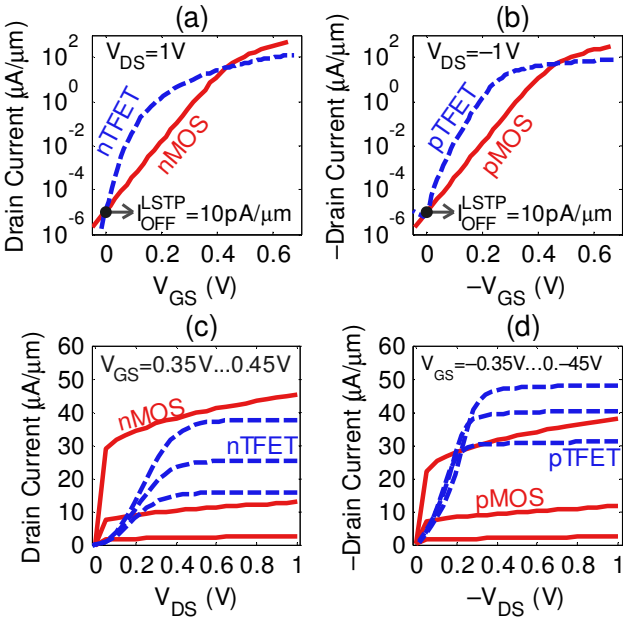

Fig.2. I_D-V_{GS} characteristics at $|V_{DS}|$ = 1 V of the considered n-type (a) and p-type (b) devices. I_D-V_{DS} characteristics of the n- (c) and p-type (d) devices ($|V_{GS}|$ = 0.35 V, 0.4 V, 0.45 V).

channel-drain regions to ensure a sufficient robustness against ambipolar leakage. Although the integration of III-V materials and Ge-on-Si CMOS substrate can be a challenging task, it has been already successfully explored in [22] with the integration of III-V nMOSFETs together with Ge pMOSFETs.

The TFET design has been performed with Sentaurus TCAD, starting from the reference MOSFET structure [8] and by choosing appropriate materials (and the related parameters) and doping levels to get complementary n- and p-TFET devices featuring sufficiently symmetric I-V characteristics. BtBT has been simulated with the *dynamic non-local path BtBT model*. Material parameters, such as the energy gap E_G and electron affinity χ, conduction and valence band density of states (N_C^{DOS} and N_V^{DOS}), BtBT model constants (*Apath*, *Bpath*, *Rpath)* have been calibrated against experimental data for the Ge-source nTFET [5] and against atomistic simulations for the InAs/GaSb pTFET [4,13].

Materials and doping levels are reported in Fig.1 for all the considered devices. The thickness of the pTFET is set to 5 nm, since the physical parameters [13] (band-gap, tunneling-rate, etc.) calibrated on the device published in [4], can be considered trustworthy only for a device with the same thickness.

Fig.2 show the I-V characteristics of the four devices depicted in Fig.1. In Fig.2a-b, the I_D-V_{GS} characteristics are aligned – through a fine tuning of the metal gate work-function of any single device – to get the same normalized off-current, taking as target the value suggested by the ITRS for *low standby power* applications (I_{OFF}^{LSTP} = 10 pA/μm). For the chosen I_{OFF}, TFETs feature larger on-current than the corresponding MOSFETs up to a V_{GS} of ~ 400÷450 mV. Fig.2c-d shows the superliner output characteristics of TFETs along with the ones of the corresponding MOSFETs. The

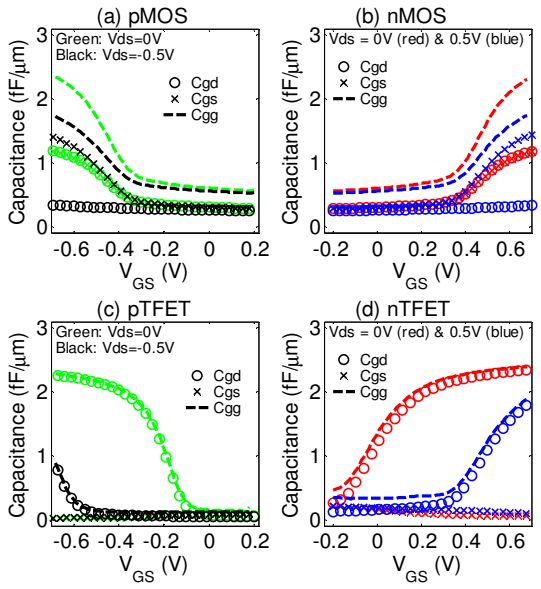

Fig.3. Gate capacitances versus V_{GS} for the (a) p-type MOSFET, (b) n-type MOSFET, (c) p-type TFET and (d) n-type TFET.

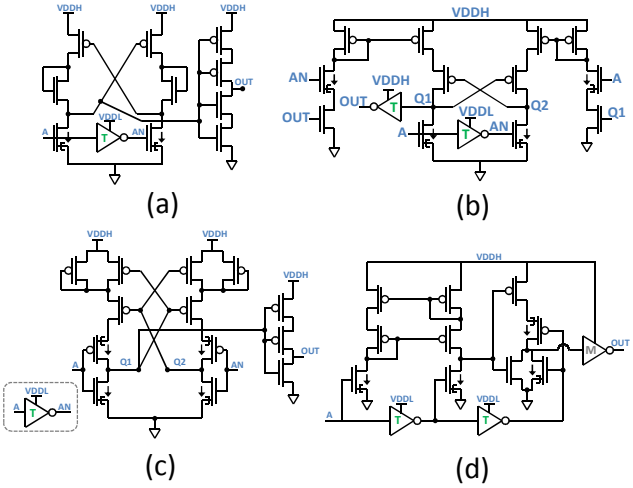

Fig.4. Mixed TFET-MOSFET LS design version of circuits reported in (a) [18], (b) [19], (c) [20] and (d) [21]. The "T" and "M" labels on the inverters mean all TFET and all MOSFET implementation, respectively. "A" and "AN" are the input signal and its inverted version.

delayed turn-on behavior of TFETs is well known in the literature [2,3] and it has been shown that it degrades the inverter voltage-transfer-characteristic (VTC) and negatively impacts any CMOS-like logic gate [6-8]. Conversely, when the V_{DS} increases above 500 mV, TFET output characteristics show a flatter current than MOSFETs as a result of the higher robustness of the designed TFETs against the short-channel effects.

Capacitance characteristics are reported in Fig.3 for $|V_{DS}|$ = 0 V and 0.5 V. Due to symmetric geometry, in MOSFETs the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}) are overlapped (for any V_{GS}) when V_{DS} = 0 V, whereas C_{GS} becomes the main contribution to the overall gate capacitance (C_{GG}) when the device is switching on (i.e. as V_{GS} and V_{DS} are increased). On the contrary, the TFET C_{GG} is dominated by the C_{GD}. Interestingly, as V_{DS} increases, the onset of the rising C_{GD} with V_{GS} is shifted toward larger V_{GS} [8]. Due to convergence limits, the BtBT model was not activated in the AC analysis performed to generate the C_{GS} and C_{GD} characteristics. However, since the charge produced by the BtBT is not large enough to influence the device electrostatics (i.e. to modify the shape of the band diagrams), the impact of such simplification in the computed C_{GS} and C_{GD} is negligible.

III. Level Shifters: Benchmarks and Simulation Methodology

In this Section, the LS circuit topologies referenced in this work are briefly discussed. After that, the circuit simulation methodology is detailed.

A. Circuit Description

Four of the most recent and efficient LS designs [18-21] were considered as case study. For each LS design the conventional MOSFET, the pure TFET and the mixed TFET-MOSFET (shown in Fig.4) implementations were considered. In the mixed TFET-MOSFET designs, only the MOSFETs directly driven by the low-voltage signals are replaced by TFET devices.

The key feature of the circuit proposed by *Zhao et al.* [18] (shown in Fig.4a) is the use of two NMOS-diodes to limit the current drawn by the opposing pull-up network (PUN) during the discharge of internal nodes (either Q1 or Q2). A similar achievement is obtained in the LS circuit proposed by *Hosseini et al.* [19] (depicted in Fig.4b) through the use of two current generators. The design proposed by one of the authors of this work [20] (shown in Fig.4c), exploits a different idea based on self-adapting PUNs to speed-up both high-to-low and low-to-high transitions of internal nodes Q1 and Q2. Finally, the circuit proposed by *Luo et al.* [21] (shown in Fig.4d), is based on a hybrid structure comprising a modified Wilson current mirror and a NOR CMOS logic gate to achieve effective voltage up-conversion while limiting stand-by power consumption.

B. Simulation methodology

Although it is possible to describe with the TCAD simulator simple circuit topologies implemented with few devices in the mixed device/circuit mode [11], the computation time becomes unacceptable when the number of devices increases up to approximately 10 (note that this number is strongly influenced by the complexity of the single device mesh and by models activated in the TCAD simulator). Furthermore, the model used in this work to take in account BtBT (i.e. the most physically accurate BtBT model available today in the TCAD simulator, the *dynamic non-local path BtBT*) shows poor convergence properties in the mixed-mode environment as well as in AC or transient simulations. For this reason, we have restricted the use of the TCAD simulator only to design the devices and to generate Look-Up Tables (LUT), in a defined

range of V_{GS} and V_{DS}, with drain current (I_D) and capacitances (C_{GS} and C_{GD}) characteristics. Concerning the circuit level, *Cadence* has been used for time-efficient simulations by defining black-box devices in the Verilog-A description language. Such solution has allowed us also to perform (in a reasonable time) a statistical analysis of the effects at circuit level due to threshold voltage variability.

In our simulations, all the circuits are driven by an identical inverter in order to duly take into account the input gate capacitances of TFET and MOSFET devices. Additionally, output of the circuits drives a capacitance of 20 fF, which is a fairly conservative loading value, given that the input capacitance of a minimum-size inverter is ~ 0.2 fF.

The referenced MOSFET designs have been sized to achieve the minimum energy delay product (EDP) for 0.3 V to 1 V voltage conversion and considering a 500 kHz input pulse. In TFET-based circuits, TFET devices maintain the same sizes of replaced MOSFETs to assure similar leakage targets (as discussed in Section II, we set the same I_{OFF} for both MOSFETs and TFETs).

IV. Results and Discussion

This Section presents the simulation results performed on the various LS implementations. In order to facilitate the discussion and to drive the reader toward the main goal of this work (i.e. showing the potentialities of the hybrid design with respect to the conventional MOSFET and full-TFET design strategies), only the results related to the topology proposed in [20] will be initially discussed in detail, focusing on the specific features of the three possible device implementations (i.e. MOSFET, full-TFET and mixed TFET-MOSFET); the impact of device variability will be presented too. Afterwards, the potentiality of the mixed solution will be investigated in the full range of topologies discussed so far, in order to show that the achievements are mostly independent on the particular circuit topology.

A. *Dynamic figures of merit*

Fig.5 illustrates the transient behavior of the LS circuit initially proposed in [20]. It is easy to observe that when TFETs are used to replace MOSFETs driven by the low-voltage signals, the current contention at discharging internal nodes (either Q1 or Q2) is greatly reduced due to the higher switching currents carried by the TFETs which cause the positive feedback to be triggered faster. Note that the switching speed of the pure TFET solution is favored by the increased drive strength of the pull-down networks (PDNs) in discharging internal nodes (as occurs for the mixed TFET-MOSFET circuit) but, at the same time, this effect is in part jeopardized by the slower rising voltage transition on the charging internal node due to the reduced drive strength of the pTFET-based PUNs.

It is worth pointing out that the faster switching allows for a significant reduction of the short-circuit current (and consequently energy consumed per transition) occurring during the change of the state of the LS. This is particularly

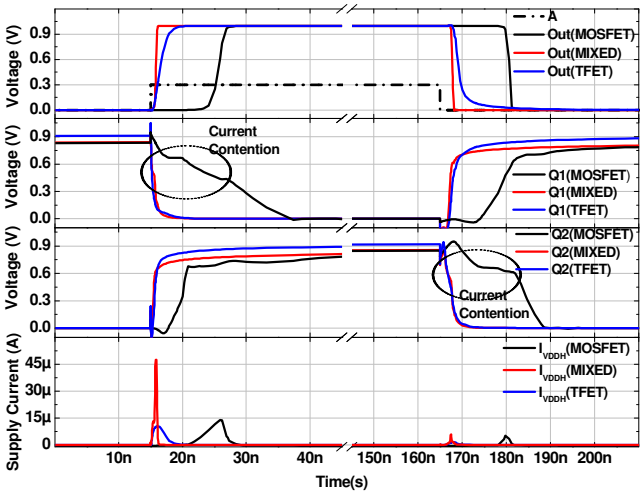

Fig.5. Transient behavior of the circuit in [20] (Fig.4c).

crucial when the input signal has slow slew rate and ultralow voltage level.

The impact on energy and delay of the conventional MOSFET, pure TFET and mixed TFET-MOSFET options is better quantified in Fig.6 (data are given in Table I). In this analysis, V_{DDL} ranges from the deep sub-threshold regime to 0.6V, whereas the V_{DDH} is fixed to 1V.

The higher switching current and the better SS of TFETs considerably improve the speed of the TFET-based circuits for the lower input voltages. As an example, for a 0.2 V input signal the pure TFET solution reduces the delay more than 6X in comparison to the conventional MOSFET design. For the same voltage conversion operation, the hybrid design, which benefits of both the merits of TFETs (i.e. strengthened PDNs) and MOSFETs (faster triggering of the positive feedback in the PUNs), achieves even higher speed advantages, thus resulting to be faster than 2X and 12.5X in comparison to the pure TFET and conventional MOSFET implementations, respectively. Note also that the effective voltage range for improved speed of the mixed TFET-MOSFET LS is broadened in comparison to the only-TFET solution. Only when the input voltage level becomes higher than ~ 0.4 V the conventional MOSFET solution attains the best dynamic performance.

TFET-based solutions also achieve better energy results for V_{DDL} up to about 0.4 V, mainly due to the reduced short circuit current. The weaker PUNs of the pure TFET design are favorable from the energy point of view when the input voltage level is extremely low. On the contrary, as the input voltage level increases above approximately 0.3 V, the weaker PUNs negatively impact the short circuit current occurring during the switching of the LS. The hybrid solution exhibits energy consumption close to the minimum over the whole considered input voltage range.

Fig.6c shows that the combined reduction in terms of delay and energy leads the mixed TFET-MOSFET circuit to achieve the best Energy-Delay-Product (EDP) results for V_{DDL} less than ~ 0.4 V (i.e. about three orders of magnitude at V_{DDL} =

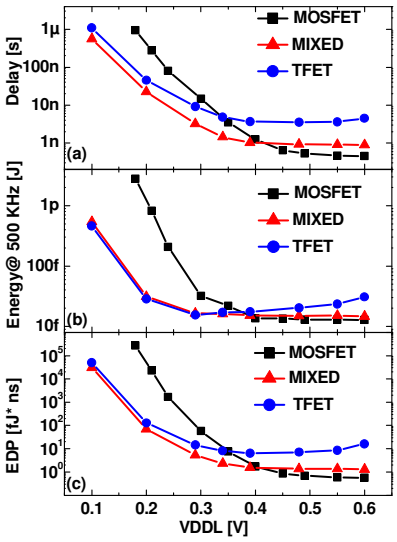

Fig.6. Dynamic performance versus V_{DDL} (@ V_{DDH} = 1V) for the LS proposed in [20] (Fig.4c): (a) worst case delay , (b) average energy-per-transition (@ 500 kHz) and (c) energy-delay product.

0.2 V), whereas, for higher input voltage levels, the MOSFET design shows only marginal EDP improvements over the mixed solution (less than 5% at V_{DDL} = 0.6 V).

B. Impact of device variability

Work-function variation (WFV), the Line Edge Roughness (LER) and the Random Dopant Fluctuations (RDF) are considered as the leading sources of variability for both MOSFET and TFET devices [12, 23-26]. Due to computational time and resource constraints, a rigorous variability analysis at both device and circuit level is essentially unfeasible, because it would require the generation of a statistically meaningful number of device instances through the TCAD simulator (and the corresponding LUTs for the I-V and C-V curves) to be used in Monte Carlo (MC) simulations performed at the circuit level. Thus, in our work we consider only WFV. The effect of this source of variability is projected on dynamic and static characteristics of the circuits by 150 runs MC simulations, performed modeling the threshold voltage (V_{th}) variation with a gaussian distribution with a standard deviation obeying to the Pelgrom's law, where A_{Vth} = 1 mV·µm was assumed [27].

The variation on V_{th} has been modeled at the circuit simulator level, by adding a DC voltage generator in series with the gate of each transistor, whose voltage is randomly determined at any run of the MC simulations. This allows one to use only the Verilog-A LUTs with the characteristics of the nominal devices (i.e. only one set of I_D-V_{GS}-V_{DS}, C_{GD}-V_{GS}-V_{DS} and C_{GS}-V_{GS}-V_{DS} for any device type), since the considered variability effect is a pure horizontal shift in V_{GS} of the characteristics. This is a simplified view of WFV, since more accurate models require the generation of sample devices with random distribution of gate metal grains [23-25]. As said above, this is not feasible for complex circuits using LUTs.

Fig.7 compares the normalized spreads of EDP and static power for MOSFET, mixed and pure TFET configurations. The MOSFET circuit exhibits lower variability in terms of static behavior (static power) and higher variability in terms of dynamic behavior (EDP) with respect to pure TFET and mixed circuits. As reported in Table II, the larger EDP spread of the MOSFET implementation is a consequence of higher variability of the dynamic figures of merit: energy and delay. The observed different variability of static and dynamic parameters can be ascribed mainly to the different normalized slope of the I_D-V_{GS} characteristics (g_m/I_D, where $g_m = dI_D/dV_{GS}$) of MOSFETs and TFETs. From the transfer characteristics in Fig.2a-b, it is evident that TFETs exhibit a higher g_m/I_D than MOSFET counterparts at V_{GS} close to 0 (corresponding to the better SS) and a lower g_m/I_D than MOSFETs for V_{GS} higher than about 300 mV. We thus infer that the higher variability of static parameters and the lower variability of dynamic parameters are intrinsic properties of all TFET-based circuits and not specific properties of the LS topology.

C. Impact of the circuit topology

In this subsection, the impact of different circuit topologies is evaluated considering both mixed TFET-MOSFET and conventional MOSFET solutions. Since the pure TFET implementation has never proved to be the most competitive solution in the above-analyzed operating conditions, it was excluded from the comparative analysis described in the following.

Table I shows the characteristics of the analyzed LS designs for voltage up-conversion from 0.3 V to 1 V of a 500 kHz input pulse. In this operating condition, the mixed TFET-MOSFET solutions perform significantly better than their conventional MOSFET counterparts. More precisely, the delay is reduced from 5.7 times (for the circuit proposed in [20]) to 7.2 times (for the LS described in [18]). At the same time, energy per operation is more than halved for almost all the circuit topologies. In addition, slight improvements in terms of stand-by power are observed. Interestingly, the significantly higher driving current of TFETs allows for a reduction of the minimum voltage level $V_{DDL}^{min,500kHz}$ (evaluated as the minimum voltage allowing a successful up-conversion to 1 V of a 500 kHz input pulse) in the deep sub-threshold domain.

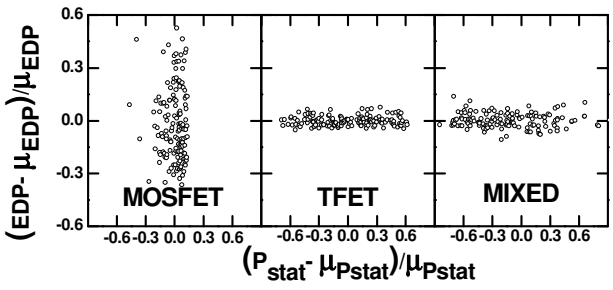

Fig.7. EDP-P_{stat} plots from Monte Carlo simulations for V_{DDH} = 1 V and V_{DDL} = 0.3 V, considering the LS proposed in [20] (Fig.4c).

TABLE I
FIGURES OF MERIT FOR DIFFERENT LS TOPOLOGIES
(V_{DDH} = 1 V, V_{DDL} = 0.3 V, FREQ = 500 KHZ)

Design	Delay [ns]	Energy [fJ]	EDP [fJ*ns]	I_{leak} [pA]	$V_{DDL}^{min,500kHz}$ [mV]
[18] MOSFET	12.9	45.2	583.1	36.7	160
[18] MIXED	1.8	18.4	33.1	30.8	70
[19] MOSFET	13.8	68	938.4	130	140
[19] MIXED	2.2	15.3	33.6	13.1	120
[20] MOSFET	18.1	32.1	581	10.3	180
[20] MIXED	3.2	16.5	52.8	6.01	100
[21] MOSFET	19.3	24.4	470.9	6.18	170
[21] MIXED	2.5	12.9	32.2	6.35	110

TABLE II
VARIABILITY RESULTS FOR THE VARIOUS LS TOPOLOGIES
(V_{DDH} = 1 V, V_{DDL} = 0.3 V, FREQ = 500 KHZ)

Design	Delay			Energy			I_{leak}		
	μ [ns]	σ [ns]	σ/ μ	μ [fJ]	σ [fJ]	σ/ μ	μ [pA]	σ [pA]	σ/ μ
[18] MOSFET	13.8	3.5	0.25	47.3	8.9	0.19	16.4	4.6	0.28
[18] MIXED	2.5	0.2	0.08	18.7	0.7	0.04	11.3	4.4	0.39
[19] MOSFET	14.3	3.1	0.22	90.4	7.9	0.09	144	50	0.35
[19] MIXED	2.3	0.4	0.17	15.6	0.9	0.06	14.9	7	0.47
[20] MOSFET	18.9	3.1	0.16	32.2	3.5	0.11	8.6	0.9	0.10
[20] MIXED	3.2	0.1	0.03	15.9	0.3	0.02	8.7	5.5	0.63
[21] MOSFET	19.5	3.7	0.19	25.6	2.8	0.11	4.5	0.5	0.11
[21] MIXED	1.8	0.1	0.06	12.7	0.2	0.02	3.3	0.6	0.18

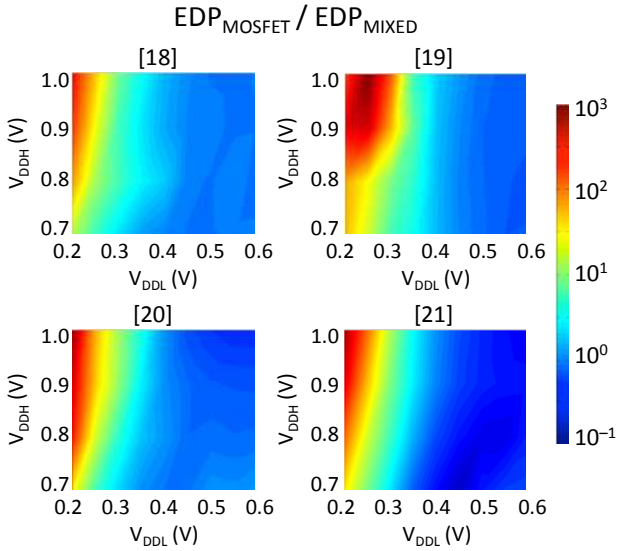

Fig.8. EDP of MOSFETs vs. mixed solution as a function of V_{DDH} and V_{DDL}.

Fig.8 shows the EDP ratio between MOSFET and mixed circuits in the entire voltage range investigated in this work, that is V_{DDL} ranging from 0.2 V to 0.6 V and V_{DDH} ranging from 0.7 V to 1 V. Due to significant reduction in terms of both delay and energy, the mixed solutions improve the EDP parameter up to two orders of magnitude for lower V_{DDL} and higher V_{DDH} with only negligible losses for higher V_{DDL} and lower V_{DDH} (i.e. when the required voltage conversion ratio V_{DDH}/V_{DDL} is significantly reduced).

Table II provides MC comparison data obtained using the above described simulation methodology. From the given results, the dynamic parameters of the mixed TFET-MOSFET circuits appear to be more robust against V_{th} random variations than those of the correspondent MOSFET solutions, at the expense of higher leakage variability. This result is in agreement with the arguments discussed in Section IV-B.

Table III reports the impact of the V_{th} variability on the minimum V_{DDL} (V_{DDL}^{min}) that can be successfully up-converted to 1V. To evaluate V_{DDL}^{min}, we set V_{DDH} to 1 V,

TABLE III
MC ANALYSIS OF THE MINIMUM V_{DDL}
FOR SUCCESSFUL UP-CONVERSION TO 1V

Design	μ [mV]	σ [mV]	μ + 3σ [mV]
[18] MOSFET	46.7	17.3	98.5
[18] MIXED	29.3	10.0	59.2
[19] MOSFET	46.2	22.1	112.6
[19] MIXED	40.5	20.7	102.7
[20] MOSFET	52.4	22.0	118.4
[20] MIXED	34.4	16.2	83.1
[21] MOSFET	45.5	23.4	115.6
[21] MIXED	44.1	19.0	101.0

swept V_{DDL}, and measured the minimum input voltage level that produced a correct up-conversion to V_{DDH} , for each MC run [28]. It can be easily seen that the MIXED LS designs always allow dependable level up-conversion from lower V_{DDL} voltage compared to their MOSFET counterparts (i.e. the extreme μ+3σ V_{DDL} value is always lower for MIXED designs).

In this paper, we have benchmarked circuit topologies and design strategies focusing on energy and performance figures of merit without taking into account the area occupancy. For the sake of clarity, we want to point out that the fabrication of TFET devices is still immature, so that layout rules do not exist yet. It is thus very difficult to give a quantitative estimation of the area of the investigated circuits. In this respect, we have used devices with the same length and width to make the comparison as fair as possible. However, the integration of the mixed TFET/MOSFET implementations is likely to result in an area penalty with respect to the full MOSFET and pure TFET implementations, due to the need for a larger number of wells to accommodate devices implemented exploiting different materials.

V. CONCLUSIONS

This device-circuit co-design study demonstrates the potentialities of TFET device for the implementation of LS for voltage up-conversion from the ultralow voltage regime. We

propose a mixed TFET-MOSFET strategy of LS design, based on the introduction of TFET devices in the low supply circuit sections. The mixed LS exhibits superior dynamic performance at the same static power consumption than conventional MOSFET and pure TFET solutions. Compared to conventional MOSFET implementation, the mixed solution offers an improvement of the energy delay product up to 3 decades and allows minimum voltage level for successful up-conversion to be extended towards significantly lower values. The hybrid LS exhibits lower variability of dynamic parameters, but higher variability in terms of static behavior with respect to conventional MOSFET counterpart. The study on four different topologies confirms that the design of LSs for voltage up-conversion from the deep-voltage regime is intrinsically suitable for a mixed TFET-MOSFET implementation.

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