Mobile Robot Framework Designing and Transferring of Data by PCI Controller

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ABSTRACT

In this paper, a differential robot is designed and controlled by PCI card. This card connected between personal computer and microcontroller. Furthermore PID controller was designed by A sic device and implemented on robot. In this paper, instead of using that massive hardware's, it designed a single FPGA chip to perform the same motion control of robot wheels. We developed a general purposed motion control of robot using a field programmable gate array (FPGA). In order to obtain independent robots movement, the main PID controller is implemented with a Field Programmable Gate Array. The main PID controller routine was designed to be fairly general purpose and modular form. While it is used to control a DC motor, it could be re-deployed to other situations where some parameter has to be controlled to a set value under varying conditions. The actual control software is located in a single function and its major inputs and output are held in a structure. Although it was designed originally for a specific job it is really only intended as an example of the basic techniques involved and to allow those with no control system knowledge to experiment with a simple PID system.

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1. INTRODUCTION

The emergence of reconfigurable Field Programmable Gate Arrays (FPGA) has given rise to a new platform of complete Mobile robot control system. By using FPGA devices, the designer may tailor the design to fit the requirement of control system functions for a mobile robot. General-purpose computer can provide acceptable performance for mobile robot control when the tasks are not too complex. While a single processor system cannot guarantee real time response for any task when the complexity of tasks have been increased[1-3], a FPGA-based control system is designed to solve the platform of parallel tasks to achieve control precision.

A FPGA-based robot control chip improves upon the single processor computer in following areas:

1. Scalability of the control system. A FPGA chips can integrate and perform the pervious defined tasks efficiently, especially when more tasks achieving are required.
2. Increase the availability of I/O channels.
3. Directly map the logical designed to the computing elements in FPGA devices.
4. Support parallel design scheme which leads itself to guarantee the control response time, realtime.
5. Low power consumption can be compared to the single processor computer or even the micro-controller.

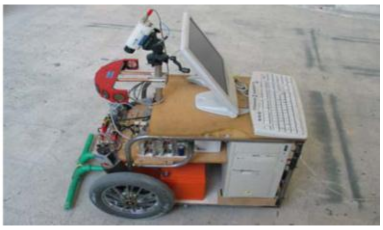


Figure 1. Previous Robot.

In our previous researches, we have built the robot hand system that uses 80196KC micro controllers and ISA card. It requires a serial communication box to communicate micro controllers with a PC or need ISA CARD. The overall system is shown in figure1 and the whole system appears to be bulky [4-6].

In this paper, instead of using that massive hardware's, it designed a single FPGA chip to perform the same motion control of robot wheels. We developed a general purposed motion control of robot using a field programmable gate array (FPGA). The FPGA is known as a programmable hardware device that a user can design his/her algorithms and download it to a single chip. By using the high modifiable capacity of a FPGA, the additional hardware such as an encoder counter and a PWM generator can also be implemented in a single FPGA device.

As a result, the total controller size and power dissipation are effectively reduced by using a FPGA motion controller. Experimental results show that the robot, follows the desired speed trajectories [7-9].

2. OVERALL SYSTEM

The new designed system block diagram of robot control is shown in Figure 2.It consists of robot, a FPGA controller, PCI Card, a motor driver, and a PC.

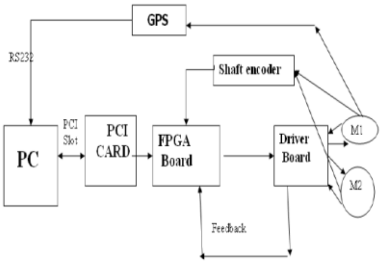
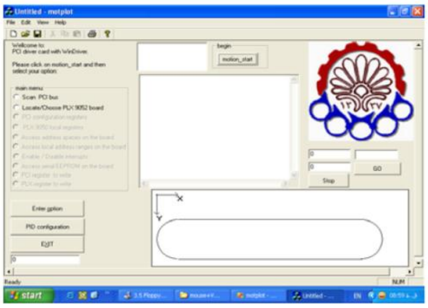


Figure 2. Overall Structure of Robot

Difference between of the previous model and new design is shown in figure 1, where a FPGA is replaced for several MCUs or ISA card. The PC communicates to PCI card through a PCI slot. The PCI card communicates with a FPGA chip to transfer desired speed and controller gains at each sampling time. The FPGA chip programmed or PID controller generates PWM signals to motor drivers. Then each motor is actuated and each motor's encoder measurement is transferred to FPGA chip for making positional errors.
We also developed a PC GUI program for an efficient interface control between a motor and a PC.

The GUI has several functions such as setting of PID control parameters, downloading of the trajectory, displaying the control states, and so on. A user can specify PID controller gains through GUI program in PC. Those gains are transmitted though a PCI communication to a PCI card with Win driver function. And then its end them to a FPGA.

The interfacing GUI program helps the users to manipulate controller's gains and to observe the response of each motor. Figure 3 and 4 shows the GUI window that has many functions.
Each part has the following function:
1-Motion control part (start, stop)
2-PID gain selection
3-Trajectory planner
4-Motors Selection
5-Diagniose of PCI card



Wellcome to:
PCI driver card with WinDriver.

Please click on motion_start and then select your option.

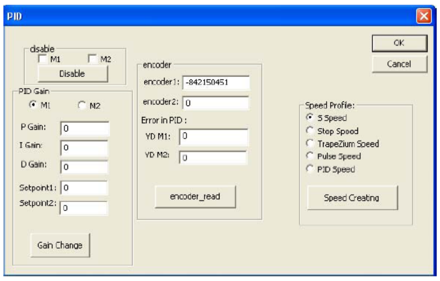
Untitled - motplot
File Edit View Help
begin
motion_start
main menu
○ Scan PCI bus
○ Locate/Choose PLX 9052 board
○ PCI configuration registers
○ PLX 9050 local registers
○ Access address spaces on the board
○ Access local address ranges on the board
○ Enable / Disable interrupts
○ Access serial EEPROM on the board
○ PCI register to write
○ PLX register to write
Enter option
PID configuration
EXIT
0
0
0
GO
Stop
X
Y
Ready
NUM
start

Figure 3. GUI on PC

3. PID CONTROLLER ON FPGA

3.1. Overall Structure

The PID control method is very simple and important, especially in robot control applications. The PID controllers are implemented in a FPGA chip having (Spartan II) 150,000 gates made from Xilinx company. The design of PID motion controller is programmed by ISE6.2.



disable
□ M1 □ M2

PID Gain
● M1 ○ M2

P Gain: 0
I Gain: 0
D Gain: 0
Setpoint1: 0
Setpoint2: 0

encoder
encoder1: -842150451
encoder2: 0
Error in PID :
YD M1: 0
YD M2: 0

Speed Profile:
● S Speed
○ Step Speed
○ TrapeZium Speed
○ Pulse Speed
○ PID Speed

Figure 4. PID GUI

Figure 5 shows the schematic design of the controller. The FPGA based PID controller consists of several blocks such as a communication block, an encoder counter block, a PID calculation block, and a PWM generation block.

Table 1 lists functions of each pin show in Figure 5.

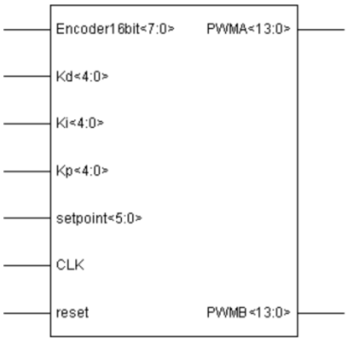


Figure 5. The design of motion controller on ISE

3.2. The Communication Block

It receives PID gains and desired trajectory, and transfers encoder data from the controller to a FPGA whenever they are needed. Data is writing from the PC to FPGA to the motion controller included PID gains, enable/disable, and the motion controller reset. Table 2 shows commands and their data encoder. Datais read from the motion controller to an MCU. Since the size of encoder data is 16 bit, it should be read as high and low bytes separately.

Table 1. The Pin name and its function

	Pin name	functions
Input	M1_CHA	Motor 1 encoder phase A
	M1_CHB	Motor 1 encoder phase B
	M2_CHA	Motor 2 encoder phase A
	M2_CHB	Motor 2 encoder phase B
	main_clk	FPGA system clock
	Cs	Chip select
	Rd	Read
	Wr	Write
	c_d	Command, data
	data_HL	High, low byte
Output	M1_motor_in1	Motor 1 output 1
	M1_motor_in2	Motor 1 output 2
	M2_motor_in1	Motor 2 output 1
	M2_motor_in2	Motor 2 output 2
	enable1	Motor 1 enable
	enable2	Motor 2 enable
Bidirection	data[7..0]	8bits data bus

Table 2. Communication command

Command	Data	Command	Data
Motor 1 Kp	0x01	Motor 2 Kp	0x11
Motor 1 Ki	0x02	Motor 2 Ki	0x12
Motor 1 Kd	0x03	Motor 2 Kd	0x13
Motor 1 Yd	0x04	Motor 2 Yd	0x14
Motor 1 enable	0x05	Motor 2 enable	0x15
Motor 1 disable	0x06	Motor 2 disable	0x16
Read encoder Motor 1	0x07	Read encoder Motor 2	0x17
FPGA reset	0x08		

3.3. Motor Control Block

Figure 6 shows the motor control block. It consists of encoder counter, PID controller, and PWM generator. The clock synchronizes the process. It generates the trigger signal at each 1KHZ sampling timeand sends it to encoder counter block and PID controller block and it synchronize the process of encoder counter and PID controller.

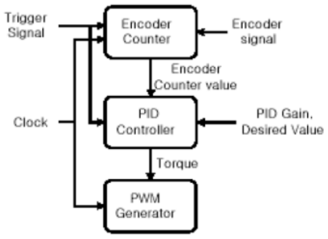


Figure 6. The structure of motor control block

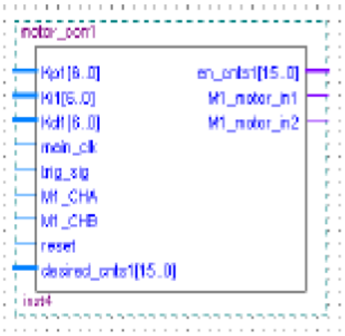


Figure 7. The designed symbol of motor control block

Figure 7 shows the designed motor control symbol. It takes PID gains,a clock, a trigger signal, encoder signals, a reset signal as input and PWM signal and encoder counter values as output.

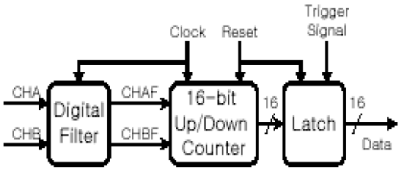


Figure 8. The structure of encoder counter

3.3.1. Encoder Counter Block

It counts and determines the direction of motor rotation from encoder signal. The block diagram is shown in Figure 8. The Difference in phases A and B determines the direction of rotation. Noise of a mechanical system can be filtered out by digital filters shown in figure 8. Every trigger signal enables to generate counter values. 16 bit of counter limits the range of the movements.

3.3.2. PID Controller Block

PID controller block receives encoder data from the encoder counter block and compares them with desired values to generate positional errors and then generate PID controllers. PID controller equations are

$$\tau(n) = K_p e(n) + K_i s(n) + K_d\{e(n) - e(n-1)\} \tag{1}$$

$$s(n) = \begin{cases} s_i & \sum e(n) > s_i \\ \sum e(n) & -s_i \le \sum e(n) \le s_i \\ -s_i & \sum e(n) < -s_i \end{cases} \tag{2}$$

$\tau(n)$is control input, $e(n)$is errorK_p,K_i, K_d are PID gains, $s_i$is a threshold value.

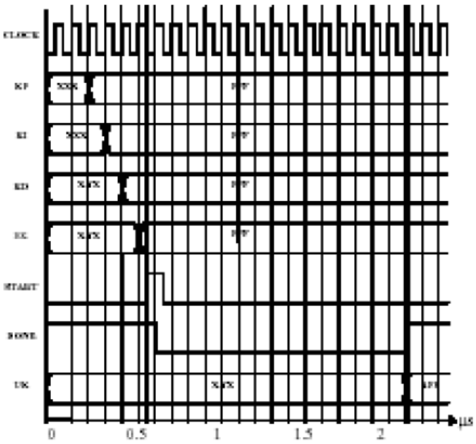


Figure 9. Timing diagram of the simulation of PID.

4. AVR MICROCONTROLLER CODE

The main PID controller routine was designed to be fairly general purpose and modular form. While it is used to control a DC motor, it could be re-deployed to other situations where some parameter has to be controlled to a set value under varying conditions. The actual control software is located in a single function and its major inputs and output are held in a structure. Although it was designed originally for a specific job it is really only intended as an example of the basic techniques involved and to allow those with no control system knowledge to experiment with a simple PID system.

The routines that gather the inputs and process the output are kept in separate functions in another module. The code vision compiler was used for simplicity as well to allow the easy modification of the important PID gain parameters, the AT mega 10-bit analog to digital converter was used to derive 10-bit resolution inputs from simple trimmer potentiometers. The PWM used to drive the motor was chosen as 10-bits so that motor speed can be defined to approximately 0.1%, sufficient for most practical application. The ATmega128 high resolution dedicated PWM unit could have been used to increase this to a supersonic 19.5 kHz but to allow easy porting to other AT mega variants this route was not taken.

Fortunately the use of a 10 bit resolution on the inputs and output makes some of the arithmetic easier. The Atmega128 IO pins are allocated as:

P2.0 optical chopper encoder input
P2.1 channel 2 - PWM drive output
P5.0 analog channel 0 - set point input
P5.1 analog channel 1 - derivative gain input
P5.2 analog channel1 proportional gain input
P5.3 analog channel 1 - integral gain

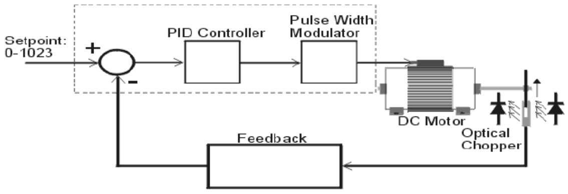


Figure 10. Implementation OF PID on AVR Atmega28

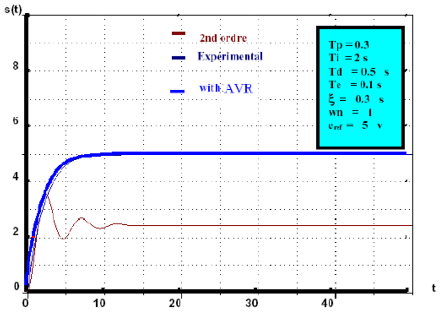


Figure 11. Compare of PID on FPGA and AVR

5. CONCLUSIONS

In this paper, a directly driven robot with three wheels, which we designed, is presented. The PID controller for two wheels is implemented by a FPGA. Control using a FPGA was successful and join movement is displayed on GUI. Implementing controller with FPGA turned out to be very effective since the size of the whole system was remarkably reduced and it was cost effective as well.

REFERENCES

[1] Jingo Kim, Sun Su Kim, Saul Jung. Implementation and Motion control of Linkage Bar Fingers. *ICCAS*. 2002; 2091-2094.

[2] G.W. Lucas, "A Tutorial and Elementary Trajectory Model for the Differential Steering System of Robot Wheel Actuators,"

[3] http://rossum.sourceforge.net/papers/DiffSteer/DiffSteer.html, 2005.

[4] A. C. Victorino, P. Rives, J.J. Borrelly, "Safe Navigation for Indoor Mobile Robots. Part II: Exploration, Self-Localization and Map Building", 2004.

[5] T. Duckett, "A Genetic Algorithm for Simultaneous Localization and Mapping", 2003.

[6] M. Quigley, D. Stavens, A. Coates, and S. Thrun. Sub-meter indoor localization in unmodified environments with inexpensive sensors. In Proc. of the IEEE/RSJ Int. Conf. on Intelligent Robots and Systems (IROS), 2010.

[7] G. Grisetti, R. Kummerle, C. Stachniss, U. Frese, and C. Hertzberg.Hierarchical optimization on manifolds for online 2d and 3d mapping.In Proc. of the IEEE Int. Conf. on Robotics & Automation (ICRA), 2010.

[8] T.Aoyama,QianyiWang,R.Suematsu,R.Shimizu,U.Nagashima,"Learning algorithms forneural network in FPGA".Proceedingsoft the 2002 International Joint Conferenceon Neural Networks,vol.1,pp.1007-1012,2002.

[9] M.Krips, TLammert,A.Kummert."FPGA implementation of neural network for real-time hand traking system"Proceedings of the First IEEE Internatinal Workshop on Electronic Design, Test and Applications, pp.313-317,2002.

[10] M.Cristea,J.Khor,M.McCormick;"FPGAfuuzy logic controller for variable speed generators", Proceedings of the 2001 IEEE International Conference on Control Application,pp301-304,2001.

[11] Abdelkrimk, Oudjidaetal. Areconfigurable counter controller for digital motion control application. *Microelectronics Journal*. 1997; 28(6-7).

[12] F.Thomas et al, "Design and implementation of a wheel speed measurement circuit using field programmable gate arrays in a spacecraft" Microprocessors and Microsystems,pp.553-560,1999.

[13] S.N oh et al,"Design of a biped robot using DSP and FPGA", Proceeding 2002 FIRA Robot World congress, 698-701.

[14] A.Kongmunvattana ,Pchongstivatana,"A FPGA-Based behavioral Control system for a mobileRobot ",The 1998 IEEE Asia –PacificConference on Circuits andSystems,pp.759-762,24-27,Nov 1998.

[15] Sung-Su kim and SeulJung, "Implementation of an intelligent controller with a DSP and a FPGA fornonlinear system" to appear inICCAS2003.