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SUPPLEMENTARY INFORMATION

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Supporting information

for

Mobility engineering and metal-insulator transition in monolayer MoS_2

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S1. Device fabrication

Degenerately-doped Si wafers covered with 270 nm thermally grown SiO_2 serve as the substrate and back-gate for the MoS_2 devices. Single and few-layer MoS_2 flakes are obtained by standard micromechanical cleavage technique.[1] Flakes are identified by an optical microscope and their thickness is ascertained by optical contrast measurements[2] and atomic-force microscopy. The source, drain and voltage probes were defined by electron-beam lithography followed by deposition of 90 nm thick Au electrodes. In the inset of Figure 1a we present an optical image of the device after standard lift-off procedure performed in acetone. In order to remove resist residue and decrease contact resistance in our devices, we perform annealing at 200 ºC in Ar atmosphere for 2 hours. After this step, we shape the MoS_2 flakes into Hall bars using oxygen plasma etching and an e-beam defined etching mask. Some of our devices were further processed and a 30 nm-thick HfO_2 layer was deposited by atomic layer deposition (ALD) followed by another e-beam lithography process defining the top-gate electrode. The top-gate electrode is made by depositing Cr/Au (10/50 nm) layer by electron-beam evaporation and lift-off in acetone. The optical image of one of our top-gated devices is shown in Figure 1a. All devices are wirebonded onto chip carriers and transferred to a cryostat where the transport measurements were performed in vacuum from room temperature down to 300 mK.

S2. Device details

We have performed measurements on two devices in single-gate configuration, two devices in single-gate configuration covered with a 30 nm thick HfO_2 layer and six devices in dual-gate configuration. Their characteristics are summarized in the following table:

Table 1. Device details

Device	Configuration	W (μm)	L_{12} (μm)	$k_F \cdot l_e$	n_{MIT} (10^{13} cm^{-2})	γ	μ(cm^2/Vs) T=4K	μ(cm^2/Vs) T=260K
Monolayer1	Single-gate	3.9	0.7	-	-	1.4	6.4	17.2
Monolayer2	Dual-gate	3.0	1.2	1.8	1	0.3	87.7	56.9
Monolayer3	Dual-gate	3.7	-	-	-	1.29	50.1	16.5
Monolayer4	Dual-gate	3.0	1.4	0.9	-	0.52	46.2	13.9
Monolayer5	Dual-gate	1.9	1.6	2.5	1	0.73	174	63
Monolayer6	Dual-gate	2.3	2.00	1.76	-	0.53	60	31.1
Monolayer7	Single-gate, with dielectric	3.20	1.3	-	-	-	30.9	30.6
Double-layer	Dual-gate	1.6	1.6	2	1.3	1.47	117.6	26.4
Three-layer	Single-gate, with dielectric	4.9	1.8	2	1.1	0.75	84	24
Four-layer	Single-gate	4.6	1.3	-	-	-	1	30.1

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W is the channel width and L_{12} is the distance between voltage probes used in four-contact measurements. $k_F \cdot l_e$ is the Ioffe-Regel parameter related to the metal-insulator transition point and n_{MIT} is the electron concentration at which the transition occurs, extracted from Hall-effect measurements.

S3. Top-gate efficiency

We have performed measurements on six devices in double-gate configuration where the electron concentration in the MoS_2 channel can be as high as $3.6 \cdot 10^{13}$ cm^{-2} due to a very efficient top-gate, Figure S1.

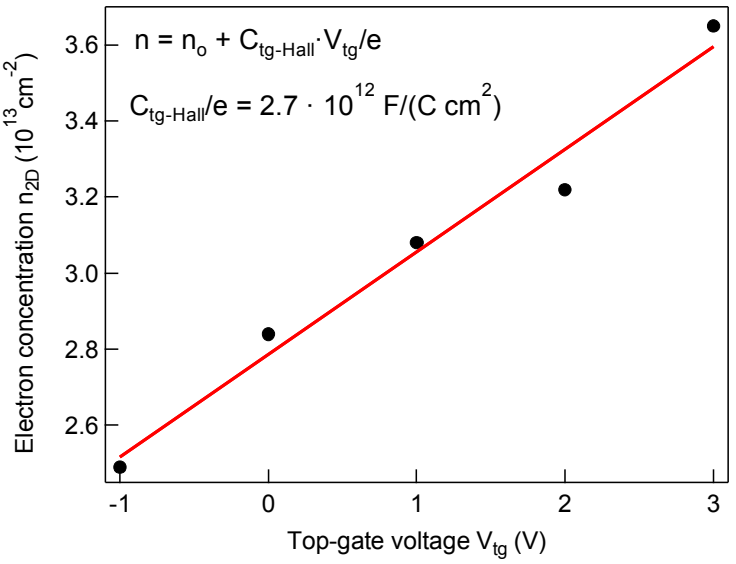

Figure S1. Electron concentration n_{2D} extracted from R_{xy} for different values of the top-gate voltage V_{tg} demonstrating electron concentration as high as $3.6 \cdot 10^{13}$ cm^{-2}. Measurements were performed on the device Monolayer2 from Table 1.

S4. Schottky barrier height in a single-gate device

From the temperature dependence of conductance for different gate voltages (Figure 2b in the main text) we were able to extract activation energy E_a dependence on gate voltage V_{bg}, Figure S2. From the deviation of the E_a from the linear trend, occurring when barrier tunneling becomes the dominant mechanism for charge carrier injection, we estimate a Schottky barrier height $\Phi_{SB} \sim 45$meV. This value is relatively small and does not have a significant influence on our mobility extraction from four-contact measurements.

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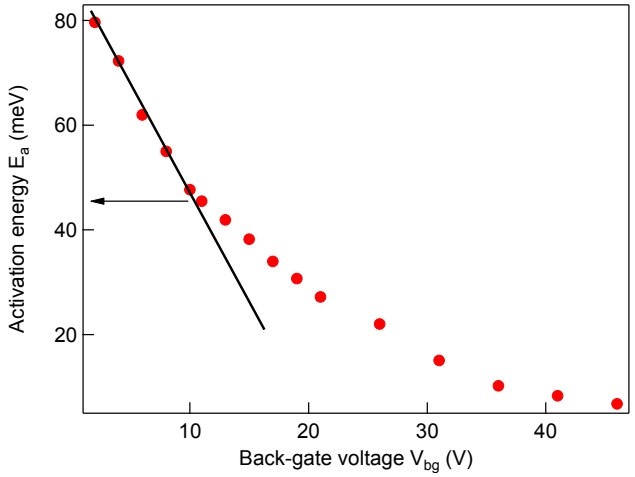

Figure S2. Activation energies E_a for monolayer MoS_2 in a single-gate configuration in the insulating regime. Dependence of activation energy E_a on V_{bg}. From the deviation of the E_a from the linear trend, occurring when barrier tunneling becomes the dominant mechanism for charge carrier injection, we estimate a Schottky barrier height for the charge carrier injection from gold electrodes into monolayer MoS_2 of Φ_{SB}~ 45 meV.

S5. Hysteresis in G - V_{tg} curves

Double sweeps of conductance G as a function of the top gate voltage V_{tg} at several temperatures for the double-gated device presented in the manuscript are shown in Figure S3 demonstrating no hysteresis for all temperatures. This excludes the possibility of device hysteresis being behind the observation of the metal-insulator transition.

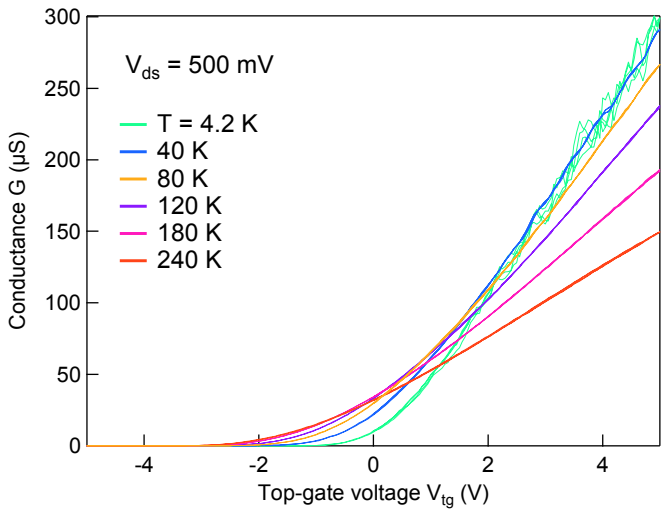

Figure S3. Conductance G double-sweeps as a function of the top gate voltage V_{tg} at several temperatures for the double-gated device presented in the manuscript demonstrating no hysteresis for all temperatures, excluding the possibility of its influence on the MIT.

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S6. Capacitance determination

We extract device capacitance from Hall effect measurements and the transverse Hall resistance R_{xy} for all MoS_2 devices covered with a dielectric layer in order to accurately determine the mobility. The contact resistance for uncovered devices is too large to perform meaningful R_{xy} measurements. From the inverse slope of R_{xy} vs magnetic field (an example is shown on figure 5a in the main manuscript), we can directly determine the electron density n_{2D} in the MoS_2 channel. The variation of the electron density extracted from R_{xy} as a function of the control-gate voltage for two typical situations encountered in the literature is shown in Figure S4. In Figure S4a, we show the dependence of the charge density on the back-gate voltage for a device in which the MoS_2 channel is covered with a 20nm thick HfO_2 layer. From the slope, we can extract the correct capacitance of the back-gate, $C_{bg\text{-}Hall}$, which in this case is 2.4 times higher than the capacitance calculated using the parallel-plate capacitance model $C_{geom} = \varepsilon_0 \varepsilon_r / d_{ox,bottom}$. The capacitive coupling between the MoS_2 channel and the back-gate is therefore increased due to the presence of the dielectric covering MoS_2 and any mobility estimate that would use the geometric capacitance instead of would yield a mobility value overestimated by a factor of 2.4. Similarly, in Figure S4b we present charge density measurements for a device in which the top gate has been disconnected. In this case we find that the capacitive coupling is increased by a factor of 53. This shows that using the parallel-plate capacitance model in place of an actual, measured capacitance in this type of situations can result in underestimating the strength of the capacitive coupling and field-induced charge density and lead to an overestimated mobility.

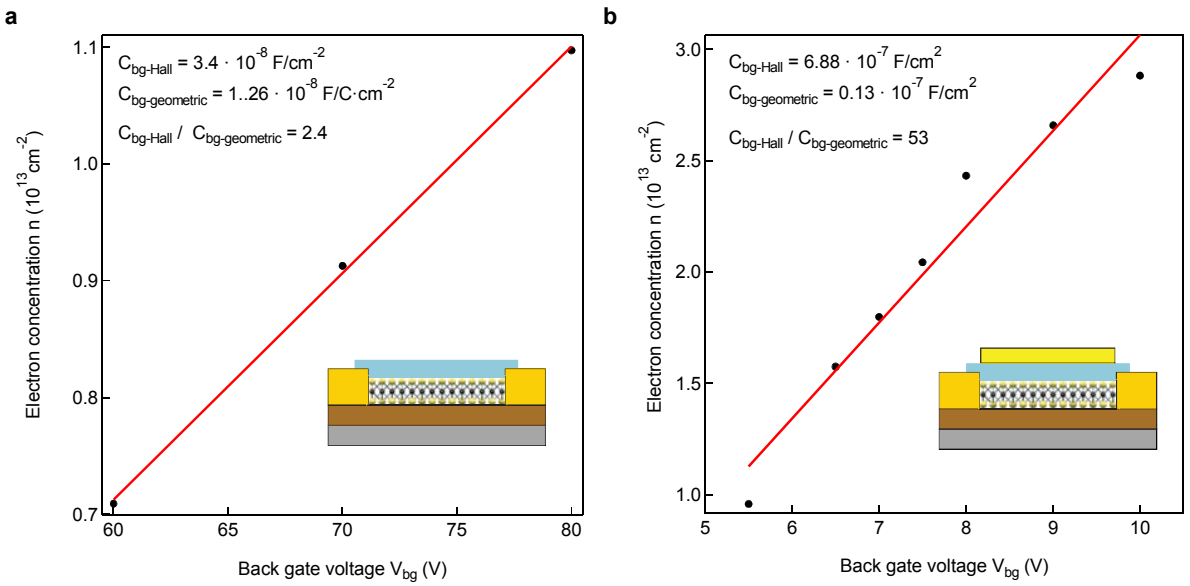

Figure S4. Electron concentration *n* extracted from R_{xy} for different values of the control gate voltage. a, Charge density vs. bottom gate voltage for the three-layer device from Table 1. The conductivity is controlled using a bottom gate, while the channel is covered by a 30 nm thick HfO_2 layer. The presence of the dielectric increases the back-gate capacitance by a factor of 2.4 with respect to the parallel-plate capacitance, commonly used for mobility estimates. **b,** Charge density vs. bottom gate voltage for the top-gated monolayer device (monolayer 4 in Table 1) measured as a function of the bottom gate while the top gate is disconnected. The capacitance is increased by a factor of 53 with respect to the parallel-plate capacitance where one plate is the back-gate and the other the MoS_2 channel.

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S7. Interface trap density

The charge traps are located in the interface between MoS_2 layer and SiO_2 substrate, and MoS_2 and HfO_2 dielectric. Assuming that activated behavior arises from activation of electrons from the Fermi energy E_F to conduction band edge E_c, we can write $E_a = E_c - E_F$. Then this implies $\frac{dE_F}{dV_{tg}} = -\frac{dE_a}{dV_{tg}}$. Quantity $\frac{dE_F}{dV_{tg}}$ is given by $\frac{dE_F}{dV_{tg}} = \frac{eC_{tg}}{(C_{tg}+C_{bg}+C_q)}$, where $C_{tg} >> C_{bg}$ ($C_{tg} \sim 45C_{bg}$) and $C_q = e^2D(E)$ is the quantum capacitance related to the density of localized states $D(E)$. From the slope of the curve (main text, solid black line in Figure 4b) related to monolayer device in Figure 4b at lower gate voltages when the device is fully depleted, that corresponds to a bandwidth of 44 meV, we estimate the concentration of depleted charges to be $n_t \sim 6.3 \cdot 10^{11}$ cm^{-2}.

References

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