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ORIGINAL ARTICLE

Mobility enhancement of strained Si transistors by transfer printing on plastic substrates

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Strain engineering has been utilized to overcome the limitation of geometric scaling in Si-based thin-film transistor (TFT) technology by significantly improving carrier mobility. However, current strain engineering methods have several drawbacks: they generate atomic defects in the interface between Si and strain inducers, they involve high-cost epitaxial depositions and they are difficult to apply to flexible electronics with plastic substrates. Here, we report the formation of a strained Si membrane with oxidation-induced residual strain by releasing a host Si substrate of a silicon-on-insulator (SOI) wafer. The construction of the suspended Si/SiO_2 structures induces $>0.5\%$ tensile strain on the top Si membrane. The fabricated TFTs with strained Si channels are transferred onto plastics using a roll-based transfer technique, and they exhibit a mobility enhancement factor of 1.2–1.4 compared with an unstrained Si TFT.

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INTRODUCTION

A critical path in the development of advanced silicon electronics involves a reduction in the dimensions of device geometries such as the channel thickness, channel length and gate dielectric thickness to increase the operating speed with lower power consumption and the density of integration in circuits.[1–4] Continued performance improvement through geometric scaling has faced increasingly difficult challenges.[5,6] Recent research focused on this issue has explored strain engineering that can increase the charge carrier mobility by creating tensile strain in Si with a capping stressor film,[7] local stressors under channel[8] or embedded source/drain stressors.[9,10] In particular, the introduction of an $Si_{1-x}Ge_x$ buffer layer with a large lattice constant represented by an epitaxial template can successfully generate biaxial tensile strain in Si.[11,12] The $Si_{1-x}Ge_x$ virtual buffer layer allows the fabrication of wafer-scale strained Si membranes[13,14] and approximate doubling of the mobility enhancement factors of electrons in Si layers for fast, flexible electronic device applications.[15–17] However, the process for introducing the $Si_{1-x}Ge_x$ buffer leads to undesirable misfit dislocations and interdiffusion of Ge in the Si/SiGe interface and requires uniform growth of the $Si_{1-x}Ge_x$ layer with precisely controlled composition of Si and Ge, which is challenging.[18–21]

Here, we present a new strain engineering approach to induce a biaxial tensile strain to the active Si device layer without using an additional epitaxial stressor layer. In this approach, the tensile strain in Si is naturally created in the process of etching and physical transfer for building flexible Si devices with high performance on plastic substrates. A strained Si nanomembrane is fabricated by releasing the bilayer of Si and SiO_2 from the host Si layer of a silicon-on-insulator (SOI) wafer. The oxidation-induced compressive strain in the SiO_2 layer of the SOI wafer is activated by forming a suspended structure via the etching of the host Si that leads to planar expansion of the Si/SiO_2 bilayer and resultantly induces biaxial tensile strain in the top Si layer. The extent of strain sharing depends on the relative thicknesses of the two layers. The transfer step is inevitably required for the proposed Si devices that well fits this approach to flexible electronics. After transferring the strained Si membrane to the plastic substrate, the fabricated Si devices exhibited a 20–40% greater charge carrier mobility. The strained Si membrane can benefit from the well-established SOI electronics and offers an important advantage over the conventional method that uses a $Si_{1-x}Ge_x$ stressor layer.

EXPERIMENTAL PROCEDURE

Fabrication of strained Si transistors

The schematic illustrations of whole fabrication steps for strained Si thin-film transistors (TFTs) are displayed in Supplementary Figure S1. SOI wafer was used to fabricate the Si TFTs. The SOI wafer was composed of 0.43–1.5 μm top Si, 1 μm SiO_2 and bulk Si. A top Si layer of SOI wafer was n^+ doped to form ohmic contacts with the source and drain electrodes of the TFTs by implantation with phosphorus (dose $=5\times10^{15}\,cm^{-2}$, energy $=15$ KeV). Si layers outside the device parts were etched using SF_6 plasma by reactive-ion etching to prohibit the interference of currents flowing into each device. A SiO_2 dielectric layer (70 nm) was grown by a thermal oxidation process at 900 °C for 39 min. An opening process was performed to make a via hole between the

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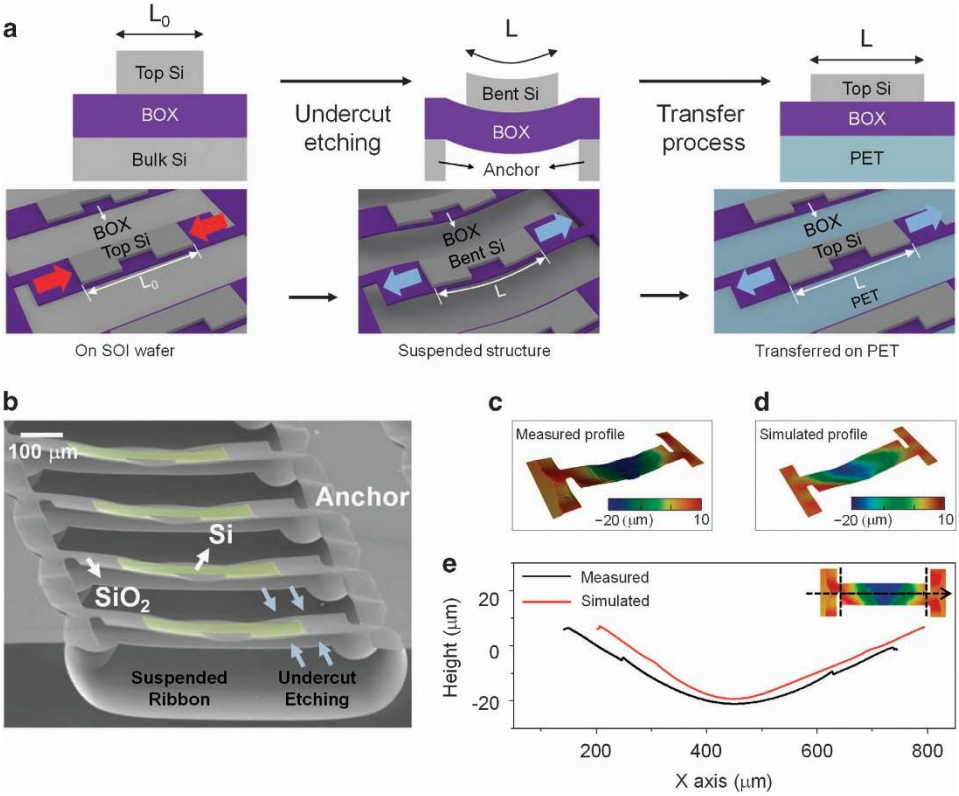

Figure 1 (**a**) A schematic of the processes used to apply tensile strain to a Si ribbon. (**b**) A scanning electron microscope (SEM) image of suspended Si/SiO_2 ribbons after removing bulk Si. Visualized height profiles of the suspended Si/SiO_2 ribbon (**c**) measured by white light interferometer (left) and (**d**) simulated by finite element method (FEM; right). (**e**) Height profiles of the center part of suspended Si/SiO_2 ribbons along the longitudinal direction. The black solid curve is for the measured height profile by white light interferometry, and the red solid curve is for the simulated one by finite element analysis (FEA), respectively. BOX, buried oxide; PET, polyethylene terephthalate; SOI, silicon-on-insulator.

sources and drains of the Si and electrodes by wet etching of SiO_2. Cr/Au layers with thicknesses of 5 and 95 nm, respectively, were deposited by thermal evaporation and defined as source/drain and gate electrodes by photolithography.

Roll-based transfer processes

Patterns of ribbons with a length of 610 μm and a width of 160 μm were formed using AZ33XT (10 μm) followed by a hard baking process at 115 °C for 3 min. A lateral dry etching process using an inductively coupled plasma reactive-ion etcher (SF_6, 130 sccm, 50 mTorr, 35 min) was carried out to remove the bulk Si underneath the buried oxide (BOX) layer to form suspended device ribbons. A roll transfer process was then used to carry out the reliable transfer of suspended device ribbons with precise control of the transfer load. Roll transfer equipment generally consists of a roller, a load cell, a *z*-axis actuator and a transfer plate as shown in Supplementary Figure S2. The inset shows the schematic illustration of the roll transfer system. The roller is parallel to the transfer plate, and its vertical motion is controlled by two *z*-axis actuators. The exact load applied to the devices is accurately measured by the load cell and is controlled by the input system connected to the actuators. The transfer processes are mainly divided into two steps: picking step and placing step. In the picking step, large-area suspended device arrays held onto the transfer plate by vacuum were placed in contact with the roller that was covered by a polydimethylsiloxane film with an optimized contact load. Suspended device arrays were detached from the wafer and attached to polydimethylsiloxane by van der Waals adhesion force. In this procedure, the angular displacement of the roller was synchronized with the in-plane displacement of the transfer plate to prohibit device arrays from being misaligned by shear stress. In the placing step, the target substrate should be held onto the second transfer plate. Contact between device arrays attached to the roller and a target substrate was made with the optimized load. Adhesives such as NOA 63 (Norland Products Inc., Cranbury, NJ, USA) and SU-8 2005 (Microchem Corp., Newton, MA, USA) were coated on the surface of the target substrate to facilitate a larger adhesion force between the devices and the target substrate than that between the devices and the roller. Through the rolling steps with the synchronized motion of the roller and the plate at 90 °C, picked devices were transferred onto a target substrate. The resultant devices realized by the roll-based transfer technique are shown in Supplementary Figure S3. Large-area device arrays including ~3000 devices in 4 × 4 cm scale were transferred onto plastics with robust operation.

RESULTS AND DISCUSSION

Figure 1a illustrates the application of self-sustained biaxial tensile strain to Si/SiO_2 ribbon arrays suspended on a wafer by releasing residual compressive stress confined in SiO_2. An SOI wafer with a top Si (100) layer of various thicknesses on a BOX layer was used to fabricate strained Si ribbons. A large volume expansion accompanies the oxidation process of Si to form the BOX layer because the molar volume of SiO_2 is larger than that of Si. However, the volumetric expansion of SiO_2 is constrained because it is bonded to the underlying Si handle wafer, and hence a high residual compressive stress of 0.2–6 GPa is biaxially developed in the BOX layer.[22–26] Etching out of the underlying handle Si leads to a biaxial expansion of the BOX and, as a result, creates biaxial tensile strain in the top Si ribbon that is tightly bonded to the BOX. The tensile strain in the Si is determined by equilibrating the force between the Si and the SiO_2. The suspended ribbons are anchored on both edges, and hence the biaxial tensile stress in the ribbons generally generates a boat shape because of

buckling (Figure 1b).[27,28] The extent and distribution of strain can be evaluated by analyzing the degree of buckling and the deformed shape.[29]

Figure 1c presents the result of a three-dimensional height profile of the suspended Si/SiO_2 ribbon measured by white light interferometry. The deformation of the ribbon was evaluated by measuring the change of transverse and longitudinal length in the Si and SiO_2 regions. Based on the dimensions of the suspended ribbon (Supplementary Figure S4), the residual stress in the BOX layer and the average tensile strain applied to the suspended Si layer were estimated to be 854 MPa and 0.318%, respectively (Supplementary Note S1). To confirm these results, finite element analysis was carried out on a model of the suspended Si/SiO_2 ribbon under the same conditions (Supplementary Note S2); the simulated three-dimensional profile of the suspended ribbon (Figure 1d) was analogous to the measured one. The distance between the center and the edge of the ribbon along the longitudinal direction was 23.89 μm in the simulated profile and 26.05 μm in the measured ribbon (Figure 1e).

Figure 2a presents finite element analysis results of the distribution of in-plane principal strain on a suspended Si/SiO_2 ribbon. The contour map of strain shows that a tensile strain of ~0.310% is uniformly applied to the whole area of the table-shaped Si on SiO_2. This measurement agrees with the result of the height profile measurement (0.318%). The distribution of strain along the x and y axes of a ribbon are displayed in Figures 2b and c, respectively, showing different average values of tensile strain ($\varepsilon_{x,\ avg} = 0.207\%$, $\varepsilon_{y,\ avg} = 0.271\%$) with a nonuniform distribution. This is because the ribbon is longitudinally and asymmetrically linked to the anchors and constrained by the rigid edges while being transversely free without any constraint (Supplementary Figure S5).

Raman spectroscopy was used to measure the distribution of the induced strain in a suspended Si ribbon, and the results were compared with the results above. The strain in the Si was directly calculated by observing the shift of a strong Raman peak near 520 cm^{-1}.[30,31] Figure 3a presents the contour mapping image of Raman shift for unstrained Si on an unetched region and a strained, suspended Si ribbon that displays a clearly distinguished, uniform strain distribution on two regions. Raman peaks of unstrained Si and strained Si were observed at 520.46 and 517.98 cm^{-1}, respectively.

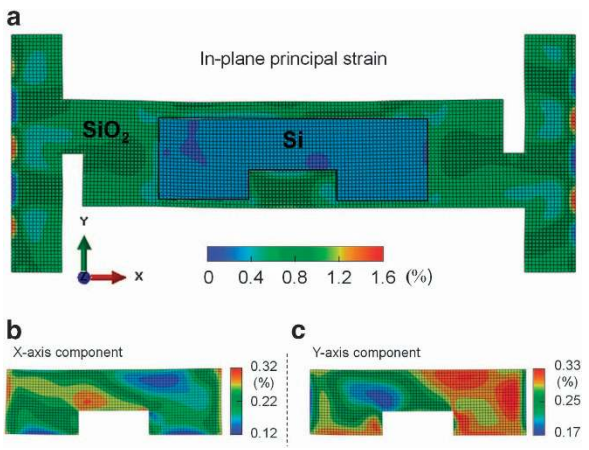

Figure 2 (**a**) A contour map of the in-plane principal strain distribution on the suspended Si/SiO_2 ribbon simulated by finite element analysis (FEA). The FEA contour maps of (**b**) normal strain in the x direction (left) and (**c**) normal strain in the y direction (right) in the suspended Si area.

This image shows good agreement with the simulated one shown in Figure 2a. Figure 3b shows Raman spectra that illustrate the change in strain at different conditions: bulk, anchored, suspended and transferred Si. Raman peaks of bulk and anchored Si appeared at 520.46 cm^{-1}, and peaks of suspended and transferred Si ribbons were observed at 517.98 and 518.22 cm^{-1}, respectively. Based on the Raman peak of unstrained Si (520.46 cm^{-1}), those of the suspended and transferred ribbons were downshifted ($\Delta\omega$) by 2.48 and 2.24 cm^{-1} with a tensile strain (ε_{Si}) of 0.316 and 0.286%, respectively, given by[31]

$$\Delta\omega = b \times \varepsilon_{Si} \quad (1)$$

In Equation (1), b is the strain shift coefficient of the Si–Si phonon mode on strained Si, -784 ± 4 cm^{-1}. Although uniform tensile strain was distributed in the transferred ribbon (Supplementary Figure S6), a slight decrease in the strain value of the Si ribbon may be created during the transfer to a polyethylene terephthalate (PET) substrate.[32] When an Si/SiO_2 ribbon is transferred to the PET substrate, it is heated to ~100 °C to cure the polymer adhesive and improve the bonding strength between the ribbon and the substrate. A cooling process after heating can induce a slight compressive strain on the ribbon because of the higher thermal expansion coefficient (α) of the PET substrate ($\alpha_{PET} = 5.9 \times 10^{-5}\ K^{-1}$) than that of Si/$SiO_2$ ($\alpha_{Si} = 2.6 \times 10^{-6}\ K^{-1}$, $\alpha_{SiO_2} = 0.35 \times 10^{-6} K^{-1}$). However, we observed that transferred ribbons maintained their original state without detectable deformation in Raman shift for 28 days (Supplementary Figure S7).

The tensile strain applied to the Si layer is controllable by adjusting the stiffness ratio of Si and SiO_2 because the residual strain from the bottom SiO_2 layer is more effectively transferred to the thinner Si layer. To assess the effects of the thickness ratio, Si/SiO_2 ribbons with different Si thicknesses (0.43–1.5 μm) and a constant thickness of SiO_2 (~1 μm) were transferred to a foreign substrate, and the induced tensile strain was measured by Raman spectroscopy (Figure 3c). The specific Raman peak of unstrained, bulk Si at 520.46 cm^{-1} showed larger downshifts as Si thickness decreased from 2.17 cm^{-1} for 1.5 μm-thick Si ($\varepsilon_{Si} = 0.277\%$) to 4.70 cm^{-1} for 0.43 μm-thick Si ($\varepsilon_{Si} = 0.568\%$; Figure 3d). The measured strain values are in good agreement with those obtained from finite element analysis (Supplementary Note S3). Ultimately, the strain level can be achieved up to 1% as predicted by the calculation.

A primary purpose for applying tensile strain in Si is to improve its electronic properties; the strain reduces carrier scattering and the effective transport mass of electrons.[33,34] The roll-based transfer approach of a strained Si layer can effectively provide important benefits to the development of high-performance strained Si TFTs for large-area flexible electronic applications.[15–17,35] Figure 4a shows the key fabrication steps for a strained Si TFT array on a flexible PET film using an automated roll transfer method. All device processes, including doping, oxidation and metallization, were performed on SOI wafers with different top Si thicknesses of 0.43–1.5 μm through a similar method to the conventional process.[36,37] After measuring the pristine characteristics of the device on a wafer, the device array (~3000 transistors on a 4 × 4 cm area) was printed on a PET substrate after undergoing the etching and roll transfer processes (Supplementary Figures S2 and S3). As seen in the magnified image, the surface of a strained Si TFT transferred onto a PET substrate looks smooth and clean because the distortion induced by the anchors was relieved by the sliding on the polydimethylsiloxane stamp (Supplementary Figure S8). In addition, no cracks were observed in the transferred devices, particularly on the SiO_2 layer. Thus, it is

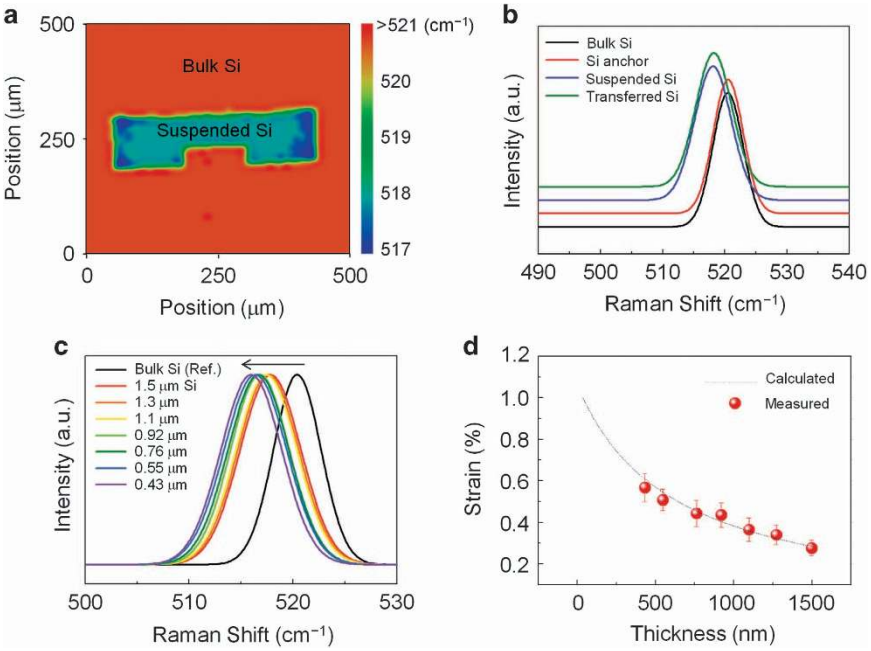

Figure 3 (**a**) A contour map of Raman peaks in a suspended Si ribbon. (**b**) Raman spectra of bulk Si (black), Si anchor (red), suspended Si (blue) and transferred Si (green). (**c**) Raman spectra of suspended Si ribbons with various thicknesses ranging from 0.43 to 1.5 μm. (**d**) Calculated and measured strain levels according to the thickness of the top Si layer in a suspended Si/SiO_2 ribbon.

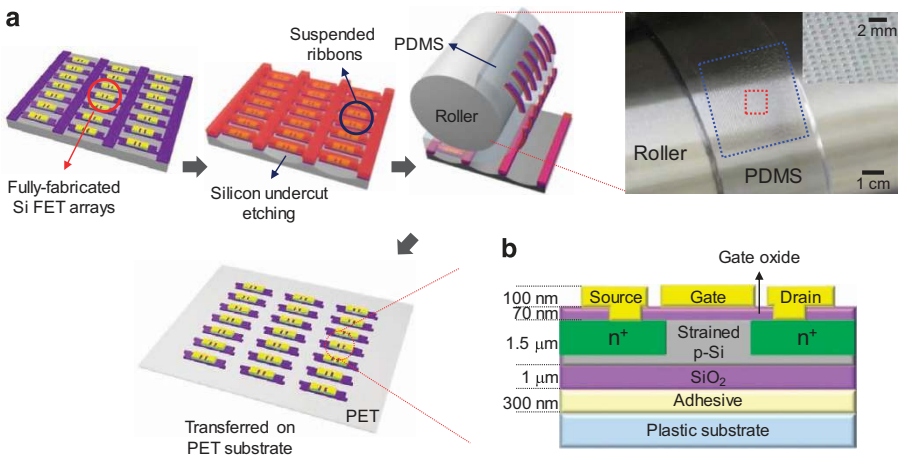

Figure 4 (**a**) Schematics of the steps to fabricate the strained Si thin-film transistors (TFTs) onto a polyethylene terephthalate (PET) substrate including suspending steps of devices by undercut etching and transfer steps using roll-based transfer printing. (**b**) An illustration of the cross-sectional view of the strained Si TFT on the PET substrate. PDMS, polydimethylsiloxane.

determined that the thin SiO_2 in the device is stable under the strain level of 0.5% because it forms a good interface with the Si through strong covalent bonds.

In contrast to the Si/SiO_2 ribbon, the induced strain of the Si channel in the TFT can be affected by additional layers, such as a dielectric layer, and electrodes that are required to produce a top-gated TFT structure (Figure 4b). The top SiO_2 dielectric layer (~70 nm) grown thermally on Si can induce strain on the Si, as with the bottom SiO_2, and also increase the applied strain on the Si by reducing the overall Si thickness. In contrast, a metal electrode (~100 nm) deposited on the SiO_2/Si can attenuate the straining effect of the top SiO_2 layer on the Si layer. It was calculated that the top-gated structures induce a slight increase in tensile strain applied to the Si layer compared with pristine Si/SiO_2 ribbons (from 0.277 to 0.292% for 1.5 μm-thick Si and from 0.568 to 0.584% for 0.43 μm-thick Si). These values indicate that the effect of the two additional layers is not great (Supplementary Note S4).

The strained Si devices transferred onto PET displayed significant improvement in device characteristics as shown in Figure 5. The drain current (I_d), compared with that of the unstrained device on a rigid wafer, increased by 16.8% for 1.5 μm-thick Si. I_d then gradually increased with decreasing thickness of the Si, and for 0.43 μm-thick Si, I_d was 30.5% greater than that of the unstrained rigid wafer (Figure 5a). The on/off ratio ($>10^5$) was unaffected by the Si thickness. $I_d - V_g$ characteristics also exhibited clear increases in drain currents in both linear and saturation regions, indicating the effects of

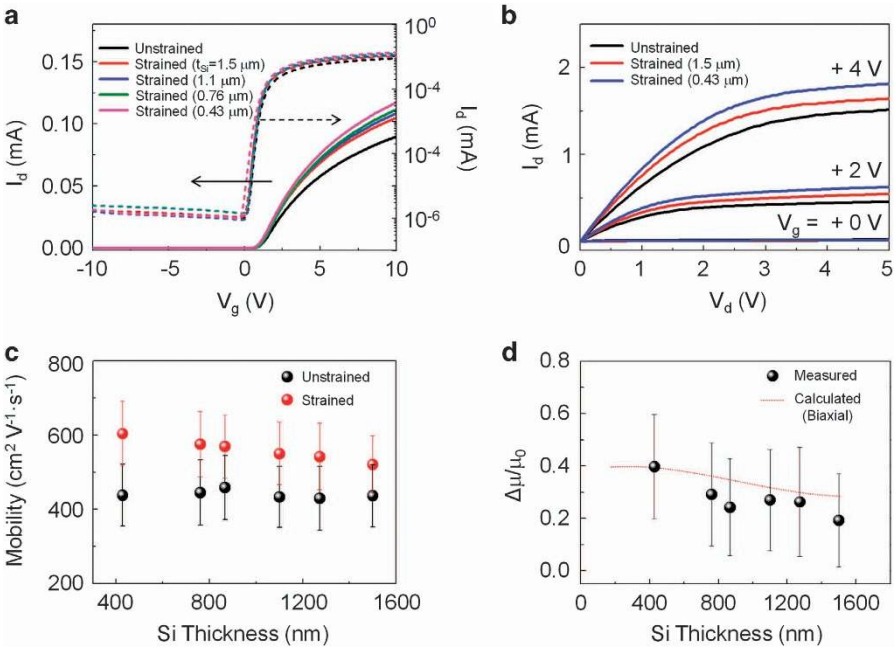

Figure 5 (**a**) Transfer characteristics of the Si thin-film transistor (TFT) on a wafer and strained Si TFT with various Si thicknesses (0.43–1.5 μm) on a polyethylene terephthalate (PET) substrate on a linear scale (line, left y axis) and a log scale (dash, right y axis) for a channel width of 100 μm and length of 10 μm at a drain voltage of 0.1 V. (**b**) Output characteristics of the Si TFT on a wafer and strained Si TFT with various Si thicknesses (0.43–1.5 μm) on a PET substrate at gate voltages from 0 V (bottom) to 4 V (top). (**c**) Mobility enhancement of strained Si TFTs with various Si thicknesses (0.43–1.5 μm) compared with unstrained Si TFTs. (**d**) Normalized change of mobility of strained Si TFTs with various Si thicknesses (0.43–1.5 μm). The red dot curve indicates the calculated results.

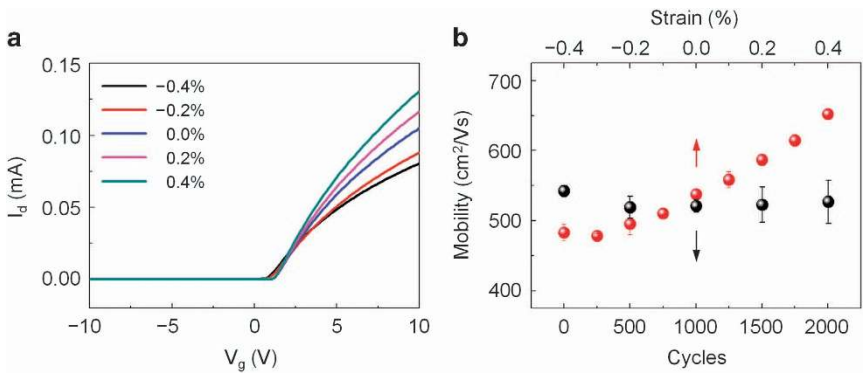

Figure 6 Uniaxial strain effects on electrical properties of strained Si thin-film transistors (TFTs) under bending. (**a**) Transfer characteristics of strained Si TFTs with a 1.5-μm-thick top Si layer under various bending strains. (**b**) The change in carrier mobility of strained Si TFTs under bending strain and after cycling tests.

strong strain in thin Si devices (Figure 5b). The average effective mobility, μ_{FE}, of unstrained Si TFTs on a wafer before the transfer was calculated as $440.2 \pm 84.9\ cm^2\ V^{-1}\ s^{-1}$ (Supplementary Figures S9 and S10 and Supplementary Note S5). The mobility of the strained Si devices on PET substrates increased from 520.7 ± 77.3 to $604.1 \pm 87.4\ cm^2\ V^{-1}\ s^{-1}$ with decreasing thickness of the Si (Figure 5c and Supplementary Figure S11). The mobility of strained Si TFTs improved by 20–40% over unstrained Si TFTs owing to the tensile strain of 0.292–0.584% without a serious increase in the gate leakage current (Supplementary Figure S12). The degree of this enhancement agrees well with the theoretical calculation based on the electronic properties of biaxially strained silicon (Figure 5d and Supplementary Note S6).[34] The performance of strained Si TFT would be saturated at 40% with a higher level of tensile strain.[40]

In addition, the enhanced mobility and threshold voltages exhibit a similar tendency as the channel length increased from 10 to 30 μm (Supplementary Figures S13 – S15). We measured the device performance for 28 days to confirm the stability of strained Si devices after transferring them to a plastic substrate. The strained Si TFTs exhibited stable operation and no strain relaxation under general environmental conditions for the entire duration of the experiment (Supplementary Figure S16) because the residual strain in the Si devices was induced by the underlying SiO_2 layer rather than the PET substrate that has time-dependent relaxation.[38]

Figure 6a shows the transfer characteristics of Si TFTs with 1.5 μm thickness on PET substrates under various strains. Uniaxial strains between −0.4 and 0.4% were applied by bending the flexible substrates along the channel direction. Drain currents in the on-state gradually increased with increasing bending strain. This mechanically applied uniaxial strain induced an additional reduction in the effective mass and charge scattering of electrons along the channel direction.[39,40] As expected, a tensile bending strain of 0.4% led to a 21% increase in mobility (from 537.57 to 652.1 $cm^2 V^{-1} s^{-1}$). In contrast, a compressive strain of 0.4% led to a 10% decrease in mobility because of an opposite influence on the Si channel. This change in mobility against the external strain shows that the TFTs were operating in a stable manner. Even after the repeated bending test to a tensile strain of 0.4%, during which the TFT was bent 2000 times, the strained Si devices were unscathed without failure (Figure 6b). Thus, these devices demonstrate reliable operation under repeated bending.

CONCLUSION

Biaxial tensile strain was residually generated in the Si layer of a Si/SiO_2 structure by utilizing the oxidation-induced volumetric strain of the BOX layer in SOI wafers. The induced strain was analyzed by measuring the mechanically stretched configuration of the suspended Si/SiO_2 ribbons by Raman spectroscopy and white light interferometry and confirmed by finite element analysis. The tensile strain in transferred Si TFTs was induced from 0.292 to 0.584%, depending on the thickness ratio of the bilayer of Si and SiO_2. Because the biaxial tensile strain applied to the Si channel reduced the intervalley scattering and effective mass of electrons, the suspended and transferred Si TFTs showed a 19–40% increase in carrier mobility as compared with the unstrained devices on a bulk wafer. Furthermore, realization of large-area, strained Si device arrays (4 cm × 4 cm) were demonstrated by a roll-based transfer onto a plastic substrate.

In conclusion, improved electrical performance was demonstrated in thin Si TFTs on a flexible substrate by strain engineering without relying on the epitaxial stressor, and this process is compatible with the roll-based transfer methods with high productivity. This approach shows promise for strain-engineered large-area flexible electronics with high performance and productivity.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

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