## Mobility Extraction in Uniaxially and Biaxially Strained N-MOSFETs

T. Bensidhoum<sup>1,2</sup>, F. Lime<sup>1</sup> and G. Ghibaudo<sup>1</sup> <sup>1</sup>IMEP, ENSERG, Grenoble, France <sup>2</sup> Université M. Mammeri, Tizi-Ouzou, Algeria

Strained-Si technology is of great interest since it allows enhanced carrier mobility which in its turn increases drive current [1]. However, it is not clear whether the mobility gain of strained Si nMOSFETs is due to the gain in conduction mass [2,3] or to reduced phonon scattering rate [4]. In this paper, we present a detailed parameter extraction method for the analysis of mobility between the process induced (uniaxial) and the substrate induced (biaxial) strained nMOSFETs.

We have used tensely strained-Si nMOS devices with two different architectures and featuring poly-gate material. Indeed, two different approaches were used to strain the channel [1]. The first one consists of an epitaxy of 15nm Si on a relaxed Si<sub>0.8</sub>Ge<sub>0.2</sub> substrate (sSi) to induce biaxial stress in the Si layer. The second one is a process induced type of stress, as it relies on the contact Etch Stop Layer (ESL) to induce uniaxial stress [2]. These two different strained-Si devices were compared with their own reference, a process matched for ESL and a threshold matched for sSi.

The measurements were done with a HP 4155B semiconductor parameter analyzer at wafer level using a SussMicroTec LT probe station. Mobility was extracted from the drain current at low  $V_d$  (10-50mV). It is well known that this extraction can be difficult in modern cutting edge devices due to the strong gate current and uncertainties in the effective gate length of short channel devices. This is why we compensated for the gate current using the method given in [3, 4], and, we extracted the effective gate length using capacitance measurements made on short channel devices [5]. Moreover, it should be noted that the method used for mobility extraction is independent of the source-drain series resistance [6].

The parameter extraction of the devices was conducted using the transfer characteristics measured in ohmic regime (Vd=10mV). Fig. 1 and Fig. 2 show typical Id(Vg) and gm(Vg) curves obtained for SiGe NMOS devices for gate lengths varying from L=30nm to 10 $\mu$ m. Note the excellent behaviour of the characteristics even at small gate lengths, emphasizing the very good control of short channel effects. Note also the strange behaviour of the drain current for long devices (10  $\mu$ m to 1  $\mu$ m) exhibiting a turn-around at strong inversion due to the high gate leakage current component in this ultra gate oxide devices. In order to extract reliably

the MOSFET parameters, the intrinsic drain current curves Id0(Vg) of the channels have been obtained after removing the gate current influence [3,4].



Fig.1: Transfer characteristics Id(Vg) of the devices for various gate lengths from 20nm up to  $10\mu$ m in linear scale (a) and log scale (b). Vd=10mV.



Fig.2: Trans-conductance vs gate voltage, gm(Vg), characteristics for various gate lengths.

From the function  $Y(V_g)$ , which is defined as Eqn. (1), we can extract the main MOSFET parameters,

$$Y(V_{g}) = \frac{I_{d}}{\sqrt{g_{m}}} (V_{g}) = \sqrt{\frac{W}{L} C_{ox} \mu_{0} V_{d}} . (V_{g} - V_{t})$$
(1)

where,  $C_{OX}$  is the gate oxide capacitance,  $V_d$  is the drain voltage,  $\mu_0$  is the low field mobility and  $V_t$  is the charge threshold voltage. The advantage of using this function is that it eliminates the influence of the access series resistance. Moreover, it allows the determination of threshold voltage Vt and low field mobility. Typical Y(Vg) characteristics are illustrated in Fig. 4.



Fig.3: Variations of the Y(Vg) function for various gate lengths.



Fig.4: Low field mobility variations with gate length for the strained nMOS and their respective reference.



Fig.5: Low field mobility gain extracted from Fig.4.

The channel length mobility dependence will be discussed. It is plotted in Fig. 3 for two types of stress and their reference. The mobility of the sSi reference is lower than that of the ESL due to a higher channel doping.

It is clear from Fig. 4 that the low field mobility gain is quite different from the two architectures. For the sSi case, the higher gain is obtained on the longer channels with a maximum of 50% and decreases with gate length. For ESL, the mobility gain is zero for the long channel case, but increases with gate length reduction until it reaches a maximum of 50% at approximately 0.16µm before it falls off. This latter behaviour was expected as the strain in the ESL case is located near the source and the drain, and therefore it becomes stronger with short channels. Furthermore, it is worth noting that, even if the mobility gain decreases below 0.1µm in both cases, the ESL gain seems better between 50nm and 0.3µm gate lengths.

We can also see in Fig. 4 that the low field mobility gain of short channel devices is weak and nearly constant with temperature, meaning that the mobility is governed by a similar mechanism in the strained-Si devices and their references. The constant positive mobility gain of sSi short channel devices. However, it is an artefact due to different implantation/diffusion conditions as compared to the reference. To confirm this issue, we have extracted the mobility gain at high field ( $Qi = 10^{-6}$  C/cm<sup>2</sup>). In that case, the Coulomb scattering is strongly attenuated due to the screening of the inversion layer. As expected, in these curves, the artefact is removed. For the long channel case, Fig. 5 shows a slightly increased mobility gain at high field, which can also be attributed to the reduced Coulomb scattering. In the ESL case, the Coulomb scattering is lower and there is little difference between the high field and low field curves.

In this paper, we have investigated the mobility in two different strained-Si technologies. We found that the mobility gain of our device is nearly lost on short channels. The short channel loss observed in both cases is attributed to a bigger contribution of Coulomb scattering and to a larger sub-band splitting due to pocket implants.

## References

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