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Model-Based Predictive Control with Graph Theory Approach Applied to Multilevel Back-to-Back Cascaded H-Bridge Converters

Gabriel Gaburro Bacheti [1], Renner Sartório Camargo [2], Thiago Silva Amorim [1], Imene Yahyaoui [3] and Lucas Frizera Encarnação [1,*]

[1] Department of Electrical Engineering, Federal University of Espírito Santo (UFES), Av. Fernando Ferrari, Vitória 29075-910, Brazil; gabriel.bacheti@edu.ufes.br (G.G.B.); thiago.s.amorim@edu.ufes.br (T.S.A.)
[2] Department of Control and Automation Engineering, Federal Institute of Espírito Santo (IFES), Rod. ES010, Serra 29173-087, Brazil; rscamargo@ifes.edu.br
[3] Department of Applied Mathematics, Materials Science and Engineering and Electronic Technology, Superior School of Experimental Sciences and Technology-ESCET, University Rey Juan Carlos, 28933 Madrid, Spain; imene.yahyaoui@urjc.es
* Correspondence: lucas.encarnacao@ufes.br

Abstract: The multilevel back-to-back cascaded H-bridge converter (CHB-B2B) presents a significantly reduced components per level in comparison to other classical back-to-back multilevel topologies. However, this advantage cannot be fulfilled because of the several internal short circuits presented in the CHB-B2B when a conventional PWM modulation is applied. To solve this issue, a powerful math tool known as graph theory emerges as a solution for defining the converter switching matrix to be used with an appropriate control strategy, such as the model-based predictive control (MPC). Therefore, this research paper proposes a MPC with the graph theory approach applied to CHB-B2B which capable of not only eliminating the short circuit stages, but also exploring all the switching states remaining without losing the converter controllability and power quality. To demonstrate the proposed strategy applicability, the MPC with graph theory approach is tested in four different types of SST configurations, input-parallel output-parallel (IPOP), input-parallel output series (IPOS), input-series output-parallel (ISOP), and input-series output series (ISOS), attending distribution grids with different voltage and power levels. Real-time experimental results obtained in a hardware-in-the-loop (HIL) platform demonstrate the proposed strategy's effectiveness, such as DC-link voltages regulation, multilevel voltage synthesis, and currents with reduced harmonic content.

Keywords: graph theory; model-based predictive control; multilevel converters; hardware in the loop; prohibitive states matrix

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1. Introduction

The continuous growth and development of smart grids, as well as the distributed generation unit's proliferation, heterogeneous in their source, has been increasing the electrical power systems complexity [1,2], changing its behavior, having been passive and static, and now becoming more active and dynamic [3]. As a result, there has been an increase in connected power electronics-based devices to maintain the electrical power systems' stability and power quality providing acceptable voltage levels, harmonic distortions, minimum supply interruptions, and minimum power losses, thus limiting their vulnerability and improving their reliability [4]. In addition to the power electronics-based devices, a significant improvement in communication, control, and information systems should also be performed to accomplish smart grid functionalities applied to electrical power systems.

Among the engineering solutions presented to modernize electrical power systems, the use of the mathematical tool known as graph theory is widespread. In a simplified way, the graph theory was initially proposed by Euler in 1736 as a solution to the problem of Königsberg's seven bridges and referred to the study of relationships between objects of a given set [5]. The graph theory representation greatly facilitates the development of almost intuitive algorithmic rules [6]. Thus, the correspondence between each element provided by such a theory is similar to many kinds of engineering systems, being able to provide solutions that can be applied in problems related to information systems [7], electrical power systems [8], communication systems [9], and others [10,11].

More specifically, in the electrical power systems branch, graph theory helps to solve several problems through graphical representations, called graphs, facilitating the visualization and converting the behavior of certain systems [8].

For example, in [12,13], graph theory is used to calculate the impedance matrix through nodal and branching analysis for fault current determination. In [14], the authors proposed a new method for allocating losses for hybrid electricity market using a system behavior loop-based representation using graph theory concepts. In [15], a graph representation was used to deal with self-healing algorithms applied to automated distribution grids. In [10], a graph analysis was performed to guarantee optimal phase measurement unit (PMU) placement for complete system observability.

In addition, graph theory also can be used in power flow estimations for three-phase unbalanced distribution grids [16], power distribution grids reinforcement against voltage sags [4], and aids in autonomous decision making, utilizing topological properties of radial grids [15]. Furthermore, graph theory can also be used in power electronics-based devices, for optimal power flow control in transmission systems with Flexible AC transmission systems (FACTS) [17] and energy balance in multi-input and multi-output buck-boost converters [18].

Recently, also for power electronics-based devices, some researchers proposed the use of graph theory for mapping all the possible switching states of multilevel converters, applied to motor drive [19], static synchronous compensation (STATCOM) [20,21], and solid-state transformers (SST) applications [2]. In fact, these works use the semiconductor switches to map all existing current paths, identifying prohibitive states, resulting in a switching matrix containing only the possible device combinations. However, these works only present the graph theory application results, for example, the prohibitive states matrix, combined with a model-based predictive control (MPC), to suppress short circuit states inherent to the studied topologies.

Thus, this research paper presents in detail the graph theory methodology applied to multilevel converters for mapping the possible switching states. Cascaded multilevel converters with a back-to-back configuration (CHB-B2B) in different arrays such as input-parallel output-parallel (IPOP), input-parallel output-series (IPOS), input-series output-parallel (ISOP), and input-series output-series (ISOS), are adopted to show the proposed methodology's scalability. The dynamic CHB-B2B equations and the MPC strategy developed by the authors are also presented in this research paper. The simulation results in the Simulink/MatLab platform and real-time experimental results obtained in a hardware-in-the-loop (HIL) platform demonstrate the proposed strategy's effectiveness.

The paper is structured as follows: Section 2 presents the short circuit limitation of the cascaded multilevel converters with a back-to-back configuration (CHB-B2B). The proposed graph theory methodology for mapping the possible switching states is detailed in-depth in Section 3, and a brief review of the MPC principles is approached in Section 4. Section 5 details generalized modeling for multiple CHB-B2B converter modules, while Section 6 presents the simulation results in the Simulink/MatLab platform for a 4-modules CHB-B2B in four different arrays. Section 7 presents the real-time experimental results of the Typhoon HIL platform for a 2-modules CHB-B2B in four different arrays, followed by the conclusions in Section 8.

2. Cascaded Multilevel Converters with a Back-to-Back Configuration (CHB-B2B)

The use of equipment based on multilevel converters has developed in a consistent and promising way, developing various equipment, such as back-to-back converters for driving motors or static loads connection; solid-state transformers (SST) for connecting a wide variety of energy sources and grid power flow control; unified power quality conditioners (UPQC) to actively improve the power grid quality; static synchronous compensation (STATCOM) for reactive power compensation, stability improvement, harmonic mitigation, power factor control; and others [19,22–25].

Furthermore, the increase in voltage levels due to the greater demand for electrical energy has increasingly required the use of multilevel converters to enable direct connections to the medium voltage grid without exceeding the semiconductor switches' constructive limits. However, the converters' structural complexity increases considerably with the rise in their voltage levels, making their design and especially their control more difficult. Figure 1 graphically illustrates the number of the components by voltage levels ratio evolution of classical multilevel converter topologies, namely diode-clamped multilevel converter (DCMC); capacitor-clamped multilevel converter (CCMC); modular multilevel converter (MMC); and cascaded H-bridge multilevel converter (CHB). As can be seen in Figure 1, the CHB topology can achieve higher voltage levels with fewer components (it is considered a half-bridge configuration for MMC topology). Furthermore, due to its modular structure, the CHB enables straightforwardly the additional of series cells connection if an output voltage increase is required without any need for including clipping circuits [26].

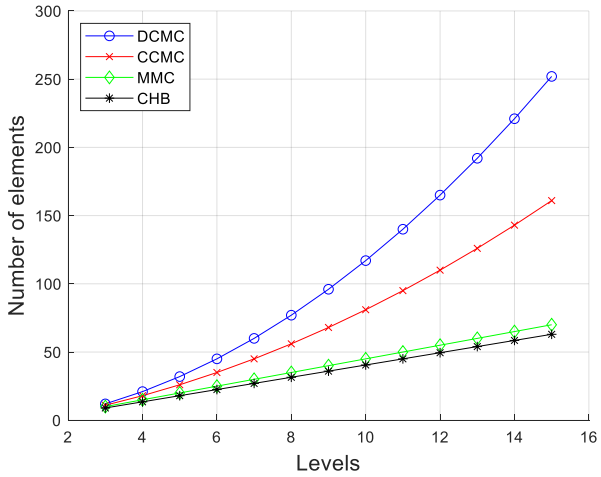


Figure 1. Comparison between classical multilevel converter topologies.

Figure 2 shows a single-phase CHB multilevel converter with three B2B modules, composed of six H-bridge cells, with an input series and output-parallel (ISOP) arrays. Other arrangements are developed in Section 5 to demonstrate the proposed graph theory methodology scalability.

The CHB-B2B structure presents singularities regarding the control strategies used, such as the impossibility to drive this topology through conventional pulse width modulation (PWM) due to the appearance of several internal short circuit states, as highlighted in Figure 2. For example, for the 3-modules CHB-B2B in the ISOP array, the converter has 24 semiconductor switches, totaling 2^{12} different switching states (4096), of which 104 switching states are valid and do not generate internal short circuits, representing approximately only 2.5% of the converter total switching states. This limitation corroborates the importance of developing an automatic methodology for mapping all the prohibitive converter states. Thus, the proposed mapping graph theory methodology is addressed in Section 3 to support the MPC strategy used to control the CHB-B2B converter.

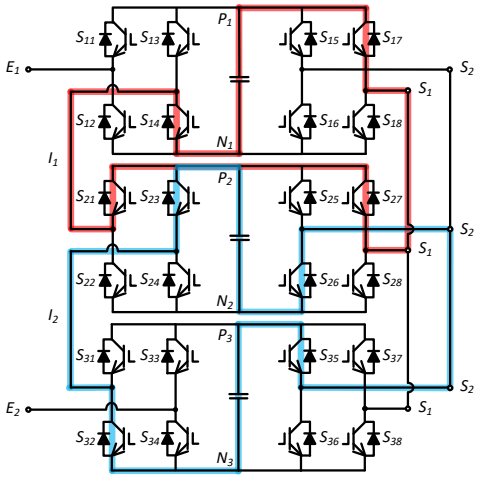


Figure 2. CHB-B2B with 3 modules in the ISOP array.

3. Graph Theory Methodology for Mapping the Possible Switching States

As mentioned, a CHB-B2B structure applied as a static converter to achieve some control objective may generate internal short circuits according to the switching performed, making it necessary to find out in which switching states this event is observed. This can be done from a circuit visual inspection. However, the bigger it is, the greater the complexity of this task. Moreover, it is not possible to know whether all the prohibitive states have been found, making this strategy inefficient and doubtful. Hence, an efficient alternative solution that arises to this question is the use of graph theory.

A graph is a mathematical structure used to model relationships between objects of a certain set and is defined as $G = G(V, E)$, in which V is a non-empty finite set of elements denominated as vertices, and E is a set of subsets $\{u, v\}$, where u,v ϵ V are denominated as edges. A graph can be directed or not, in which for the first case, the edges will consist of ordered pairs called arcs. Thus, an $e = \{u, v\}$ arc will be directed from u (head) to v (tail). From a graph, it is possible to trace paths, which can be informally defined as a sequence of vertices and edges, without repetition. A path that does not have loops, orientation and multiple edges is defined as simple. A path that starts and ends at the same vertex consists of a cycle. However, a graph that does not fulfill this condition is called acyclic. In the case that in a graph there is at least one path that interconnects any pair of its vertices, it is called a connected graph. If this same graph is acyclic, it will consist of a tree [27].

In the graph theory universe, some algorithms can be used to trace specific paths. Among them, breadth-first search (BFS) appears as an option to find all possible simple paths from one vertex to another. This algorithm is used for either directed or undirected graphs, and briefly, its working principle consists of the following: starting from an origin vertex u, the BFS algorithm explores systematically the edges of a graph to find all other vertices that are reachable from vertex u and computes the distance between them. The algorithm produces a u-origin tree that contains all reachable vertices. For each vertex v attainable from the origin vertex u, the simple path that connects these two vertices in the obtained tree will also consist of the shortest path that connects these elements in the analyzed graph [28].

Considering electrical nodes as vertices, and electrical switches as edges, a CHB-B2B electrical circuit can be modeled as a connected and undirected G graph [29] (Figure 3) for a namely 3-modules CHB-B2B in ISOP array (Figure 2), where the vertices of the resulting graph are highlighted (P_1, P_2, P_3, N_1, N_2, N_3, E_1, E_2, S_1, S_2). The list of edges of the formed graph and a correlation of these with the static switches are presented in Table 1. As can be observed, three paths are tracked in Figure 3. The red one corresponds to the short circuit highlighted in red in Figure 2. The others, in blue, correspond to distinguish paths that form the short circuit highlighted in blue in Figure 2.

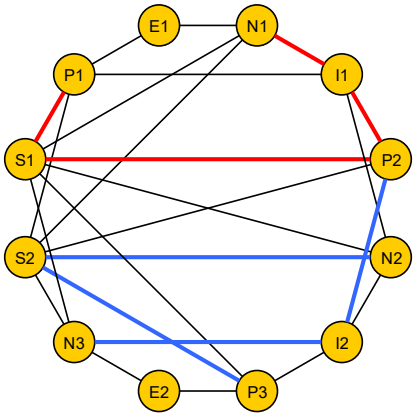


Figure 3. *G* graph of the 3-modules CHB-B2B in the ISOP array.

Table 1. Edge list for *G* graph of the 3-modules CHB-B2B in ISOP array.

Module 1			Module 2			Module 3		
Edge $\{u, v\}$		Switch	Edge $\{u, v\}$		Switch	Edge $\{u, v\}$		Switch
P_1	E_1	S_{11}	P_2	I_1	S_{21}	P_3	I_2	S_{31}
E_1	N_1	S_{12}	I_1	N_2	S_{22}	I_2	N_3	S_{32}
P_1	I_1	S_{13}	P_2	I_2	S_{23}	P_3	E_2	S_{33}
I_1	N_1	S_{14}	I_2	N_2	S_{24}	E_2	N_3	S_{34}
P_1	S_1	S_{15}	P_2	S_1	S_{25}	P_3	S_1	S_{35}
S_1	N_1	S_{16}	S_1	N_2	S_{26}	S_1	N_3	S_{36}
P_1	S_2	S_{17}	P_2	S_2	S_{27}	P_3	S_2	S_{37}
S_2	N_1	S_{18}	S_2	N_2	S_{28}	S_2	N_3	S_{38}

To find all the converter prohibitive switching states, initially, the conditions that can lead to a short circuit must be defined, which are as follows: the terminals of each capacitor become shorted (as highlighted in red in Figure 2), and the opposite terminals of a group of capacitors become connected (as highlighted in blue in Figure 2), which implies a ring with series connections of these capacitors. This results for the topology are used as an example, in the interconnections between capacitors, as it is shown in Figure 4. Thus, by finding simple paths in a graph that interconnect vertices which represent both terminals of a capacitor ($[P_1, N_1]$, $[P_2, N_2]$, $[P_3, N_3]$), it is possible to visualize part of the prohibitive switching states, which results in circuits like the ones highlighted in Figure 4a–c. The other part of the prohibitive switching states is obtained by joining disjoint paths (paths that do not share any vertex) that interconnect different pairs of opposite terminals for any number of capacitors ($[P_1, N_2]$, $[P_1, N_3]$, $[P_2, N_1]$, $[P_2, N_3]$, $[P_3, N_1]$, $[P_3, N_2]$). These paths must be disjointed because an electric current flows "from one vertex to another", without repetition. Thus, vertex sequences $[P_1, N_2, P_2, N_1]$, $[P_1, N_3, P_3, N_1]$, $[P_2, N_3, P_3, N_2]$, $[P_1, N_3, P_3, N_2, P_2, N_1]$ and $[P_1, N_2, P_2, N_3, P_3, N_1]$ can be formed, which will have the same meaning of circuits as the ones highlighted in Figure 4d–h, respectively.

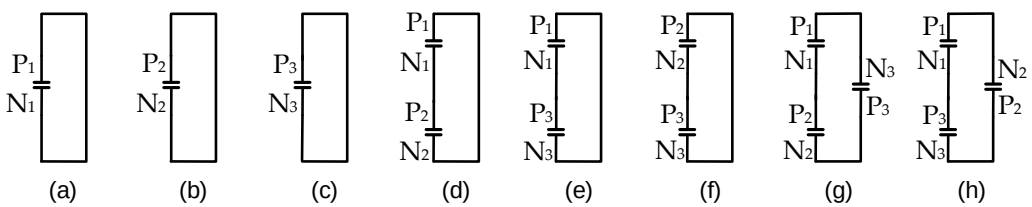


Figure 4. Possible example of one capacitor (**a**–**c**), two capacitors (**d**–**f**) and three capacitors (**g**,**h**) interconnections topology.

All these paths can be found using a modified BFS algorithm. However, the algorithm should be able to ignore paths that represent obvious short circuits, such as those that occur when two switches of the same H-bridge's leg are turned on. This condition itself is ignored by the converter control law, which should interlock these switches, limiting the sample space of the switching possibilities, reducing it to 2^L states, where L is the number of legs in the converter topology.

The biggest challenge that emerges from this task is to check all possible combinations that form the mentioned ring with a series capacitor connection, which increases exponentially, as there is an increment in the number of the capacitors. A short circuit could occur with two, or as many capacitors the topology has, and their position into the series connection could be permuted, with each representing a different converter switching state. To solve this issue, a possible solution is to apply an abstraction that models a new directed graph named H, in which vertices consist of a representation of terminals' pairs from different polarities and capacitors (P_1N_2, P_1N_3, P_2N_1, P_2N_3, P_3N_1, P_3N_2). Notably, each of these H vertices correspond to a set of traced paths that interconnect the G graph vertices. Meanwhile, the edges will interconnect vertices whose negative terminal on the first corresponds to the same capacitor as the positive terminal of the second vertex (e.g., [P_1N_2, P_2N_3]), as shown in Table 2 for 3-modules CHB-B2B in the ISOP array. Figure 5 presents the resulting H graph.

Table 2. Edge list for H graph of the 3-modules CHB-B2B in ISOP array.

Arcs {*u*, *v*}	
u	***v***
P_1N_2	P_2N_1
P_1N_2	P_2N_3
P_1N_3	P_3N_1
P_1N_3	P_3N_2
P_2N_1	P_1N_2
P_2N_1	P_1N_3
P_2N_3	P_3N_1
P_2N_3	P_3N_2
P_3N_1	P_1N_2
P_3N_1	P_1N_3
P_3N_2	P_2N_1
P_3N_2	P_2N_3

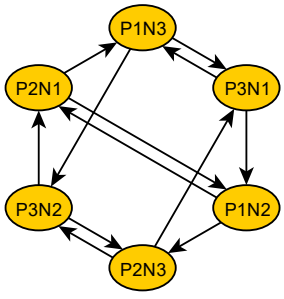


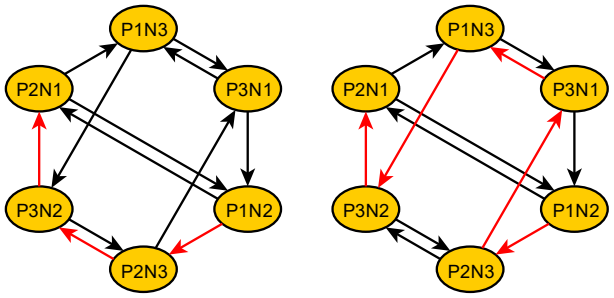
Figure 5. H graph of the 3-modules CHB-B2B in ISOP array.

Finally, all possible combinations of interconnection between the capacitors are obtained using BFS from the tracing of some possible paths that respect certain laws. Each path must have a source u and a target vertex v in which the positive terminal index of the representation of a vertex u coincides with the negative terminal index of the representation of a vertex v (e.g., [P_1N_3, P_2N_1]), as shown in Table 3 for the 3-modules CHB-B2B in ISOP array. However, not all possible paths found generate only one short circuit possibility for series-connected capacitors. Indeed, there are some restrictions, such as paths being unable

to have vertices with the same positive terminal index in the corresponding interconnection (e.g., P_1N_2 and P_1N_3). Moreover, paths cannot have vertices that have the same negative terminal index (e.g., P_1N_2 and P_3N_2) in the corresponding interconnection. These restrictions are necessary, as they represent interconnections between capacitors with multiple short circuits and would only consist of unnecessary redundancies. Two cases in which this situation occurs in the H graph are highlighted (in red) in Figure 6, where the connection between the vertices P_1N_2 with P_2N_1 is performed.

Table 3. Auxiliary table to track H graphs.

Paths Construction	
Source	**Target**
P_1N_2	P_2N_1
P_1N_2	P_3N_1
P_1N_3	P_2N_1
P_1N_3	P_3N_1
P_2N_1	P_1N_2
P_2N_1	P_3N_2
P_2N_3	P_1N_2
P_2N_3	P_3N_2
P_3N_1	P_1N_3
P_3N_1	P_2N_3
P_3N_2	P_1N_3
P_3N_2	P_2N_3



(**a**) (**b**)

Figure 6. Excluded paths (**a**,**b**) to define capacitors' interconnections.

Figure 7 elements show the possible paths (in blue) that can be traced with the BFS algorithm for the 3-modules CHB-B2B in the ISOP array. It can be highlighted that Figure 7a,e represent the same capacitors interconnection, and the same thing occurs for other Figure 7 elements, such as Figure 7b,g,j; Figure 7c,f,k; Figure 7d,i; and finally, Figure 7h,l. Relating all the paths shown in Figure 7 with Figure 4 elements, it can be observed that the elements Figure 7a–d,h represent the connection conditions of Figure 4d–h, respectively.

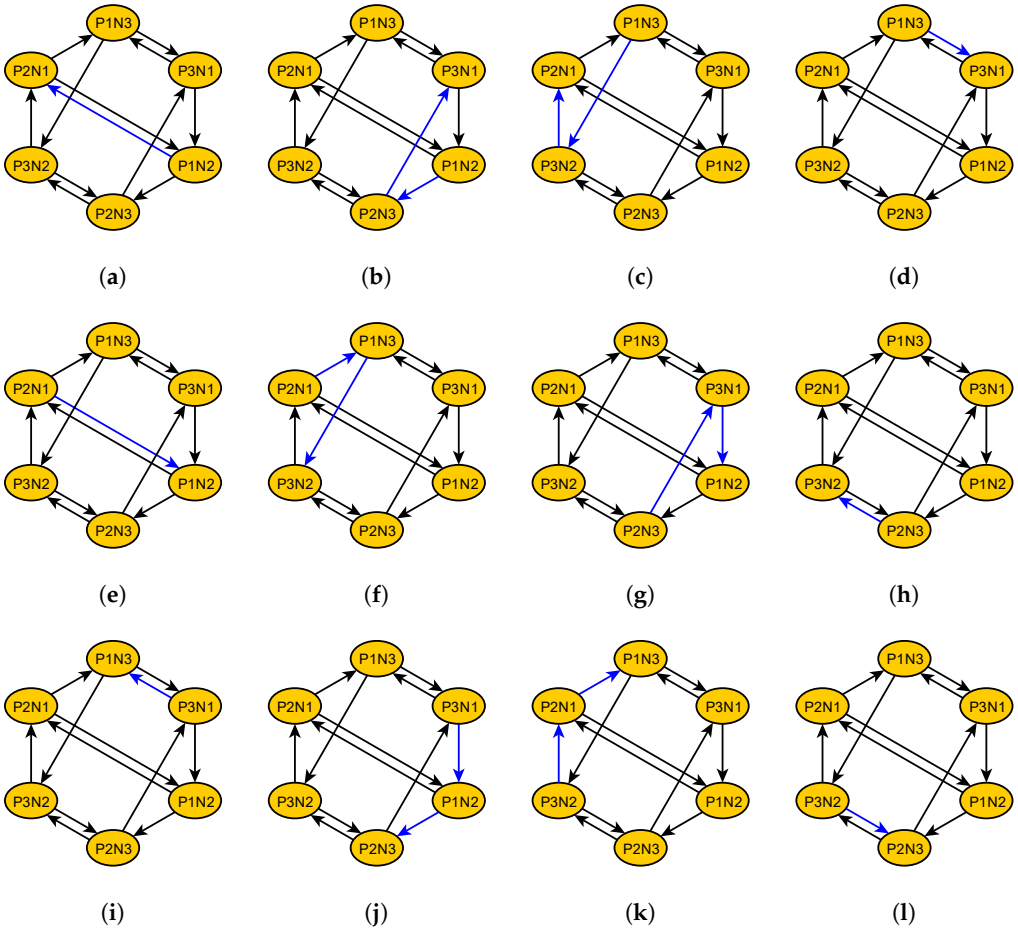


Figure 7. Desired paths (**a**–**l**) to define capacitors' interconnections.

As discussed, with the results obtained from paths traced in the H graph, each vertex of these paths corresponds to a set of paths traced in the G graph, which can be combined to obtain a physical path of the electric current that represents a state of the short circuit in the converter. For each finally obtained path, the union of consecutive vertices to be visited corresponds to an edge, which has the physical meaning of a static switch with an ON state. The edges that are not part of the analyzed path have an indeterminate state, being able to assume ON and OFF values. Thus, a converter's prohibitive switching matrix containing all the prohibitive switching states of the converter can be formed and used to obtain the valid converter switching matrix from a matrix containing all possible switches.

Figure 8 presents a flowchart overview of the proposed strategy to obtain the desired converter switching matrix.

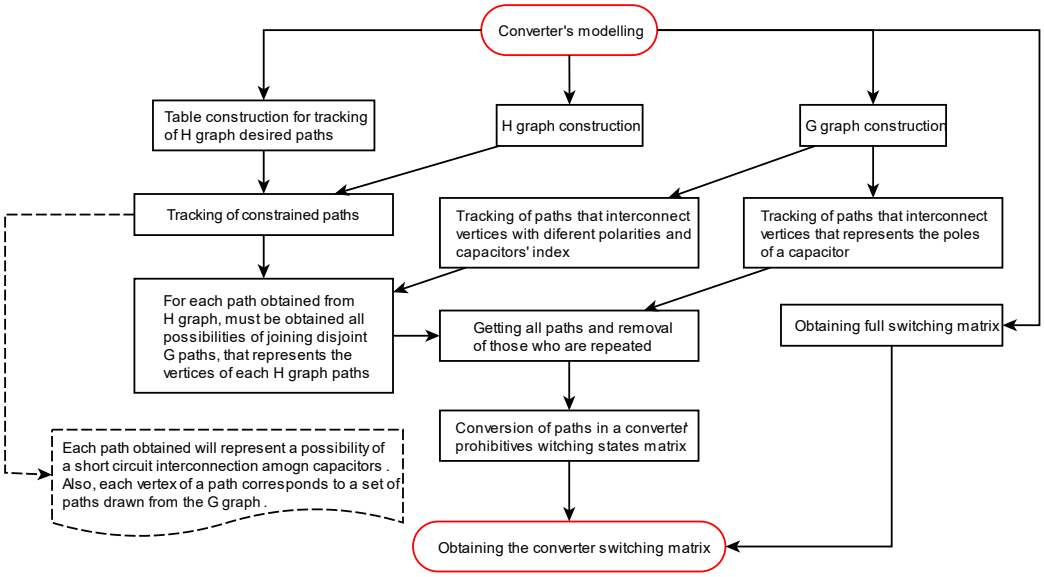


Figure 8. Flowchart of a methodology based on graph theory to identify prohibitive states of CHB-B2B converters' switching matrices.

4. Model Predictive Control (MPC)

Model predictive control, initially introduced in the process industry in the 1970s, addresses a broad concept, consisting of predicting all system future states in a given time horizon, based on a mathematical model [30–34]. An optimized control action is then chosen to minimize a function that is based on a reference and predicted states, also known as a cost function. The use of MPC in power electronics began in the 1980s in low switching frequency applications since higher switching frequencies require more complex calculations due to the fact that cost function optimization requires a lot of computational effort, which was not available at that time [30,31,35,36]. It was only from the 1990s onwards that this technology had a leap of development due to the great technological advance of microprocessors capable of performing a large number of mathematical operations. Thus, the interest in using the MPC in applications with previously unfeasible high switching frequency has intensified, gaining the attention of power electronics researchers. Furthermore, the MPC is a simple and intuitive way to control the converters, being capable of dealing with multivariable goals, with good controllability, fast dynamic response, and the capacity to incorporate, in a straightforward way, nonlinearities and constraints into the control law [37]. MPC is divided into two classes regarding the optimization problem nature, as shown in Figure 9.

Due to the discrete characteristics of power electronics applications, the finite control set MPC (FCS-MPC) makes their implementation simpler since it does not require modulation techniques to act on the converter [30,37,38]. The optimal switching vector MPC (OSV-MPC) was the first predictive control strategy adopted in power electronics applications and is still the most widely used today due to its low implementation complexity and rapid dynamic response. However, as a disadvantage, this class presents a variable switching frequency. Nevertheless, some studies aim to minimize the frequency harmonic spectrum dispersion by incorporating specific goals into the cost function [38,39].

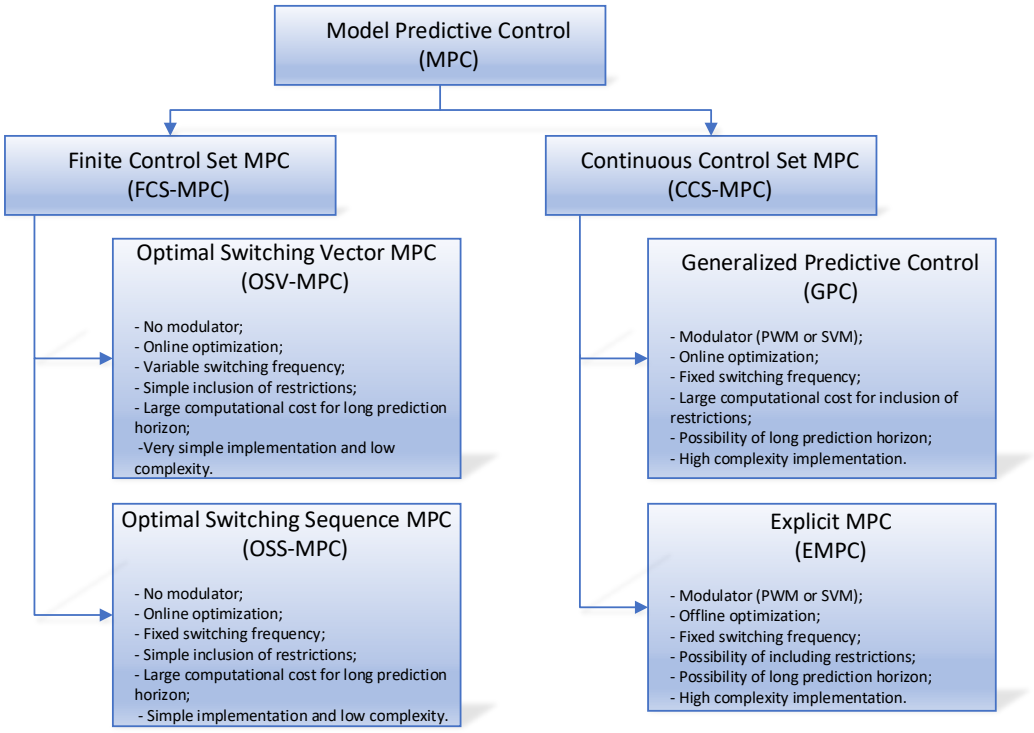


Figure 9. Model predictive control classification.

Power electronics-based systems have as their main characteristic the finite number of switching states, so in power electronics converters, the control action is limited to the set of switching states possible in the converter, making the MPC an option that is feasible and easy to implement. Its cost function is directly associated with the controlled variables set.

At each sampling time, the microprocessors perform various calculations and predict the variables future for each possible switching state based on the predictive model, measurements and system states. Then, the switching state with the lowest cost is applied to the converter. Thus, this control technique is intrinsically linked to the switching process, dispensing the use of a modulation technique.

Although the MPC is an open-loop optimization algorithm, when repeated at each sampling time, it behaves like a feedback loop control based on optimization, making its dynamic response quick in the face of reference variations or disturbances [30].

5. CHB-B2B Converter Modeling

The presented strategy based on graph theory to obtain the switching matrix of any CHB-B2B converter is evaluated via computational simulations (Section 6) and physical implementation through an HIL platform (Section 7). Thus, different CHB-B2B configurations are proposed, and the MPC principles are applied as a control strategy. Therefore, it is necessary to determine the whole system, the filters designs, the control goals, and the mathematical models for predicting the control variables for the different proposed topologies. All these steps are presented in this section.

5.1. Generalized M-Modules CHB-B2B Converter

Figure 10 presents a generalized representation of the M-modules CHB-B2B converter, in which the input array and output array blocks (hatched areas) consist of series or parallel connections between the different converters' H-bridge cells. The index m represents which converter module that a given variable is referring to. On the other hand, the variable n is related to the side of the converter. Thereby, for the module's currents in each module highlighted above, i_{1m} is considered the current on the primary side ($n = 1$) of the m'th module, and i_{2m} as the current on the secondary side ($n = 2$) of the m'th module. In a

similar way, V_{dcm} represents the DC-link voltage of the m'th module, v_{1m} is the switched voltage on the primary side ($n = 1$) of the m'th module, and v_{2m} is the switched voltage on the secondary side ($n = 2$) of the m'th module. Either the primary or secondary converter sides are connected to electrical grids, with the power flow from the first one (v_{g1}) to the second (v_{g2}). Thus, the main objective control is to synthesize an appropriate power quality output current i_2, necessitating a voltage balance in the DC-links through their capacitances. Consequently, the converter's power flow control must be achieved by controlling the primary input current i_1. Both current controls can be obtained by applying an inductive filter with a small resistance representing electrical losses. However, the design of these elements may be hampered due to the variable switching frequency inherent in the OSV-MPC strategy.

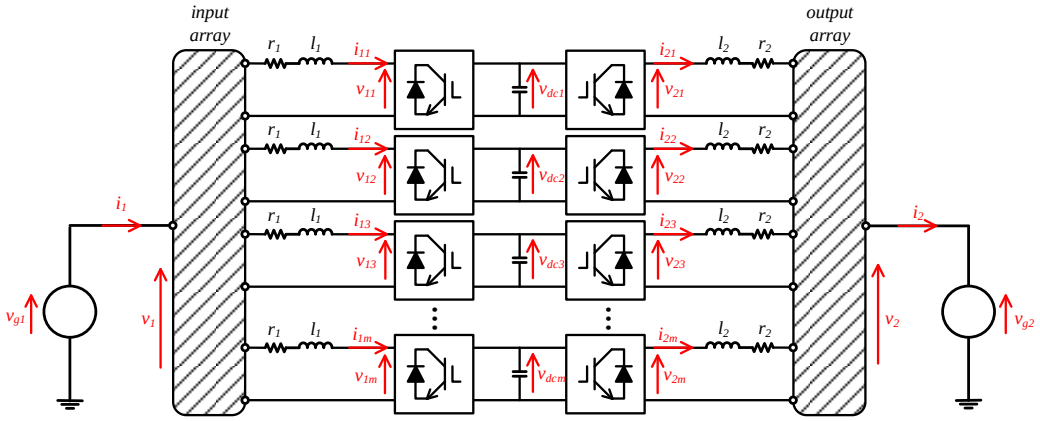


Figure 10. A generalized representation of a m-modules CHB-B2B converter.

As it can be noted, for the converter's primary side, if the input array consists of a series connection between the H-bridge cells, the input current i_1 is equal to each module's primary current (i_{1m}). The same thing occurs for the converter's secondary side, in which, for a series connection output array, the output current i_2 is the same as the module's secondary current (i_{2m}). However, inversely, the switched voltages v_1 and v_2 consist in the summation of each module's switched voltages that composes each side of the converter (e.g., $v_1 = \Sigma_1^M v_{1m}$ and $v_2 = \Sigma_1^M v_{2m}$). For a different condition, with an input and output array consisting of parallel connection, input and output current (i_1 and i_2, respectively) now consist in the summation of each module's currents (e.g., $i_1 = \Sigma_1^M i_{1m}$ and $i_2 = \Sigma_1^M i_{2m}$).

5.2. Primary/Secondary Inductive Filters and DC-Link Capacitances

The design of the currents' filters can be obtained by the following methodology. Defining the nominal rating of the DC-link voltage as V_{dc}, the maximum allowed variation of the filter current in each module as Δ_{inm} and f_s as the switching frequency of the converter, the required filter inductance for any module of the n side of the converter (primary and secondary) can be calculated with Equation (1). The value of Δ_{in} which defines Δ_{inm} (according to connection type and number of modules) can be determined from a defined percentage of the nominal filter current peak value $i_{n,pk}$; in this research paper, a value of 5% is considered. For the OSV-MPC control strategy, as the switching frequency is variable due to the dispersed harmonic spectrum, f_s is considered as the control's operation frequency, which corresponds to the inverse of the sampling period T_s.

$$l_n = \frac{V_{dc}}{2\Delta_{inm} f_s} \tag{1}$$

The procedure to calculate the value of $i_{n,pk}$ is presented in (2), in which P_T corresponds to the power demanded by the converter, and V_{gn} is the grid nominal effective value.

$$i_{n,pk} = \sqrt{2} i_n = \sqrt{2} \frac{P_T}{V_{gn}} \tag{2}$$

For modeling the parasitic resistance present in each filter (r_n), its value is adopted as a percentage of the reactance relative to the filter's inductance, as described by Equation (3), where f_g corresponds to the primary grid frequency.

$$r_n = \frac{X_{ln}}{100} = \frac{2\pi f_g}{100} \tag{3}$$

The DC-link capacitance design for the m'th module (C_{dcm}) can be obtained from Equation (4) by setting the desired voltage ripple variation ΔV_{dc} and from the already defined variable P_T [20], where ω is the angular velocity defined as $2\pi f_g$, and M is the number of modules connected in a back-to-back configuration in the converter. The value of ΔV_{dc} can be determined from a defined percentage of the nominal DC-link voltage V_{dc}. In this research paper, a value of 1% is considered for ΔV_{dc}.

$$C_{dcm} = \left(\frac{1}{M}\right) \frac{P_T}{\omega V_{dc} \Delta V_{dc}} \tag{4}$$

After defining the filters' structures and the elements of the system, the mathematical models of the controlled electrical variables for MPC application can be obtained and are described in the next sections for different CHB-B2B converter configurations. Furthermore, a cost function is defined to fulfill the OSV-MPC strategy and its minimization defines the optimal switching sequence. For its construction, the reference variables must be defined according to the control objectives.

5.3. Mathematical Models and Cost Function for Different Topologies

The OSV-MPC strategy implementation requires the dynamic equations for the converter's primary and secondary currents, and for the DC-links voltage that must be regulated for a nominal value. Considering S_{mj} representing the j'th S switch in the m'th converter's module (e.g., Figure 2), it can be determined Equations (5) and (6) that express the state of each primary or secondary H-bridge cells of the m'th module, defined as d_{1n} and d_{2n}, respectively. Consequently, according to the switches' states, d_{1n} and d_{2n} can assume the values set of $(-1, 0, 1)$.

$$d_{1m} = S_{m1} S_{m4} - S_{m2} S_{m3} \tag{5}$$

$$d_{2m} = S_{m5} S_{m8} - S_{m6} S_{m7} \tag{6}$$

Therefore, the following relationships can be defined, according to the realized connection's type. For series connections, Equations (7) must be used, while for parallel connections, Equation (8) is valid.

$$v_n = \sum_{m=1}^{M} d_{nm} V_{dcm} \tag{7}$$

$$i_n = \sum_{m=1}^{M} d_{nm} i_{nm} \tag{8}$$

5.3.1. Generic M-Modules ISOS (Input-Series Output-Series)

An example of an ISOS CHB-B2B configuration is highlighted in Figure 11a. The dynamic equation for the m'th module DC-link voltage level (V_{dcm}) can be obtained con-

sidering the input (i_1) and output (i_2) filters' currents and is presented in Equation (9). As can be observed, if d_{1m} has a positive and d_{2m} a negative value, the DC-link is going to be charged, whereas, for opposite values for these terms, DC-link must be discharged.

$$\frac{\mathrm{d}V_{dcm}}{\mathrm{d}t} = \frac{1}{C_{dcm}}(d_{1m}i_{1m} - d_{2m}i_{2m}) \tag{9}$$

As the control loop is composed of the grid connections and inductive filters, the dynamic models of the described i_1 and i_2 currents can be represented by Equations (10) and (11), in which v_1 and v_2 values are obtained from Equation (7).

$$\frac{\mathrm{d}i_1}{\mathrm{d}t} = \frac{1}{Ml_1}(v_{g1} - Mr_1i_1 - v_1) \tag{10}$$

$$\frac{\mathrm{d}i_2}{\mathrm{d}t} = \frac{1}{Ml_2}(v_2 - Mr_2i_2 - v_{g2}) \tag{11}$$

Figure 11b presents a diagram block that exemplifies the implementation of the OSV-MPC, necessary to achieve the control objectives, namely synthesizing the appropriate i_1 and i_2 currents, keeping the DC-links regulated. The system's electrical magnitudes (v_{gn}, i_n, V_{dcm}) are measured and, by modeling the system, these variables are predicted for a future instant. Based on the dynamic equations above, Equations (9)–(11), the discrete equations necessary for the OSV-MPC application are obtained using the Euler numerical integration method and defining $[k]$ and $[k+1]$, as the present and future instants, respectively. They are presented in Equations (12)–(14) below, considering the T_s sampling period. From these predictions and the determination of references for the control variables, a cost function is defined, whose minimization provides which switching is the most optimal in the future instant for the control objectives.

$$V_{dcm}[k+1] = V_{dcm}[k] + \frac{T_s}{C_{dcm}}d_{1m}[k]i_{1m}[k] - \frac{T_s}{C_{dcm}}d_{2m}[k]i_{2m}[k] \tag{12}$$

$$i_1[k+1] = \left(1 - \frac{r_{1m}}{l_{1m}}\right)i_1[k] + \frac{T_s}{Ml_{1m}}v_{g1} - \frac{T_s}{Ml_{1m}}v_1[k] \tag{13}$$

$$i_2[k+1] = \left(1 - \frac{r_{2m}}{l_{2m}}\right)i_2[k] - \frac{T_s}{Ml_{2m}}v_{g2} + \frac{T_s}{Ml_{2m}}v_2[k] \tag{14}$$

To obtain the OSV-MPC cost function, the next step is to define the reference signals for the V_{dcm}, i_1 and i_2 control variables, which is represented with an asterisk suffix, as presented in Figure 11b. For V^*_{dcm}, DC-link voltage nominal operating rating is used. Applying Equation (2), i^*_2 can be generated from a sinusoidal signal with f_g frequency and nominal i_2 peak value ($i_{2,pk}$). The primary reference current i^*_1 is dynamically calculated and is in phase with the v_{g1} grid voltage from PQ theory [40], together with a second order generalized integrator (SOGI) [41], as presented in Figure 11c. This current enables the power flow control to be achieved ensuring DC-links capacitance–voltage maintenance and system balance. Therefore, the cost function g^N can be defined by Equation (15), with $\overline{V_{dc}}$ consisting of the average of the DC-link voltages, where N is the valid switching states defined by the graph theory which do not result in an internal short circuit. Weights are defined to designate which control object should be prioritized: i^*_1 current synthesis (W_1), i^*_2 current synthesis (W_2), regulation of DC-links (W_{dc}), or balance of DC-links (W_{bl}). In this research paper, all weights are defined with unit values ($W_1 = W_2 = W_{dc} = W_{bl} = 1.0$). Thus, all the cost function objectives have the same importance.

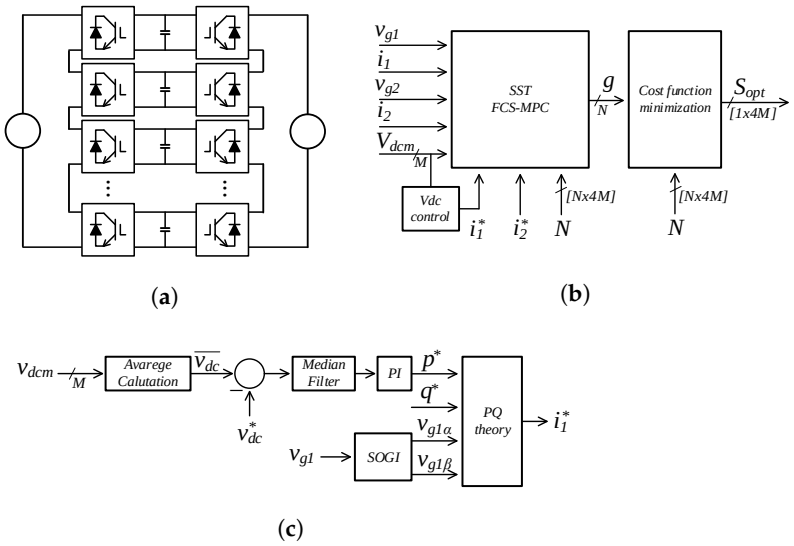


Figure 11. Generic M-modules ISOS CHB-B2B converter: (**a**) topology configuration, (**b**) MPC diagram block, (**c**) primary side current reference acquisition.

$$g_{ISOS}^{N} = \frac{W_{dc}}{M}\sum_{m=1}^{M}(V_{dc}^{*} - V_{dcm})^2 + \frac{W_{bl}}{M}\sum_{m=1}^{M}(\overline{V_{dc}} - V_{dcm})^2 + W_1(i_1^{*} - i_1)^2 + W_2(i_2^{*} - i_2)^2 \quad (15)$$

Multiple values of the cost function are obtained, totaling N values, for different switching states of the converter. The cost function minimization, that is, the switching state that produces the lowest value corresponds to an optimal switching (S_{opt}) that should be used at the time step $[k+1]$.

5.3.2. Generic M-Modules IPOP (Input-Parallel Output-Parallel)

An example of an IPOP CHB-B2B configuration is highlighted in Figure 12a. The generic dynamic Equation (9) for the m'th module DC-link voltage level (V_{dcm}) can be obtained considering the m'th module input (i_{1m}) and output (i_{2m}) currents, since in this case, they differ from the input (i_1) and output (i_2) currents of the converter, respectively. The same previous capacitor charge and discharge analysis will remain valid for this situation.

Differently for the ISOS converter case, the input (i_1) and output (i_2) currents are indirectly controlled by the individual control of each module's currents. Therefore, dynamic models of i_{1m} and i_{2m} currents are necessary and can be represented by Equations (16) and (17).

$$\frac{\mathrm{d}i_{1m}}{\mathrm{d}t} = \frac{1}{Ml_1}(v_{g1} - r_1 i_{1m} - v_{1m}) \quad (16)$$

$$\frac{\mathrm{d}i_{2m}}{\mathrm{d}t} = \frac{1}{Ml_2}(v_{2m} - r_2 i_{2m} - v_{g2}) \quad (17)$$

Figure 12b presents a diagram block that exemplifies the implementation of the OSV-MPC for IPOP configuration. The system's electrical magnitudes (v_{gn}, i_{nm}, V_{dcm}) are measured, and these variables are predicted for a future instant by the modeled system. Again, the discrete equations necessary for the OSV-MPC application are obtained using the Euler numerical integration method, using (9), (16), and (17), and they are expressed by Equations (12), (18), and (19).

$$i_{1m}[k+1] = \left(1 - \frac{r_1}{l_1}\right) i_{1m}[k] + \frac{T_s}{l_1} v_{g1} - \frac{T_s}{l_1} v_{1m}[k] \quad (18)$$

$$i_{2m}[k+1] = \left(1 - \frac{r_2}{l_2}\right) i_{2m}[k] - \frac{T_s}{l_2} v_{g2} + \frac{T_s}{l_2} v_{2m}[k] \tag{19}$$

For the cost function definition, the V^*_{dcm} reference is newly considered as the DC-link voltage nominal operating rating value. The secondary currents of m'th module (i^*_{2m}) reference values are obtained by applying Equation (2) and generating a sinusoidal signal with f_g frequency and an amplitude corresponding to the m'th part of the nominal i_2 peak value ($i_{2,pk}/M$). Similarly, to the ISOS case, i^*_{1m} references are obtained, as seen in Figure 12c, by PQ theory application together with a second order generalized integrator (SOGI). Therefore, the cost function g^N can be defined by Equation (20).

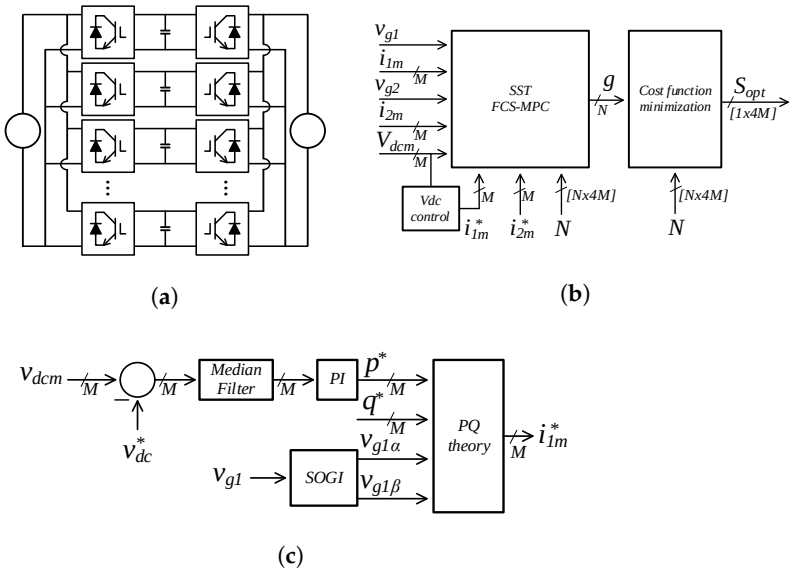


Figure 12. Generic M-modules IPOP CHB-B2B converter: (**a**) topology configuration, (**b**) MPC diagram block, (**c**) primary side currents reference acquisition.

$$\begin{aligned} g^N_{IPOP} = &\frac{W_{dc}}{M} \sum_{m=1}^{M} (V^*_{dc} - V_{dcm})^2 + \frac{W_{bl}}{M} \sum_{m=1}^{M} (\overline{V_{dc}} - V_{dcm})^2 + \\ &\frac{W_1}{M} \sum_{m=1}^{M} (i^*_{1m} - i_{1m})^2 + \frac{W_2}{M} \sum_{m=1}^{M} (i^*_{2m} - i_{2m})^2 \end{aligned} \tag{20}$$

5.3.3. Generic M-Modules ISOP (Input-Series Output-Parallel)

ISOP CHB-B2B configuration consists of recombining the ISOS and ISOP configurations which are already presented (Figure 13a). Figure 13b presents a diagram block that exemplifies the implementation of the OSV-MPC for ISOP configuration. The system's electrical magnitudes ($v_{gn}, i_1, i_{2m}, V_{dcm}$) are measured, and these variables are predicted for a future instant by the modeled system.

The primary side of this topology has the same dynamics as the ISOS configuration and, therefore Equations (10) and (13) here are also valid. The secondary side, in turn, has the same dynamics as the IPOP configuration and, therefore, Equations (17) and (19) must be considered. Finally, as previously discussed, the dynamic for m'th module DC-link voltage level (V_{dcm}) is described by Equation (9), and its discretization results in (12).

The reference signal V^*_{dcm} still consists of the nominal value of V_{dc}. The same i^*_1 reference applied in the ISOS, as presented in Figure 13c, and i^*_{2m} reference applied in the IPOP configurations is used to define the ISOP converter cost function, which is presented in (21).

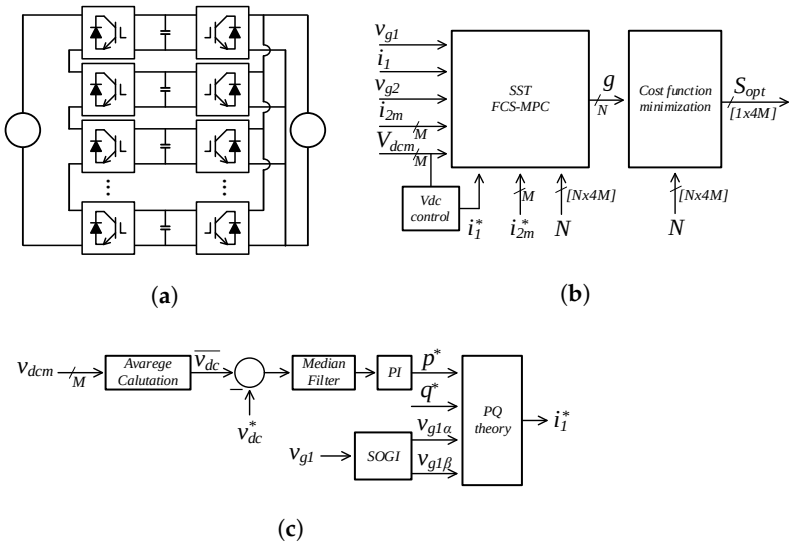


Figure 13. Generic M-modules ISOP CHB-B2B converter: (**a**) topology configuration, (**b**) MPC diagram block, (**c**) primary side current reference acquisition.

$$g^N_{ISOP} = \frac{W_{dc}}{M}\sum_{m=1}^{M}(V^*_{dc} - V_{dcm})^2 + \frac{W_{bl}}{M}\sum_{m=1}^{M}(\overline{V_{dc}} - V_{dcm})^2 + W_1(i^*_1 - i_1)^2 + \frac{W_2}{M}\sum_{m=1}^{M}(i^*_{2m} - i_{2m})^2 \quad (21)$$

5.3.4. Generic M-Modules IPOS (Input-Parallel Output-Series)

An example of an IPOS CHB-B2B configuration is highlighted in Figure 14a. This configuration consists of recombination between the IPOP and ISOS configurations, which are already presented. Figure 14b presents a diagram block that exemplifies the implementation of the OSV-MPC for IPOS configuration. The system's electrical magnitudes ($v_{gn}, i_{1m}, i_2, V_{dcm}$) are measured, and these variables are predicted for a future instant by the modeled system.

The primary side of this topology has the same dynamics as the IPOP configuration and therefore, Equations (16) and (18) here are also valid. The secondary side, in turn, has the same dynamics as the ISOS configuration and, therefore, Equations (11) and (14) must be considered. Finally, as previously discussed, the dynamic for m'th module DC-link voltage level (V_{dcm}) is described by Equation (9), and its discretization results by (12).

The reference signal V^*_{dcm} still consists of the nominal value of V_{dc}. The same i^*_{1m} reference applied in the IPOP, as presented in Figure 14c, and i^*_2 reference applied in the ISOS configurations is used to define the IPOS converter cost function, which is presented in Equation (22).

$$g^N_{IPOS} = \frac{W_{dc}}{M}\sum_{m=1}^{M}(V^*_{dc} - V_{dcm})^2 + \frac{W_{bl}}{M}\sum_{m=1}^{M}(\overline{V_{dc}} - V_{dcm})^2 + \frac{W_1}{M}\sum_{m=1}^{M}(i^*_{1m} - i_{1m})^2 + W_2(i^*_2 - i_2)^2 \quad (22)$$

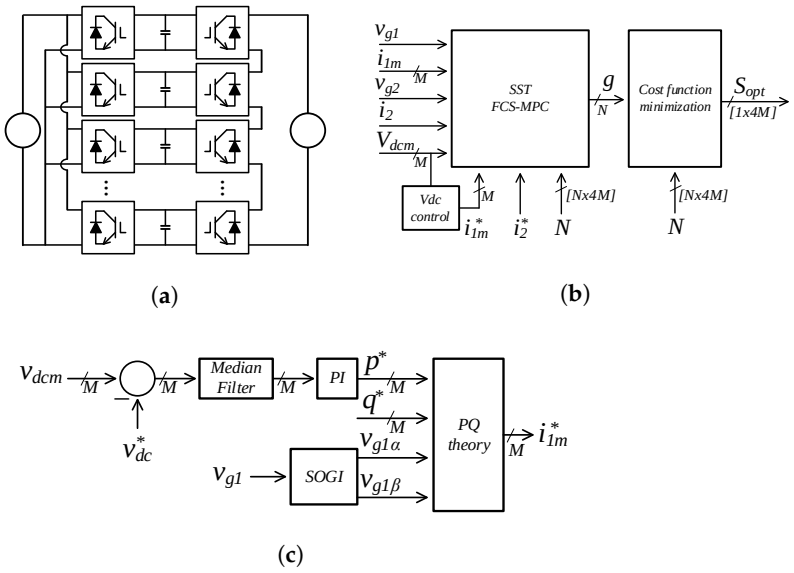


Figure 14. Generic *M*-modules IPOS CHB-B2B converter: (**a**) topology configuration, (**b**) MPC diagram block, (**c**) primary side currents references acquisition.

5.4. Graph Theory Results

From the proposed strategy based on graph theory to find the switching matrix for static converters, different results can be obtained and are presented in Table 4, which shows a review of the characteristics for different CHB-B2B topologies. Indeed, as the number of converter modules increases, the use of its switching states (U [%]) decreases, due to the increment in the possibilities of short circuits, although, at the same time, the number of valid switching states (N) increases. It is also noticed that, for the same number of modules, serial configurations present a smaller number of short circuits when compared to parallel ones. However, the main point to be highlighted is the number of levels that can be synthesized for each side of the converter. In fact, a parallel connection always synthesizes three voltage levels, but this does not occur for serial connections, where the number of modules increases, the number of possible levels to be synthesized by the converter tends to increase. For ISOS connections, all these voltage levels are achievable, therefore allowing the converter associated with a filter to have a better harmonic spectrum. However, due to the occurrence of short circuits, this does not occur for the ISOP and the IPOS configurations, in which the series side is limited to only five levels, regardless of the number of modules used.

With the increase in the number of converter modules, the switching matrix increases in an exponentially way, that is, the sample space to be analyzed by the OSV-MPC algorithm may become unfeasible for digital implementations, despite the mentioned advance in microcontrollers. As an example, shown in Table 4, the 6-module ISOS configuration control must, at each time step, perform 124,416 calculations to predict which, among 124,416 switching states, is considered optimal for the future instant. Therefore, in a first analysis, without applying some type of optimization in the control strategy, the physical implementation of this converter is unfeasible. Hence, the results presented in Table 4 demonstrate the importance of applying graph theory to the objectives proposed in this article, in which it is possible to detail the characteristics of the different configurations of CHB-B2B converters and their switching matrices, to contribute to defining the most advantageous topology and its applicability.

Table 4. Review of characteristics for different CHB-B2B converter configurations.

M	C	F	N	U [%]	LP	LS
2	ISOS	256	96	37.50	5	5
3	ISOS	4096	576	14.06	7	7
4	ISOS	65,536	3456	5.27	9	9
5	ISOS	1,048,576	20,736	1.98	11	11
6	ISOS	16,777,216	124,416	0.74	13	13
2	IPOP	256	18	7.03	3	3
3	IPOP	4096	22	0.54	3	3
4	IPOP	65,536	30	0.05	3	3
5	IPOP	1,048,576	46	*	3	3
6	IPOP	16,777,216	78	*	3	3
2	ISOP	256	40	15.62	5	3
3	ISOP	4096	104	2.54	5	3
4	ISOP	65,536	280	0.43	5	3
5	ISOP	1,048,576	776	0.07	5	3
6	ISOP	16,777,216	2200	0.01	5	3
2	IPOS	256	40	15.62	3	5
3	IPOS	4096	104	2.54	3	5
4	IPOS	65,536	280	0.43	3	5
5	IPOS	1,048,576	776	0.07	3	5
6	IPOS	16,777,216	2200	0.01	3	5

LEGEND:
M = Number of modules for the topology.
C = Configuration of the topology.
F = Number of all switching states possibilities.
N = Number of switching states for the converter.
U[%] = Converter utilization percentage (N/F).
LP = Number of synthesizable voltage levels in the converter primary.
LS = Number of synthesizable voltage levels in the converter secondary.
* Tiny value.

6. Simulation Results for 4-Modules CHB-B2B

After defining the discrete equations for each topology of the CHB-B2B, the values of the converter's elements must be projected to perform OSV-MPC. Initially, based on a 4-modules ISOS CHB-B2B topology, electrical grids having 1440 V peak voltage are considered. Therefore, the nominal value for the DC-links can be obtained from the division of the grid voltage and the number of converter modules ($\widehat{V_n}$ = 360 V), considering a modulation factor m_a, according to Equation (23). In this research paper, a 4/5 is considered since a minimum 3/4 modulation factor is necessary to obtain the nine voltage levels of this topology [42].

$$V_{dc} = \frac{\widehat{V_n}}{m_a} = \frac{v_{g,pk}}{Mm_a} \tag{23}$$

Thus, a 450 V is achieved for the DC-links voltage value, and it is used for all other CHB-B2B configurations (IPOP, ISOP, and IPOS). However, due to the limitations of these configurations caused by the smallest number of possible switches, a modulation factor of 2/3 is considered, in order to obtain a "slack" for the converter, resulting in a value of $\widehat{V_n}$ equal to 300 V.

The next step is to define other parameters, such as the switching frequency f_s, the power demanded by the converter P_T and the grid frequency f_g, for which 20 kHz, 10 kVA and 50 Hz values are respectively considered. Different switching and grid frequency values for each side of the converter could be considered.

For parallel connection sides, the value of $\widehat{V_n}$ should be considered as the peak voltage of the connected grid since the converter is limited to three voltage levels as discussed ($\widehat{V_n} = v_{g,pk}$). For mixed series/parallel configurations (ISOP, IPOS), due to the serial connection being limited to five levels, a value of $2\widehat{V_n}$ is considered as the peak voltage of

the connected grid ($2\widehat{V_n} = v_{g,pk}$). Finally, using Equations (1)–(4), Table 5 can be constructed, which shows the values of the converter elements for different configurations of a 4-modules CHB-B2B example.

Table 5. Sizing for the different configurations of the 4-modules CHB-B2B converter.

Parameter	ISOS	IPOP	ISOP	IPOS
M	4	4	4	4
f_s [kHz]	20	20	20	20
P_T [kVA]	10	10	10	10
f_g [Hz]	50	50	50	50
m_a	4/5	2/3	2/3	2/3
$\widehat{V_n}$ [V]	360	300	300	300
V_{dc} [V]	450	450	450	450
ΔV_{dc} [V]	4.5	4.5	4.5	4.5
$V_{g1,pk}$ [V]	1440	300	600	300
$i_{1,pk}$ [A]	13.89	66.67	33.33	66.67
Δi_1 [A]	0.69	3.33	1.67	3.33
Δi_{1m} [A]	0.69	0.83	1.67	0.83
$V_{g2,pk}$ [V]	1440	300	300	600
$i_{2,pk}$ [A]	13.89	66.67	66.67	33.33
Δi_2 [A]	0.69	3.33	3.33	1.67
Δi_{2m} [A]	0.69	0.83	0.83	1.67
C_{dcm} [mF]	3.93	3.93	3.93	3.93
l_1 [mH]	16.20	13.50	6.75	13.50
r_1 [Ω]	0.05	0.04	0.02	0.04
l_2 [mH]	16.20	13.50	13.50	6.75
r_2 [Ω]	0.05	0.04	0.04	0.02

6.1. 4-Modules CHB-B2B Simulation Results

From the dimensioning performed and presented in Table 5 for different configurations of 4-modules CHB-B2B converters, the graph theory application as a solution to obtain the switching matrix of these converters can be validated. The steady-state performance of the OSV-MPC control systems presented in this section is verified via simulation, through the Simulink/Matlab computational platform, to confirm the non-occurrence of internal short circuits in the converter and that the control objectives are reached.

6.1.1. 4-Modules ISOS Configuration

The results of the 4-modules ISOS CHB-B2B topology are presented below, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), DC link voltages (V_{dcm}) and the switching voltages on the primary (v_1), secondary (v_2) of each converter module (v_{nm}) are highlighted. As can be seen in Figure 15a,b, the converter can synthesize the expected nine voltage levels, both on the primary and secondary sides. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 15c shows that the DC-links could be tuned to nominal values, as compared to the V_{dc}^* reference, which is essential for the correct control operation. However, as CHB does not have natural three-phase characteristics, the DC-links voltages present an oscillation with the double of the fundamental grid frequency (50 Hz) [20]. In Figure 15c, a maximum 2 V (0.44%) oscillation in the magnitude is observed, which conforms to the DC-link design requirements (4.5 V).

The currents in the primary and secondary of the converter are verified in Figure 15d,e, respectively. As can be seen, they satisfactorily follow the i_1^* and i_2^* references and are in phase with the v_{g1} and v_{g2} grid voltages, making the converter power factor unitary. A maximum 0.2 A (1.44%) oscillation in i_1 is obtained, while for i_2, a 0.14 A (1%) value is observed, which conforms to the filter design requirements (0.69 A). Finally, it can be

concluded that the control system operates properly, making it possible to affirm that the used converter switching matrix eliminates all the prohibitive switching states.

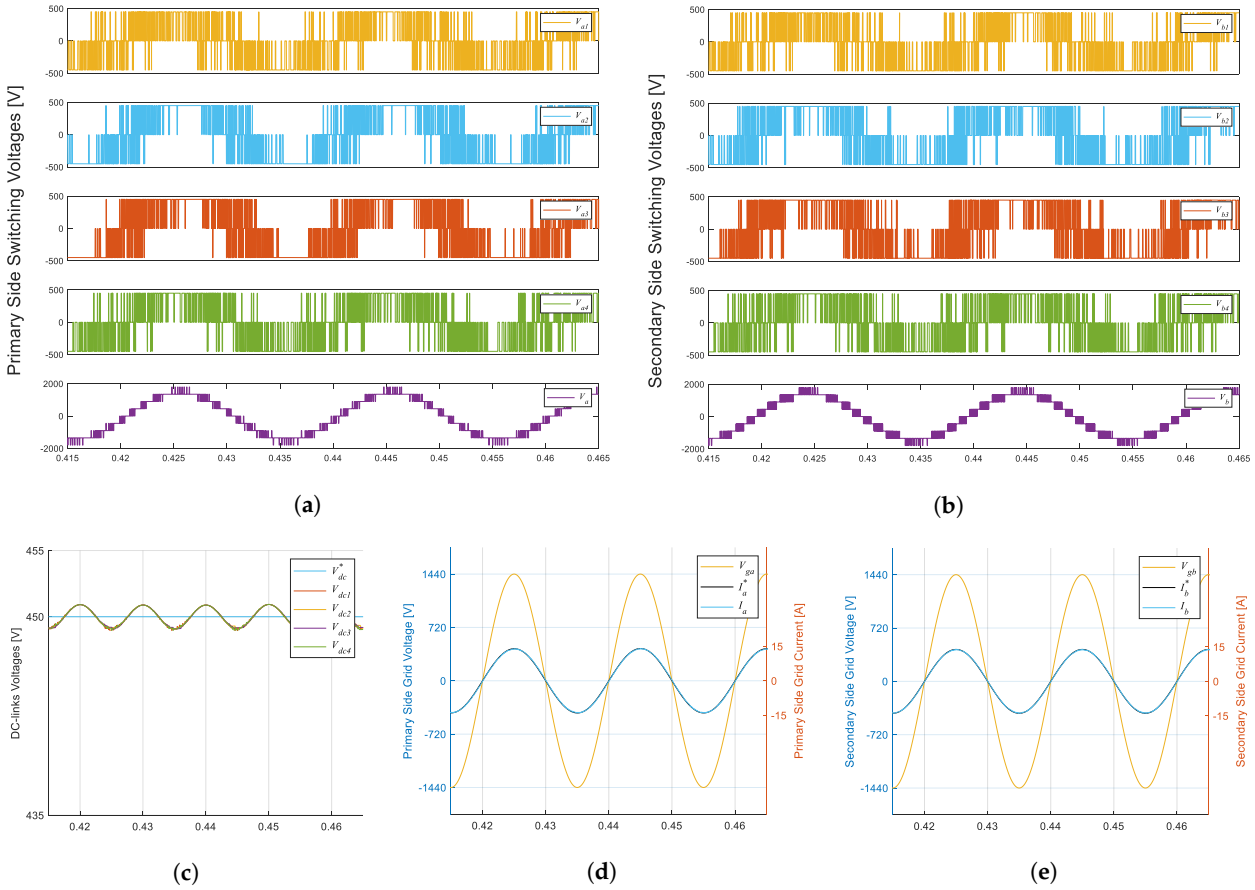


Figure 15. The 4-modules ISOS configuration simulation results: (**a**) primary side switching voltages, (**b**) secondary side switching voltages, (**c**) DC-links voltages, (**d**) primary side grid voltage and current, (**e**) secondary side grid voltage and current.

6.1.2. 4-Modules IPOP Configuration

The results of the 4-modules IPOP CHB-B2B topology are presented below, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), modules' currents (i_{nm}), DC link voltages (V_{dcm}) and switching voltages of each converter module (v_{nm}) are highlighted. As can be seen in Figure 16a,b, the converter can synthesize only three voltage levels, both on the primary and on the secondary sides, as it is expected. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 16c shows that the DC-links could be tuned to nominal values. Compared to the V_{dc}^* reference, a maximum 2.5 V (0.55%) oscillation in the magnitude is obtained, which conforms to the DC-link design requirements (4.5 V). The currents in the primary and secondary of the converter are verified in Figure 16d,e, respectively. As it can be seen, they satisfactorily follow the i_1^* and i_2^* references and are in phase with the v_{g1} and v_{g2} grid voltages, making the converter power factor unitary. Each primary module's currents which constitute i_1 are the same and they are superimposed on the graph. The same thing happens for the currents that constitute i_2.

A maximum of 2.15 A (3.25%) oscillations in i_1 and i_2 current components are observed, which conforms to the filter design requirements (3.33 A). Finally, the control system operates properly, which affirms that the used converter switching matrix eliminates all the prohibitive switching states.

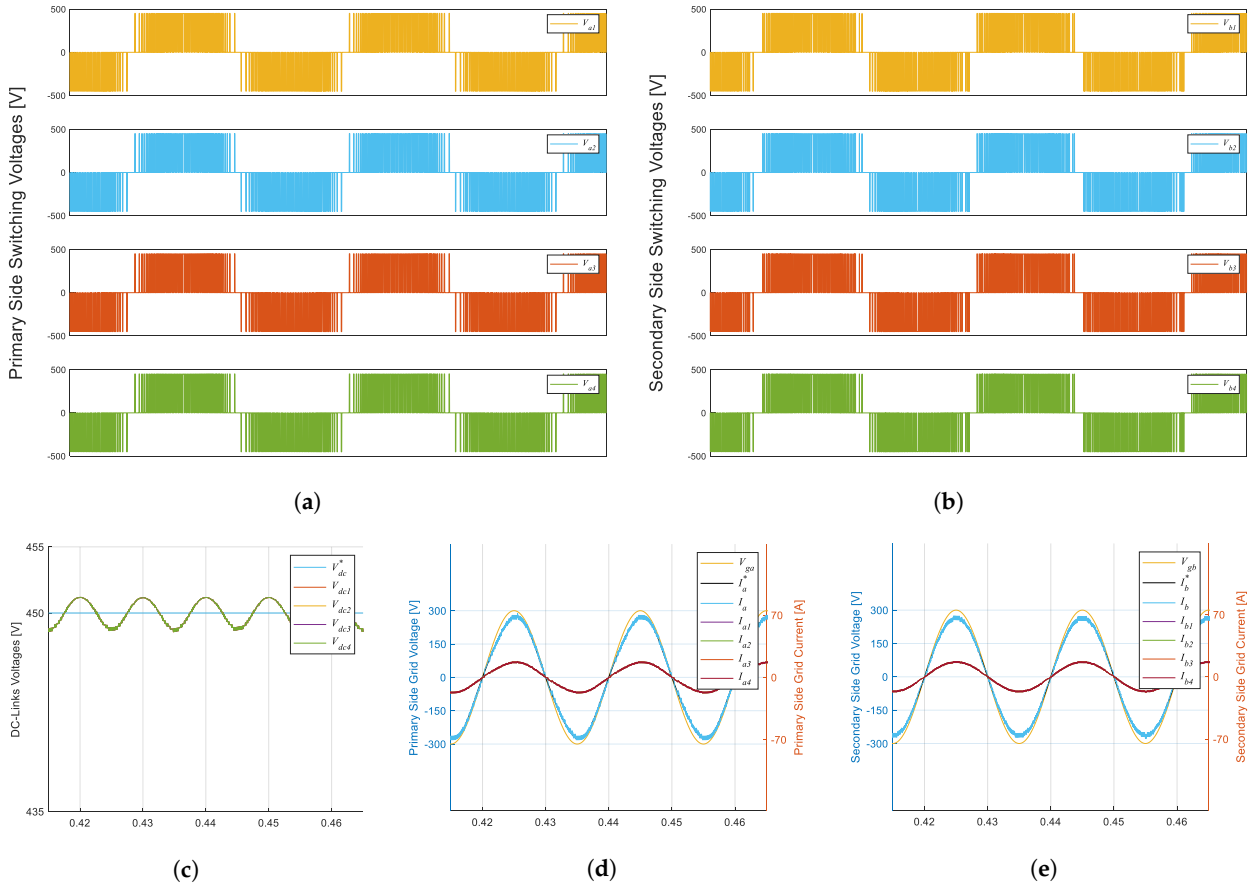


Figure 16. The 4-modules IPOP configuration simulation results: (**a**) primary side switching voltages, (**b**) secondary side switching voltages, (**c**) DC-links voltages, (**d**) primary side grid voltage and currents, (**e**) secondary side grid voltage and currents.

6.1.3. 4-Modules ISOP Configuration

The results of the 4-modules ISOP CHB-B2B topology are presented below, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), secondary modules' currents (i_{2m}), DC link voltages (V_{dcm}) and switching voltages on the primary (v_1) and of each converter module (v_{nm}) are highlighted. As can be seen in Figure 17a,b, the converter can synthesize only five voltage levels as expected, on the primary side. On the secondary side, due to the parallel connection, only five voltage levels are synthesized. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 17c shows that the DC-links could be tuned to nominal values, as compared to the V_{dc}^* reference, with a maximum 3.5 V (0.77%) oscillation in the magnitude, which conforms to the DC-link design requirements (4.5 V). The currents in the primary and secondary of the converter are verified in Figure 17d,e, respectively. As it can be seen, they satisfactorily follow the i_1^* and i_2^* references and are in phase with the v_{g1} and v_{g2} grid voltages, making the converter power factor unitary. Each secondary modules' currents which constitute i_2 are the same, and they are superimposed on the graph.

A maximum of 0.27 A (0.81%) oscillation in i_1 is obtained, while for i_2 current components a 1.08 A (1.62%) is observed. This conforms to both filter design requirements (Δ_{i1} = 1.67 A and Δ_{i2} = 3.33 A). Finally, it can be concluded that the control system works properly, making it possible to affirm that the used converter switching matrix eliminates all the prohibitive switching states.

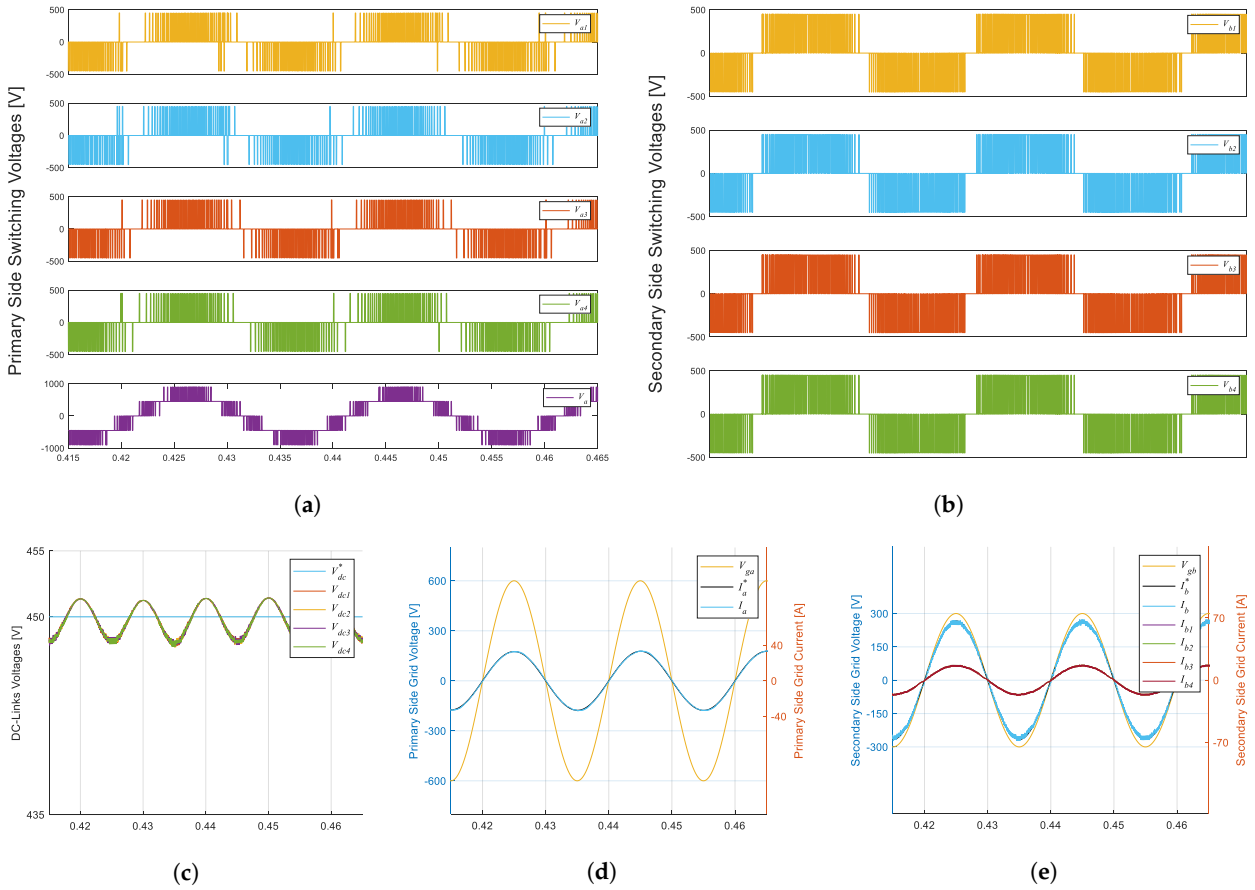


Figure 17. The 4-modules ISOP configuration simulation results: (**a**) primary side switching voltages, (**b**) secondary side switching voltages, (**c**) DC-links voltages, (**d**) primary side grid voltage and current, (**e**) secondary side grid voltage and currents.

6.1.4. 4-Modules IPOS Configuration

The results of 4-modules IPOS CHB-B2B topology are presented below, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), primary modules' currents (i_{1m}), DC link voltages (V_{dcm}) and switching voltages on the secondary (v_2) and of each converter module (v_{nm}) are highlighted. As can be seen in Figure 18a,b, the converter can synthesize only five voltage levels as it is expected, on the secondary side. On the primary side, due to the parallel connection, only three voltage levels are synthesized. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 18c shows that the DC-links could be tuned to nominal values. When compared to the V_{dc}^* reference, a maximum 3.88 V (0.86%) oscillation in the magnitude is obtained, which conforms to the DC-link design requirements (4.5 V). The currents in the primary and secondary of the converter are verified in Figure 18d,e, respectively. As can be seen, they satisfactorily follow the i_1^* and i_2^* references and are in phase with the v_{g1} and v_{g2} grid voltages, making the converter power factor unitary. Each primary module's currents which constitute i_1 are the same, and they are superimposed on the graph.

A maximum of 2.12 A (3.18%) oscillation in i_1 current is obtained, while for i_2, a 0.28 A (0.84%) is observed. This conforms to both filter design requirements (Δ_{i1} = 3.33 A and Δ_{i2} = 1.67 A). Finally, it can be concluded that the control system works properly, making it possible to affirm that the used converter switching matrix eliminates all the prohibitive switching states.

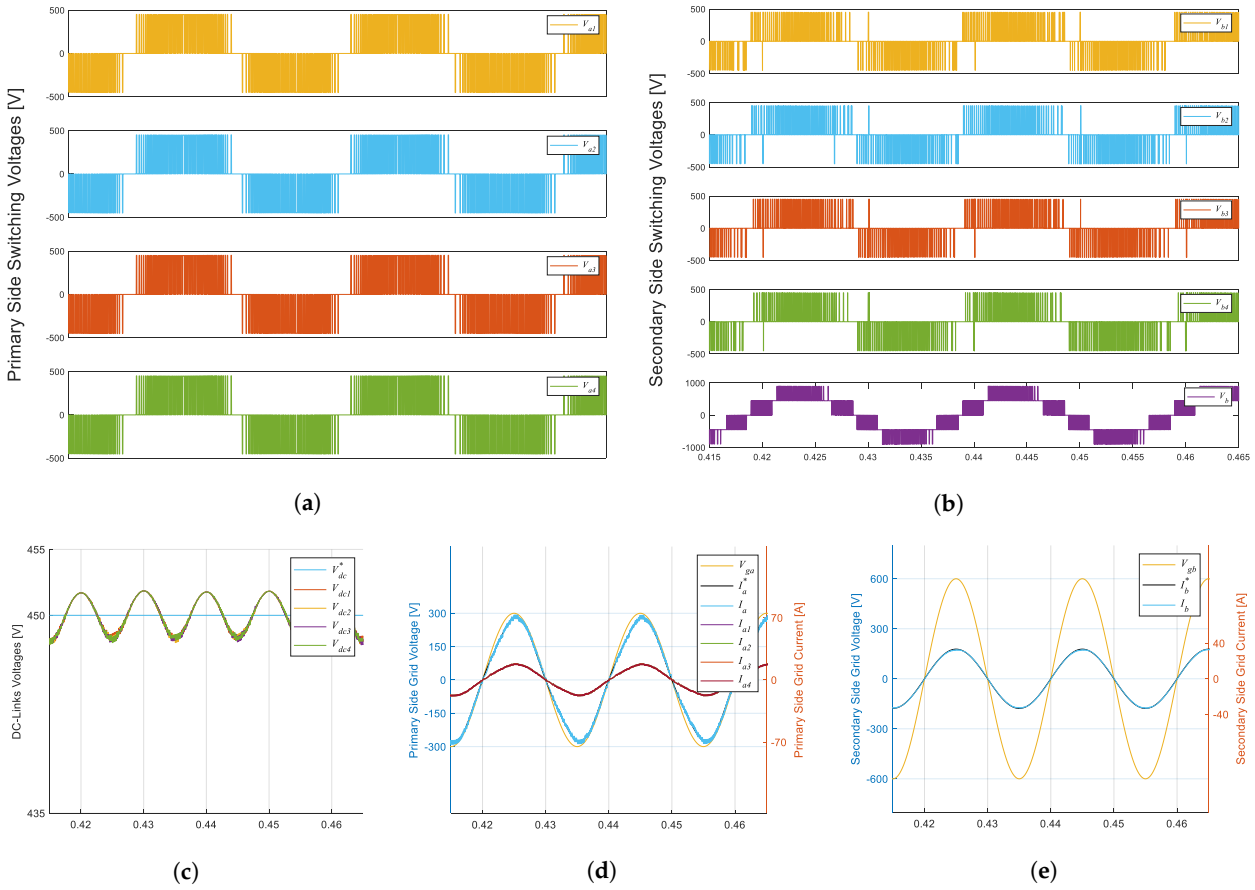


Figure 18. The 4-modules IPOS configuration simulation results: (**a**) primary side switching voltages, (**b**) secondary side switching voltages, (**c**) DC-links voltages, (**d**) primary side grid voltage and currents, (**e**) secondary side grid voltage and current.

6.2. Hybrid Configurations

As discussed, and analyzing Table 5, the ISOP and IPOS configurations for topologies with more than two modules do not allow the synthesis of more than five voltage levels for the side connected in series, due to the switching states that generate short circuits in the converter, making it impossible to take advantage of all the levels. A solution for this, keeping the characteristics of these topologies, is to divide the parallelism into pairs of modules connected in parallel. Thus, all levels on the series side can be synthesized. Therefore, new hybrid topologies could be proposed, namely HISOP (hybrid input-series output-parallel) and HIPOS (hybrid input-parallel output-series), and their characteristics are highlighted in Table 6.

Table 6. Review of characteristics for different CHB-B2B converter hybrid configurations.

M	C	P	F	N	U [%]	LP	LS
4	HISOP	2	65,536	1600	2.44	9	3
6	HISOP	3	16,777,216	64,000	0.38	13	3
4	HIPOS	2	65,536	1600	2.44	3	9
6	HIPOS	3	16,777,216	64,000	0.38	3	13

LEGEND:
M = Number of modules for the topology.
C = Configuration of the topology.
P = Number of parallel pairs in the configuration.
F = Number of all switching states possibilities.
N = Number of switching states for the converter.
U[%] = Converter utilization percentage (N/F).
LP = Number of synthesizable voltage levels in the converter primary.
LS = Number of synthesizable voltage levels in the converter secondary.

7. Real-Time Experimental Results

All previously presented results were restricted to converter topologies with four modules each in a Simulink/MatLab platform. To obtain more diverse and realistic results, different configurations with two modules were tested using a Typhoon HIL platform in real-time test bench using a software-in-the-loop (SIL) environment. Real results are obtained using an oscilloscope and are presented in this section. The same sizing procedure of the system components performed is necessary. The real-time simulation platform is presented in Figure 19. A Typhoon HIL 402 module is responsible for power and control system real-time simulation. The supervisory control and data acquisition (SCADA) platform provided by HIL402 is used for real-time test-bench configuration and supervision. Finally, a TBS1064 Tektronix oscilloscope is used to acquire the real-time simulation results.

Figure 19. An overview of the real-time simulation platform for acquiring experimental results.

7.1. 2-Modules CHB-B2B Design and Experimental Results

For 2-modules converters, the same 450 V voltage level used previously is considered. Due to the number of modules being reduced by half, the grid voltage levels and the power demanded by the converter P_T are reduced in the same proportion for all configurations (ISOS, IPOP, ISOP, and IPOS). The same values of switching frequency f_s and grid frequency f_g are maintained. Using Equations (1)–(4), Table 7 can be constructed, which shows the converter elements values for different configurations of a 2-modules CHB-B2B example.

Next, the performance in the steady-state of the OSV-MPC control system is verified by employing experimental results, in which the non-occurrence of internal short circuits in the converter can be confirmed. Therefore, the graph theory application as a solution to obtain the switching matrix of these converters is validated. It is also checked whether the control objectives have been achieved.

Table 7. Sizing for the different configurations of the 2-modules CHB-B2B converter.

Parameter	ISOS	IPOP	ISOP	IPOS
M	2	2	2	2
f_s [kHz]	20	20	20	20
P_T [kVA]	5	5	5	5
f_g [Hz]	50	50	50	50
m_a	2/3	2/3	2/3	2/3
$\widehat{V_n}$ [V]	300	300	300	300
V_{dc} [V]	450	450	450	450
ΔV_{dc} [V]	4.5	4.5	4.5	4.5
$V_{g1,pk}$ [V]	600	300	600	300
$i_{1,pk}$ [A]	16.67	33.33	16.67	33.33
Δi_1 [A]	0.83	1.67	0.83	1.67
Δi_{1m} [A]	0.83	0.83	0.83	0.83
$V_{g2,pk}$ [V]	600	300	300	600
$i_{2,pk}$ [A]	16.67	33.33	33.33	16.67
Δi_2 [A]	0.83	1.67	1.67	0.83
Δi_{2m} [A]	0.83	0.83	0.83	0.83
C_{dcm} [mF]	3.93	3.93	3.93	3.93
l_1 [mH]	13.50	13.50	13.50	13.50
r_1 [Ω]	0.04	0.04	0.04	0.04
l_2 [mH]	13.50	13.50	13.50	13.50
r_2 [Ω]	0.04	0.04	0.04	0.04

7.1.1. 2-Modules ISOS Configuration

The results of the 2-modules ISOS CHB-B2B topology are presented in Figure 20, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), DC link voltages (V_{dcm}) and switching voltages on the primary (v_1), secondary (v_2) and of each converter module (v_{nm}) are highlighted. As can be seen in Figure 20a,b, the converter can synthesize the expected five voltage levels, both on the primary and the secondary sides. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 20c shows that the DC-links (orange and blue) could be tuned to nominal values. When compared to the V_{dc}^* reference (450 V), a maximum of $0.378\sqrt{2} = 0.534$ V (0.12%) oscillation in the magnitude is obtained, which conforms to the DC-link design requirements (4.5 V). The currents in the primary and secondary of the converter are verified (in blue) in Figure 20d,e, respectively. As can be seen, they have an adequate RMS value corresponding to their nominal values, with a small error in the DC-links measurements, due to the oscilloscope's impression. Additionally, they are in phase with the v_{g1} and v_{g2} grid voltages (in orange), making the converter power factor unitary.

A maximum of 0.56 A (3.36%) oscillation in i_1 is obtained, while for i_2, 0.55 A (3.27%) is observed, which conforms to the filter design requirements (0.83 A). Finally, it can be concluded that the control system works properly, making it possible to affirm that the used converter switching matrix eliminates all the prohibitive switching states.

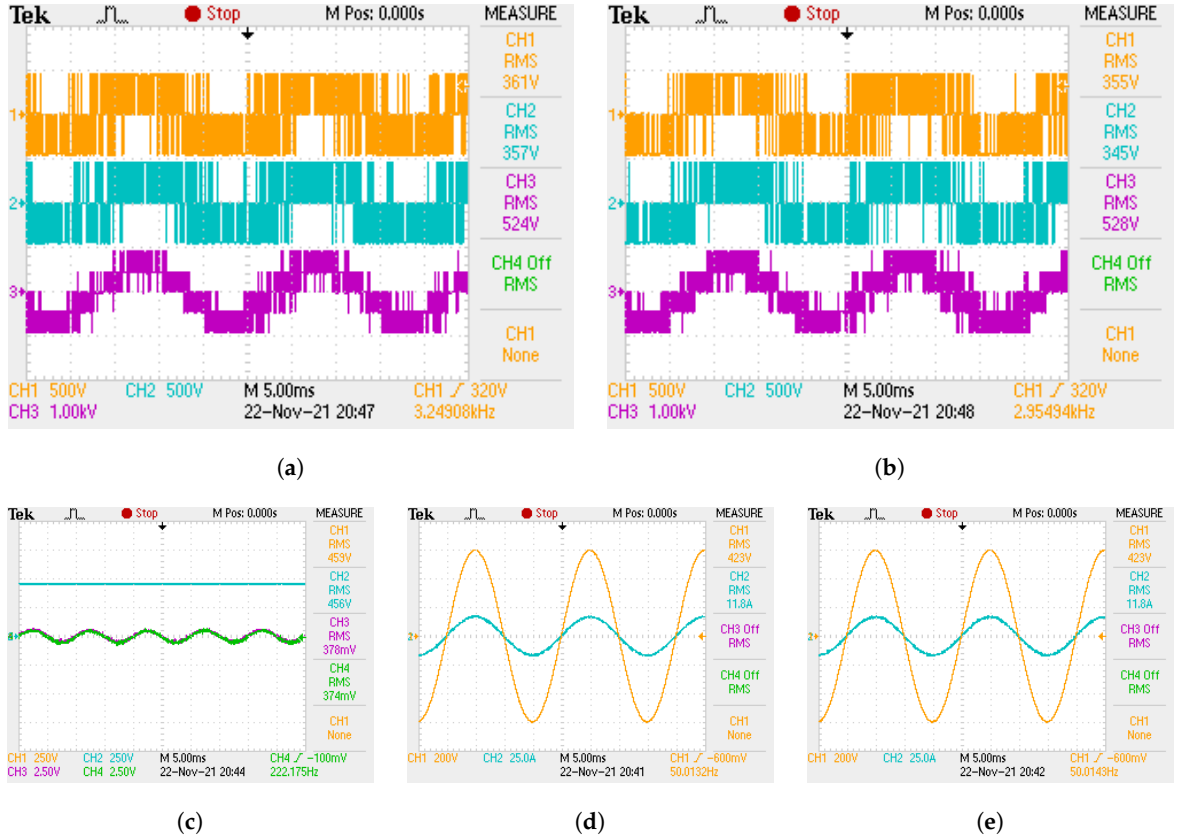


Figure 20. The 2-modules ISOS configuration experimental results: (**a**) primary side switching voltages, (**b**) secondary side switching voltages, (**c**) DC-links voltages, (**d**) primary side grid voltage and current, (**e**) secondary side grid voltage and current.

7.1.2. 2-Modules IPOP Configuration

The results of the 2-modules IPOP CHB-B2B topology are presented in Figure 21, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), modules' currents (i_{nm}), DC link voltages (V_{dcm}) and switching voltages of each converter module (v_{nm}) are highlighted. As can be seen in Figure 21a,b, the converter can synthesize only three voltage levels, both on the primary and the secondary sides, as expected. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 21c shows that the DC-links (orange and blue) could be tuned to nominal values. When compared to the V_{dc}^{*} reference (450 V), a maximum $0.782\sqrt{2} = 1.11$ V (0.25%) oscillation in the magnitude is obtained which conforms to the DC-link design requirements (4.5 V). The currents in the primary and secondary of the converter are verified (in blue) in Figure 21d,e, respectively. As can be seen, they have an adequate RMS value corresponding to their nominal values, with a small error in the DC-links measurements, due to the oscilloscope's impression. Additionally, they are in phase with the v_{g1} and v_{g2} grid voltages (in orange), making the converter power factor unitary. Each primary module's currents which constitute i_1 are the same and they are superimposed on the graph (violet and green signals). The same thing happens for the currents that constitute i_2.

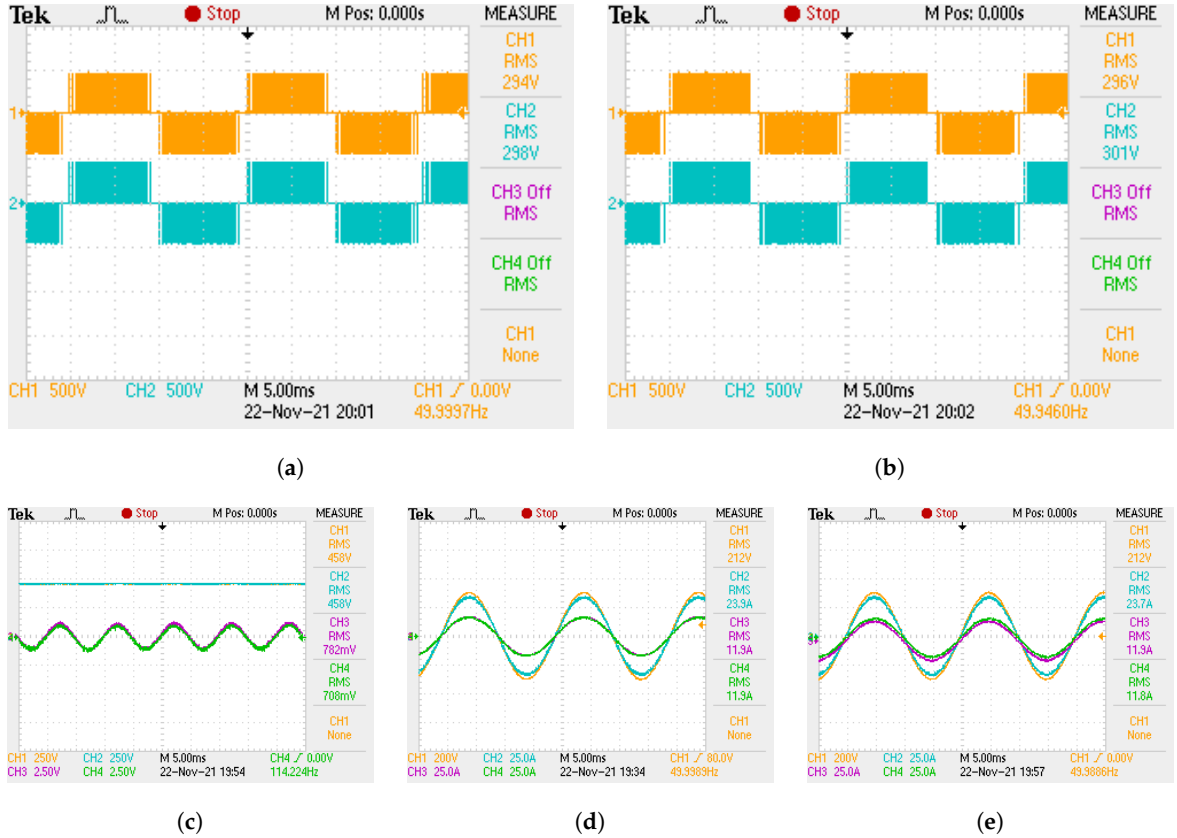


Figure 21. 2-modules IPOP configuration experimental results: (**a**) Primary side switching voltages, (**b**) Secondary side switching voltages, (**c**) DC-links voltages, (**d**) Primary side grid voltage and currents, (**e**) Secondary side grid voltage and currents.

A maximum 1.12 A (3.36%) oscillation in i_1 is obtained, while for i_2, 1.09 A (3.26%) is observed, which conforms to the filter design requirements (1.67 A). Finally, it is concluded that the control system works properly, making it possible to affirm that the used converter switching matrix eliminated all the prohibitive switching states.

7.1.3. 2-Modules ISOP Configuration

The results of the 2-modules ISOP CHB-B2B topology are presented in Figure 22, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), secondary modules' currents (i_{2m}), DC link voltages (V_{dcm}) and switching voltages on the primary (v_1) and of each converter module (v_{nm}) are highlighted. As can be seen in Figure 22a,b, the converter can synthesize only five voltage levels as it is expected, on the primary side. On the secondary side, due to the parallel connection, only three voltage levels are synthesized. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 22c shows that the DC-links (orange and blue) could be tuned to nominal values, since when compared to the V_{dc}^* reference (450 V), a maximum $0.574\sqrt{2} = 0.812$ V (0.18%) oscillation in the magnitude is obtained, which conforms to the DC-link design requirements (4.5 V). The currents in the primary and secondary of the converter are verified in Figure 22d,e, respectively. As can be seen, they have an adequate RMS value corresponding to their nominal values, with a small error in the DC-links measurements, due to the oscilloscope's impression. Also, they are in phase with the v_{g1} and v_{g2} grid voltages, making the converter power factor unitary. Each secondary modules' currents which constitutes i_2 are the same and they are superimposed on the graph (violet and green signals).

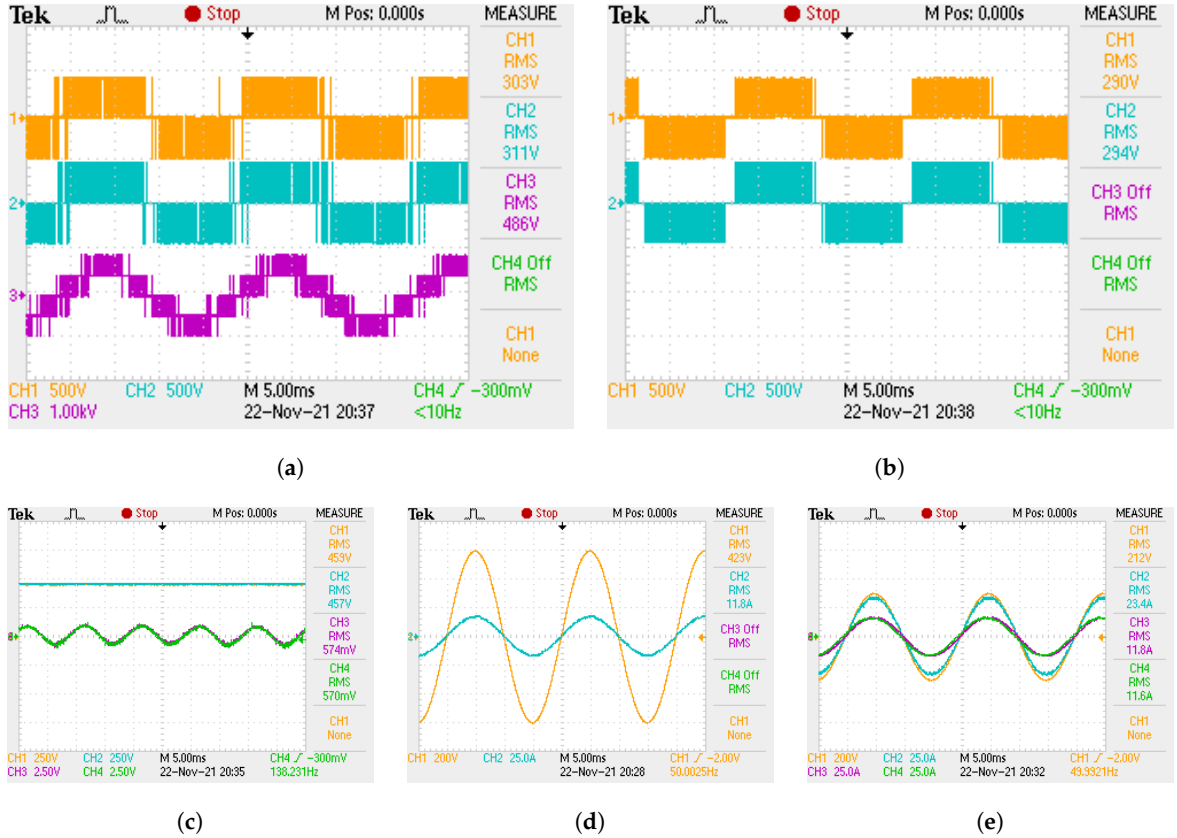


Figure 22. 2-modules ISOP configuration experimental results: (**a**) Primary side switching voltages, (**b**) Secondary side switching voltages, (**c**) DC-links voltages, (**d**) Primary side grid voltage and current, (**e**) Secondary side grid voltage and currents.

A maximum of 0.55 A (3.30%) oscillation in i_1 is obtained, while for i_2, 1.09 A (3.27%) is observed. This conforms to both filter design requirements (Δ_{i1} = 0.83 A and Δ_{i2} = 1.67 A). Finally, it is concluded that the control system operates properly, making it possible to affirm that the used converter switching matrix eliminated all the prohibitive switching states.

7.1.4. 2-Modules IPOS Configuration

The results of the 2-modules IPOS CHB-B2B topology are presented in Figure 23, in which the steady-state behavior of the currents on the primary (i_1) and secondary sides (i_2), primary modules' currents (i_{1m}), DC link voltages (V_{dcm}) and switching voltages on the secondary (v_2) and of each converter module (v_{nm}) are highlighted. As can be seen in Figure 23a,b, the converter can synthesize only five voltage levels as expected, on the secondary side. On the primary side, due to the parallel connection, only three voltage levels are synthesized. It is also verified that each module presents a variable switching frequency, without a defined pattern.

Figure 23c shows that the DC-links (orange and blue) could be tuned to nominal values, since when compared to the V_{dc}^* reference (450 V), a maximum $0.556\sqrt{2} = 0.786$ V (0.175%) of oscillation in the magnitude is obtained, which conforms to the DC-link design requirements (4.5 V). The currents in the primary and secondary of the converter are verified in Figure 23d,e, respectively. As can be seen, they have an adequate RMS value corresponding to their nominal values, with a small error as the DC-links measurements, due to the oscilloscope's impression. Also, they are in phase with the v_{g1} and v_{g2} grid voltages, making the converter power factor unitary. Each primary module's currents which constitute i_1 are the same, and they are superimposed on the graph (violet and green signals).

A maximum of 1.09 A (3.27%) oscillation in i_1 is obtained, while for i_2, 0.56 A (3.33%) is observed. This conforms to both filter design requirements (Δ_{i1} = 1.67 A and $\Delta_i 2$ = 0.83 A). Finally, it is concluded that the control system works properly, making it possible to affirm that the used converter switching matrix eliminates all the prohibitive switching states.

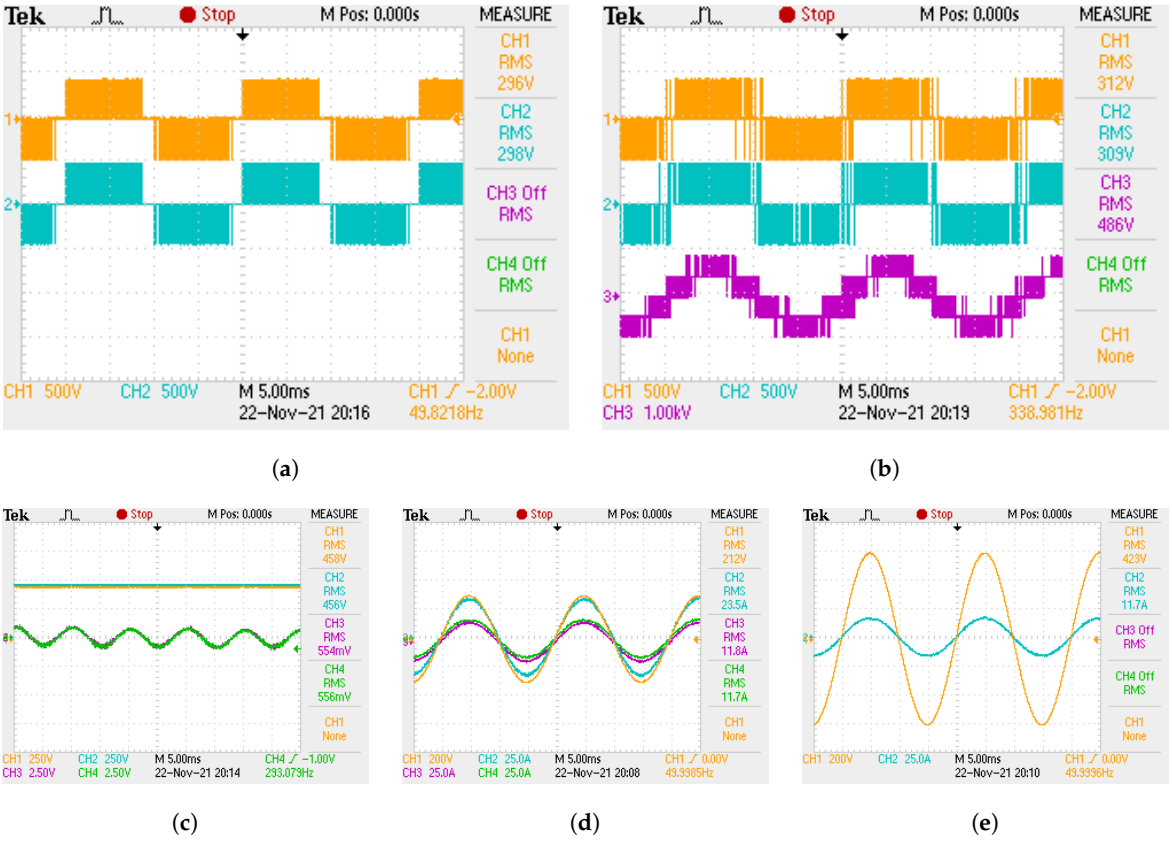


Figure 23. The 2-modules IPOS configuration experimental results: (**a**) primary side switching voltages, (**b**) secondary side switching voltages, (**c**) DC-links voltages, (**d**) primary side grid voltage and currents, (**e**) secondary side grid voltage and current.

8. Conclusions

This research paper demonstrates that graph theory plays a key role in controlling CHB-B2B converters, identifying states of internal short circuits and mapping an adequate switching matrix for the use of appropriate control strategies, in which the MPC is highlighted as an effective solution. A methodology based on graph theory is developed to determine the switching states of CHB-B2B converters with multiple modules and different topologies. Thus, it is possible to verify the feasibility of different proposed configurations for CHB-B2B, including hybrid topologies that emerge as a solution for the better use of the number of voltage levels synthesized by the converter, when there are parallel connections. Based on the steady-state simulational and experimental results, the application of graph theory is validated for different configurations of the CHB-B2B converter with two and four modules, suggesting its applicability for all different types of configurations (various numbers of modules and topologies), disregarding the computational cost linked to the MPC that may be an obstacle to practical application.

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