Model Predictive Control of an Asymmetric Flying Capacitor Converter

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***Abstract*—Multilevel converters and, in particular, flying capacitor (FC) converters are an attractive alternative for medium-voltage applications. FC converters do not need complex transformers to obtain the dc-link voltage and also present good robustness properties, when operating under internal fault conditions. Unfortunately, with standard modulation strategies, to increase the number of output voltage levels of FC converters, it is necessary to increase the number of cells and, hence, the number of capacitors and switches. In this paper, we develop a finite-state model predictive control strategy for FC converters. Our method controls output currents and voltages and also the FC voltage ratios. This allows one to increase the number of output voltage levels, even at high power factor load conditions and without having to increase the number of capacitors and switches. Experimental results illustrate that the proposed algorithm is capable of achieving good performance, despite possible parameter mismatch.**

***Index Terms*—Multilevel converters, power electronics, predictive control.**

NOMENCLATURE

y^j	Variable y at instant j.
y_x	Variable y of the respective x output phase, where $x \in \{a, b, c\}$.
$\mathbf{y}$	Measured value of variable y.
Y	Constant or average value of y.
s_{ij}	Switch state under evaluation, where $s_{ij} \in \{0, 1\}$.
S_{ij}	Switch state applied, where $S_{ij} \in \{0, 1\}$.

I. INTRODUCTION

BY USING medium-voltage semiconductors, multilevel converters are capable of attaining the high power levels required by present-day industrial applications (see, e.g., [1]–[4] and the many applications reported in [5]–[10]). One of the most important multilevel converter topologies is the flying capacitor (FC), also known as multicell [3]. This topology and its derivations have been the focus of many works [11]–[13], most of them related with FC voltage balance (or control). For example, in [12], it has been demonstrated that in steady-state operation and using phase-shifted pulsewidth modulation (PWM), the capacitor voltage of cell n tends to stabilize its value at n per unit (p.u.), where 1 p.u. corresponds to the voltage of cell 1 capacitor (as shown in Fig. 1).

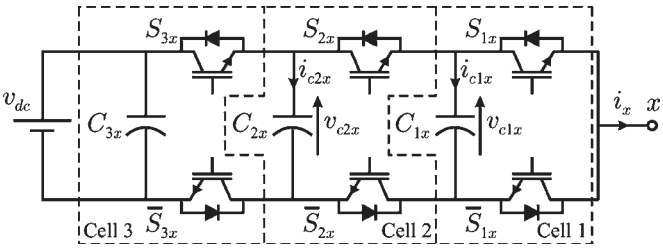

Fig. 1. Three-cell FC inverter leg.

In [14], it has recently been shown how the natural balancing process can be significantly accelerated by actively controlling the capacitor voltages using finite-state (FS) model predictive control (MPC; FS-MPC). As in other MPC algorithms (see, e.g., [15]–[18]), in [14], the actuation signal is chosen to minimize a cost function, which quantifies a tracking error. A key aspect of FS-MPC, as used in [14], [19]–[21], is that the fact that force-commutated converters can generate a finite number of actuation values is explicitly taken into account. Thus, the optimal switching combination, i.e., that which minimizes the cost function, can be found by searching over a finite set. An advantage of FS-MPC methods is that the cost function can merge in a single-expression electrical and nonelectrical variables, e.g., tracking of currents and balancing of capacitor voltages and semiconductor switching frequency [22].

While most work on the FC topology deals with balancing of the FC voltages, in [23], it was shown that if the FCs are replaced by dc sources with a nontraditional ratio, then the number of output voltage levels can be increased. This opens the possibility to design output voltages with a lower distortion. Another consequence of operating FC in nonbalanced modes lies in that redundant states decrease and the currents provided by the floating dc sources have a nonzero average value. This characteristic is analyzed in [11], where the dc sources are replaced by capacitors. More precisely, in [11], it is established that for a three-cell inverter, the operation can be sustained only if the output voltage levels are four or five, while the operation with six, seven, and eight levels is suitable only for reactive power compensation.

In this paper, we develop an FS-MPC technique for the FC topology. In our approach, floating capacitor voltages are controlled. In particular, the strategy enables one to force nontraditional voltage ratios and increase the number of levels

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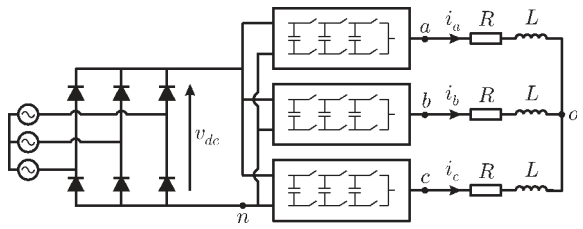

Fig. 2. Three-phase three-cell FC converter.

up to eight (the theoretical maximum). At the same time, the FS-MPC controls the output currents, obtaining good tracking and a high output power factor (PF). Experimental results for a 2-kW prototype illustrate the performance of the proposed algorithm.

II. FC Converter

FC converters have emerged as an attractive multilevel topology for medium-voltage application. The main reason is that, unlike cascade multicell converters [4], these converters do not require isolated dc sources and, hence, bulky multisecondary transformers. FC converters also exhibit good performance when operating under internal fault conditions [24].

This paper is focused on a three-phase FC converter feeding a resistive–inductive load, as shown in Fig. 2. Each output phase is based on a three-cell FC topology, as shown in Fig. 1. Each cell is a modular structure composed of one capacitor $C_{\rm jx}$ and two switches $S_{\rm jx}$ and $\overline{S}_{\rm jx}$, which work in a complementary way. This avoids short circuits between the FCs of different cells and open-circuiting the load.

The internal FC equations per phase can be expressed as

$$v_{\rm xn}(t) = S_{3x}(t)v_{\rm dc} - (S_{3x}(t) - S_{2x}(t))\, v_{\rm c2x}(t) - (S_{2x}(t) - S_{1x}(t))\, v_{\rm c1x}(t) \quad (1)$$

$$i_{\rm c1x}(t) = i_x(t)\,(S_{2x}(t) - S_{1x}(t)) \quad (2)$$

$$i_{\rm c2x}(t) = i_x(t)\,(S_{3x}(t) - S_{2x}(t)) \quad (3)$$

$$v_{\rm c1x}(t) = \frac{1}{C_1}\int_{-\infty}^{t} i_{\rm c1x}(\tau)d\tau \quad (4)$$

$$v_{\rm c2x}(t) = \frac{1}{C_2}\int_{-\infty}^{t} i_{\rm c2x}(\tau)d\tau \quad (5)$$

whereas the load equations are given by

$$Ri_x(t) + L\frac{di_x(t)}{dt} = v_{\rm xn} - v_{\rm on} \quad (6)$$

$$v_{\rm on}(t) = \frac{v_{\rm an}(t) + v_{\rm bn}(t) + v_{\rm cn}(t)}{3}. \quad (7)$$

In the aforementioned expressions, $v_{\rm xn}$, $i_{\rm c1x}$, and $i_{\rm c2x}$ are discontinuous functions which depend on the switching state of the converter, as detailed in Table I.

The most commonly used capacitor voltage ratio is $v_{\rm dc} : v_{\rm c2x} : v_{\rm c1x} = 3:2:1$. In this case and based on Table I, the inverter output voltage per phase reaches a maximum of four levels,

TABLE I
Switching Combinations for a Three-Cell Inverter Leg

S_{3x}	S_{2x}	S_{1x}	$v_{xn}(t)$	$i_{c1x}(t)$	$i_{c2x}(t)$
0	0	0	0	0	0
0	0	1	$v_{c1x}(t)$	$-i_x$	0
0	1	0	$v_{c2x}(t) - v_{c1x}(t)$	i_x	$-i_x(t)$
0	1	1	$v_{c2x}(t)$	0	$-i_x(t)$
1	0	0	$v_{dc} - v_{c2x}(t)$	0	$i_x(t)$
1	0	1	$v_{dc} - v_{c2x}(t) + v_{c1x}(t)$	$-i_x(t)$	$i_x(t)$
1	1	0	$v_{dc} - v_{c1x}(t)$	$i_x(t)$	0
1	1	1	v_{dc}	0	0

TABLE II
Number of Redundant States per Voltage Level for Different Capacitor Voltages' Ratios

	Voltage ratio $v_{dc} : v_{c2x} : v_{c1x}$				
Level	3:2:1	4:2:1	5:3:1	6:3:1	7:3:1
0	1	1	1	1	1
1	3	2	1	1	1
2	3	2	2	1	1
3	1	2	2	2	1
4	–	1	1	1	1
5	–	–	1	1	1
6	–	–	–	1	1
7	–	–	–	–	1

using the eight possible switch combinations. It is worth noting that some voltage levels can be generated by multiple switch combinations, i.e., there is a certain degree of redundancy in the switching state combinations. These redundant states can be used to control the capacitor voltages and, hence, to keep them at the desired ratio.

In [23], using different ratios in order to increase the number of levels (not the power) and, hence, increase the quality of the output currents is proposed. The main disadvantage of this approach is that the redundancy decreases (see Table II); hence, the control of the capacitor voltages requires additional control effort. In [11], a simple algorithm to control the capacitor voltages is proposed. First, a PWM modulator selects a desired voltage level, and then, taking into account the output current, the redundant switch combination which reduces the capacitor voltages' error is applied. This allows for an operation with four and and output voltage levels for a wide range of output PF. However, for six, seven, and eight output voltage levels, the PF is below 0.5. Thus, the technique of [11] is mainly applicable for highly reactive loads. Overcoming these limitations constitutes the main motivation for developing the controller to be presented in the following section.

III. FS-MPC of an Asymmetric FC Converter

In this section, we present an MPC method for the three-phase FC converter topology shown in Fig. 2. Key to our proposal is the fact that not only output currents but also capacitor voltages are controlled. In particular, the ratios of the capacitor voltages can be regulated to nontraditional values. This increases the number of output voltage levels and, thus, reduces the harmonic content in the output current.

A. Overview

The proposed controller fits into the general framework of *FS-MPC*, as described, e.g., in [19]–[21], [25], and [26]. It operates in discrete time with a fixed sampling period Δ and directly provides the switching states to be implemented at the converter. Consequently, no intermediate modulation stages are needed, cf., [15]–[17].

At each discrete time instant k, first measurements of the capacitor voltages $\mathbf{v}_{\mathrm{c}1x}^k$ and $\mathbf{v}_{\mathrm{c}2x}^k$ and output currents $\mathbf{i}_x^k$ of each phase $x \in \{a, b, c\}$ are taken. These measurements are then used by the controller to decide upon the switch states which are to be implemented at time $k+1$. We note that the effect of the latter will be observed only at time $k+2$.

B. Optimization Criterion

As foreshadowed in Section I, the proposed controller chooses the switch states to be implemented at time $k+1$, namely S_{ix}^{k+1} and $i \in \{1, 2, 3\}$, through minimization of the following cost function:

$$g^k = g_a^k + g_b^k + g_c^k \tag{8}$$

where

$$g_x^k = \left(i_x^* - i_x^{k+2}\right)^2 + W_{v_{\mathrm{c}1}} \left(v_{\mathrm{c}1}^* - v_{\mathrm{c}1x}^{k+2}\right)^2 + W_{v_{\mathrm{c}2}} \left(v_{\mathrm{c}2}^* - v_{\mathrm{c}2x}^{k+2}\right)^2, \qquad x \in \{a, b, c\}. \tag{9}$$

In (9), variables with superscript * are reference values *corresponding to time* $k+2$, whereas the weighting factors $W_{v_{\mathrm{c}1}}$ and $W_{v_{\mathrm{c}2}}$ give the control designer two degrees of freedom to improve the tracking of capacitor voltages and/or output currents.

C. Control Calculations

To minimize the cost function g^k defined earlier, the model predictive controller examines all possible switching states S_{ix}^{k+1} explicitly. As the FS-MPC requires an important number of calculations, the associated delay must be taken into account. Therefore, it is convenient to separate the control calculations, as follows.

1) Given measurements and switching states S_{ix}^k at time k, calculate capacitor voltages and output currents at time $k+1$. We will call this the *Estimation Step*.
2) Given the results of the Estimation Step, evaluate the effect of switching states S_{ix}^{k+1} on g^k. We will refer to this as the *Prediction Steps*.

Fig. 3 shows the situation. Both the Estimation Step and the Prediction Steps use discrete time recursions which are derived from the FC converter model presented in Section III. Next, we will give further details on the control calculations.

1) Estimation Step: The switch values S_{ix}^k (which were calculated at time $k-1$) are kept constant during the sampling period Δ. Thus, the capacitor voltages and output currents at instant $k+1$ can be approximated by the following discretization of (1)–(7)[1]:

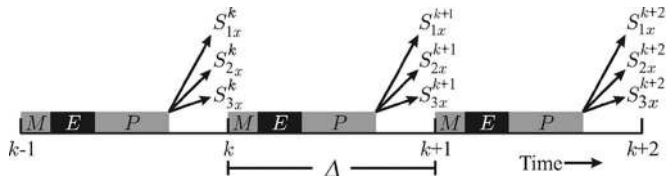

Fig. 3. Control calculations timeline. Measurement, estimation, and prediction.

$$v_{\mathrm{xn}}^{k+1} = S_{3x}^k V_{\mathrm{dc}} - \left(S_{3x}^k - S_{2x}^k\right) \mathbf{v}_{\mathrm{c}2x}^k - \left(S_{2x}^k - S_{1x}^k\right) \mathbf{v}_{\mathrm{c}1x}^k \tag{10}$$

$$v_{\mathrm{on}}^{k+1} = \frac{v_{\mathrm{an}}^{k+1} + v_{\mathrm{bn}}^{k+1} + v_{\mathrm{cn}}^{k+1}}{3}. \tag{11}$$

To obtain an expression for the output currents at $k+1$, it is assumed that the capacitor voltages change slowly when compared with the output currents. This gives

$$i_x^{k+1} = K_a \mathbf{i}_x^k + K_b \left(v_{\mathrm{xn}}^k - v_{\mathrm{on}}^k\right) \tag{12}$$

where the constants K_a and K_b are given by

$$K_a = e^{-\Delta \frac{R}{L}} \tag{13}$$

$$K_b = (1 - K_a) \frac{1}{R} \tag{14}$$

in accordance with (6).

Finally, a trapezoidal discretization of (4) and (5) is used

$$v_{\mathrm{c}1x}^{k+1} = \mathbf{v}_{\mathrm{c}1x}^k + \frac{\Delta}{2C_1} \left(i_x^{k+1} + \mathbf{i}_x^k\right) \left(S_{2x}^k - S_{1x}^k\right)$$

$$v_{\mathrm{c}2x}^{k+1} = \mathbf{v}_{\mathrm{c}2x}^k + \frac{\Delta}{2C_2} \left(i_x^{k+1} + \mathbf{i}_x^k\right) \left(S_{3x}^k - S_{2x}^k\right). \tag{15}$$

The aforementioned values are used as a starting point for the Prediction Steps described in the following.

2) Prediction Steps: In the Prediction Steps, the effect of the decision variables S_{ix}^k on g^k is evaluated. To minimize g^k, in principle, all possibilities for S_{ix}^k need to be examined. Each three-cell FC output phase can generate up to eight different switching states. Since the output phases interact through the load neutral point by v_{on}, this leads to a total of $8^3 = 512$ possible combinations. The associated predictions need to be evaluated for all possibilities online and at every discrete time instant. Thus, the computational burden may be too high for many practical applications.

To reduce computation times, in this paper, we propose to ignore the interaction through the load neutral point in the Prediction Steps (note that these interactions are explicitly taken into account in the Estimation Step). Consequently, to quantify the impact of the future switch combinations, we regard each output phase as an isolated unit. This gives a search space having only $3 \cdot 8 = 24$ elements.

[1]Note that the main dc-link voltage v_{dc} is assumed as a constant value and is not included as a measured quantity.

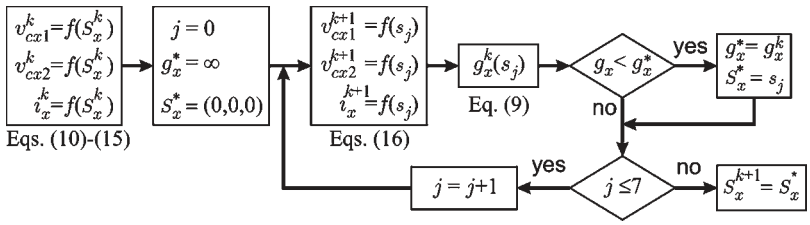

Fig. 4. Flow diagram for the x phase ($x = a, b, c$).

TABLE III
MAIN PROTOTYPE PARAMETERS

Param.	Value	Param.	Value
V_{dc}	400 V	R	35 Ω
C_1	750 μF	L	20 mH
C_2	750 μF	PF@50 Hz	0.98
C_3	900 μF	$f_m = 1/\Delta$	15 kHz

The same discretization used in the Estimation Step is also used for the predictions. The only difference is that $v_{\rm on}$ is set to zero, yielding

$$\begin{aligned} v_{\rm xn}^{k+2} &= s_{3x}^{k+1} V_{\rm dc} - \left(s_{3x}^{k+1} - s_{2x}^{k+1}\right) v_{\rm c2x}^{k+1} \\ &\quad - \left(s_{2x}^{k+1} - s_{1x}^{k+1}\right) v_{\rm c1x}^{k+1} \\ i_x^{k+2} &= K_a i_x^{k+1} + K_b v_{\rm xn}^{k+1} \\ v_{\rm c1x}^{k+2} &= v_{\rm c1x}^{k+1} + \frac{\Delta}{2C_1}\left(i_x^{k+1} + i_x^{k+2}\right)\left(s_{2x}^{k+1} - s_{1x}^{k+1}\right) \\ v_{\rm c2x}^{k+2} &= v_{\rm c2x}^{k+1} + \frac{\Delta}{2C_2}\left(i_x^{k+1} + i_x^{k+2}\right)\left(s_{3x}^{k+1} - s_{2x}^{k+1}\right). \end{aligned} \quad (16)$$

3) Resultant Optimization Algorithm: The FS model predictive controller proposed requires the evaluation of the estimation equations (12) and (15) once and the prediction equations (16) eight times per phase. The switch combination which gives the lowest value of g^k will be applied at the beginning of the next sampling time, i.e., at $k+1$. Fig. 4 shows a flow diagram of the resultant optimization algorithm.

IV. EXPERIMENTAL RESULTS

To test the FS-MPC strategy developed in Section IV, a 2-kW prototype of the topology of Fig. 2 was built based on discrete insulated-gate bipolar transistors (IGBTs) IRG4PC30KD. The most relevant prototype parameters are presented in Table III. The converter was controlled by a digital platform which uses a TMS320C6713 DSP for the proposed control algorithm and an XC3s400 field-programmable gate array for driving the peripheral devices, including analog-to-digital converters and trigger pulses. This digital system performs the complete FS-MPC algorithm in 18 μs. However, the sampling time was set to only 15 kHz in order to reduce the commutation frequency of the converter IGBTs. This is comparable with traditional sinusoidal PWM schemes, which require a lower calculation power, but cannot control the dc-link voltages' ratio. A deeper comparison is available in [21].

A. Design of Capacitor Voltage Ratio

Fig. 5 shows the converter behavior at different voltage ratios. As the number of levels increases, the number of redundant states decreases, as mentioned before. In order to keep the capacitor voltages controlled, the FS-MPC controller uses some unexpected switch combinations or spikes, introducing additional high-frequency components. However, due to the low-pass filter characteristic of the load, those components have only a minor effect in the output currents, as shown in Fig. 5(c). As shown in Fig. 5(b1), there are no spikes for the 3 : 2 : 1 operation, since all levels used by the FCs have redundant combinations. When operating with the ratio 5 : 3 : 1, the spikes appear around levels 1 and 5 [Fig. 5(b2)], which, according to Table II, do not have redundant states. Finally, when operating with the ratio 7 : 3 : 1, where no redundant states exist for any level, the spikes are equally distributed along the $v_{\rm an}$ waveform, as shown in Fig. 5(b3).

Table IV summarizes the capacitor voltage references used to achieve the different operation ratios. It is worth noticing that operation with a nontraditional ratio allows one to use FCs rated at a lower voltage. However, switches must be rated at a higher value, as given by the voltage difference between capacitors of adjacent cells. Thus, from a converter construction point of view, the selection of the voltage ratio will depend on the cost of semiconductors versus capacitors. For example, when comparing the 5 : 3 : 1 operation with the 3 : 2 : 1 operation, we have that the capacitor voltage rate is reduced by 40% and by 10% for C_1 and C_2, respectively, whereas the semiconductors voltage rate is increased by 20%.

Finally, Fig. 5(c) shows the current waveforms obtained for the different operation ratios. It can be observed that the currents are, overall, very similar. However, as the number of output levels increases, the high-frequency distortion increases, too. On the other hand, as the number of voltage levels decreases, the low-frequency distortion increases. The calculated $\rm THD_c$ confirms that, with the present strategy, the best current waveform is obtained by setting the capacitor voltage ratio to 5 : 3 : 1.

The current spectra for the three operation ratios are shown in Fig. 6 and confirm that the currents are very similar. However, with a larger number of levels, the distortion at lower frequencies tends to be lower, and the distortion at higher frequencies tends to increase. Interestingly, the spectra are not concentrated as with traditional PWM modulators; the latter having a higher concentration around $f_m/2$ and f_m. It is also worth noting that all the harmonics have a magnitude lower than 1%, most of them being below 0.3%.

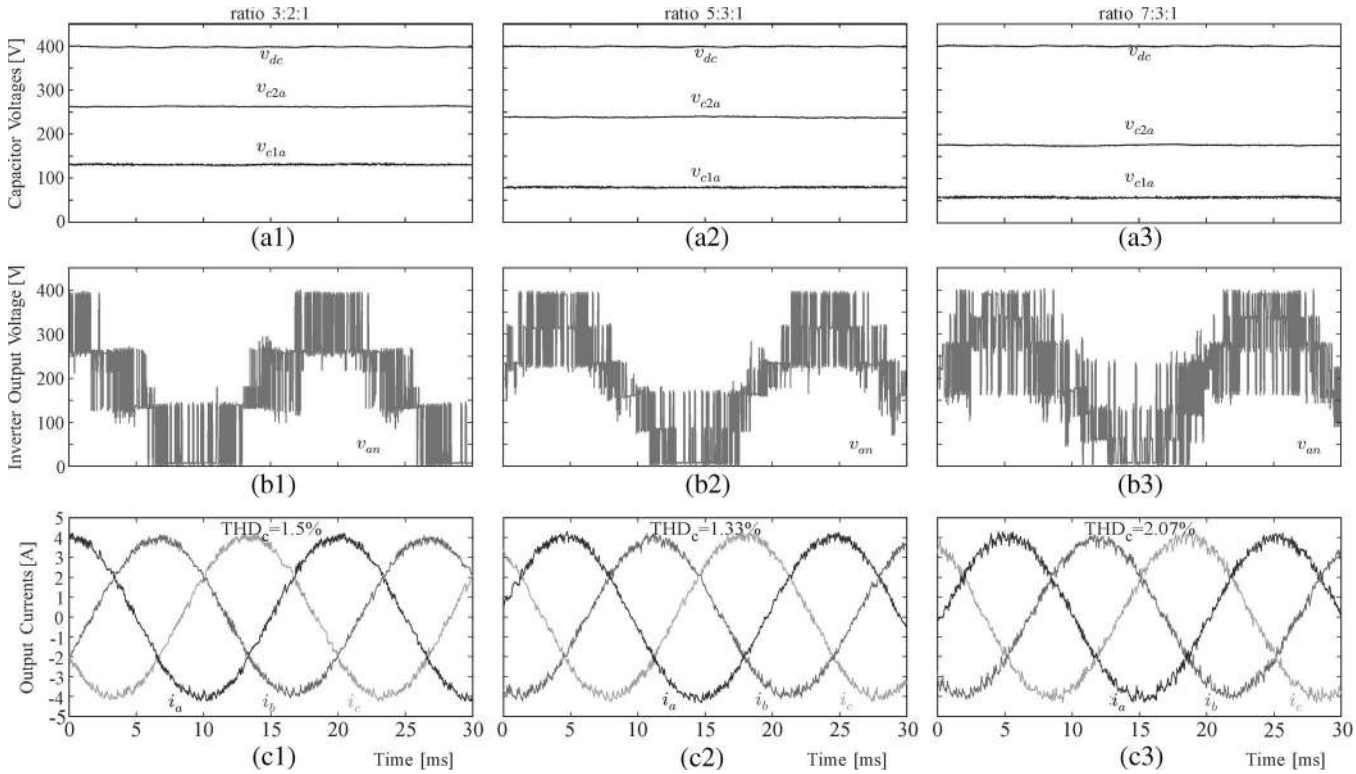

Fig. 5. Operation at different capacitor voltages' ratios. (a) Capacitor voltages. (b) Inverter output voltage. (c) Output currents.

TABLE IV
COMPARISON OF THE FS-MPC CONTROLLER AT DIFFERENT CAPACITOR VOLTAGES' RATIOS

ratio	v_{dc}	v_{c1x}	v_{c2x}	$v_{dc} - v_{c1x}$	$v_{c2x} - v_{c1x}$
3:2:1	400 V	133 V	266 V	133 V	133 V
5:3:1	400 V	80 V	240 V	160 V	160 V
7:3:1	400 V	57 V	171 V	229 V	114 V

We emphasize that previous works only allow for a maximum operative PF of 0.3 and 0.05 for six- and eight-level operations, respectively [11]. The present results where obtained with a load PF of 0.98. This represents an increase of 320% and 1960% for the six- and eight-level operations, respectively.

B. Parameters' Sensitivity

It follows from (10)–(16) that the FS-MPC requires information about the converter parameters to carry out the estimation and prediction calculations needed for finding the optimal switching combination for the next step. Therefore, it is important to test the controller behavior under parameter changes.[2]

Fig. 7 shows the converter operation for a large distortion in the main dc-link voltage $v_{\rm dc}$. This value is not measured by the control system. Consequently, even if $v_{\rm dc}$ has a ripple of ± 50 V, the FS-MPC algorithm assumes that $V_{\rm dc} = 400$ V.

[2]Although it is possible to extend the proposed algorithm in order to work with resistive–inductive–active loads R–L–e, for the sake of brevity, tests are applied only to a resistive–inductive load R–L. Mismatch in the load voltage parameter did not affect, in a significant way, the overall behavior of the converter.

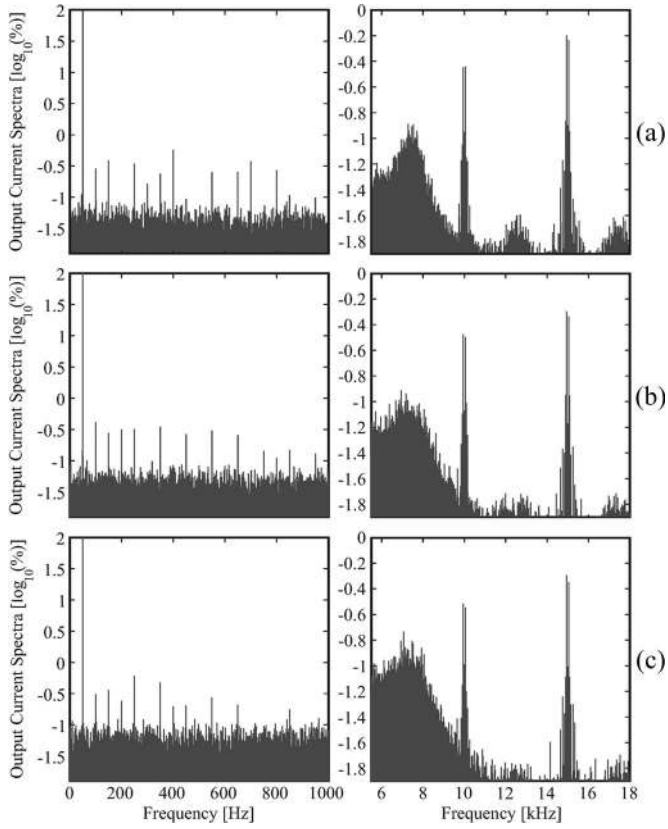

Fig. 6. Output current spectra for voltage ratios. (a) 3 : 2 : 1. (b) 5 : 3 : 1. (c) 7 : 3 : 1.

This amounts to a mismatch of 12.5%. As shown in Fig. 7(b), the ripple in $v_{\rm dc}$ significantly affects the inverter output voltage waveform. Nevertheless, the controller is able to keep the

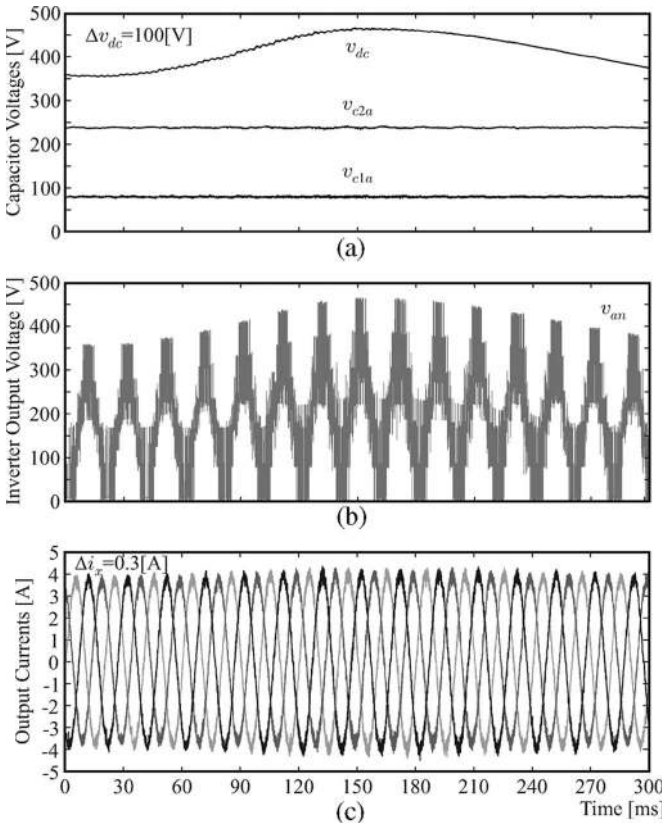

Fig. 7. Control performance for a large $v_{\rm dc}$ distortion. (a) Capacitor voltages. (b) Output voltage. (c) Output currents.

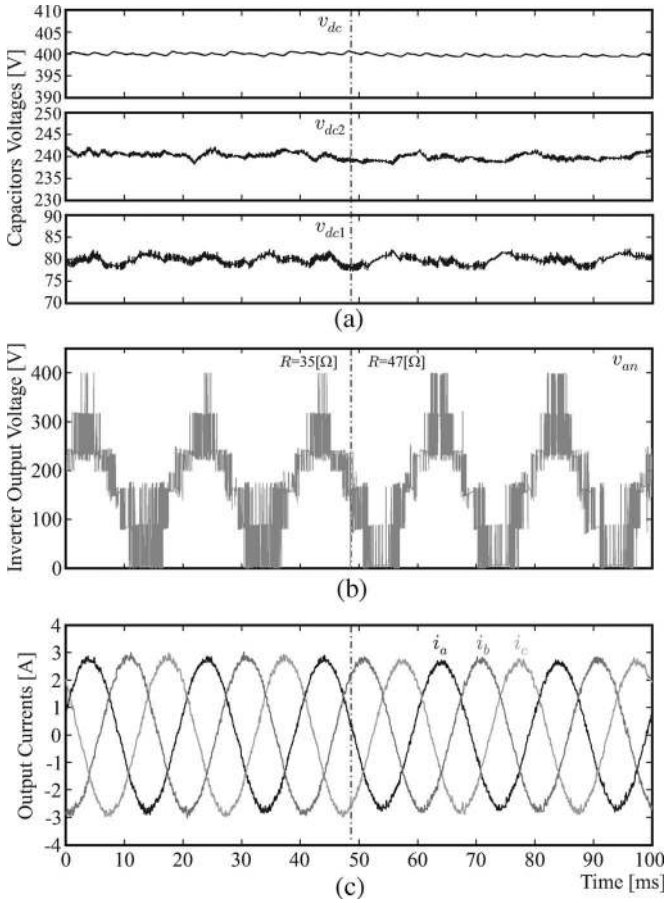

Fig. 8. Waveforms with 35% mismatch in the load resistor value. (a) Capacitor voltages. (b) Output voltage. (c) Output currents.

FC voltages at their reference values without any perceptible ripple, as shown in Fig. 7(a). The output currents show a minor distortion of ± 0.15 A, which corresponds to a tracking error of only 3.75%.

A usual problem in electrical machines is to estimate the load resistor R, since it changes, e.g., with the temperature. Fig. 8 shows the behavior of the converter for a change on the resistive component of the load from 35 to 47 Ω, i.e., the controller works with an underestimated value of about 35%. As shown in Fig. 8(a), no significant changes are observed in the dc-link voltages. The inverter output voltage, shown in Fig. 8(b), automatically increases its modulation index in order to keep the currents controlled, as shown in Fig. 8(c). A minor reduction in the output current magnitude of about 5% (less than 0.2 A) can be noticed. This effect is small when compared with the parameter mismatch.

Finally, the mismatch parameter estimation effect on the inductive component of the load is investigated. The MPC algorithm uses an estimated inductor value of $L = 15$ mH. On the right-hand side of Fig. 9, the real inductor value is 50% lower than that used for control calculations, while on the left-hand side of Fig. 9, an inductor which is 50% higher is used. As expected, when a lower inductance value is used, a higher ripple in the load current can be observed. Nevertheless, the fundamental component of the current is the same in both situations. Similarly, the capacitor voltages do not present any significant difference. The inverter output voltages are accommodated to keep the output current to the desired values.

C. Dynamic Performance

An important aspect of any control system is its dynamic response to reference changes. Fig. 10 shows the system behavior for a current reference step from 4- to 2-A peak. As in results documented earlier, although the main dc-link voltage $v_{\rm dc}$ slightly increases its value due to the reduction in the output power, the proposed control algorithm manages to keep the FC voltages at the desired values, as shown in Fig. 10(a). The inverter output voltage reduces its rms value and the number of levels used, as shown in Fig. 10(b). This change clearly affects the output currents, which rapidly change their values in order to follow the new reference. Moreover, it is possible to see how, at the step instant, the inverter applies the maximum voltage $v_{\rm dc}$ to the inverter output voltage $v_{\rm an}$, forcing the current i_a to decrease its value at maximum speed, as shown in Fig. 10(c).

Changing the FC voltages is not usual in traditional applications. However, it illustrates how flexible the proposed controller can be. Fig. 11 shows the transition from the $5:3:1$ to $7:3:1$ ratio. In absolute values, $v_{\rm c1x}$ changes from 80 to 57 V while $v_{\rm c2x}$ changes from 240 to 171 V, in approximately 80 ms. The output voltage $v_{\rm ao}$ in Fig. 11(b) reflects the change in the capacitor voltages when changing the number of levels from six to eight. Note that, in the transient, the levels are not clearly defined. While the output currents change their magnitude forcing the capacitor voltages to their new values, the currents stay sinusoidal, see Fig. 11(c). Once the capacitor

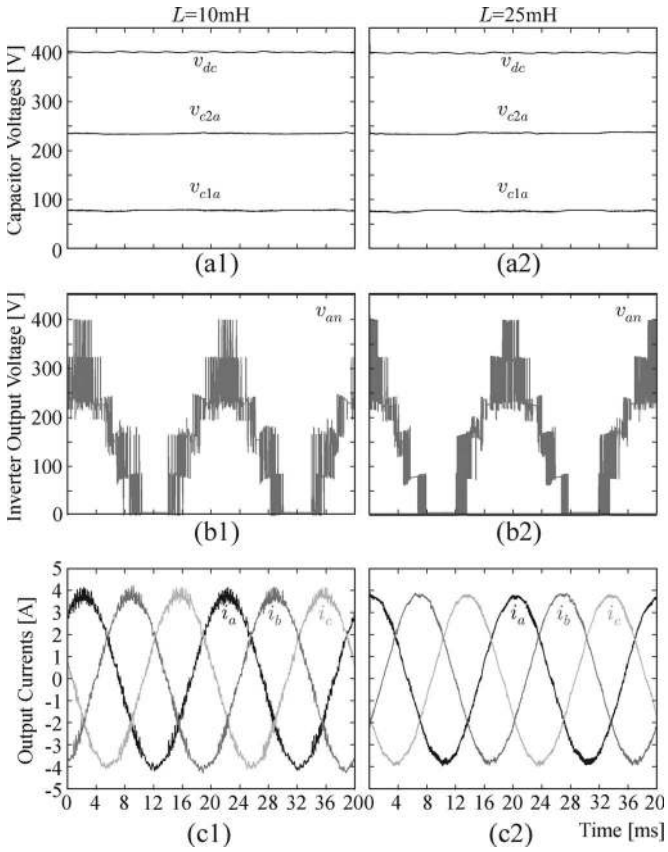

Fig. 9. Operation with a mismatch in the load inductor value. (a) Capacitor voltages. (b) Output voltage. (c) Output currents.

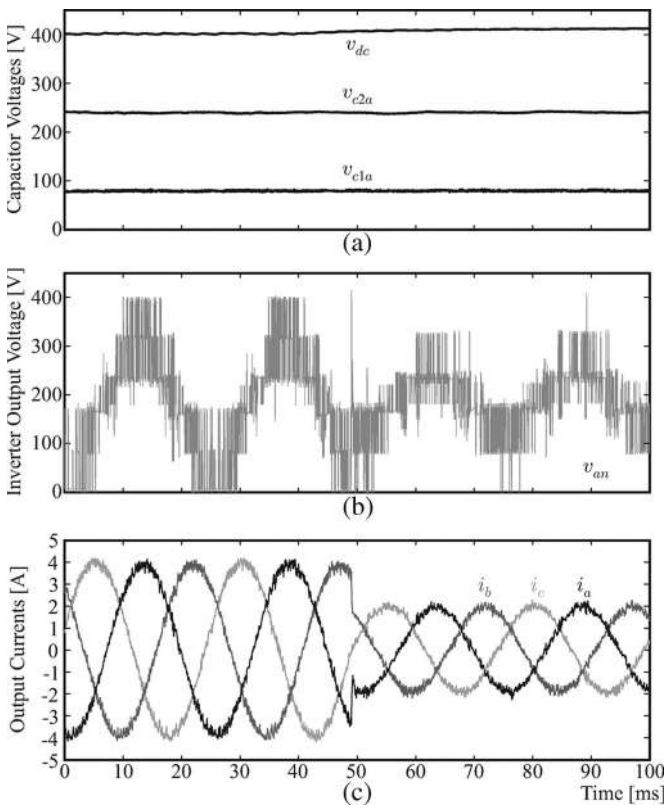

Fig. 10. Waveforms for a current reference step from 4- to 2-A peak. (a) Capacitor voltages. (b) Output voltage. (c) Output currents.

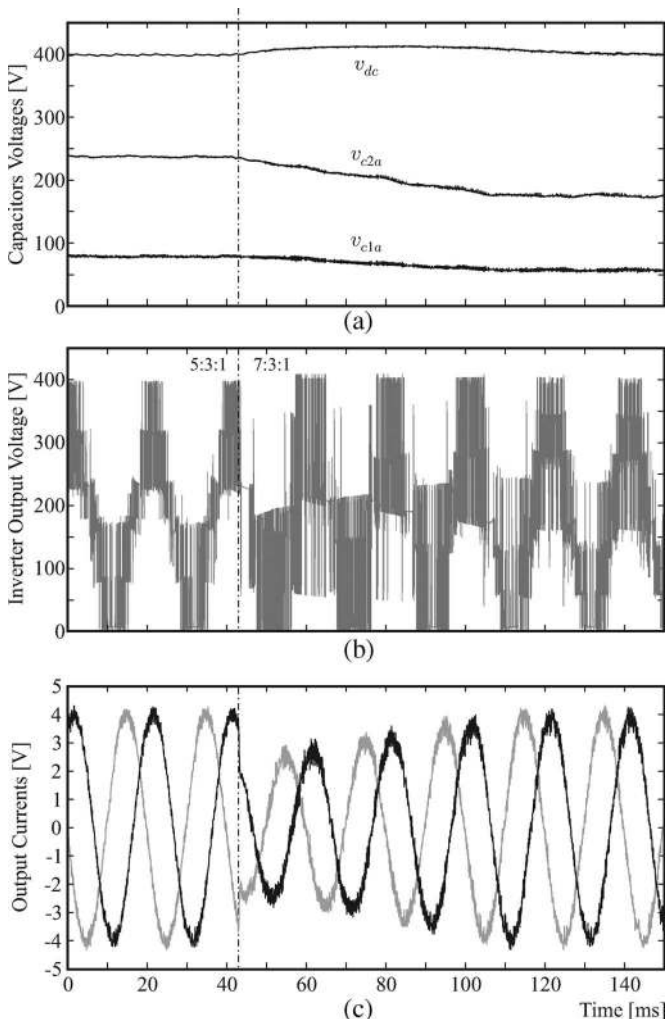

Fig. 11. Transition from 5 : 3 : 1 to 7 : 3 : 1 capacitor voltage ratio. (a) Capacitor voltages. (b) Output voltage. (c) Output currents.

voltages reach the new reference values, the output currents reach their references, too.

V. Conclusion

FC multilevel converters are complex systems due to the high number of semiconductors and electrical relationships. In this paper, we have proposed an FS-MPC strategy to achieve an increase in the possible output voltage levels and, thus, obtain better output waveforms. To keep the computational burden low, in our formulation, we have used a simplified converter model. Nevertheless, the FS-MPC method developed gives excellent performance, even when a large parameter mismatch occurs. Indeed, a significant advantage of the algorithm presented is the reduction of the output current distortion and the good dynamic behavior of the output currents and the FC voltages under reference changes.

The proposed controller gives good performance with a high-load PF even for an eight-level operation of the converter. This clearly improves upon previously reported operation limits. To reach these new FC operation modes, the FS-MPC applies brief voltage spikes which allow one to control the capacitor voltages levels. Those spikes have only a minor effect on the output

currents due to the low-pass frequency characteristic of the load. The best output currents were obtained for the six-level operation (5 : 3 : 1 voltage ratio), where voltage waveforms have fewer spikes than with the eight-level operation. Moreover, from a constructive point of view, operating at a 5 : 3 : 1 voltage ratio seems to constitute a good compromise between required capacitor voltage rates and the IGBT blocking capability rates.

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