

Modeled Tunnel Currents for High Dielectric Constant Dielectrics

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Abstract—The effect of dielectric constant and barrier height on the WKB modeled tunnel currents of MOS capacitors with effective oxide thickness of 2.0 nm is described. We first present the WKB numerical model used to determine the tunneling currents. The results of this model indicate that alternative dielectrics with higher dielectric constants show lower tunneling currents than SiO₂ at expected operating voltages. The results of SiO₂/alternative dielectric stacks indicate currents which are asymmetric with electric field direction. The tunneling current of these stacks at low biases decreases with decreasing SiO₂ thickness. Furthermore, as the dielectric constant of an insulator increased, the effect of a thin layer of SiO₂ on the current characteristics of the dielectric stack increases.

I. INTRODUCTION

AS MOSFET device dimensions continue to scale into the sub-0.1- μm regime, the required SiO₂ gate dielectric thickness is projected to reduce below 2.5 nm and the voltage supply (V_{dd}) is projected to be from 0.8 to 1.8 V [1]. At these thicknesses and voltages, a large direct tunnel current density flows between the gate electrode and the silicon substrate [2]–[4]. This large direct tunnel current increases power consumption and reduces device performance making SiO₂ undesirable in this thickness regime [4]. Therefore, there has been much interest in finding a high-permittivity gate insulator with equivalent SiO₂ thickness and sufficient barrier height as a replacement for SiO₂. However, since the barrier height tends to decrease with increasing dielectric constant [5], strong tradeoffs exist between various alternative dielectrics.

In this work we provide a comparison of the WKB modeled tunneling currents of various representative dielectrics including: SiO₂, Si₃N₄, SiO_xN_y (silicon oxynitride), high dielectric constant (25–30) insulators, and insulators formed with a layer of SiO₂ and a high dielectric constant dielectric. The modeled tunneling currents do not include the trap-assisted or Frenkel–Poole conduction mechanisms. Therefore, the results indicate the effect of changing the dielectric constant and barrier height of the insulator. Also, some authors have shown

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small trap densities for some of these dielectrics which would result in predominantly electron tunneling [5]–[8]. Overall, the goal of this study was to provide some initial first-order relationships for various dielectrics that may be used when considering development of any alternative dielectric for the gate insulator of MOS transistors.

II. TUNNELING MODEL

The following is a description of the model used to calculate the tunneling currents of n⁺p capacitors in accumulation for a Semiconductor Insulator Semiconductor (SIS) system based on a simple numerical calculation of the WKB transmission coefficient assuming equilibrium in the substrate and gate and no trap-assisted conduction.

The first part of the numerical calculations was to determine the SIS parameters with an insulator whose dielectric constant and band gap varies as a function of distance. The insulator capacitance (C_i) was calculated using

$$C_i = \left[\int_0^{t_{\text{ox}}} \frac{dx}{\varepsilon(x)} \right]^{-1} \quad (1)$$

where t_{ox} is the physical oxide thickness and $\varepsilon(x)$ is the dielectric constant as a function of distance in the insulator. The flatband voltage (V_{fb}) was calculated from the difference between the gate and substrate Fermi potentials which were determined using full Fermi–Dirac statistics [9], [10]. The gate and substrate surface potentials (ψ_{gate} , ψ_{sub}) were numerically solved from the potential and charge balance equations, [2], [9]

$$V_g = \psi_{\text{gate}} + \psi_{\text{sub}} + V_{\text{fb}} - \frac{Q_{\text{sub}}(\psi_{\text{sub}})}{C_i} \quad (2)$$

$$Q_{\text{sub}}(\psi_{\text{sub}}) + Q_{\text{gate}}(\psi_{\text{gate}}) = 0 \quad (3)$$

where Q_{sub} and Q_{gate} are the substrate and gate semiconductor charge found using full Fermi–Dirac statistics [9], [10] and V_g is the gate voltage. The oxide charge was assumed to be zero ($Q_{\text{ox}} = 0$). The potential distribution inside the insulator [$V_i(x)$], total insulator potential drop (V_{ins}) and average insulator electric field ($F_{\text{ins}} = V_{\text{ins}}/t_{\text{ox}}$) were then found by solving the Poisson equation. Finally, the insulator conduction band distribution [$E_{\text{ci}}(x)$] was determined using

$$E_{\text{ci}}(x) - E_{\text{cg}} = \phi_g(x) - qV_i(x) \quad (4)$$

where E_{cg} is the calculated polysilicon gate conduction band energy at the gate/insulator interface and $\phi_g(x)$ is the electron

affinity difference between the dielectric and polysilicon (i.e., insulator conduction band distribution at flatband). The effects of image forces were ignored.

The second part of the numerical analysis was the calculation of the tunneling current based on these SIS parameters and insulator conduction band. It was assumed that the tunneling current is due only to conduction band electrons which is a good assumption for an n^+p system biased in accumulation [11]. The tunneling current density from the gate (J_g) was calculated assuming an independent electron approximation and an elastic tunneling process [12] using the following formula [2], [10]

$$J_g = \frac{4\pi q m_t}{h^3} \int_0^{E_{fg}} dE \int_0^E T_t(E, E_t) dE_t \quad (5)$$

where E_t is the transversal energy, m_t is the transversal effective mass ($\sim 0.19m_e$), E_{fg} is the gate Fermi level at the gate/insulator (injecting) interface, E is the total energy of the tunneling electron measured from E_{cg} , T_t is the tunneling transmission probability, q is the electronic charge, and \hbar is Planck's constant. Assuming a one-band parabolic dispersion relation for the insulator conduction band, T_t can be calculated using the WKB approximation as [2], [13]

$$T_t(E, E_t) = \exp \left[-\frac{2}{\hbar} \int \sqrt{2m_t E_t - 2m_i [E - E_{ci}(x)]} dx \right] \quad (6)$$

where m_i is the insulator effective mass which is assumed constant. The integration in (6) is over all real values of the argument since we are assuming an elastic tunneling process. We have also assumed as in [10] that a single transmission probability $T_t(E, E_t) = T_t(E_{cg}, E_{cg})$ applies to all transitions in calculating the tunneling current. This approximation reduces (5) to

$$J_g = \frac{4\pi q m_t}{h^3} \frac{(E_{fg} - E_{cg})^2}{2} T_t(E_{cg}, E_{cg}). \quad (7)$$

The goal in using the above numerical model is to provide an indication of the trends expected when changing the dielectric constant and barrier height of the insulators. These tunneling calculations have a number of approximations that must be considered. Quantum-mechanical quantization effects in the semiconductor were not included. However, these quantum-mechanical effects have been shown to not strongly effect

calculated tunneling currents due to compensating effects if the calculations are performed relative to insulator potential [3]. However, for devices with thicknesses in this regime, these quantization effects must be considered when calculating surface potentials, oxide potentials, etc., as a function of gate voltage. Another issue is in the use of the WKB solution for these structures. Although the WKB solution has been shown to provide a reasonable fit to experimental data by fitting the effective mass and barrier height [2], [10], [11], the physical basis for this model for ultrathin dielectrics has been debated [3]. Furthermore, we have used a constant effective mass for all energies, thicknesses and dielectrics which may not be appropriate. There is a lack of reliable effective mass values for various dielectrics. The effective masses of the alternative dielectrics may be different and could change the magnitude of the differences in tunneling current. However, these WKB numerical calculations will provide a first order indication of the impact of dielectric constant and barrier height on tunneling currents to be used to indicate general trends expected for future dielectrics.

III. RESULTS AND DISCUSSION

To check the accuracy of our numerical calculations, the current density for an SiO_2 layer with thickness of 2.0–4.0 nm was calculated using our numerical model and compared with the current density calculated using a full numerical integration of (5) with analytical expressions for the transmission coefficients. This was done to ensure that our numerical solution correctly fit other similar WKB formulations. The transmission coefficients previously determined for direct and Fowler–Nordheim tunneling (T_{fn} , T_d) into SiO_2 with a constant barrier height (ϕ_g) and constant dielectric constant are shown at the bottom of the page in (8) and (9) [2]. Table I gives the parameters assumed for the gate electrode and Si substrate and Table II contains the parameters assumed for the SiO_2 insulator. We have fit this numerical model to experimental data for SiO_2 down to 2.0 nm using an effective mass of $m_i = 0.32m_e$. A constant effective mass of $m_i = 0.32$ was assumed for these calculations [2]. The results shown in Fig. 1 indicate good agreement between the models suggesting that our numerical formulation is in agreement with other WKB calculations.

The tunneling model described in the previous section was used to compare the tunneling currents of a variety of insulators termed: SiO_2 , Si_3N_4 , SiO_xN_y , D1, and D2. Dielectric/ SiO_2 stacked structures were also examined.

$$T_{fn}(E, E_t) = \exp \left[-\frac{4(2\pi)}{3} \frac{\sqrt{2m_i} \left(\phi_g + E_{fg} - E + \frac{m_t}{m_i} E_t \right)^{3/2}}{qh F_{ins}} \right] \quad (8)$$

$$T_d(E, E_t) = \exp \left[-\frac{4(2\pi)}{3} \frac{\sqrt{2m_i} \left(\phi_g + E_{fg} - E + \frac{m_t}{m_i} E_t \right)^{3/2} - \left(\phi_g + E_{fg} - E + \frac{m_t}{m_i} E_t + qV_{ins} \right)^{3/2}}{qh F_{ins}} \right] \quad (9)$$

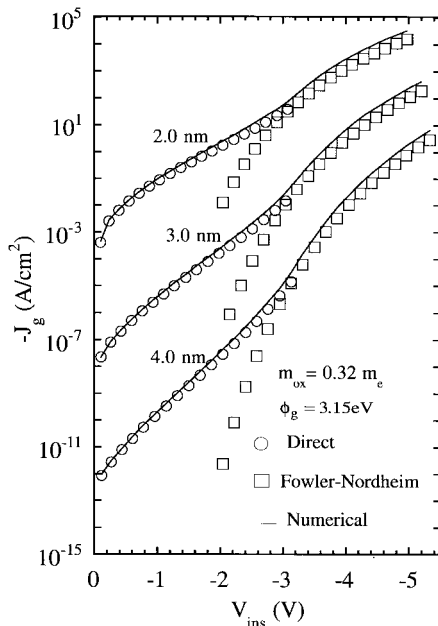


Fig. 1. Comparison of our numerical WKB model of calculating tunneling current for SiO₂ (2.0–4.0 nm) to a full numerical integration of (5) using the previously determined analytical transmission coefficients for direct and Fowler–Nordheim tunneling into SiO₂ [2].

TABLE I
GATE ELECTRODE AND Si SUBSTRATE SEMICONDUCTOR
PARAMETERS USED IN CALCULATING THE TUNNELING CURRENTS

	Gate Electrode	Si Substrate
Dielectric Constant (ϵ)	$11.8\epsilon_0$	$11.8\epsilon_0$
Doping (N_d, N_a)	$1.00 \cdot 10^{20} \text{ cm}^{-3}$	$2.00 \cdot 10^{17} \text{ cm}^{-3}$
Dopant Ionization Energy ($E_c - E_d, E_c - E_a$)	0.045 eV	1.075 eV
Energy Gap (E_g)	1.12 eV	1.12 eV
Effective Density of States in Conduction Band (N_c)	$2.80 \cdot 10^{19} \text{ cm}^{-3}$	$2.80 \cdot 10^{19} \text{ cm}^{-3}$
Effective Density of States in Valence Band (N_v)	$1.04 \cdot 10^{19} \text{ cm}^{-3}$	$1.04 \cdot 10^{19} \text{ cm}^{-3}$
Intrinsic Carrier Concentration (n_i)	$1.45 \cdot 10^{10} \text{ cm}^{-3}$	$1.45 \cdot 10^{10} \text{ cm}^{-3}$

TABLE II
INSULATOR DIELECTRIC CONSTANT AND BARRIER HEIGHT USED IN
CALCULATING THE TUNNELING CURRENTS. THE BARRIER HEIGHT IS DEFINED AS
THE CONDUCTION BAND DISCONTINUITY BETWEEN THE INSULATOR AND SILICON

	Dielectric Constant (ϵ)	Barrier Height
SiO ₂ [9]	$3.9\epsilon_0$	3.15 eV
Si ₃ N ₄ [9]	$7.5\epsilon_0$	2.10 eV
SiO _x N _y	$5.7\epsilon_0$	2.60 eV
D1	$25.0\epsilon_0$	1.30 eV
D2	$30.0\epsilon_0$	1.00 eV

Table II indicates the dielectric constant and barrier height used for each of the insulators. The barrier height is defined as the conduction band discontinuity (electron affinity difference) between the insulator and silicon. Note that the oxynitride film (SiO_xN_y) has an assumed dielectric constant and barrier height halfway between the values for Si₃N₄ and SiO₂ [9]. The values chosen for D1 and D2 are representative of several higher dielectric constant (high- k) alternative insulators (e.g., TiO₂, Ta₂O₅) [5]–[7], [14]–[20]. The total thickness of each

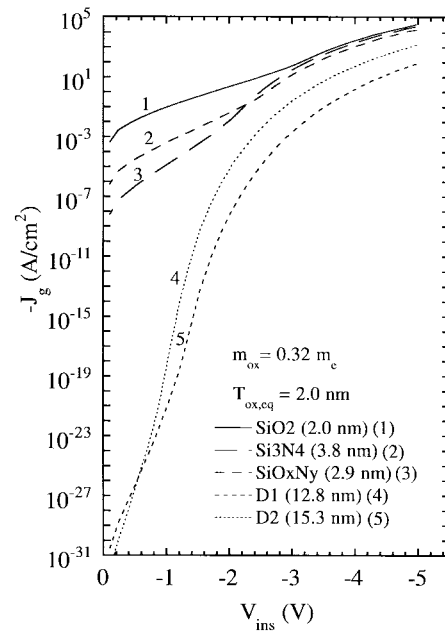


Fig. 2. Tunneling current versus insulator potential for n⁺p capacitors with various dielectrics having equivalent oxide thickness of 2.0 nm.

of the insulators was chosen to achieve an SiO₂ equivalent thickness of 2.0 nm. The effective mass was assumed constant for each insulator ($m_i = 0.32m_e$) so that the effect of barrier height and dielectric constant could be easily discerned. The tunneling currents from the gate were calculated assuming an n⁺p capacitor with the parameters given in Table I.

Fig. 2 shows the tunneling currents calculated for each of the dielectrics as a function of total insulator potential drop. The results indicate that for very low voltages, the insulators with the highest dielectric constant show the lowest tunneling currents. The currents for D1 and D2 are observed to cross at $|V_{\text{ins}}| = \sim 0.6$ V. This cross-over can be qualitatively explained by considering that the current (7) is proportional to the transmission coefficient (6). The transmission coefficient is inversely and exponentially dependent on an integration of the square root of the insulator conduction band in which the electron travels under (which we will call barrier area). Therefore, the cross-over occurs when the increase of barrier area due to the tunneling distance of D2 is compensated for by the increase in barrier area due to the barrier height of D1. A large increase of current for each of the insulators is observed for $|V_{\text{ins}}| > \phi_g$ because the tunneling electrons begin to tunnel through less of a distance and enter the insulator conduction band (Fowler–Nordheim tunneling). The results suggest that to reduce the expected tunnel current, it is more beneficial to have a high- k dielectric with ϕ_g slightly higher than the expected supply voltage ($V_{\text{dd}} \approx 1$ V) for $T_{\text{ox,eq}} = 2.0$ nm, than to have an insulator with slightly higher dielectric constant but lower ϕ_g . It is also observed that Si₃N₄ and SiO_xN_y show modest improvements over SiO₂. However, these insulators with $\phi_g > V_{\text{dd}}$ do not have the high dielectric constant needed to further reduce the current.

The results of Fig. 2 indicate that replacement of SiO₂ with an alternative dielectric results in a reduction of tunnel current

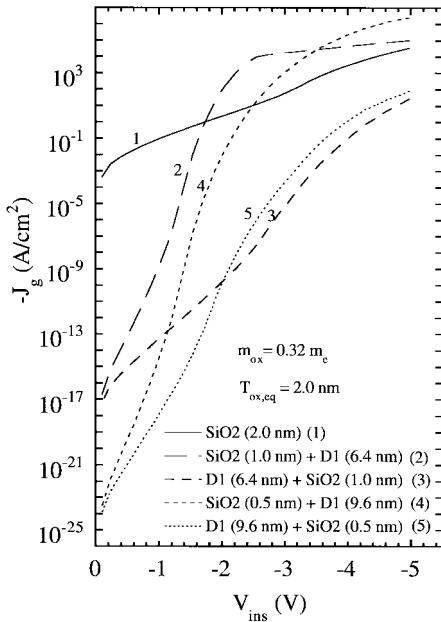


Fig. 3. Tunneling current versus insulator potential for n^+p capacitors with D1/SiO₂ stacked dielectrics having equivalent oxide thickness of 2.0 nm.

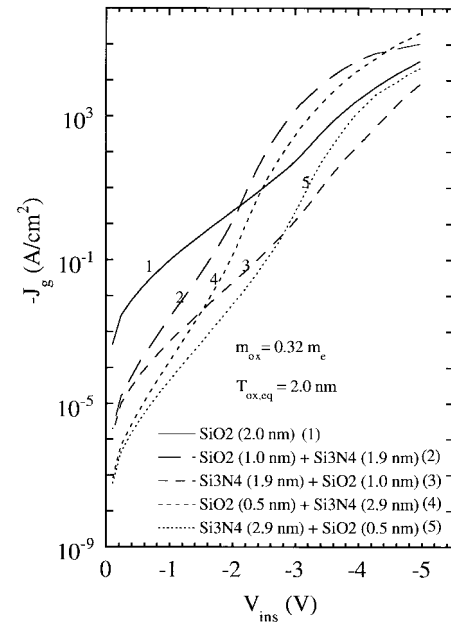


Fig. 4. Tunneling current versus insulator potential for n^+p capacitors with Si₃N₄/SiO₂ stacked dielectrics having equivalent oxide thickness of 2.0 nm.

which is most significant at lower voltage. However, instead of using only and alternative dielectric, many researchers have used SiO₂/alternative dielectric stacks [6], [21]–[23]. The reasons for this include controlling interface state density and modifying barrier properties. Also, the SiO₂ in these stacked structures can be present as a native oxide at the Si interface [18]. Figs. 3 and 4 show the calculated tunneling currents for D1/SiO₂ and Si₃N₄/SiO₂ stacked structures, respectively. The insulator which is listed first is the dielectric which the electron first tunnels through. The change in the order of the insulator stack is equivalent to changing the electric field direction on this stack.

It is observed that the tunneling currents change dramatically depending on which insulator the electron first tunnels through. Specifically, the tunnel current is much higher if the electron first tunnels through the higher barrier height material (SiO₂). This can be best understood by considering the insulator conduction band diagrams given in Fig. 5 for the SiO₂ (1.0 nm)/D1 (6.4 nm) stacks for $V_{ins} = -2.38$ V. It is observed that at this voltage (and above), an electron which first tunnels through the SiO₂, no longer tunnels through any of the D1 barrier so that the tunneling is determined only by the 1.0 nm SiO₂ barrier. However, an electron which first tunnels through the D1 barrier, will also tunnel through the SiO₂ barrier for these voltage ranges. The insulator voltage at which the electron will no longer tunnel through the second barrier approximately corresponds to the condition when the SiO₂ layer drops a voltage equivalent to the barrier height of the second layer.

Fig. 6 shows the insulator conduction band for SiO₂ (0.5 nm)/D1 (9.6 nm) stacks for the same voltage ($V_{ins} = -2.38$ V). Comparison of Figs. 5 and 6 indicate that for this insulator potential, an electron will tunnel through a larger portion of the barrier for stacks with thinner SiO₂

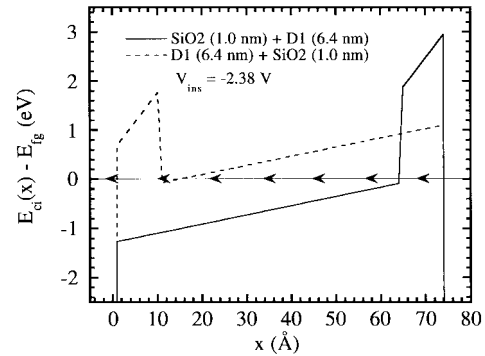


Fig. 5. Insulator conduction band distribution referenced to the gate Fermi level for SiO₂ (1.0 nm)/D1 (6.4 nm) stacked dielectrics at an insulator potential of -2.38 V.

regions. When the bias is increased further, an electron which first tunnels through the 0.5 nm SiO₂ barrier will no longer tunnel through the D1 barrier so that the tunneling is determined only by the 0.5 nm SiO₂ barrier. Therefore, for very high biases, the tunneling current for the SiO₂ (0.5 nm) + D1 (9.6 nm) stack will be greater than the tunneling current for the SiO₂ (1.0 nm) + D1 (6.4 nm) since the tunneling distance is shorter.

Comparing Figs. 3 and 4 shows that stacked insulators using Si₃N₄ result in smaller current changes than in using D1. This is simply because the current for biases when the electron is tunneling through the entire barrier is closer to the current for biases when the electron is tunneling only through the SiO₂. Furthermore, the barrier heights and dielectric constants of the Si₃N₄ and SiO₂ insulators are much closer than D1 and SiO₂ so that the total barrier for the electron is less affected for the Si₃N₄/SiO₂ stacked structures. This result indicates that a thin layer of SiO₂ with Alt1 results in a drastic difference in current as compared to Si₃N₄.

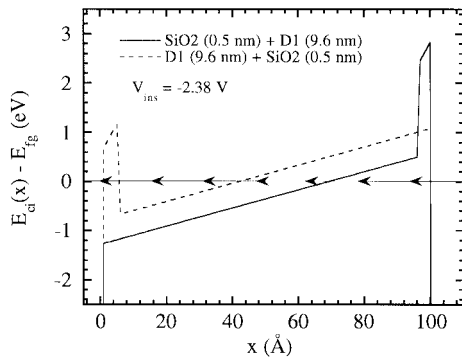


Fig. 6. Insulator conduction band distribution referenced to the gate Fermi level for SiO₂ (0.5 nm)/D1 (9.6 nm) stacked dielectrics at an insulator potential of -2.38 V.

IV. SUMMARY

The tunneling currents for insulators with an effective oxide thickness of 2.0 nm were modeled using a numerical calculation of the WKB tunneling current. Our model was shown to agree with previously determined analytical WKB formulations of tunneling current for SiO₂. The numerical tunneling model was first applied to alternative dielectrics having different barrier heights and dielectric constants. The results indicated that alternative dielectrics with higher dielectric constants resulted in lower currents at low biases. However, it was concluded that it is more beneficial to have a high- k dielectric with barrier height slightly higher than the expected supply voltage, than to have an insulator with slightly higher dielectric constant. The numerical tunneling model was then applied to SiO₂/alternative dielectric stacks. The results indicated that the tunnel current changes dramatically for these stacks with change in electric field direction (change in which barrier the electron first tunnels through). It was observed that the tunneling current of these stacks at low biases decreases with decreasing SiO₂ thickness. Furthermore, as the dielectric constant of an insulator increased, the effect of a thin layer of SiO₂ on the current characteristics of the dielectric stack increased.

Overall, the modeled tunneling current characteristics for these ideal alternative dielectrics (no trap-assisted current) have provided an indication of the trends expected when modifying the dielectric constant and barrier height of insulators. The above calculations show that if an alternative high dielectric constant material is to replace SiO₂, then it will be necessary to find one with a barrier height greater than the applied voltage and one that can be fabricated with a few atomic layers (or less) of SiO₂ at the interface. This may prove to be a difficult challenge for future IC manufacturing.

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