Modeling and Analysis of High-Speed Links

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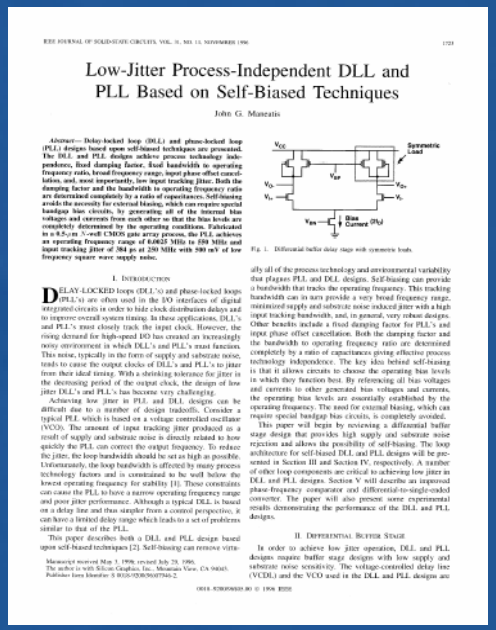
High-Speed Link Research

- Used to focus on making chip fast
  - Required precision timing – PLL
  - Require HS transmitter, receiver circuitry
  - Many papers on these topics



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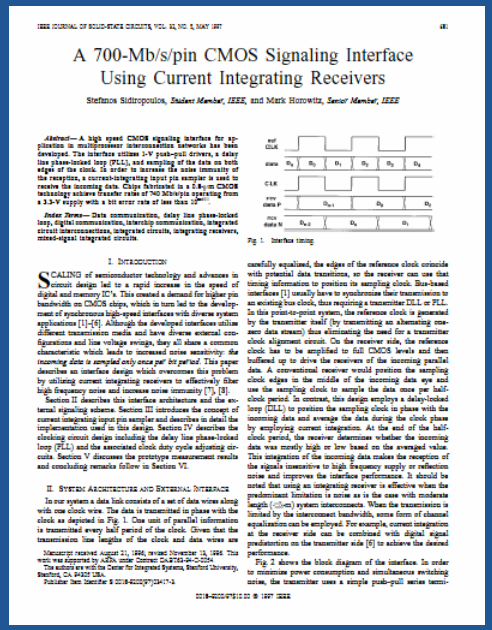
Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques

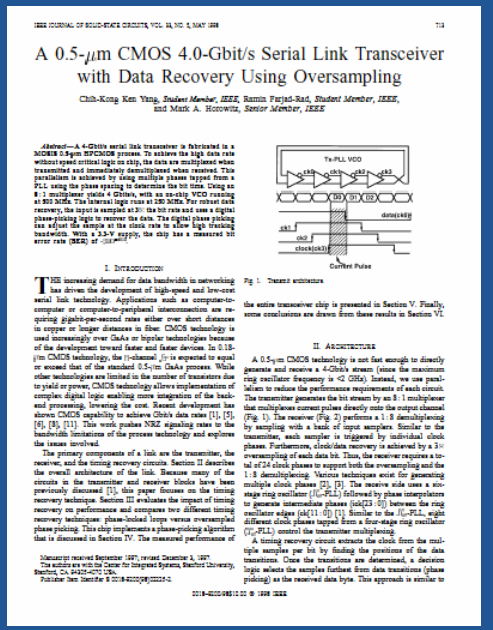
John G. Maneatis



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 32, NO. 5, MAY 1997 681

A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers

Stefanos Sidiropoulos, *Student Member, IEEE*, and Mark Horowitz, *Senior Member, IEEE*

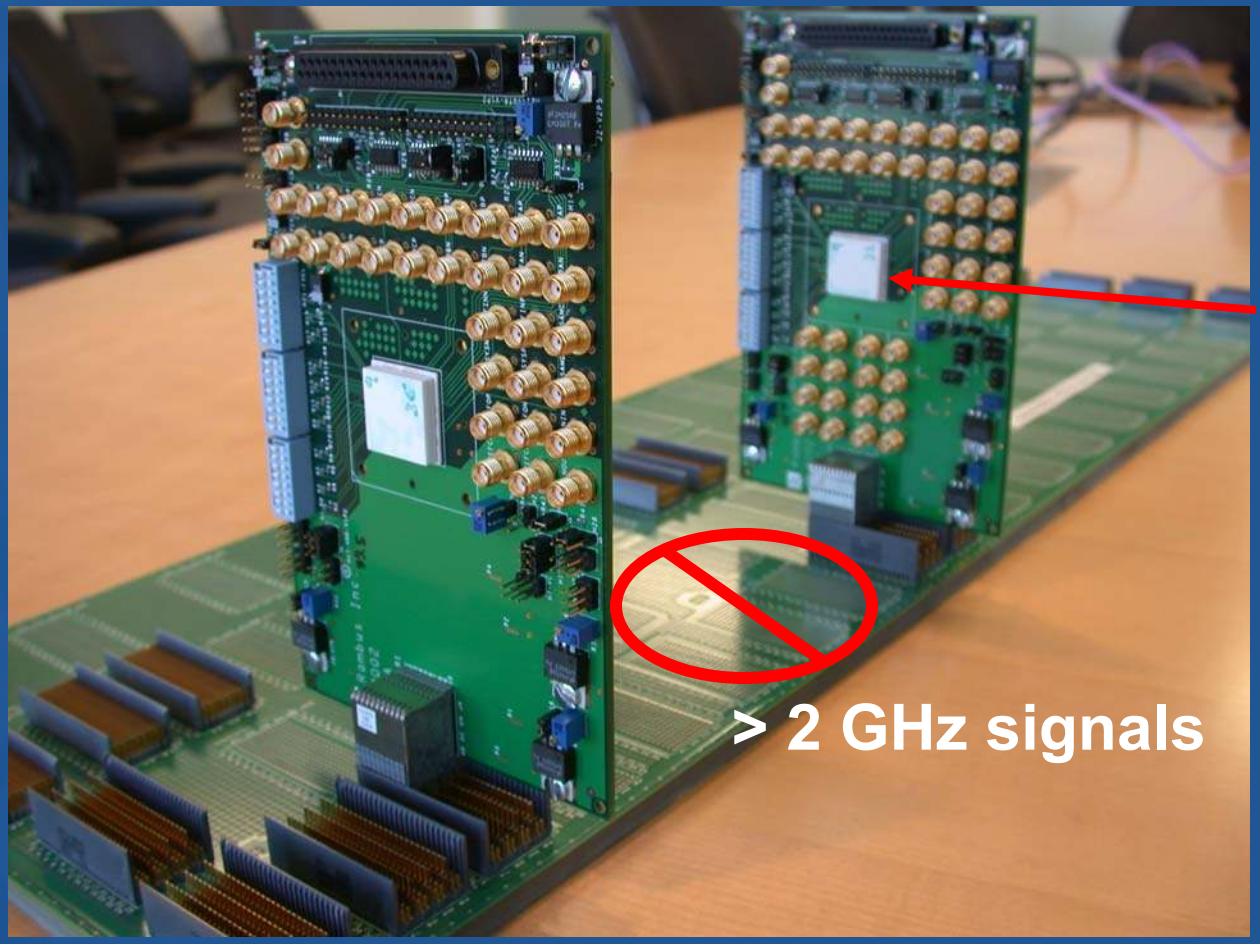


IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 32, NO. 5, MAY 1997 713

A 0.5-μm CMOS 4.0-Gbit/s Serial Link Transceiver with Data Recovery Using Oversampling

Chih-Kong Ken Yang, *Student Member, IEEE*, Ramin Farjad-Rad, *Student Member, IEEE*, and Mark A. Horowitz, *Senior Member, IEEE*

Present Problem:



- Now, the bandwidth limit is in wires

New Link Research:

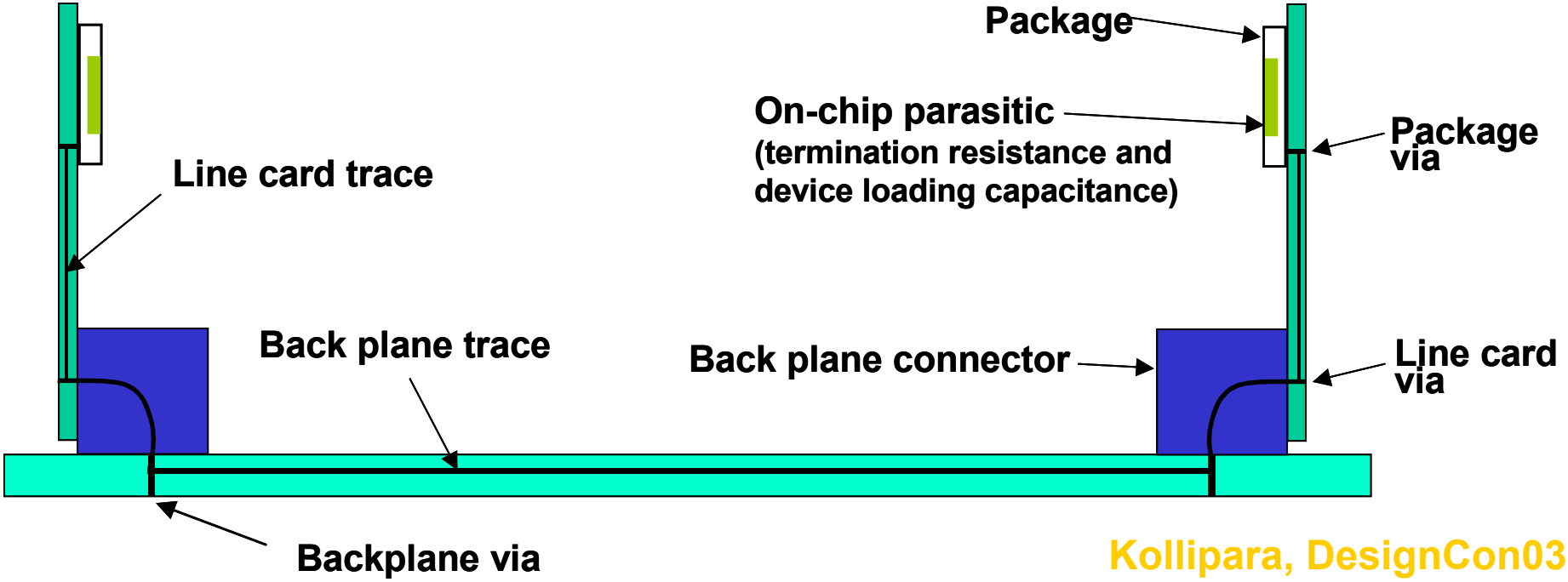
Dealing with bandwidth limited channels

- This is an old research area
  - Textbooks on digital communications
  - Think modems, DSL
- But can't directly apply their solutions
  - Standard approach requires high-speed A/Ds and digital signal processing
  - 20Gs/s A/Ds are expensive
- (Un)fortunately need to rethink issues

Outline Of This Talk

- Create a framework to evaluate trade-offs
  - For practical Gs/s digital communication systems
- Channel
  - How is the signal degraded?
- Noise (voltage and timing)
  - How large must the received signal be?
- Communication techniques
  - How much of the noise can be reduced
  - While maintaining a reasonable cost

Backplane Environment

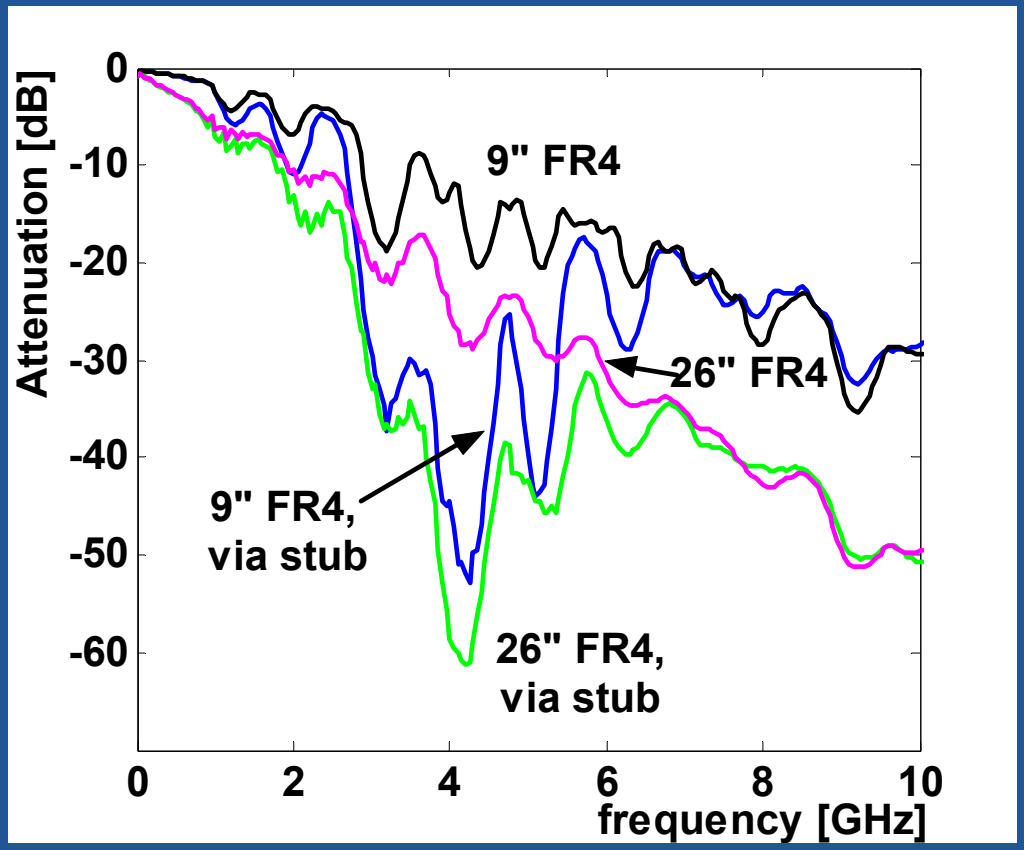


Kollipara, DesignCon03

- Line attenuation
- Reflections from stubs (vias)

Backplane Channel

- Loss is variable
  - Same backplane
  - Different lengths
  - Different stubs
    - Top vs. Bot
- Attenuation is large
  - >30dB @ 3GHz
  - But is that bad?
- Required signal amplitude set by noise

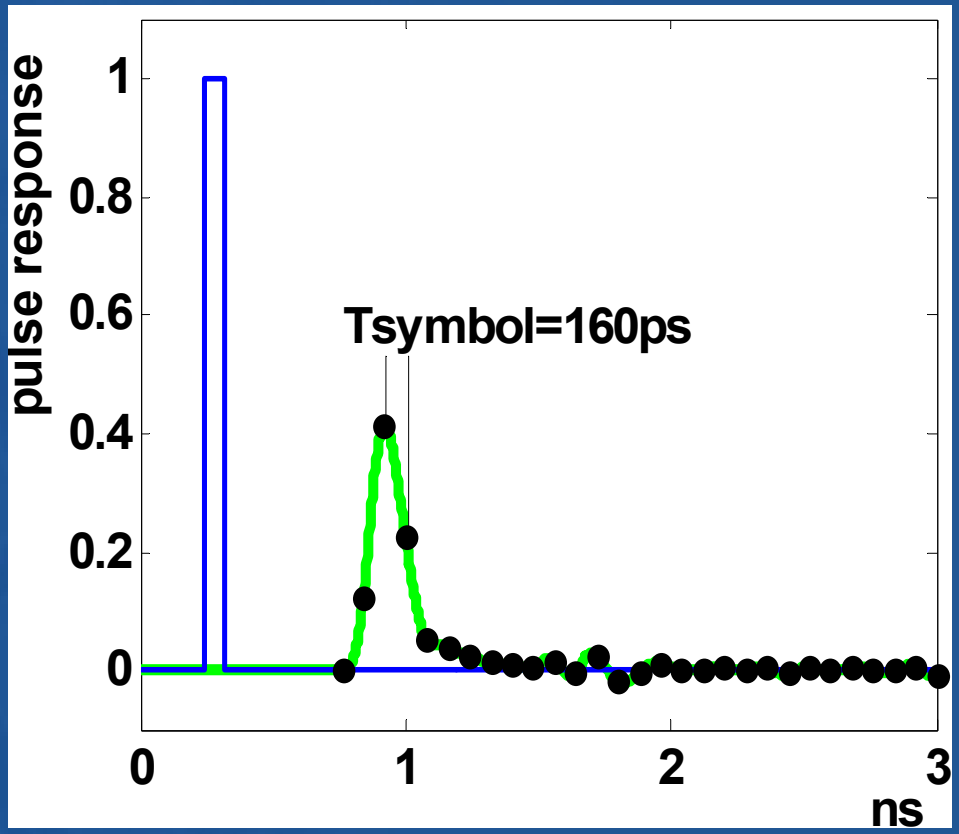


What We Will Call Noise

- Deterministic errors
  - Things we could in theory correct but don't
- Random noise
  - Have no choice
- Noise comes in two dimensions
  - Voltage
  - Timing
    - Will convert to an effective voltage noise

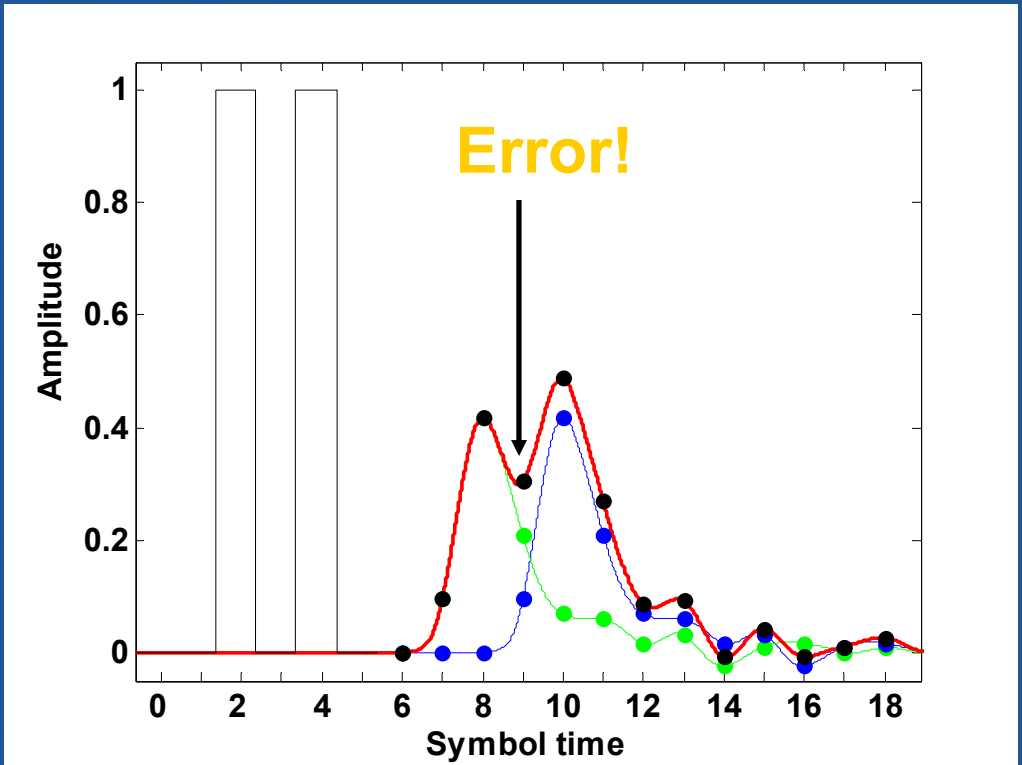
Inter-symbol Interference (ISI)

- Channel is low pass
  - Our nice short pulse gets spread out



- Dispersion – short latency (skin-effect, dielectric loss)
- Reflections – long latency (impedance mismatches – connectors, via stubs, device parasitics, package)

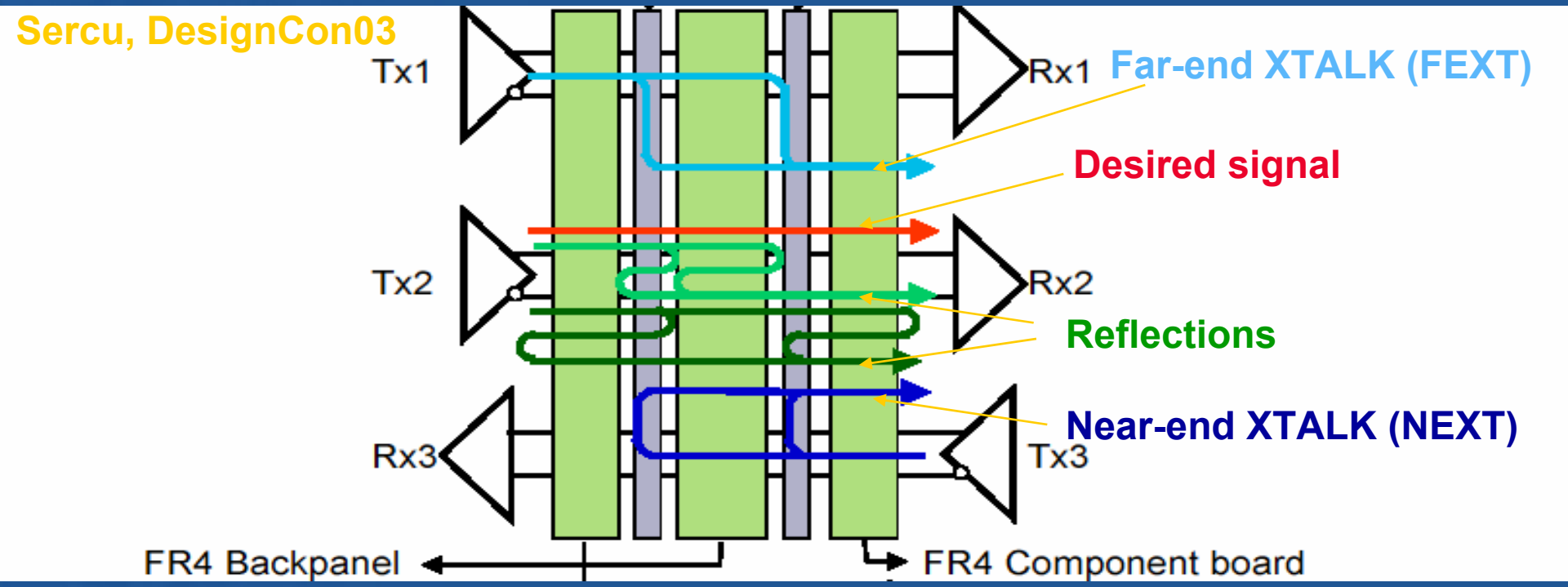
ISI



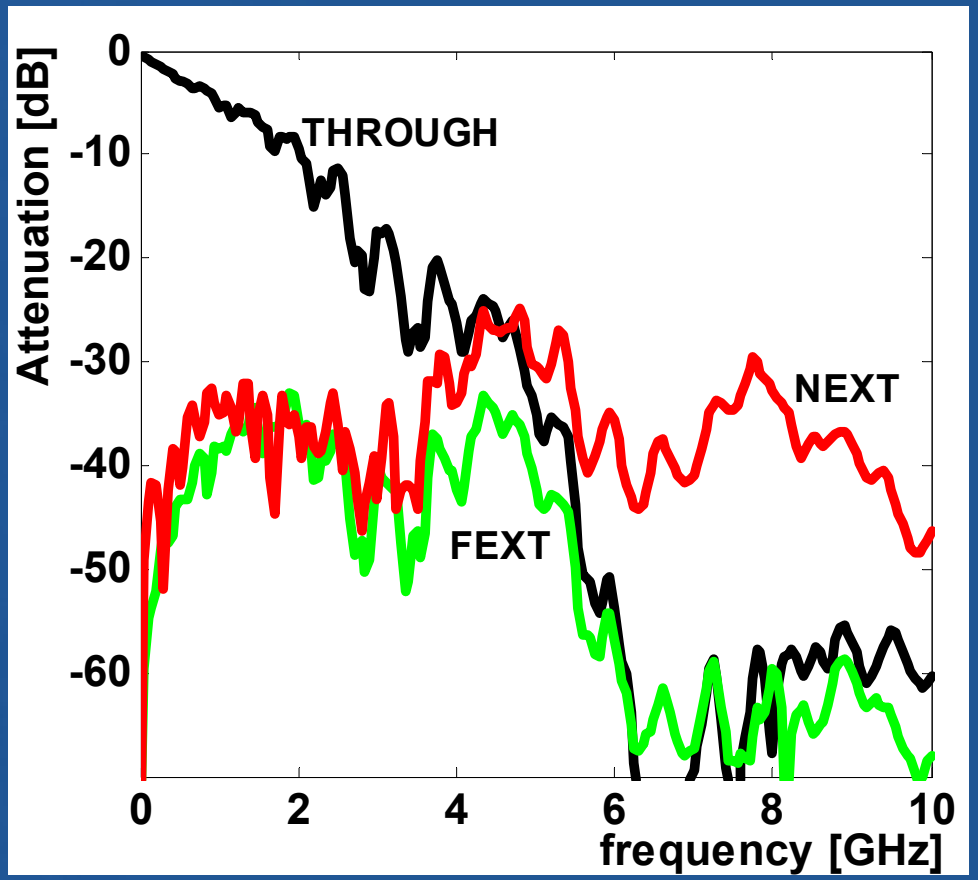
- Middle sample is corrupted by 0.2 trailing ISI (from the previous symbol), and 0.1 leading ISI (from the next symbol) resulting in 0.3 total ISI
- As a result middle symbol is detected in error

Crosstalk

- Don’t just receive the signal you want
  - Get versions of signals “close” to you
  - Vertical connections have worse coupling
    - “Close” in these vertical connection regions



Frequency View of Crosstalk



- For this example:
  - > 4GHz, noise is as large as the signal

Random Voltage Noise

- Thermal noise
  - Resistor and Device noise
- Quantization
- Estimation error
- Supply noise
- Receiver offset

Modeling “Noise” Sources

Generally use one of two methods:

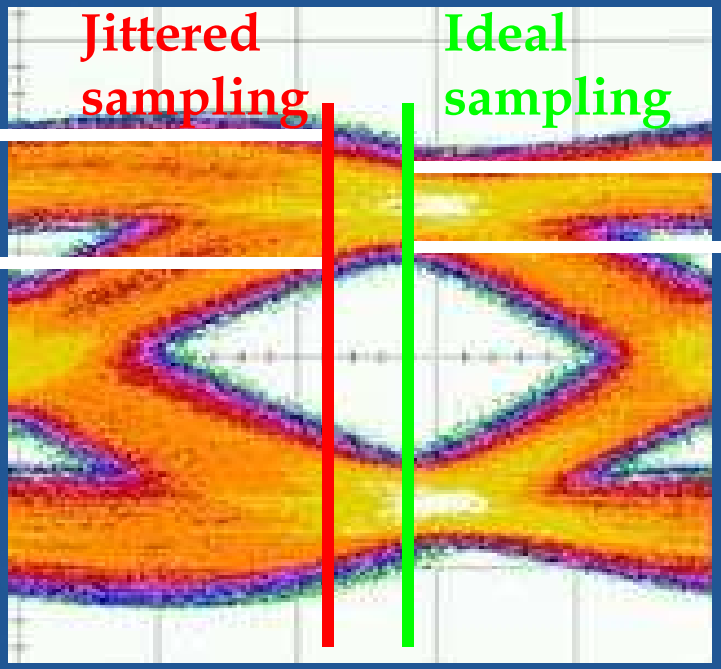
- Worst case analysis
  - Used for deterministic “noise” like ISI
  - Find worst case and subtract from signal
  - Then apply Gaussian Noise to result
- Assume Gaussian Distribution
  - Rely on Central-Limit Theorem
  - Most noise looks Gaussian, right?

Accuracy Issues

- Worst case analysis
  - Can be too pessimistic
    - If probability of worst case very small
- Gaussian distributions
  - Works well near mean
  - Often way off at tails
    - E.g. ISI distribution is bounded
- We will use direct noise statistics

Effect of Timing Noise

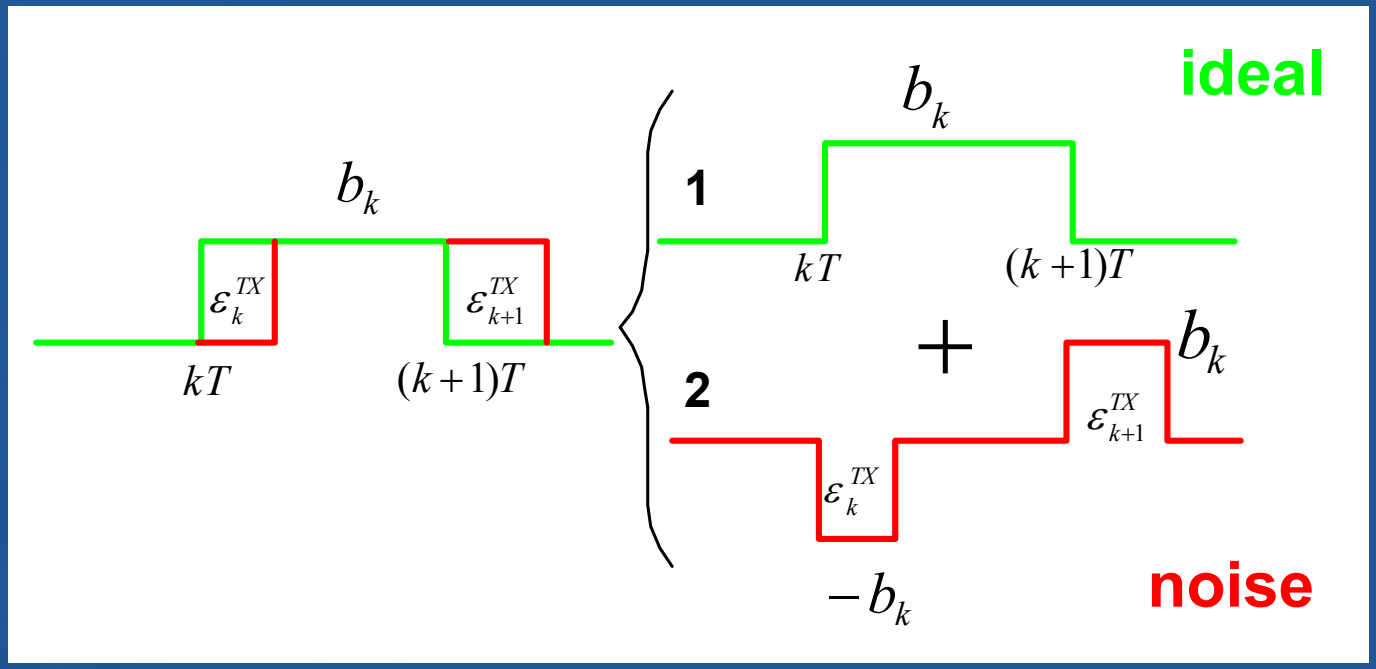
- Need to map from time to voltage



- The effect is going to depend on the size of the jitter, the input sequence, and the channel

Effect of Transmitter Jitter

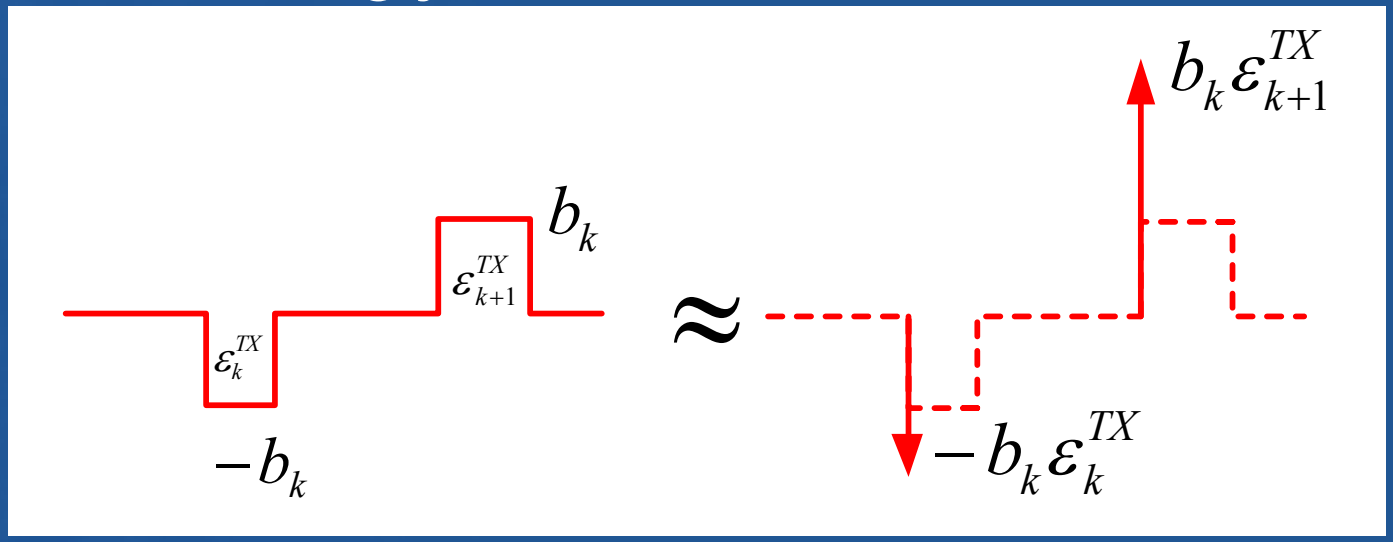
Jittered pulse decomposition



- Decompose output into ideal and noise
- Noise are pulses at front and end of symbol
  - Width of pulse is equal to jitter

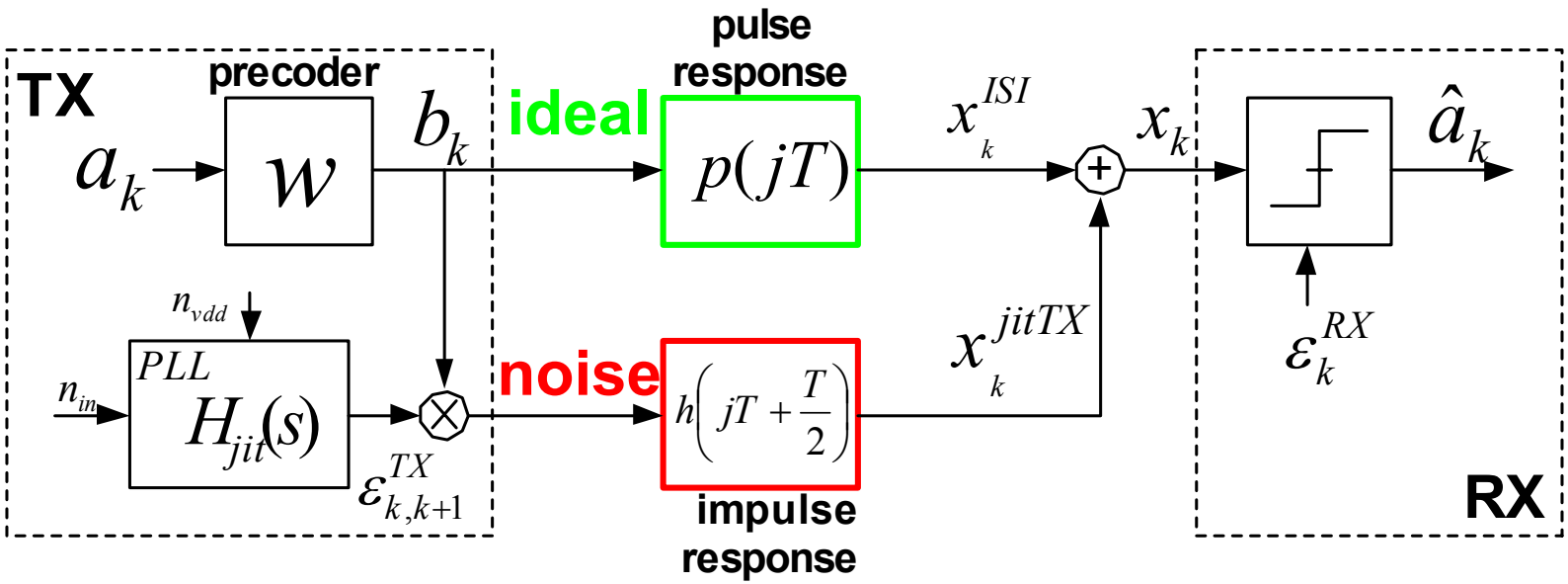
Transmitter Jitter Noise

- Approximate the noise pulses with deltas
  - Assuming jitter is small



- Channel output
  - Output with no jitter
  - Response to the noise deltas

Jitter Propagation Model



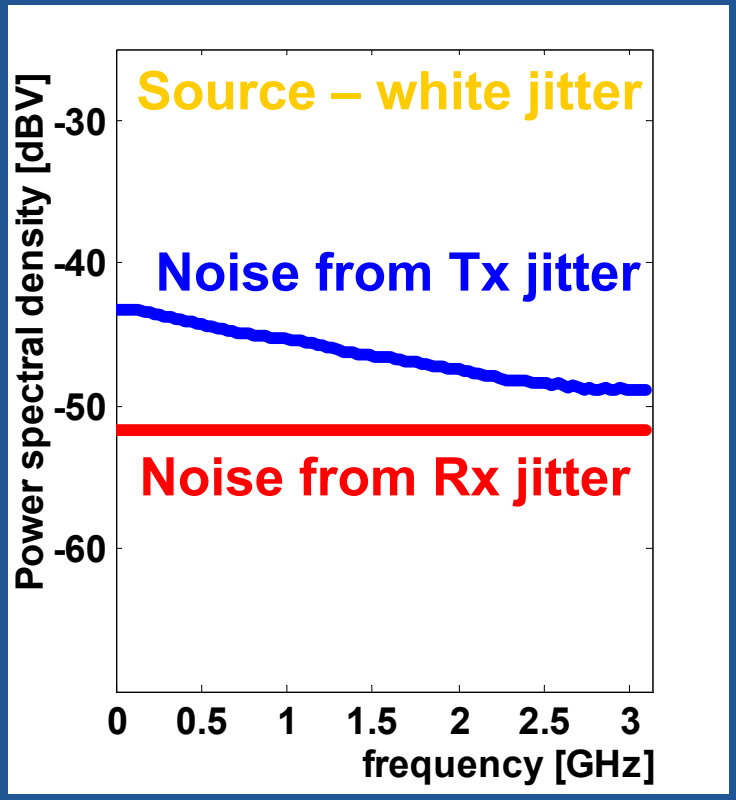
- Channel bandwidth matters
  - If h(T/2) is small, the noise is small
  - h(nT+1/2) not small, many pulses add

Jitter Effect On Voltage Noise

- Transmitter jitter
  - High frequency (cycle-cycle) jitter is bad
    - Changes the energy (area) of the symbol
    - No correlation of noise sources that sum
  - Low frequency jitter is less bad
    - Effectively shifts waveform
    - Correlated noise give partial cancellation
- Receive jitter
  - Modeled by shift of transmit sequence
  - Same as low frequency transmitter jitter

Voltage Noise From Jitter

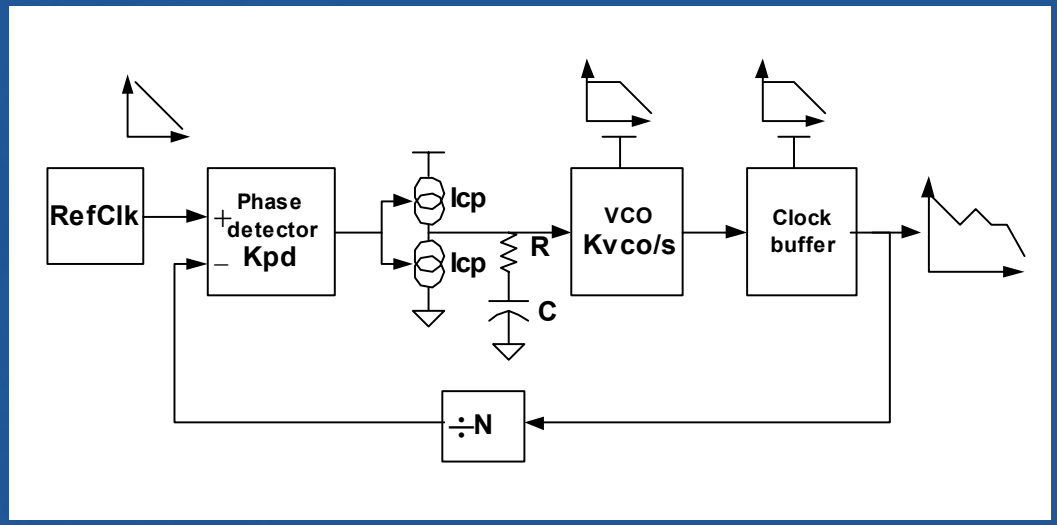
- White jitter
  - Noise from Tx much larger than from Rx jitter
  - From Rx jitter, noise is white
  - From Tx jitter, filtered by the channel
- Y-axis is noise σ (in Volts)
  - If the noise was white
  - σ = 10mV => -40dBV



- Bandwidth of the jitter is critical
  - It sets the magnitude of the noise created

Jitter Source From PLL Clocks

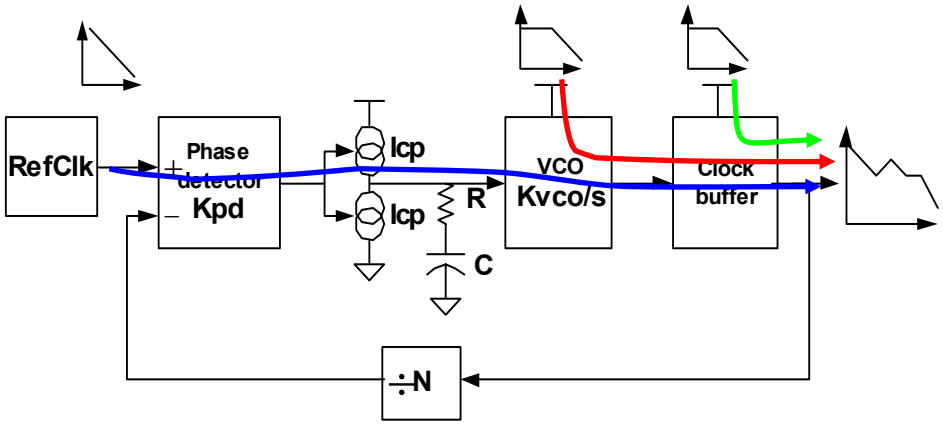
- Noise sources
  - Reference clock phase noise
  - VCO supply noise
  - Clock buffer supply noise

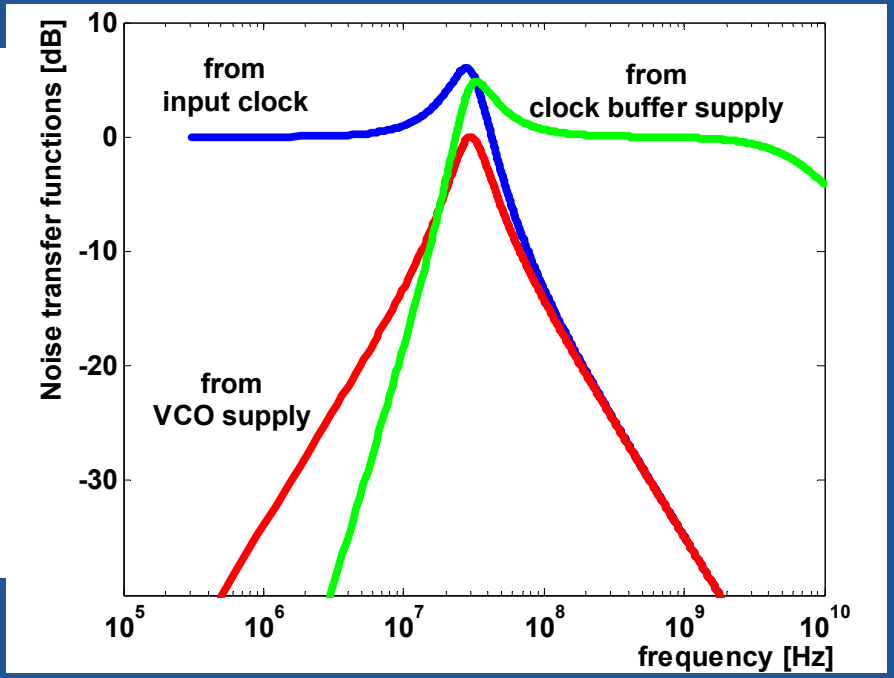


Mansuri '02

- Stationary phase-space model

Noise Transfer Functions



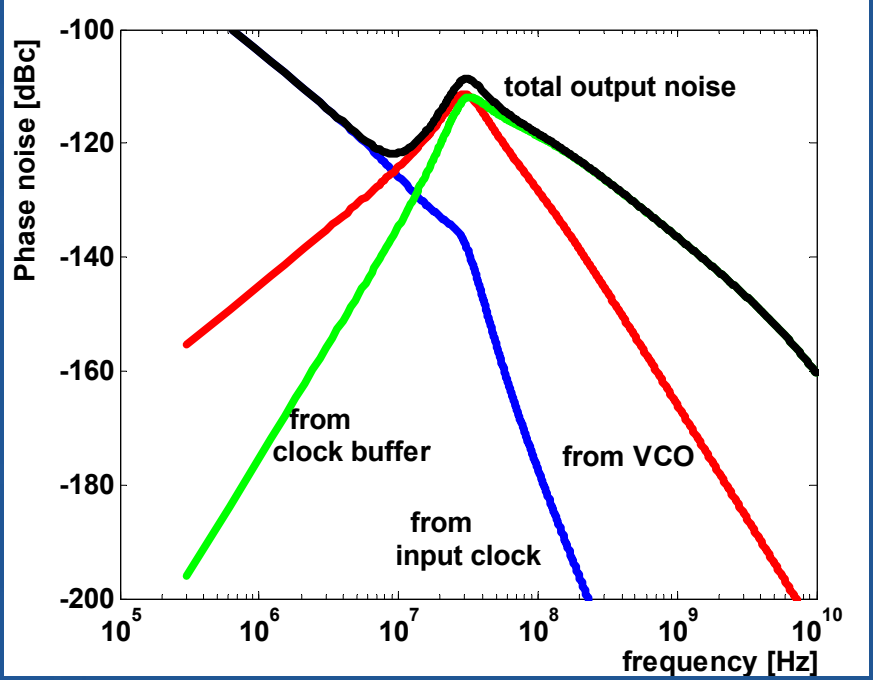


- Low-pass from reference (input clock)
- Band-pass from VCO supply
- High-pass from clock buffer supply

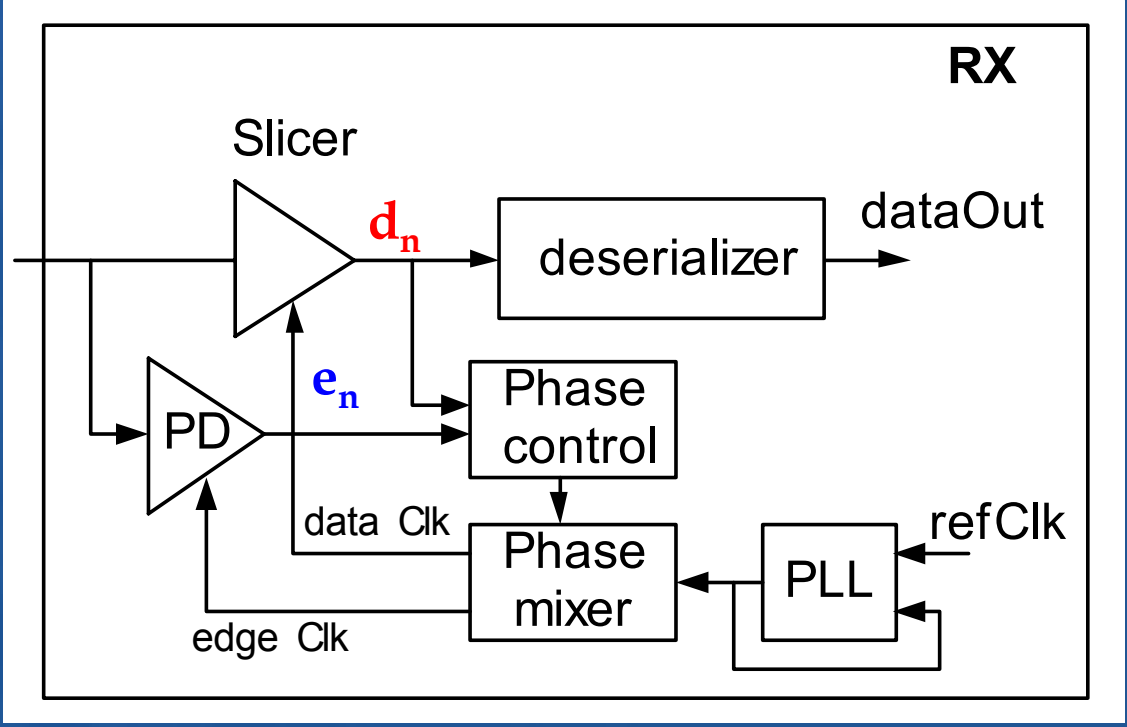
Jitter Spectrum

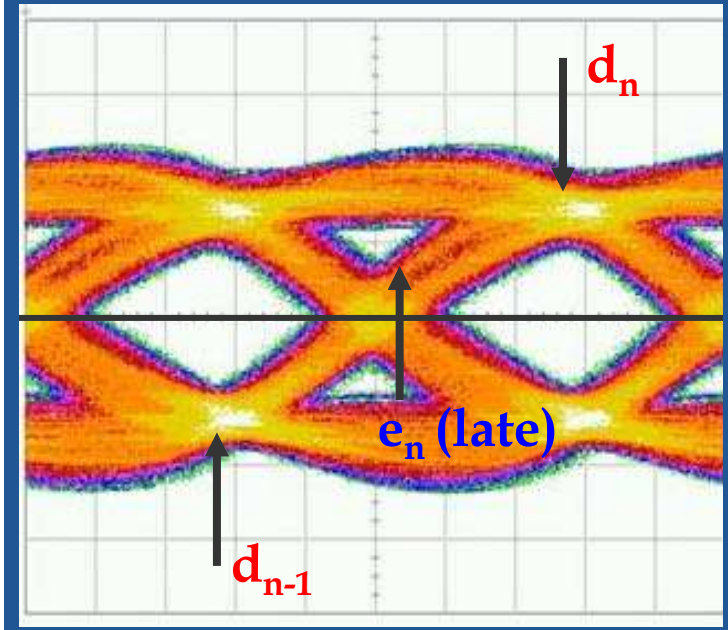
- Set by reference clock f < loop bandwidth
- Set by supply noise f ≥ loop bandwidth

Spectrum using 100MHz BW power supply noise



2x Oversampled Bang-Bang CDR



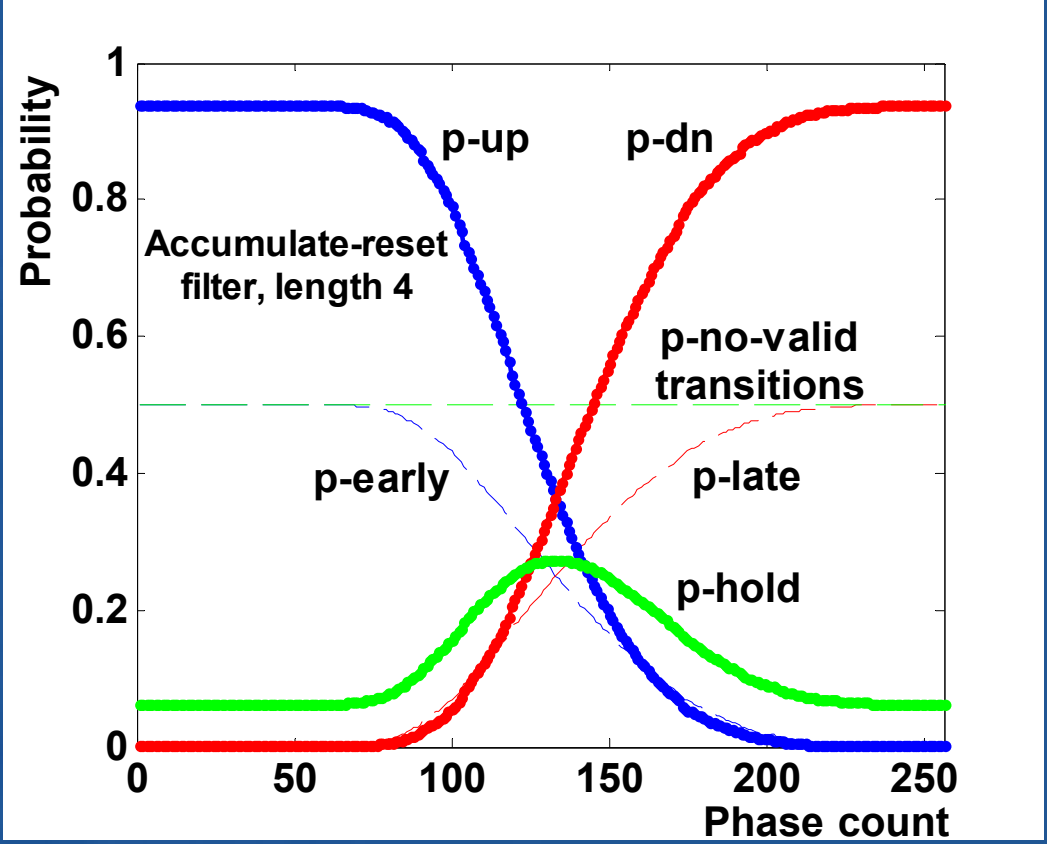


- Generate early/late from d_n,d_{n-1},e_n
  - Simple 1st order loop, cancels receiver setup time
- Now need jitter on data Clk, not PLL output

Data Clk Noise

- Model phase selector and PLL
  - Base linear PLL jitter
  - Add non-linear phase selector noise from CDR
- Model the CDR loop as a state machine
  - The current phase position is the state
  - State transitions are caused by early/late
  - Jitter on input data and PLL means
    - Possible to be late and get early PD result
    - Often filter early/late to generate up/down

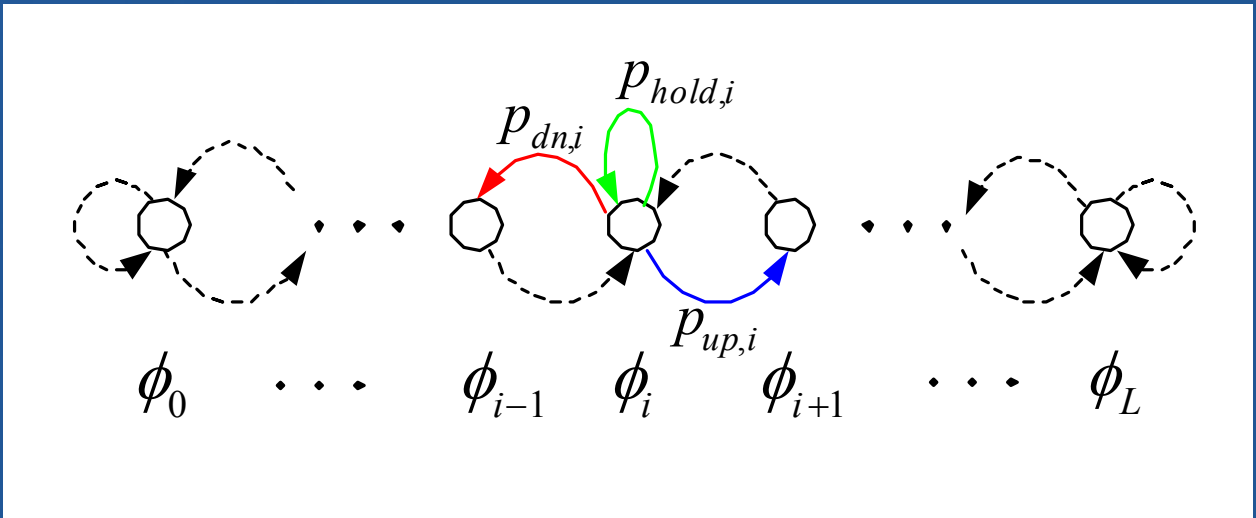
Transition Probabilities



- Example system:
  - CDR loop
  - Residual ISI
    - At edge -30dBV
  - Desired phase
    - State = 133

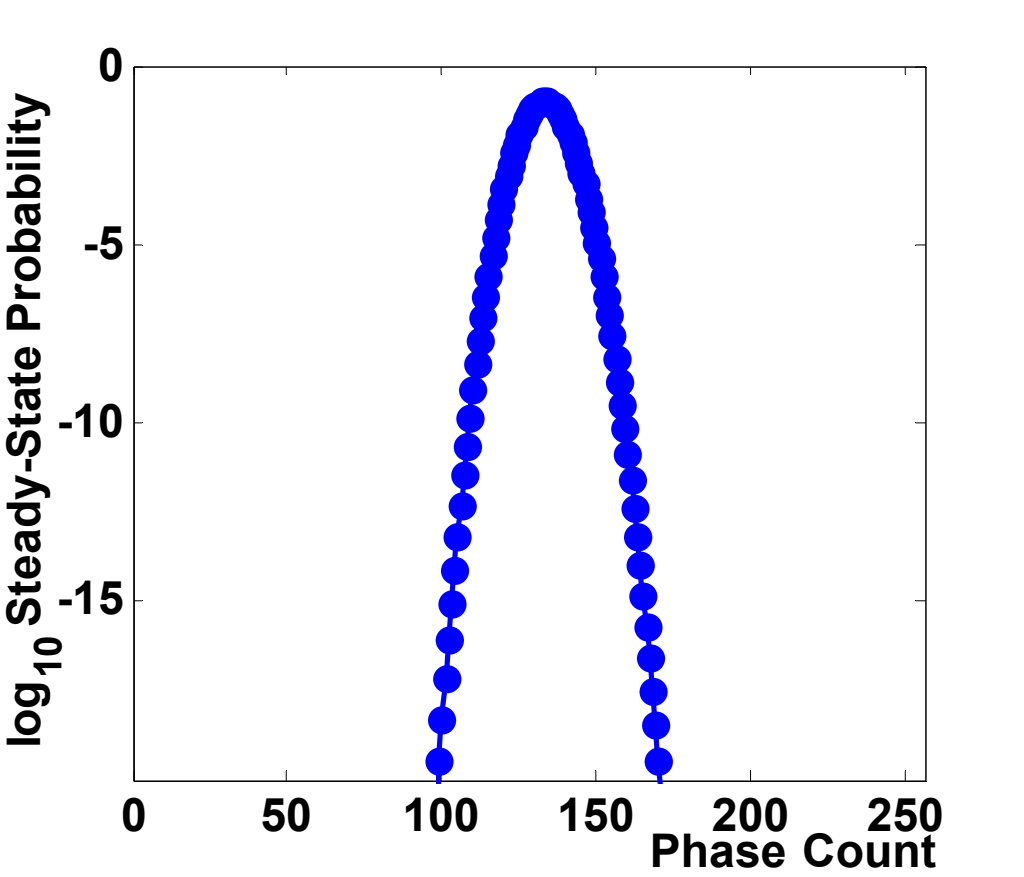
- On average move to correct position
  - But probability of wrong movement is not small
  - Need to find probability of at each phase location

Bang-Bang CDR Statistical Model



- Need steady state probabilities of the states
  - Have the transition probabilities
- Iteratively apply transition probabilities
  - Results will converge to a steady-state

Bang-Bang CDR Model

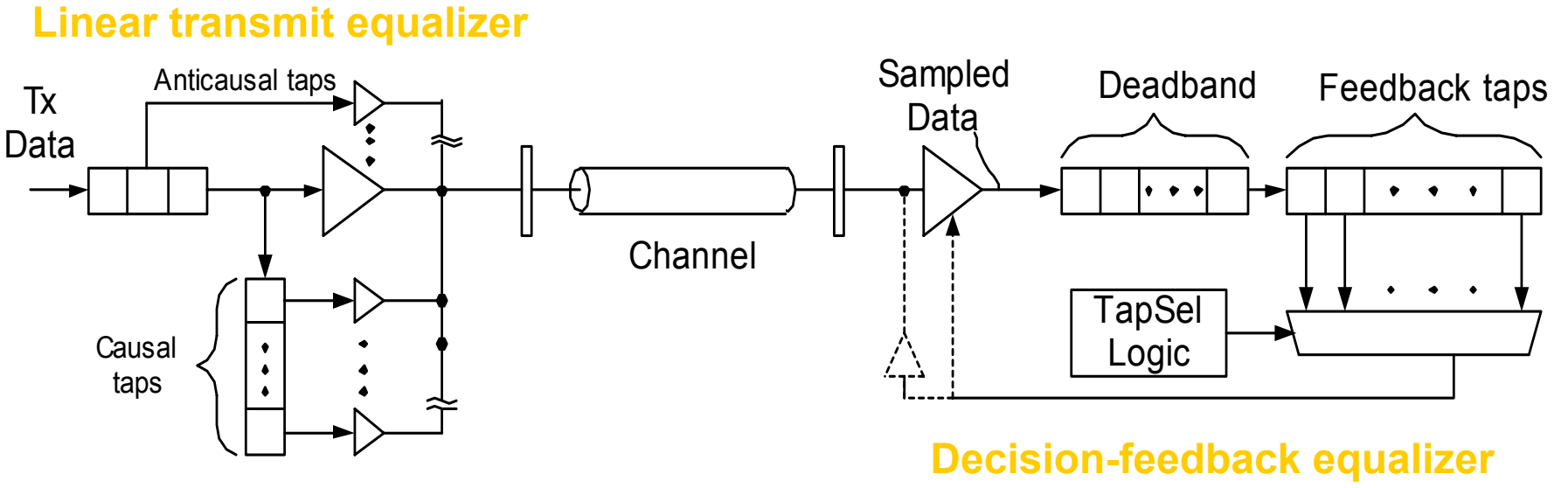


- Gives the probability distribution of phase
  - Which is the CDR jitter distribution

Noise Summary

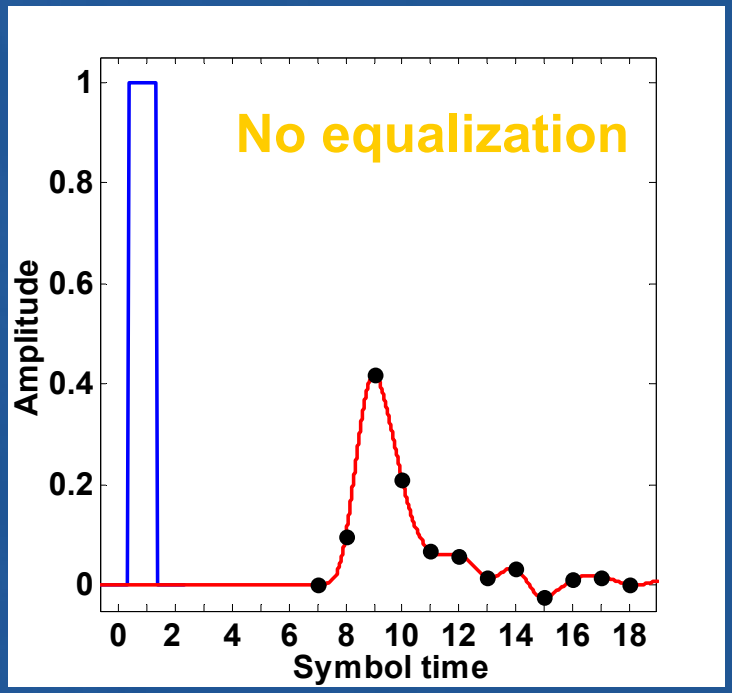
- Many important sources of noise
  - ISI, crosstalk, quantization, estimation, etc.
- Largest noise comes from ISI
  - By factor of 10x
- Timing is noisy too
  - High frequency transmitter jitter is bad
  - CDR jitter needs to be considered
    - Especially if the data input is noisy
- How much noise can we eliminate?

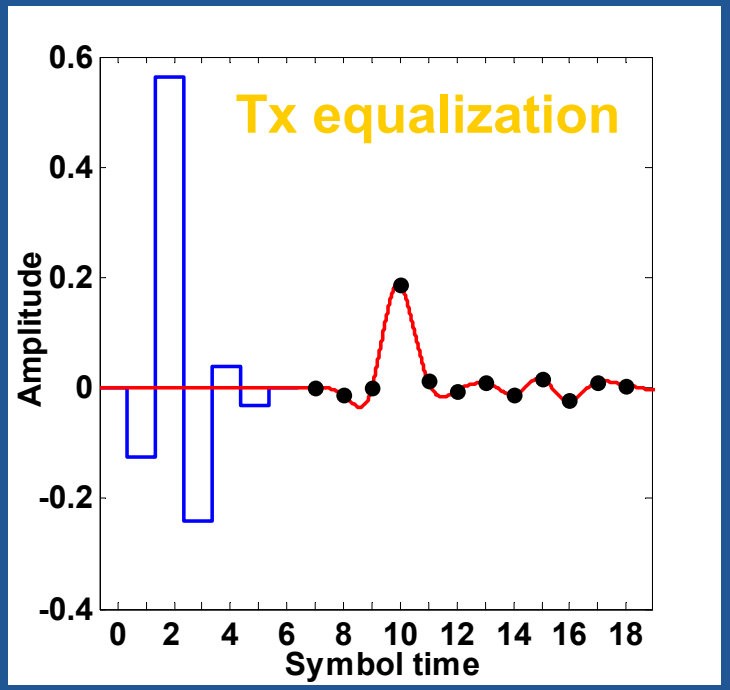
Removing ISI



- Transmit and Receive Equalization
  - Changes signal to correct for ISI
  - Often easier to work at transmitter
    - DACs easier than ADCs

Equalization Mechanisms





- Tx equalization
  - Pre-filter the pulse with the inverse of the channel
  - Filters the low freq. to match attenuation of high freq.
- Rx feedback equalization
  - Subtract the error from the signal

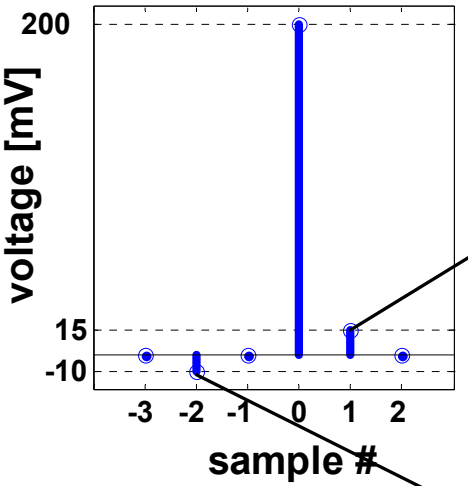
Residual Error

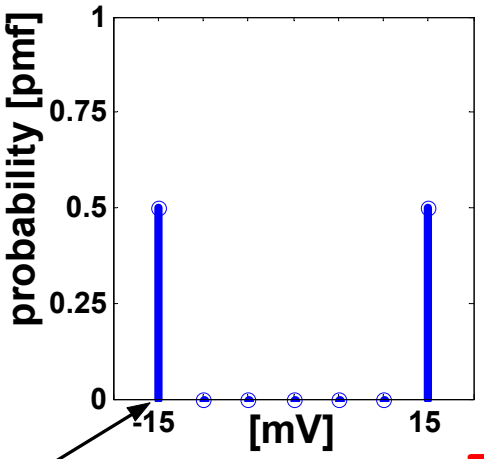
- Cannot correct all the ISI
  - Equalizers are finite length
  - EQ coefficients quantized
  - Channel estimate error
- The error affects both voltage and timing
- Need to find the distribution of this error

Generating ISI Distributions

Convolution method

Tx Equalized pulse response





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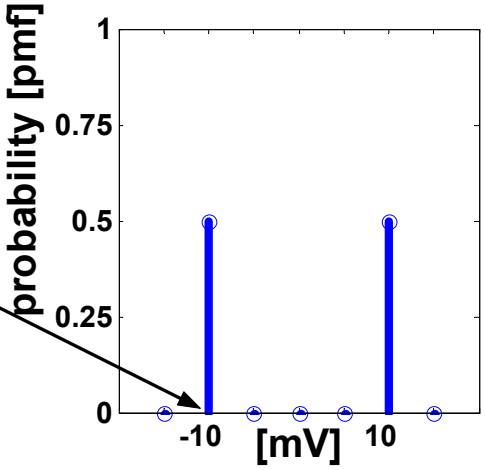

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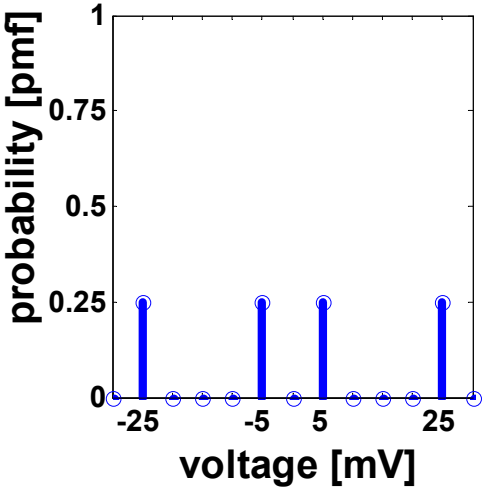
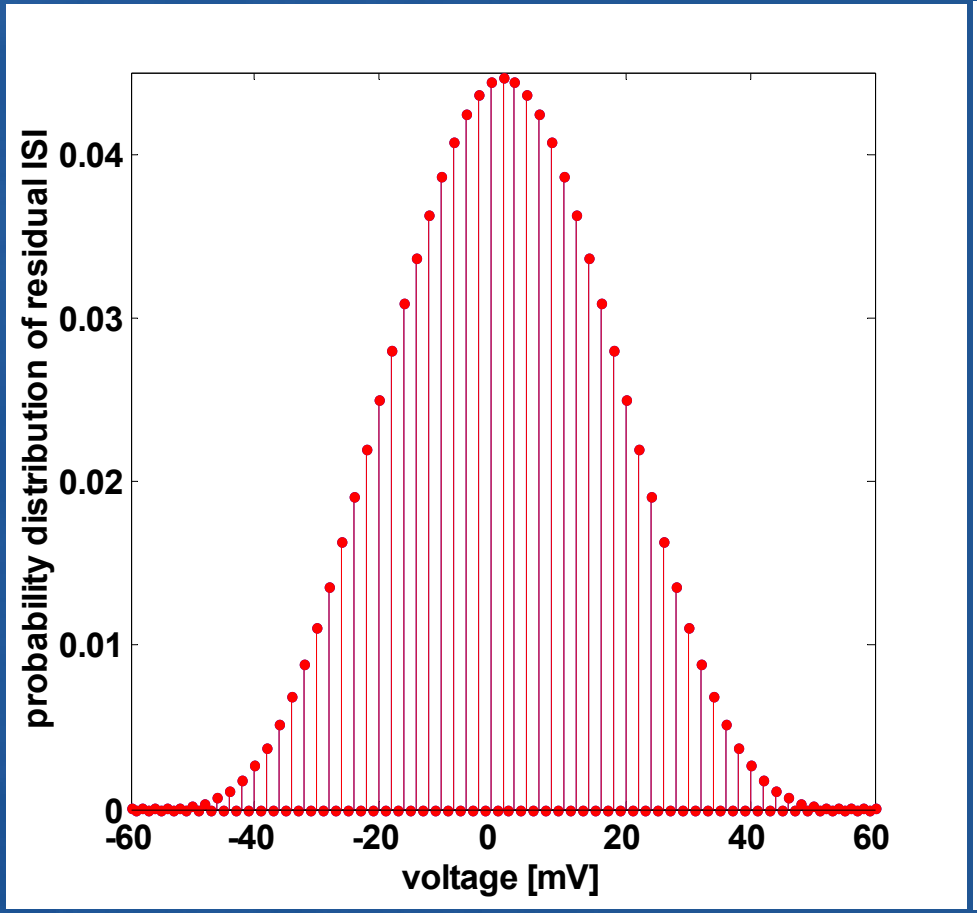
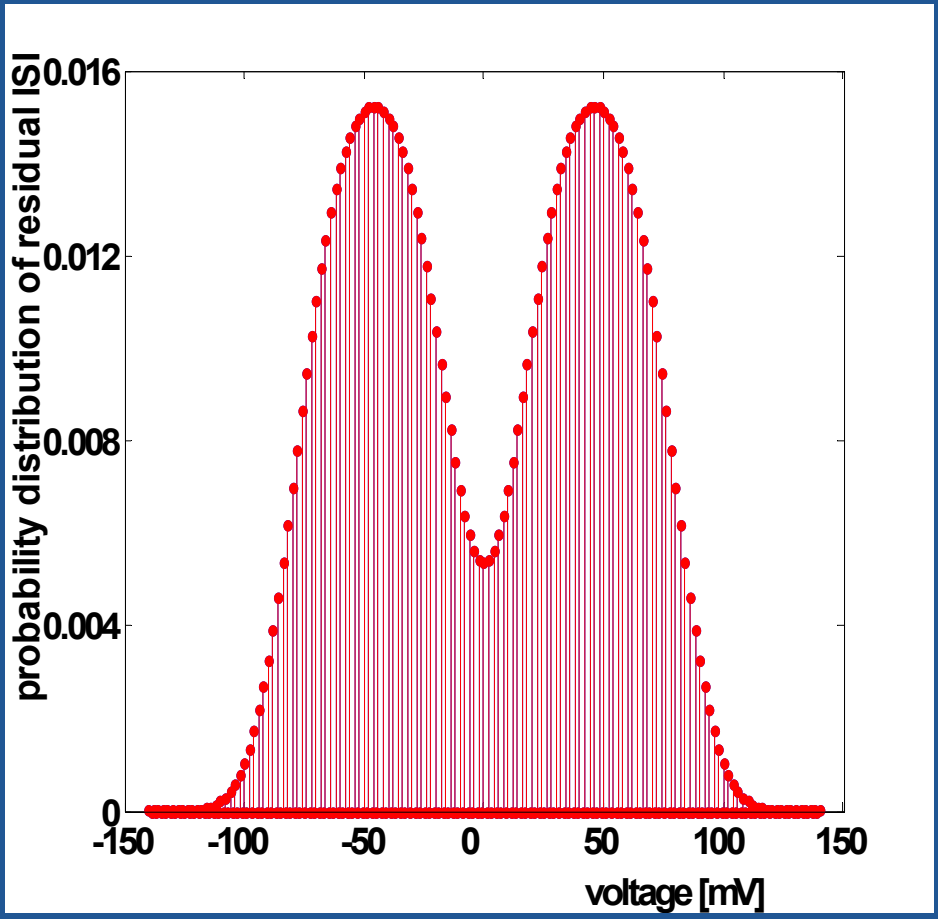
ISI distribution



Estimated Residual Error

5 Tap Transmitter Equalizer



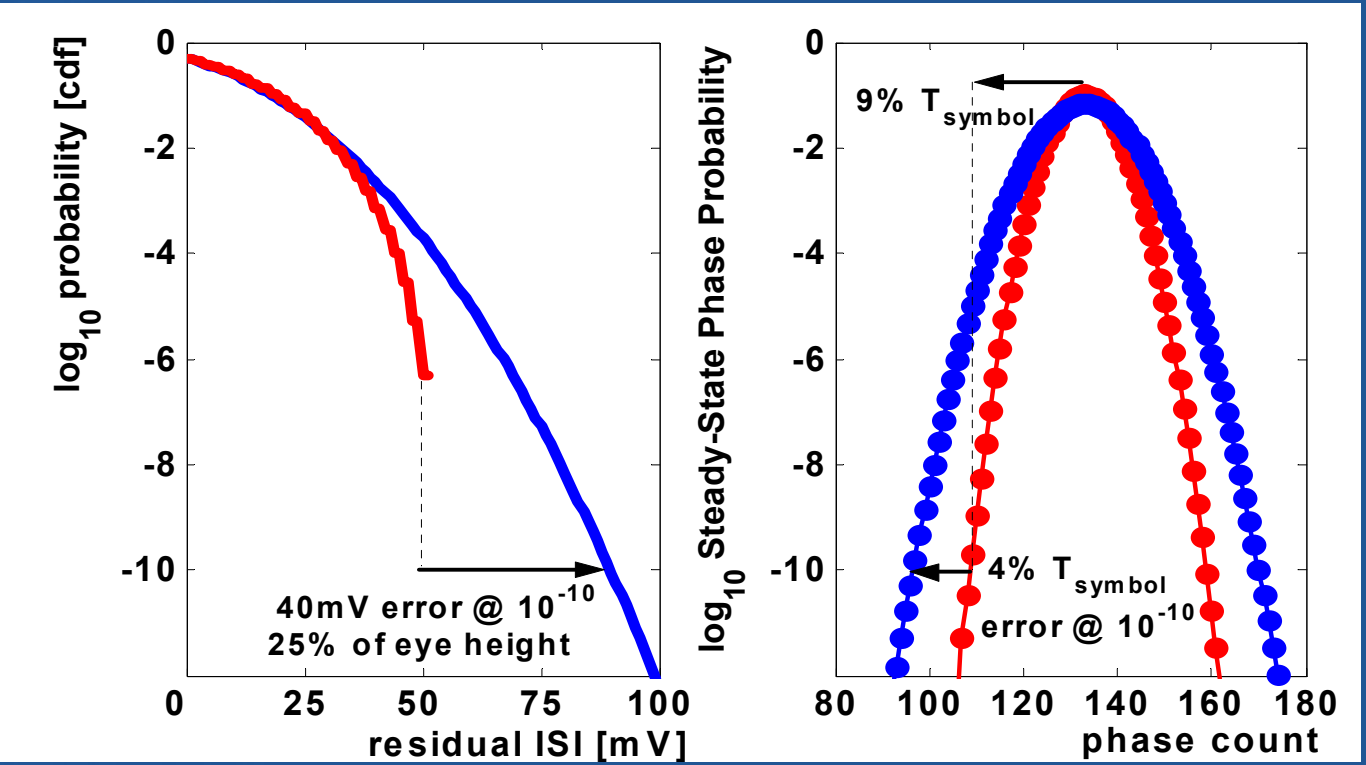


Data sample distribution

Edge sample distribution

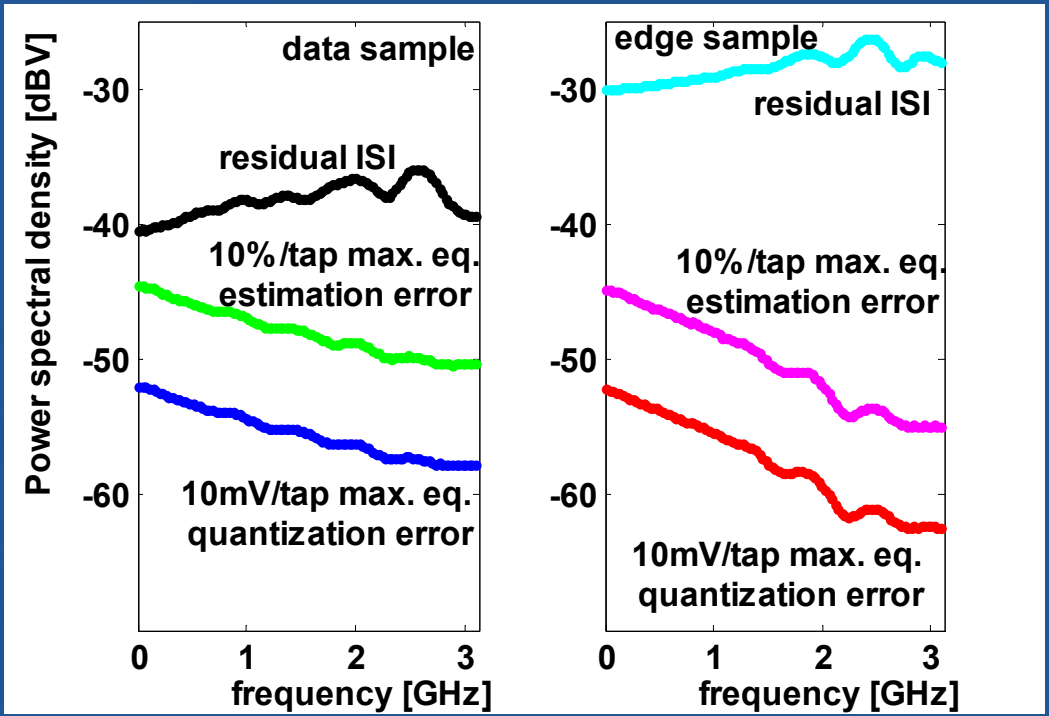
Comparison w/ Gaussian Model

Cumulative ISI distribution **Impact on CDR phase**



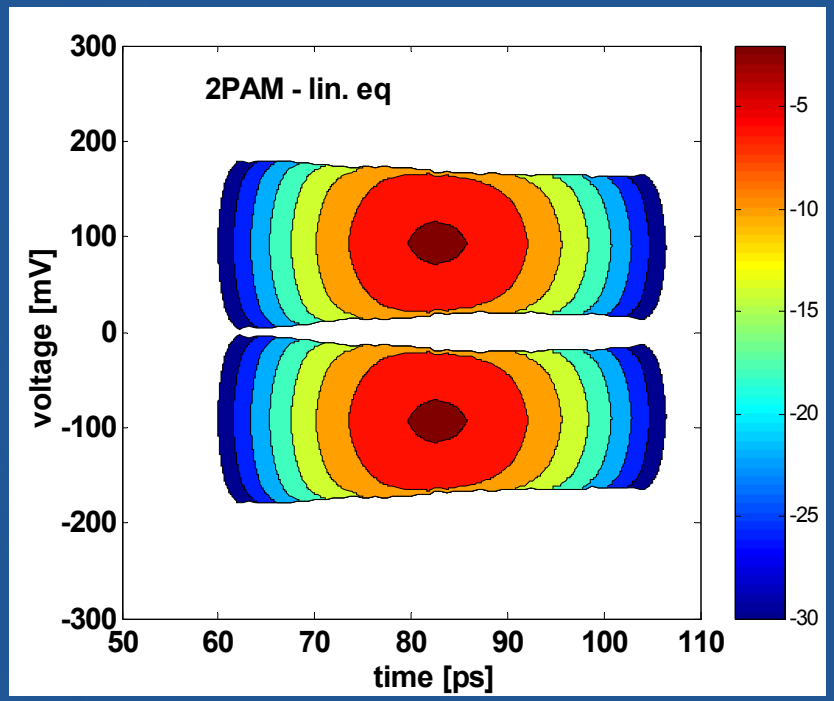
- Gaussian model only good down to 10^{-3} probability
- Way pessimistic for much lower probabilities

Equalizer Related Error Sources



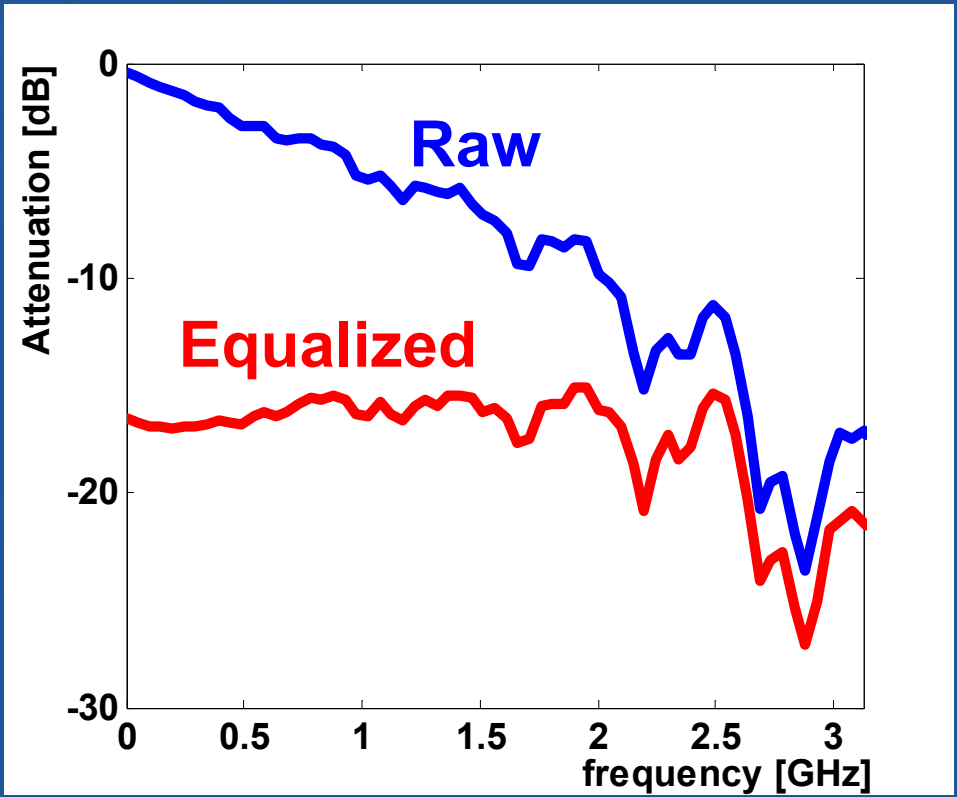
- Residual ISI is the biggest source of error
- Quantization error and equalizer estimation
  - Are significant for reasonable assumptions about accuracy

ISI and CDR Phase Distributions



- In ideal world, there would be only two dots
  - This plot shows how these dots spread out
- Vertical slice – ISI distribution per time offset
- Horizontal weight – CDR phase distribution

Tx Equalization

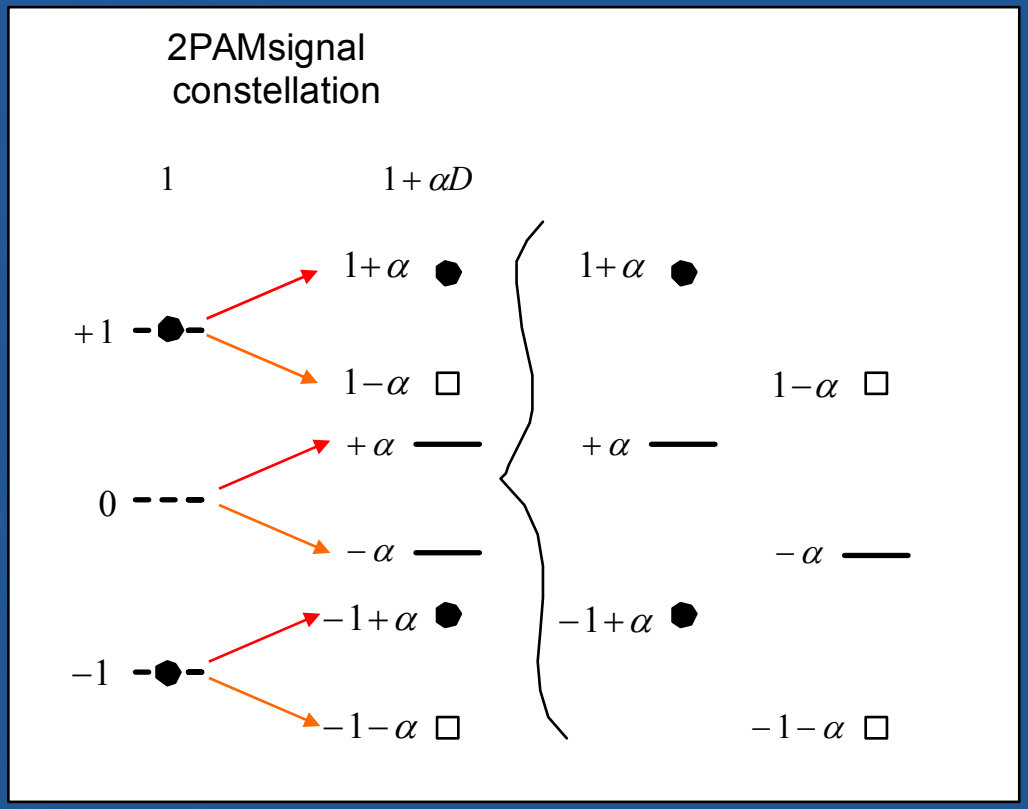


- Transmit equalization attenuates low frequencies
  - Output swing is constrained (peak power constraint)
  - Reduces ISI, but also decreases SNR (decreases signal)

Receive Equalization

- Feedback equalization (DFE)
  - Subtracts error from input
  - No attenuation
- Problem with DFE
  - Need to know values of interfering bits
  - ISI must be causal
    - And latency in the decision circuit is a problem
    - Receive latency + DAC settling < bit time
  - Can increase allowable time by loop unrolling
    - Receive next bit before the previous is resolved

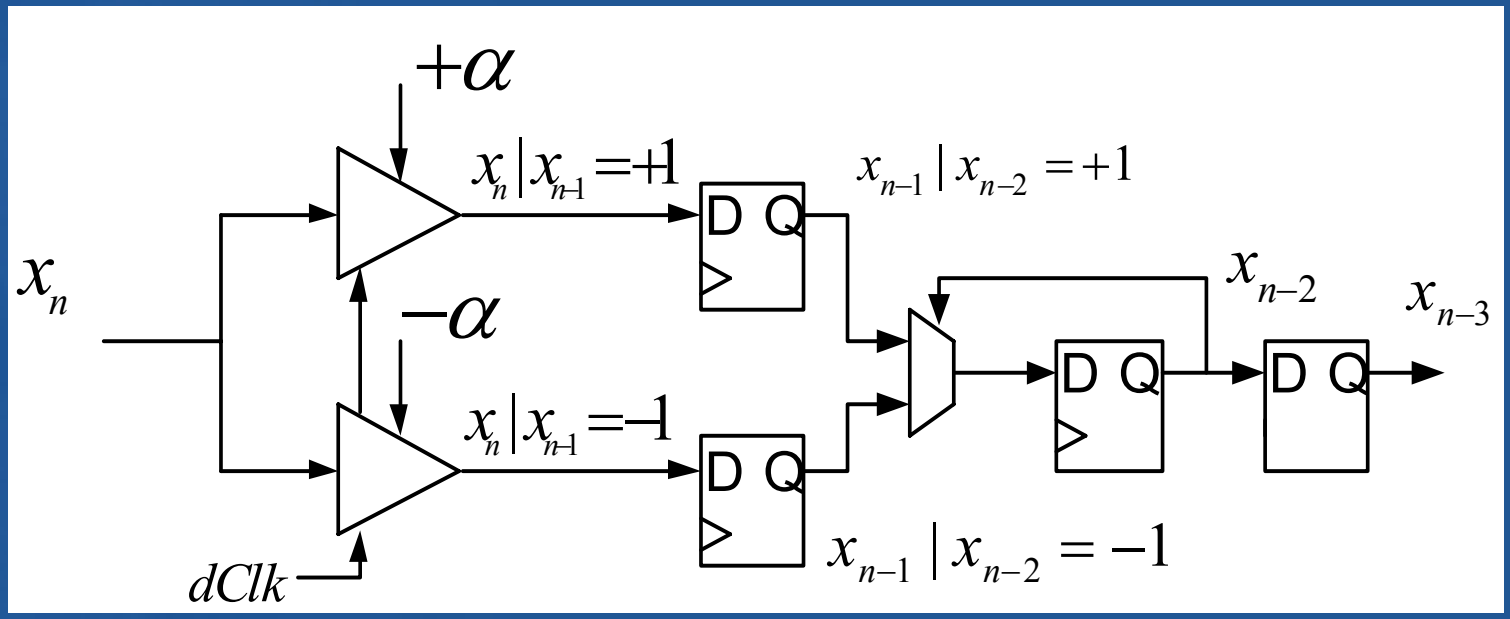
1 Bit Loop Unrolling



- Instead of subtracting the error
  - Move the slicer level to include the noise
  - Slice for each possible level, since previous value unknown

Loop Unrolling Implementation

Parhi ‘90 and Kasturia ’91



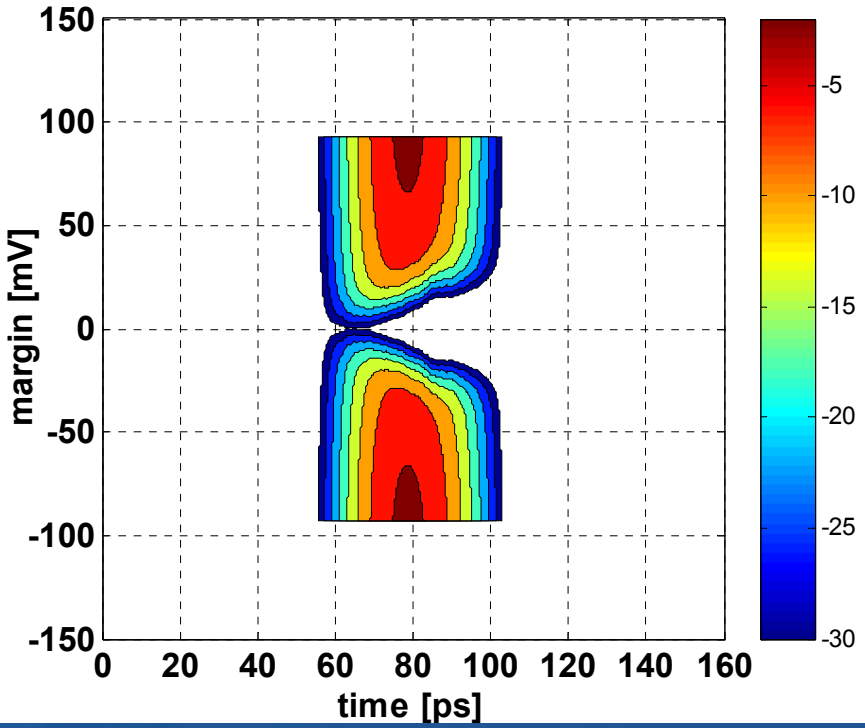
- Offset slicer levels by +/- α
  - Previous symbol selects correct value
- M^L receivers for L taps, M level signal
  - Each receiver with M-1 comparators

Putting It All Together

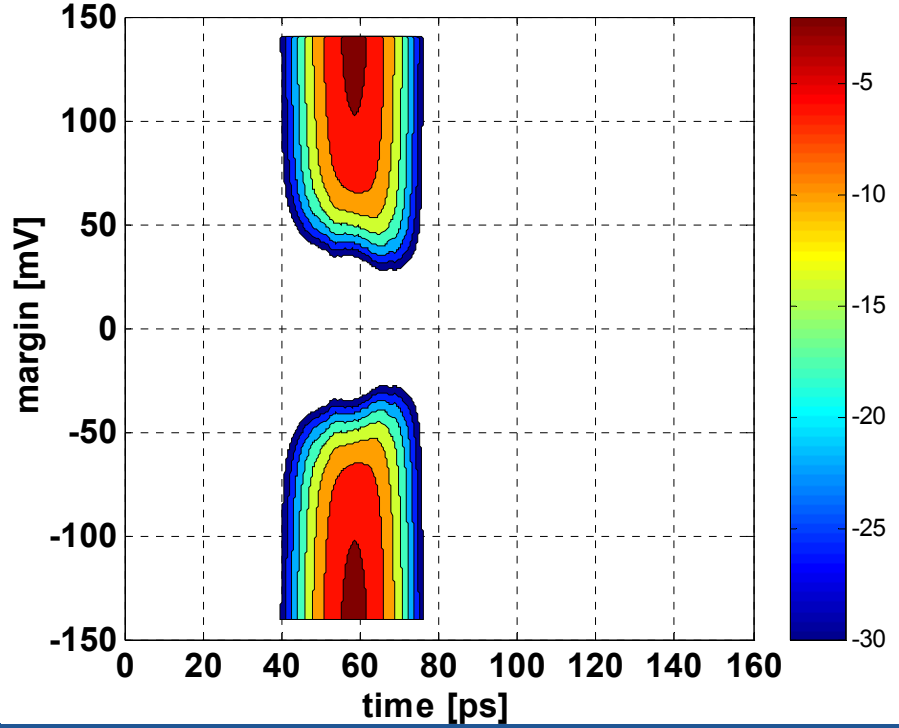
- To compare different designs
  - Compare the voltage margin at given BER
- Need to include all noise sources
  - Accurate ISI distribution
  - Transmit and receive jitter
  - CDR jitter
  - EQ quantization noise
  - Receiver offset

BER Contours

5 tap Tx Eq



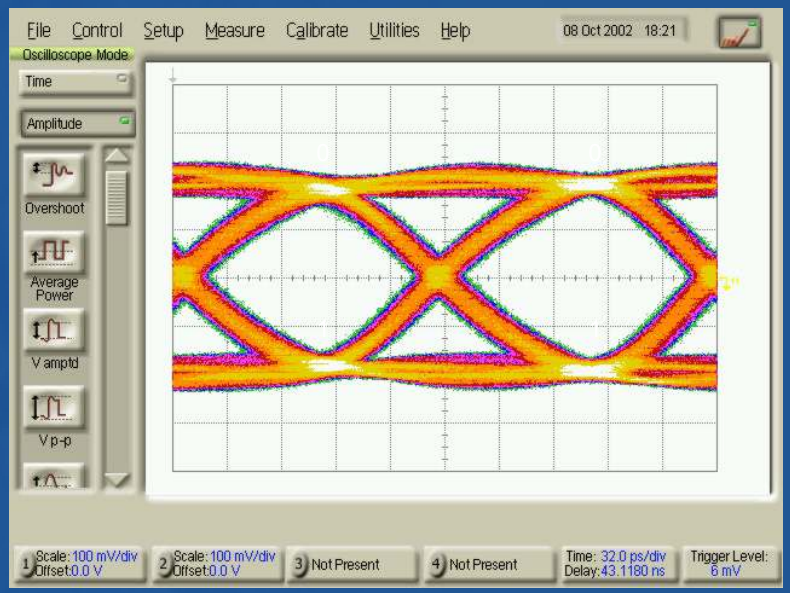
5 tap Tx Eq + 1 tap DFE

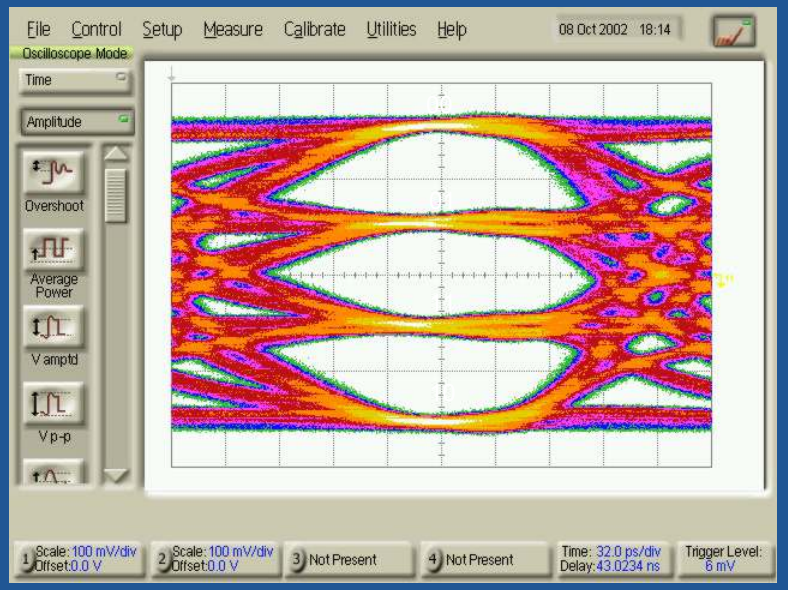


- Voltage margin
  - Min. distance between the receiver threshold and contours with same BER

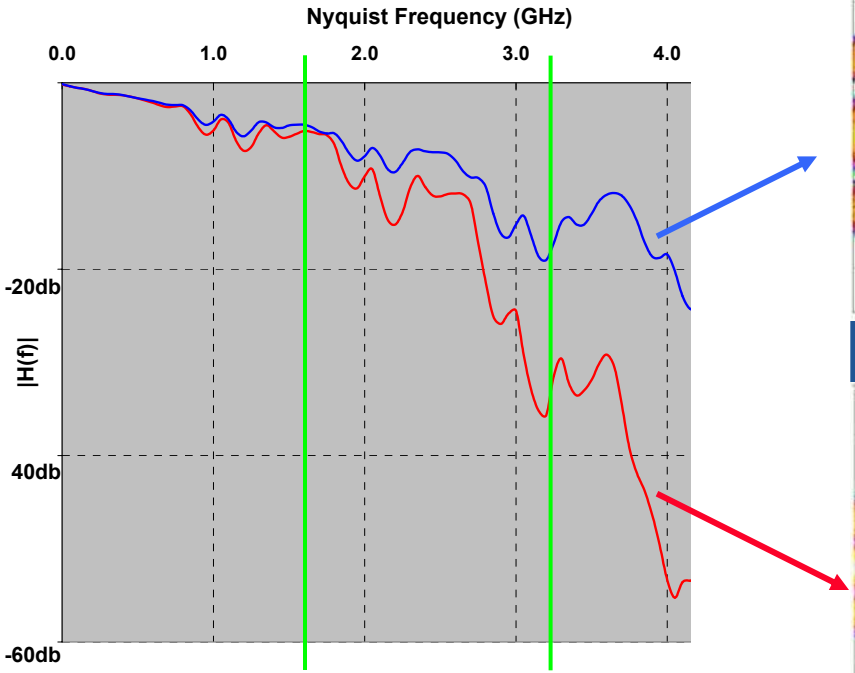
Pulse Amplitude Modulation

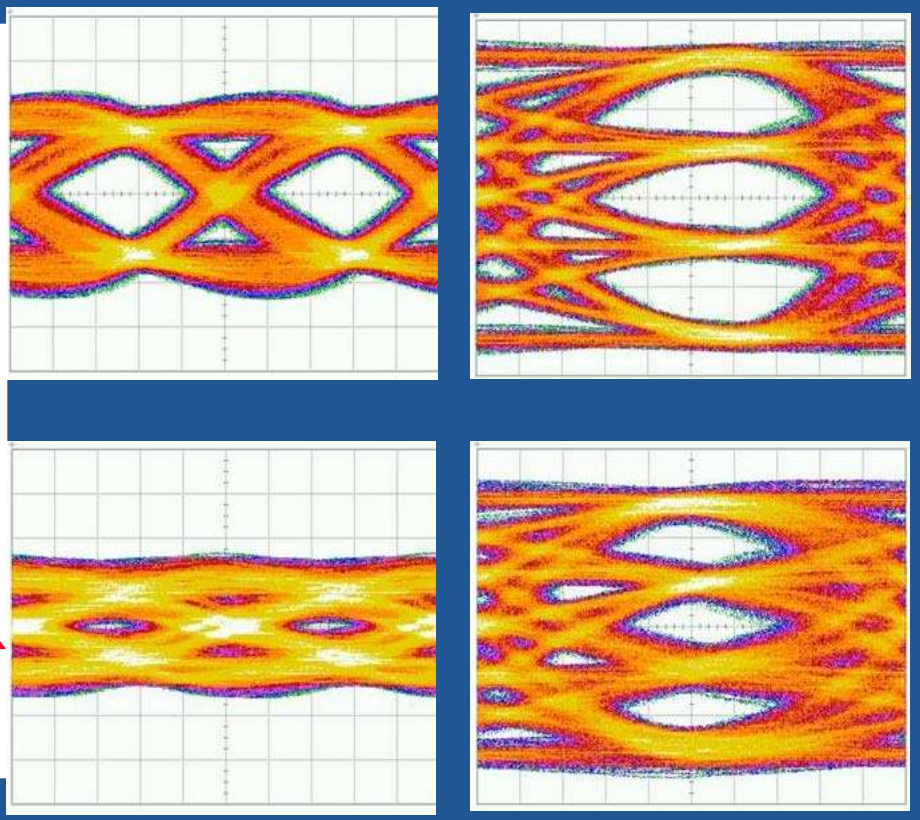
- Binary (NRZ)
  - 1 bit / symbol
  - Symbol rate = bit rate
- 4-PAM
  - 2 bits / symbol
  - Symbol rate = bit rate/2





When Does 4-PAM Make Sense?





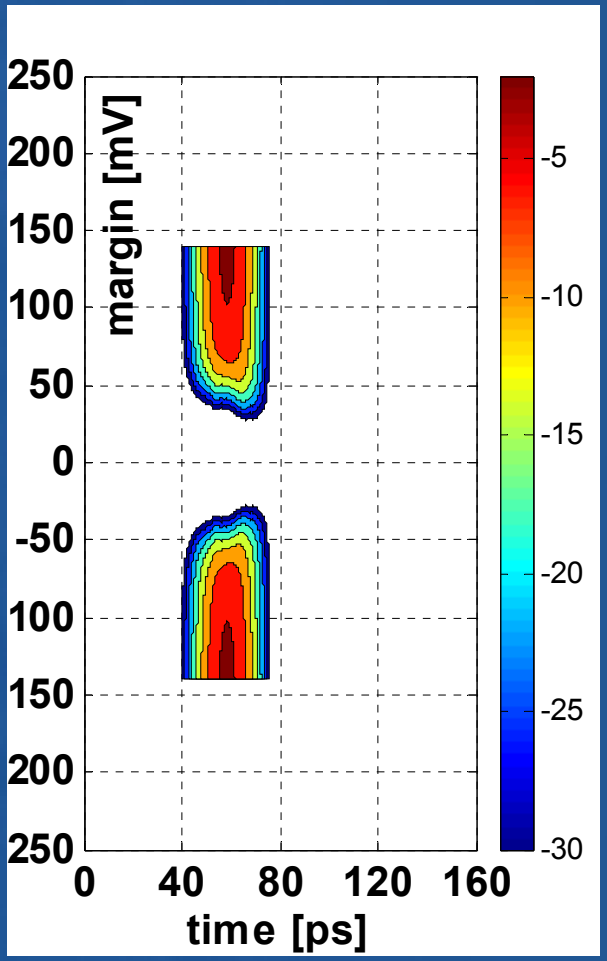
- First order : slope of S21

Zerbe et al ‘03

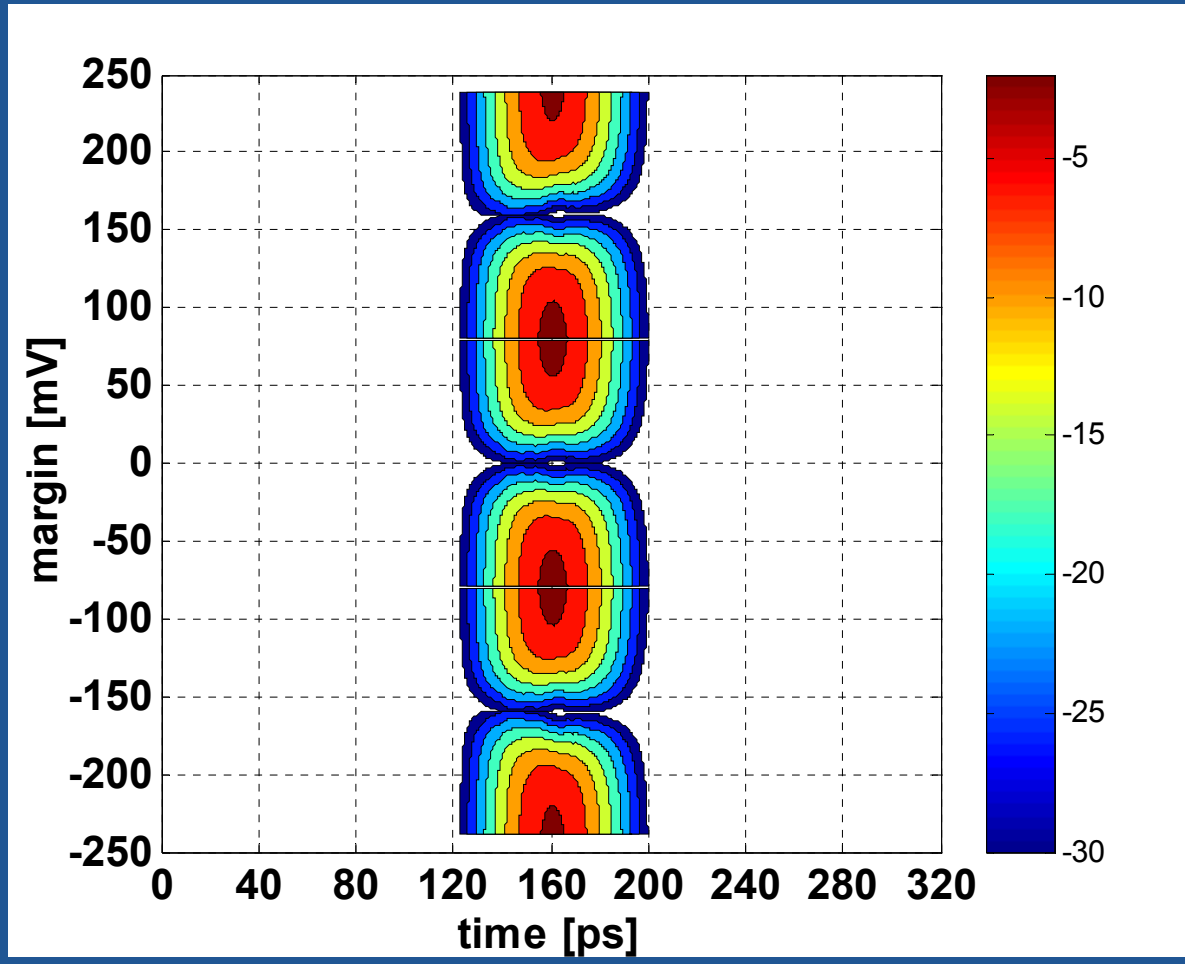
  - 3 eyes : 1 eye = 10db
  - loss > 10db/octave : 4-PAM should be considered

BER Contours

PAM2 DFE



PAM4 linear equalization



Voltage Margins [mV] at BER=10^{-12}

Eq/Mod type vs. BP length	3"	10"	20"
2PAM	32	17	19
2PAM w. DFE	79	49	44
4PAM	10	37	31

- Longer backplane channels – more ISI
- PAM2 with DFE effectively combats ISI
- PAM4 makes better use of available bandwidth
  - Less ISI

Conclusions

- Backplane links limited by the channel
- ISI is large
  - Can’t completely compensate
    - (At least not with reasonable area/power)
  - Residual ISI also increases CDR jitter
- Generally have low BER requirements
  - Accurate noise statistic important
  - Many of large noise source are bounded
- Power constrained transmitter
  - 4 PAM and simple DFE are attractive solutions