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Modeling and Analysis of Simultaneous Switching Noise Coupling for a CMOS Negative-Feedback Operational Amplifier in System-in-Package

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***Abstract*—A new hybrid modeling method is proposed for the chip–package comodeling and coanalysis. This method is designed to investigate the simultaneous switching noise (SSN) coupling paths and effects on the dc output voltage offset of the operational amplifier (OpAmp). It combines an analytical model of the circuit with a power distributed network (PDN) and interconnection models at the chip and package substrate. In order to validate the proposed model, CMOS OpAmp was fabricated using TSMC 0.25 μm. Then the dc output offset voltage of the OpAmp was measured by sweeping the SSN frequency from 10 MHz up to 3 GHz. It was successfully demonstrated that the experimental results are consistent with the predictions generated using the proposed model. We also confirmed that the dc offset voltage is strongly dependent on the SSN frequency and the PDN impedance profile of the chip–package hierarchical PDN. It shows the necessity for the chip–package comodeling and simulation of the system-in-package designs.**

***Index Terms*—Circuit modeling, electromagnetic noise, impedance matrix, operational amplifiers, power distribution lines, power distribution noise.**

I. Introduction

RECENTLY, system-in-package (SiP) has emerged as the most promising semiconductor system solution for compact mixed-mode systems, because the SiP can integrate digital processing, memory, sensors, radio-frequency (RF) chips, and passive devices into a tiny package [1]–[3]. While the package size has been scaled down, operating clock frequencies and input/output switching speeds have been increasing [4]. This technical trend causes significant noise generation, which has become the most critical consideration when designing chips and the package interconnections. The major noise coupling source is simultaneous switching noise (SSN) [5]–[7]. The SSN can be easily coupled to noise sensitive circuits, resulting in severe degradation of performance and reliability [8].

The operational amplifier (OpAmp) is the most commonly used circuit among analog blocks such as analog–digital converters (ADCs), digital–analog converters (DACs), and active filters, which are essential building blocks of analog electronics. One of the most crucial properties of the OpAmp is the dc output voltage offset. The most probable mechanism of the dc output voltage offset is RF interference (RFI) [9], [10]. The RFI that causes the dc output voltage offset of the OpAmp is most likely produced by the SSN coupling to the power distributed networks (PDNs) and the input path of the OpAmp. Consequently, it is essential to investigate the SSN coupling paths.

Previous reports analyzed the RFI susceptibility without considering SSN generation processes or noise coupling paths in the chip and package. These previous studies used a Volterra series model or analytical models to estimate the dc output offset voltage by assuming that the RFIs were added in the form of sinusoidal waves with a uniform amplitude and phase [11]–[14]; this is not practical, especially when the analog chip with the OpAmp is mounted on a multilayer package substrate. Usually, the package-level interconnections produce electromagnetic resonances due to the planar cavity structure of the PDN and parasitic elements of the interconnections [15].

In this paper, we propose a new hybrid modeling method based on a chip–package co-modeling approach to evaluate the SSN coupling effects. It combines an analytical circuit model of the dc output offset voltage in the OpAmp with models of the on-chip and off-chip PDN and the interconnections. Through the hybrid modeling process, we can analyze the SSN coupling paths and estimate the dc output offset voltage. The proposed hybrid model, which combines the two models, enables efficient and integrated coanalysis of signal integrity and power integrity of the chips and the package-level interconnections in the SiP. It can also provide accurate estimations of the RFI susceptibility and requires a much shorter simulation time than conventional 3-D full-wave simulations.

Using the proposed modeling method, we have analyzed two dominant SSN coupling paths. The first SSN coupling path is the direct SSN coupling to the power supply of the OpAmp circuit through the hierarchical chip and package PDN. The second SSN coupling path is the SSN coupling to the input of the OpAmp through a via transition in the package substrate. The via transition makes a signal trace exchange its reference planes from the ground plane to the power plane [16]–[18]. In this study, these two coupling paths were modeled based on the transmission-line matrix (TLM) method and a distributed circuit modeling approach [19]–[21].

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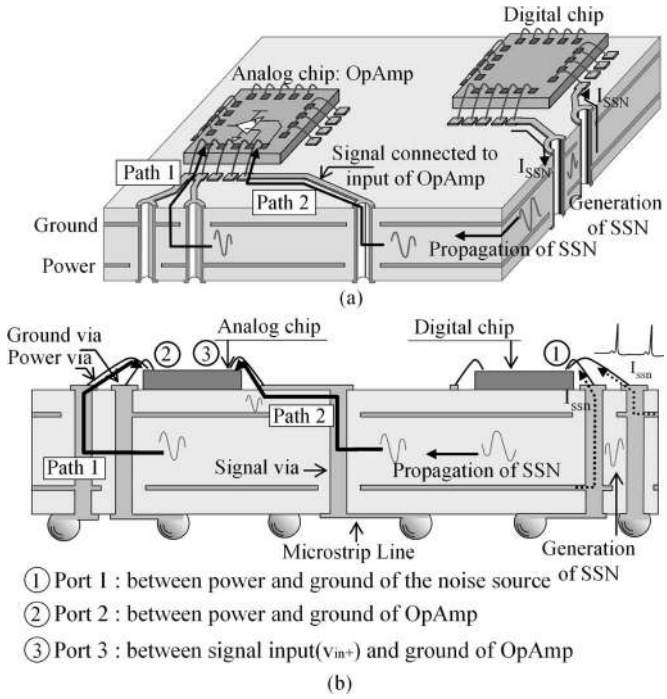


Fig. 1. (a) Schematic drawing to illustrate two SSN coupling paths from a digital chip to an analog chip with an OpAmp circuit in an SiP. Path 1 is an SSN coupling path through PDN to the power supply of the OpAmp. Path 2 is an SSN coupling path through a via transition into the input of the OpAmp. (b) Cross-sectional view of an SiP to describe the two SSN coupling paths from a digital chip to an analog chip though the package substrate of the SiP. Port 1 is the location between power and ground of the digital noise source. Port 2 is located between power and ground on the on-chip power/ground ring of the OpAmp. Port 3 is assigned between the signal input ($v_{\rm in}+$) and ground of the OpAmp.

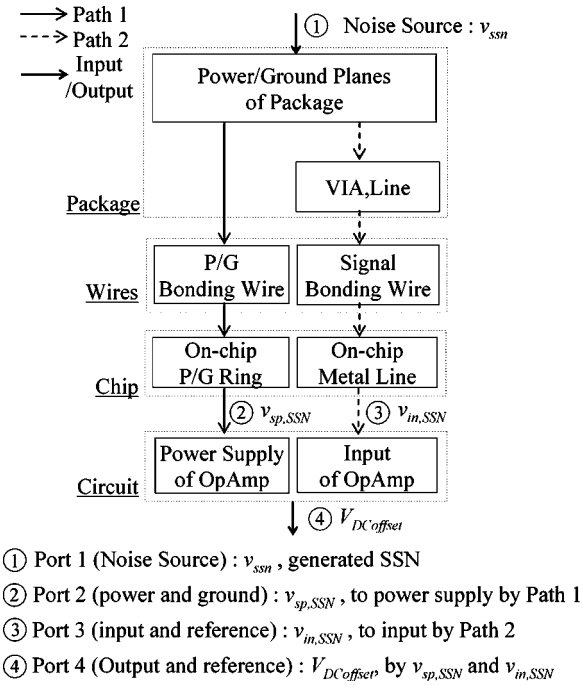


Fig. 2. Model blocks of the two SSN coupling paths. Port 1 is defined as an SSN source generated by the switching current of digital circuits in the digital chip on the SiP, while port 2 is assigned as the on-chip power supply of the OpAmp in the analog chip on the SiP. Port 3 is designated as the input of the OpAmp inside the analog chip and the reference. Port 4 is located between the output and reference (ground).

In order to validate the proposed hybrid model, we have designed a CMOS negative-feedback OpAmp chip and a package substrate. Then, we successfully demonstrated that the experimental results coincide with the expectations by the proposed model. It is also clear that both the estimated and measured dc output offset voltages exhibit a distinct frequency dependency, which shows the high-frequency electromagnetic interaction of the OpAmp circuit with the package-level PDN and interconnections. These results demonstrate the necessity of the chip–package comodeling and analysis of the SiP.

II. Modeling of Chip–Package PDN to Estimate SSN Coupling to the OpAmp

Fig. 1 illustrates the conceptual diagram of two dominant SSN coupling paths to an OpAmp circuit mounted on an SiP substrate. Path 1 is the propagation path constructed by the direct coupling to the power supply of the OpAmp ($v_{\rm sp,SSN}$) through a hierarchical on-chip and off-chip PDN. Path 2 is the SSN coupling path to the input of the OpAmp ($v_{\rm in,SSN}$) by a via transition of the input signal trace for the OpAmp ($v_{\rm in,SSN}$) circuit when the input signal trace exchanges its reference planes in the multilayer package substrate of the SiP. In order to understand and estimate the SSN coupling to the OpAmp for each path, we have modeled each component, as described in Fig. 2. For path 1, models of power/ground planes of the package substrate, bonding wires for power/ground, and power/ground rings of the chip, while path 2 needs models of the hierarchical PDN, microstrip line, through-hole via, bonding wires, and on-chip metal line. The solid arrow line and the dashed arrow line represent the connection between two modeling components.

A. Modeling of SSN Coupling Path 1: SSN Coupling to Power Supply of OpAmp

The model components of path 1 are on-package PDN, on-chip PDN, and bonding wires. First, the package substrate that consists of four layers has a size of 4 cm $\times$ 9 cm. In order to model the multilayer cavity of the package substrate, we have used a balanced TLM method [15]. $R_{\rm p}, L_{\rm p}, G_{\rm p}$, and $C_{\rm p}$ model parameters are calculated using the dimensions of the unit cell and the material constants, as referred in [19]–[21].

The second part of the models is the on-chip PDN model shown. On-chip PDN consists of a power/ground ring pair, on-chip decoupling capacitors, and MOSFETs. The top metal layer (M5) of the chip is used for the ground ring, and the metal layer 4 (M4) is for the power ring.

Also, we designed and modeled an NMOS type 144 pF decoupling capacitor for the OpAmp. The model of the unit NMOScap (1 pF) is composed of an oxide capacitor and a series resistor (equivalent series resistance, ESR), while the ESR of the unit NMOScap is 115 Ω. Capacitance and resistance model parameters of the unit NMOScap can be derived, as referred in [22].

TABLE I
MODEL PARAMETERS TO DESCRIBE THE SSN COUPLING PATH 1 USED IN MODEL BLOCKS 1, 2, AND 3 IN FIG. 2

Objective	Parameter	Total Value
Power/ground plane pair	R	0.05 ohm
	L	0.92 nH
	G	0.33 mho
	C	355 fF
Bonding wire	L_w	1 nH
On-chip power/ground ring	R_{M4}	76 mohm
	R_{M5}	41 mohm
	C_{f45}	0.27 fF
	L_{M45}	5.5 pH
On-chip decap	R_{ESR}	115 ohm
	C_{MOS}	996 fF

In addition, equivalent circuit models of the CMOS transistor used in the OpAmp circuit are needed because the on-chip power supply is connected to the nodes of the CMOS transistor through the on-chip PDN of model block 2. The equivalent circuit model is the modified conventional equivalent circuit model shown in [23]. It is also used in Sections III and IV.

The last part of the model is a wire-bond model; on-package PDN and on-chip PDN are connected using the bond wires. A bond wire can be modeled as an inductor whose value is derived using its diameter, height, and length [24]. A summary of the total model parameters and values in the SSN coupling path 1 are listed in Table I.

B. Modeling for SSN Coupling Path 2: SSN Coupling to Input of the OpAmp Through a Via Transition at Package Substrate

To describe the SSN coupling mechanism through SSN coupling path 2, as shown in Figs. 1 and 2, we have designed models of the on-chip and off-chip PDN, the signal line on the package substrate, a signal via that exchanges its reference plane in the package substrate, and CMOS transistors of the OpAmp. Models of the CMOS circuit, and the on-chip and off-chip PDN have already been introduced in the previous paragraph. The equivalent circuit model of the microstrip line is represented using the balanced TLM method, as referred in [15].

Since the chips are mounted on the top surface of the package substrate and the solder balls are mounted on the bottom surface of the package substrate, a through-hole via is an inevitable interconnection structure. Unfortunately, this results in a reference plane exchange from the power plane of Layer 3 to the ground plane of layer 2. This can cause a serious SSN coupling from the power/ground plane cavity to the signal via [15]–[18]. Model parameters of the microstrip line and a through-hole via for SSN coupling path 2 are listed in Table II.

III. ESTIMATION OF SSN COUPLING THOUGH TWO PATHS

The SSN coupling effect can be fully anticipated by the product of the SSN source characteristics and the transfer impedance of the SSN coupling paths of path 1 and path 2. Port 1 is defined as an excitation point of the SSN source in the SiP and port 2 is located between the power and the ground of the on-chip OpAmp circuit. Port 3 is assigned as the input of the OpAmp. The dashed line shown in Fig. 5 presents the calculated transfer impedance Z_{21}. From the transfer impedance Z_{21}, we can predict the SSN coupling effect onto the on-chip power supply of the OpAmp at port 2.

TABLE II
MODEL PARAMETERS OF THE EQUIVALENT CIRCUIT MODELS FOR THE MODELING OF THE SSN COUPLING PATH 2

	Parameter	Total Value
Micro strip line	R_s	0.01 ohm
	L_s	1.07 nH
	C_s	473 fF
Signal via	L_{via}	600 pH
	L_{pad}	500 pH
	C_{via}	123 fF

Based on these resonance frequencies, the Z_{21} curve can be divided into five different regions (I, II, III, IV, V). Initially at region I, the slope of the Z_{21} curve is mainly affected by the electrical series inductance (ESL) of the bulk capacitors mounted on the package substrate near port 1. As the frequency is over 160 MHz, the major model parameter determining the Z_{21} curve is $C_{\rm total}$. $C_{\rm total}$ includes the capacitances of on-chip and package. Since the Z_{21} curve increases proportionally to the bonding wire inductance and the frequency, the Z_{21} curve is dominated by the bonding wire inductance in region III. In region IV, the impedance of the Z_{21} curve is reduced with the help of the on-chip decoupling capacitor with negative slope. This means that the on-chip decoupling capacitor can suppress the Z_{21} impedance in this frequency range of region IV. The on-chip decoupling capacitors also suppress the magnitude of the cavity resonance peaks of the region V.

Similarly, we can estimate the SSN coupling effect through the SSN coupling path 2 to the input of the OpAmp circuit (port 3). Z_{31} is presented in the solid graph of Fig. 5. The Z_{31} curve exhibits similar features to the Z_{21} curve viewed in the resonance frequencies. The Z_{31} curve is heavily affected by the PDN impedance profile at the location of the through-hole via transition on the multilayer package substrate. The SSN is coupled to the input signal line of the OpAmp (at port 3) from the package-level PDN since the reference planes are exchanged and the return current path is disconnected at the through-hole via transition. The level of Z_{31} is highly affected by PDN impedance at the position of the reference changing vias. Especially in region V over gigahertz frequencies, the level of the Z_{31} is higher than that of the Z_{21} curve, because high impedance of bonding wires blocks the effect of the on-chip decoupling capacitors to suppress PDN impedance at high frequency. Therefore, path 2 is not influenced by the on-chip decoupling capacitors in the region V, while the path 1 is influenced by the on-chip decoupling capacitor in the on-chip PDN of the OpAmp to suppress the noise coupling. While the levels of Z_{21} and Z_{31} are different, they have almost same resonance frequencies in the region V. If inductance of bonding wires is small and on-chip decoupling capacitors has large capacitance, the cavity

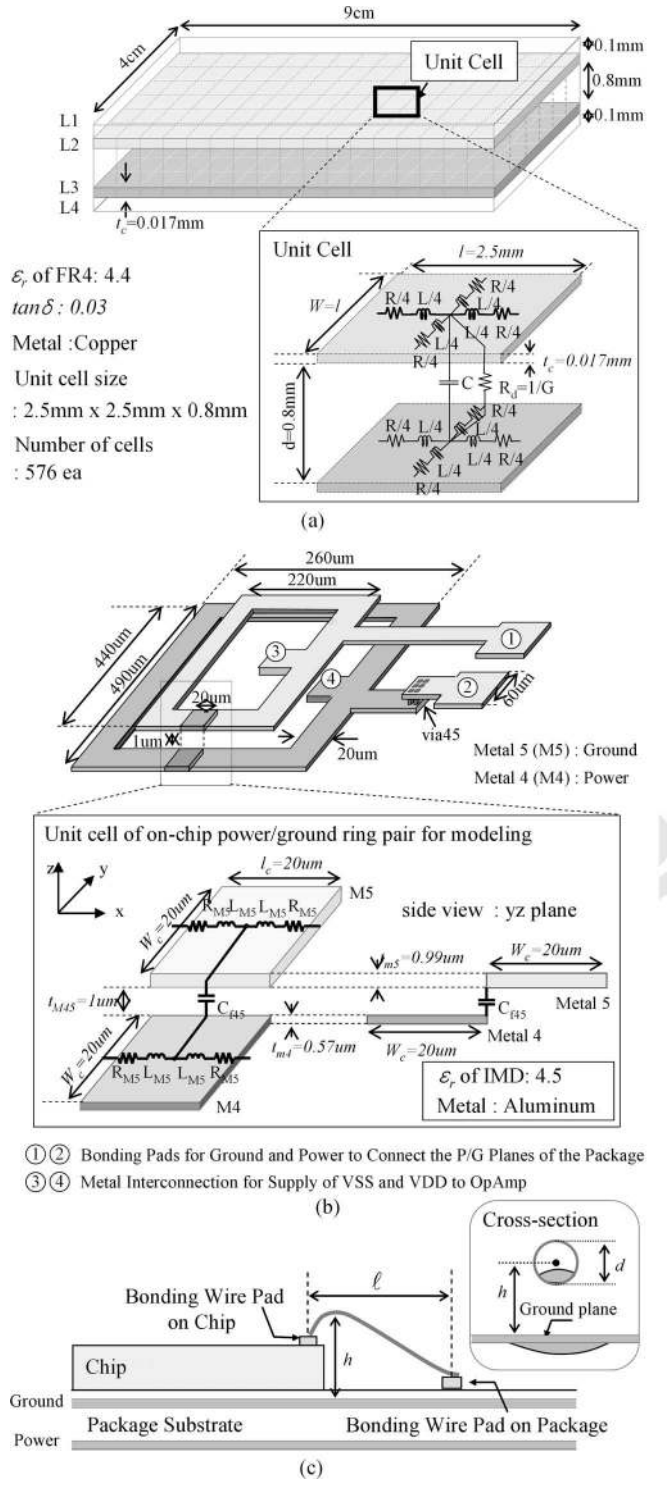


Fig. 3. PDN structure of each component and model parameters and dimension for path 1. (a) Package substrate for the SiP. The size of unit cell for the balanced TLM modeling of the power/ground plane pair is 2.5 mm × 2.5 mm, while the maximum target frequency of the simulation is kept to 3 GHz. (b) On-chip power and ground ring for the OpAmp. A unit cell consists of two metal segments of the power/ground ring pair with a unit cell size of 20 μm × 40 μm. (c) Bonding wires. The bonding wires are modeled as an inductance whose value related to its diameter, length, pitch, and height.

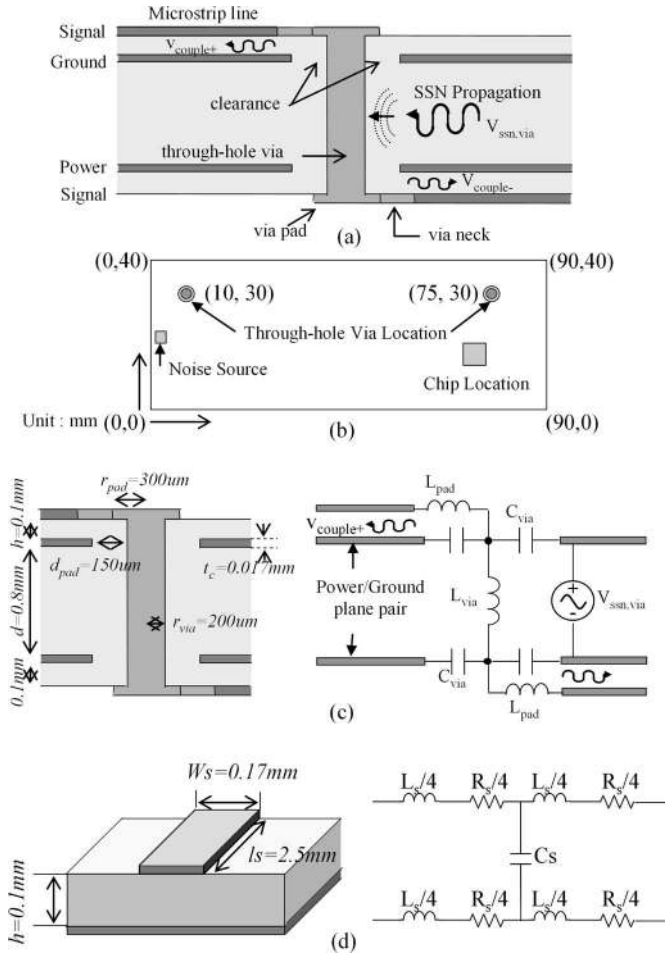


Fig. 4. (a) Cross-sectional view and the dimensions of the through-hole signal via and power/ground planes. (b) Top view of the package substrate. Through-hole vias' location on the package substrate (c) Equivalent circuit models of the through-hole signal via to present the SSN coupling to the via. (d) Equivalent circuit model of microstrip line. The unit cell size is 2.5 mm × 0.17 mm.

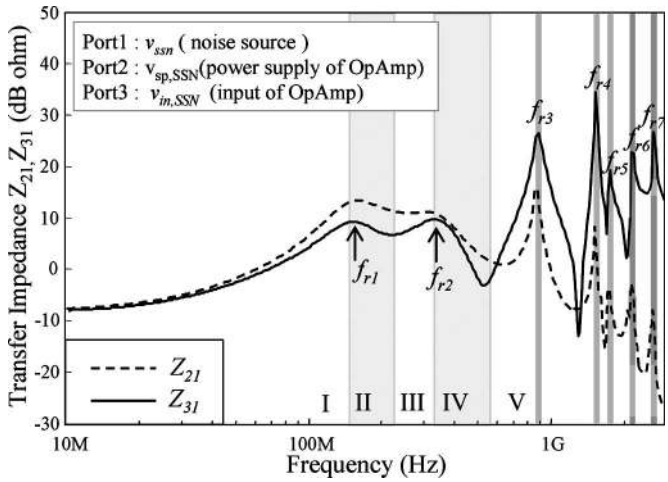


Fig. 5. Calculated transfer impedance, Z_{21} and Z_{31}.

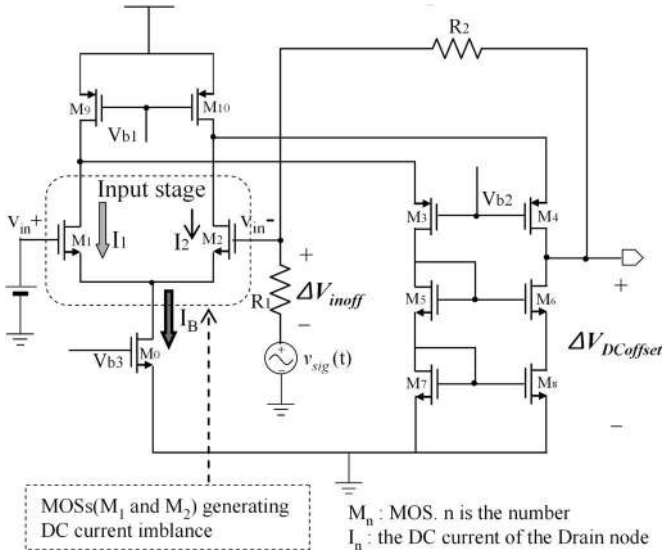


Fig. 6. Schematic of the OpAmp used in this study with the folded cascade structure. $V_{\rm sig}$ is the input signal to be amplified. $v_{\rm in}-$ is the inverting input and $v_{\rm in}+$ is the noninverting input. When the dc current imbalance occurs between M_1 and M_2, the dc output voltage offset ($\Delta V_{\rm dcoffset}$) is induced. $\Delta V_{\rm inoff}$ is the dc input offset voltage and $\Delta V_{\rm dcoffset}$ is the dc output offset voltage.

resonance frequencies ($f_{\rm r3} - f_{\rm r7}$) of Z_{31} differ from $f_{\rm r3} - f_{\rm r7}$ of Z_{31}.

IV. Analytical Model of the DC Output Offset Voltage in the OpAmp Based on Circuit-Level Analysis

A. DC Current Balance of I_1 and I_2 by Feedback ($I_1 = I_2$)

Fig. 6 shows a detailed schematic of the OpAmp. DC offset voltages of $\Delta V_{\rm inoff}$ and $\Delta V_{\rm dcoffset}$ are inversely controlling the current of I_2 through M_2, so that $\Delta V_{\rm inoff}$ can compensate the difference of the dc drain current I_1 and I_2. Therefore, the feedback configuration of the circuit can negate the dc current imbalance of I_1 and I_2, in order to equalize currents I_1 and I_2, resulting in a balanced current between I_1 and I_2 [9]. It is obvious that current I_9 equals current I_{10} because transistors M_9 and M_{10} have the same bias voltage. I_9 is the sum of I_1 and I_3, and I_{10} is the sum of I_2 and I_4. As a result, if we consider a case when I_1 is larger than I_2, I_3 should become smaller than I_4.

Thus, in the case when I_1 is larger than I_2, I_4 becomes larger than I_6. Then, the feedback dc current, $\Delta I_f = I_4 - I_6$, is conducted through the feedback resister R_2 and R_1, resulting in positive $\Delta V_{\rm inoff}$ and $\Delta V_{\rm dcoffset}$ voltages. Then, it increases the current I_2, and balances the currents I_1 and I_2. As a consequence, it can be said that the feedback configuration in the OpAmp generates the condition where $I_1 = I_2$ [9].

Imbalance between I_1 and I_2 is due to the difference between $v_{\rm gs1}$ and $v_{\rm gs2}$, which is caused by the imbalance effect of the SSN coupling to M_1 and M_2 due to the difference in termination between M_1 and M_2, such as additional loading of $R_1//R_2$ at M_2. Common-mode signals from coupled noise ($v_{\rm in,SSN}, v_{\rm in,SSN}$) generated due to junction capacitors and different termination between M_1 and M_2. Thus, the gate–source voltage $v_{\rm gs1}(t)$ differs from $v_{\rm gs2}(t)$.

B. Cause of the DC Voltage Offset: Imbalanced AC Current Component in I_1 and I_2 by SSN Coupling and Transistor Nonlinearity

First, the drain current I_1 and I_2 of M_1 and M_2 will be derived. The current of the drain node at the CMOS transistor is expressed using (1) [23]

$$i_D \approx \frac{1}{2}\mu C_{\rm ox}\frac{W}{L}(v_{\rm GS}(t) - V_{\rm th})^2 \tag{1}$$

where μ is mobility of electron or hole and $C_{\rm ox}$ means the oxide capacitance. W and L are the width and length of gate of CMOS, respectively.

Since the SSN coupled noise can be expressed as an ac noise signal, the gate–source voltage can be represented as the sum of a dc bias signal, $V_{\rm GS}$, and an ac coupled noise signal, $v_{\rm gs}$, as described in

$$v_{\rm GS}(t) = V_{\rm GS} + v_{\rm gs}(t) \tag{2}$$

$$V_T = V_{\rm GS} - V_{\rm th} \tag{3}$$

$$v_{\rm gs}(t) = |V_{\rm gs}(\omega)|\cos\,\omega t. \tag{4}$$

We use (3) to simplify the equations, while V_T is the dc voltage difference between the dc bias voltage of the gate–source and the threshold voltage of the MOS transistor. The ac coupled noise of the gate–source voltage is a sinusoidal wave as shown in (4). $V_{\rm gs}(\omega)$ is the Fourier transform of the $v_{\rm gs}.(\omega)$ is the angular frequency of the SSN coupled noise signal. Therefore, the drain current is expressed as follows:

$$i_D = \frac{1}{2}k\frac{W}{L}\left[\begin{array}{l} V_T^2 + \frac{1}{2}|V_{\rm gs}(\omega)|^2 \\ \quad +2|V_{\rm gs}(\omega)|V_T\cos\omega t + \frac{1}{2}|V_{\rm gs}(\omega)|^2\cos\,2\omega t \end{array}\right]. \tag{5}$$

The drain current can be divided into three current components. Three current components are the dc bias current (I_D) component in (6), the dc current (I_d) component in (7) produced by the ac SSN coupling and nonlinearity of the CMOS transistor, and ac currents (i_d) component in (8):

$$I_D = \frac{1}{2}k\frac{W}{L}V_T^2 \tag{6}$$

$$I_d = \frac{1}{4}k\frac{W}{L}|V_{\rm gs}(\omega)|^2 \tag{7}$$

$$i_d = \frac{1}{4}k\frac{W}{L}(4|V_{\rm gs}(\omega)|V_T\cos\omega t + |V_{\rm gs}(\omega)|^2\cos\,2\omega t). \tag{8}$$

The dc current components I_1 and I_2 flowing through the drain nodes of at M_1 and M_2 can be rewritten as

$$I = I_D + I_d = \frac{1}{2}k\frac{W}{L}V_T^2 + \frac{1}{4}k\frac{W}{L}|V_{\rm gs}(\omega)|^2. \tag{9}$$

As we have derived in the previous paragraph, dc current I_1 and I_2 are balanced by the feedback configuration of the OpAmp

$$\frac{1}{2}k\frac{W}{L}V_{T1}^2+\frac{1}{4}k\frac{W}{L}|V_{\rm gs1}(\omega)|^2=\frac{1}{2}k\frac{W}{L}V_{T2}^2+\frac{1}{4}k\frac{W}{L}|V_{\rm gs2}(\omega)|^2. \tag{10}$$

Therefore, if the SSN coupling effect to the transistor M_1 and M_2 in the OpAmp circuit is not same, in other words, if $|V_{\rm gs1}(\omega)|$ is not equal to $|V_{gs2}(\omega)|$, we find that difference between gate–source voltages of M_1 and M_2 can create the dc voltages offsets at the input and output nodes of the OpAmp as shown

$$\Delta V_{\rm inoff} = V_{T2} - V_{T1} \tag{11}$$

$$\Delta V_{\rm dcoffset} = \sqrt{V_{T1}^2 + \frac{1}{2}\left|V_{\rm gs1}(\omega)\right|^2 - \frac{1}{2}\left|V_{\rm gs2}(\omega)\right|^2}\frac{R_2}{R_1}. \tag{12}$$

C. Gate–Source Voltage to Induce the DC Offset Voltage

Fig. 7 shows the small signal equivalent circuit model of the OpAmp to induce $v_{\rm gs1}(t,\theta)$ and $v_{\rm gs2}(t,\theta)$ affected by the power supply noise ($v_{\rm sp,SSN}$), and input noise ($v_{\rm in,SSN}$) caused by the SSN coupling. $v_{\rm sp,SSN}$ and $v_{\rm in,SSN}$ are indicated in Fig. 2(a). In Fig. 7, $R_{\rm S}$ is the output resistance of the current source, and $C_{\rm S}$ is the summation of $C_{\rm bs1}, C_{\rm bs2}, C_{\rm ds1'}, C_{\rm ds2'}, C_{\rm ds0}$, and $C_{\rm L}$. Each junction capacitor is determined by physical dimensions [25].

For a standard twin-well CMOS technology process, n-channel MOS transistors are laid out in a p-well. Thus, parasitic reverse junction capacitors, $C_{\rm bs1}$ and $C_{\rm bs2}$, are connected between the source node and ground node of M1 and M2 [8], [9]. $C_{\rm ds1'}$ and $C_{\rm ds2'}$ are the modification capacitances for the Miller effect [23]. $C_{\rm ds0}$ is the junction capacitor between drain and source node of M0. $C_{\rm L}$ is parasitic capacitance induced by the layout of the transistors. $C_{\rm ps}$ is the reverse polarized junction capacitor.

1) Equations of the Gate–Source Voltage of M1 and M2 by the Power Supply Noise $v_{\rm sp,SSN}(t)$: By applying Kirchhoff's current law, we can obtain $v_{\rm gs1}(t)|_{\rm sp,SSN}$ and $v_{\rm gs2}(t)|_{\rm sp,SSN}$. The source voltage of M_1 and M_2 is assumed as $v_s(t)$. $V_s|_{\rm sp,SSN}(s)$ represents the voltage of source of M_1 and M_2 excited by the power supply noise expressed in frequency domain. $i_{d1}(s)$ and $i_{d2}(s)$ are the drain currents caused by the power supply noise $v_{\rm sp,SSN}(t)$ through M_9 and M_{10}. The voltage of source of M_1 and M_2 can be derived as in (13), shown at the bottom of the page.

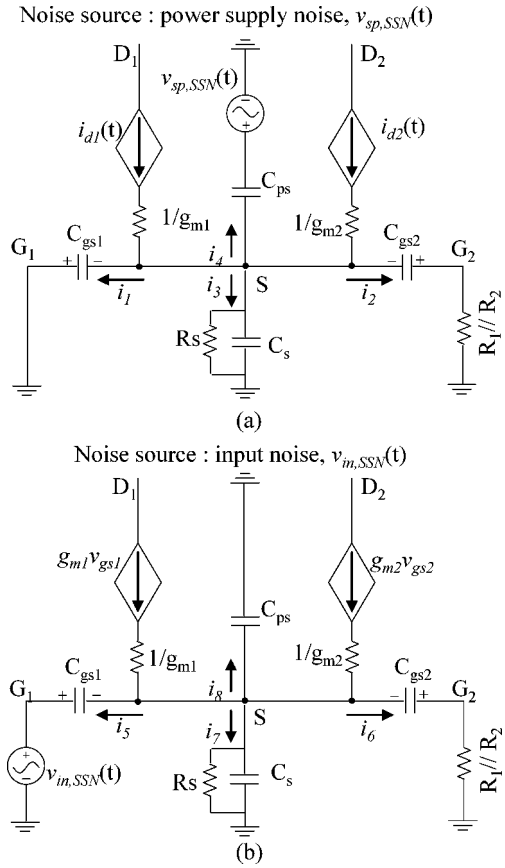


Fig. 7. Small signal equivalent circuit model of M_1 and M_2. (a) Model with the power supply noise, $v_{\rm sp,SSN}(t)$. The $v_{\rm sp,SSN}(t)$ is the coupled SSN to the power supply through path 1. $i_{d1}(t)$ and $i_{d2}(t)$ are currents from the power supply noise through M_9 and M_{10}. (b) Model with the input noise, $v_{\rm in,SSN}(t)$.

Since $C_{\rm gs1}$ equals to $C_{\rm gs2}$ and $g_{\rm m1}$ is same as $g_{\rm m2}$, we can represent $C_{\rm gs1}$ and $C_{\rm gs2}$ as $C_{\rm gs}$. $g_{\rm m1}$ and $g_{\rm m2}$ are defined as g_m. Therefore, the gate–source voltages of M_1 and M_2 caused by the power supply noise $v_{\rm sp,SSN}(t)$ are represented by (14) and (15), shown at the bottom of this page.

2) Equations of the Gate–Source Voltage of M1 and M2 by the Input Noise $v_{\rm in,SSN}(t)$: We obtain the gate–source voltage $v_{\rm gs1}(t)|_{\rm in,SSN}$ and $v_{\rm gs2}(t)|_{\rm in,SSN}$ with Fig. 7(b). $v_{\rm gs1}(t)|_{\rm in,SSN}$ and $v_{\rm gs2}(t)|_{\rm in,SSN}$ are gate–source voltages of M_1 and M_2 when the circuits have the input noise source of $v_{\rm in,SSN}(t)$ caused by the SSN coupling through the path 2. The voltage of the source

$$V_s(s)|_{\rm sp,SSN} = \frac{i_{d1}(s)+i_{d2}(s)+sC_{\rm sp}V_{\rm sp,SSN}(s)}{g_{m1}+sC_{\rm gs1}+[(g_{m2}+sC_{\rm gs2})/(sC_{\rm gs2}R+g_{m2}R+1)]+sC_S+sC_{\rm sp}} \tag{13}$$

$$V_{\rm gs1}(s)|_{\rm sp,SSN} = -\frac{i_{d1}(s)+i_{d2}(s)+sC_{\rm sp}V_{\rm sp,SSN}(s)}{(g_m+sC_{\rm gs})\left[(sC_{\rm gs}+g_m+2)/(sC_{\rm gs}R+g_mR+1)\right]+sC_S+sC_{\rm sp}} \tag{14}$$

$$V_{\rm gs2}(s)|_{\rm sp,SSN} = \frac{-1}{sC_{\rm gs2}R+1}\frac{i_{d1}+i_{d2}+sC_{\rm sp}V_{\rm sp,SSN}(s)}{g_{m1}+sC_{\rm gs1}+[(g_{m2}+sC_{\rm gs2})/(sC_{\rm gs2}R+g_{m2}R+1)]+sC_S+sC_{\rm sp}} \tag{15}$$

is as follows:

$$V_s(s)|_{\mathrm{in,SSN}} = \frac{(g_m+sC_{\mathrm{gs}})V_{\mathrm{in,SSN}}(s)}{(sC_{\mathrm{gs}}+g_m)\,(1+1/(sC_{\mathrm{gs}}R+g_m))+s(C_S+C_{\mathrm{ps}})+g_m}. \quad (16)$$

From (16), we obtain the gate–source voltages of M_1 and M_2, as represented by the following equations:

$$V_{\mathrm{gs1}}(s)|_{\mathrm{in,SSN}} = -\frac{(g_m+sC_{\mathrm{gs}})V_{\mathrm{in,SSN}}(s)}{(sC_{\mathrm{gs}}+g_m)\,(1+1/(sC_{\mathrm{gs}}R+g_m))+s(C_S+C_{\mathrm{ps}})+g_m} \quad (17)$$

$$V_{\mathrm{gs2}}(s)|_{\mathrm{in,SSN}} = -\frac{1}{sC_{\mathrm{gs}}R+1}\frac{(g_m+sC_{\mathrm{gs}})\cdot V_{\mathrm{in,SSN}}(s)}{s(2C_{\mathrm{gs}}+C_S+C_{\mathrm{ps}})+2g_m}. \quad (18)$$

3) Total Gate–Source Voltages of M1 and M2 by the Power Supply Noise $v_{\mathrm{sp,SSN}}(t)$ and the Input Noise $v_{\mathrm{in,SSN}}(t)$: The total the gate–source voltages of M_1 and M_2 by $v_{\mathrm{sp,SSN}}$ and $v_{\mathrm{in,SSN}}$ are obtained from the previously derived equations in Sections IV-C1 and C2., including (14), (15), (17), and (18). V_{gs1} is superimposed by $V_{\mathrm{gs1}}(s)|_{\mathrm{sp,SSN}}$ and $V_{\mathrm{gs1}}(s)|_{\mathrm{in,SSN}}$

$$V_{\mathrm{gs1}}(s) = -[\alpha(s)\{i_{d1}(s)+i_{d2}(s) + sC_{\mathrm{sp}}V_{\mathrm{sp,SSN}}(s)\}+\beta(s)V_{\mathrm{in,SSN}}\ (s)]\,. \quad (19)$$

V_{gs2} is superimposed by $V_{\mathrm{gs2}}(s)|_{\mathrm{sp,SSN}}$ and $V_{\mathrm{gs2}}(s)|_{\mathrm{in,SSN}}$

$$V_{\mathrm{gs2}}(s) = -[\gamma(s)\{i_{d1}(s)+i_{d2}(s) + sC_{\mathrm{sp}}V_{\mathrm{sp,SSN}}(s)\}+\kappa(s)V_{\mathrm{in,SSN}}(s)]. \quad (20)$$

To describe these equations of the gate–source voltage in the time domain, we have the following equations:

$$v_{\mathrm{gs1}}(t) = |V_{\mathrm{gs1}}(s)|\cos(\omega t+\theta_1) \quad (21)$$

$$v_{\mathrm{gs2}}(t) = |V_{\mathrm{gs2}}(s)|\cos(\omega t+\theta_2) \quad (22)$$

where θ_1 and θ_2 are phases of the gate–source voltage, if the phase of noise source, v_{SSN}, is 0°.

D. Analytical Equations to Estimate the DC Output Offset Voltage

The dc current of the drain is rewritten as (23). Here, n is the number of MOS transistors

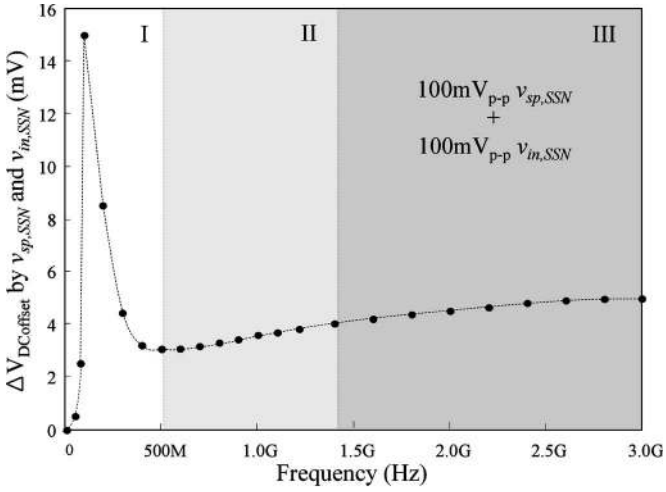
$$I_n = I_{nD}+I_{nd} = K'V_T^2+\frac{1}{2}K'|V_{\mathrm{gs}}(\omega)|^2$$

$$K' = \frac{1}{2}C_{\mathrm{ox}}\mu\frac{W}{L}. \quad (23)$$

Therefore, I_1 and I_2 can be represented by the following equation:

$$I_1 = K'\left[V_{T1}^2+\frac{1}{2}|V_{\mathrm{gs1}}(\omega)|^2\right] = K'\left[V_{T1}^2+v_{\mathrm{gs1}}^2(t)|_{\mathrm{dc}}\right] = \frac{I_B}{2} \quad (24)$$

$$I_2 = K'\left[V_{T2}^2+v_{\mathrm{gs1}}^2(t)|_{\mathrm{dc}}\right] = \frac{I_B}{2}. \quad (25)$$



	Region I	Region II	Region III
Dominant noise source	Power supply noise	Power supply & input noise	Input noise

(b)

Fig. 8. Calculated dc output offset voltage using the analytical model based on the circuit-level analysis without considering package-level PDN and interconnection models. (a) Calculated dc output offset voltage with both the power supply noise $v_{\mathrm{sp,SSN}}(t)$, and the input noise, $v_{\mathrm{in,SSN}}(t)$. (b) Noise source that affects dominantly the dc output voltage offset.

When the gate–source voltages of M_1 and M_2 are different, dc voltages (V_{T1}, V_{T2}) of M_1 and M_2 should be changed to equalize I_1 and I_2, ($I_1, I_2 = I_B/2$), which is the balance condition. Therefore, the relation described next exists

$$V_{T1}^2+v_{\mathrm{gs1}}^2(t)|_{\mathrm{dc}} = (V_{T1}+\Delta V_{\mathrm{inoff}})^2+v_{\mathrm{gs2}}^2(t)|_{\mathrm{dc}}. \quad (26)$$

Accordingly, the input offset voltage from (11), $\Delta V_{\mathrm{inoff}}$, is given by

$$\Delta V_{\mathrm{inoff}} = \sqrt{V_{T1}^2+v_{\mathrm{gs1}}^2(t)|_{\mathrm{dc}}-v_{\mathrm{gs2}}^2(t)|_{\mathrm{dc}}}-V_{T1}. \quad (27)$$

From (24), V_{T1} can be rewritten as a form of (28). Then, we can obtain (29) of the dc input offset voltage $\Delta V_{\mathrm{inoff}}$ by substituting (28) into (27) as follows:

$$V_{T1} = \sqrt{\frac{I_B}{2K'}-v_{\mathrm{gs1}}^2(t)|_{\mathrm{dc}}} \quad (28)$$

$$\Delta V_{\mathrm{inoff}} = \sqrt{\frac{I_B}{2K'}-v_{\mathrm{gs2}}^2(t)|_{\mathrm{dc}}}-\sqrt{\frac{I_B}{2K'}-v_{\mathrm{gs1}}^2(t)|_{\mathrm{dc}}}. \quad (29)$$

Finally, the dc output offset voltage is represented as (30), which is the function of the gate–source voltage of M_1 and M_2

$$\Delta V_{\mathrm{dcoffset}} = \left(\sqrt{\frac{I_B}{2K'}-v_{\mathrm{gs2}}^2(t)|_{\mathrm{dc}}}-\sqrt{\frac{I_B}{2K'}-v_{\mathrm{gs1}}^2(t)|_{\mathrm{dc}}}\right)\frac{R_2}{R_1}. \quad (30)$$

Now, we have the equation for the dc output offset voltage by substituting (21) and (22) into (30). Fig. 8 shows the calculated dc output offset voltage using (30), when the noise sources with 100 $\mathrm{mV_{p-p}}$ amplitude of $v_{\mathrm{sp,SSN}}$ and $v_{\mathrm{in,SSN}}$ are assigned.

It is clear that the amount of dc offset voltage is dependent on the frequency of the SSN noise. This graph in Fig. 8(a) can be divided into three regions based on the dominant mechanism that creates the dc voltage offset. The dc output offset voltage is dominantly affected by the power supply, $v_{\mathrm{sp,SSN}}(t)$, in region I (from low frequency to about 300 MHz). At several megahertz, the effect of junction capacitors is slight. As the frequency increases, the voltage difference between two junction capacitors, C_{gs1} and C_{gs2}, gains. When the frequency is over 100 MHz, CMOSs that configure current sources filter out the power supply noise. In region II, both $v_{\mathrm{sp,SSN}}(t)$ and $v_{\mathrm{in,SSN}}(t)$ generate the dc output voltage offset. It smoothly increases in this region because of the input noise $v_{\mathrm{in,SSN}}(t)$. This is caused by the voltage difference between v_{gs1} and v_{gs2} rise depending on the frequency. In Region III, the effect of the input noise is dominant, and the effect of the power supply is negligible. It should be reiterated that Fig. 8 is the response of the OpAmp circuit and is obtained without consideration of the chip and package-level PDN or the interconnection models in path 1 and path 2.

V. Hybrid Model of the DC Output Offset Voltage

A. Combination of PDN and Interconnection Models and the Analytical Model

In this section, we propose a complete hybrid model to estimate the dc output voltage offset of the OpAmp by combining both package-level PDN and interconnection models through the SSN coupling path 1 and path 2, as proposed in Section II with the analytical circuit model of the OpAmp circuit and as suggested in Section IV.

It will be demonstrated that when we include the package-level PDN and interconnection models through the SSN coupling paths 1 and 2, completely different frequency dependence behavior of the dc output voltage offset is observed in both the simulation and measurements compared to the curves in Fig. 8. As indicated in Section IV, the dc output offset voltage $\Delta V_{\mathrm{dcoffset}}$ is dependent on the gate–source voltages, v_{gs1} and v_{gs2}, of M_1 and M_2. Furthermore, v_{gs1} and v_{gs2} of M_1 and M_2 are determined by the power supply noise and the input noise. Therefore, the dc output offset voltage is a function of the frequency (f_{SSN}) of the SSN source at the package, $v_{\mathrm{in,SSN}}(t)$ and $v_{\mathrm{sp,SSN}}(t)$ as in the following equation:

$$\Delta V_{\mathrm{dcoffset}} = g(f_{\mathrm{SSN}},\, v_{\mathrm{sp,SSN}},\, v_{\mathrm{in,SSN}}). \tag{31}$$

Here, $v_{\mathrm{in,SSN}}(t)$ and $v_{\mathrm{sp,SSN}}(t)$ can be induced by multiplying I_{SSN} with Z_{21} and Z_{31}. I_{SSN} is the current induced by the SSN voltage in the package, as illustrated in Fig. 2(a). We have expressions for the $V_{\mathrm{sp,SSN}}$ and $V_{\mathrm{in,SSN}}$ in terms of V_{SSN} described as follows:

$$V_{\mathrm{sp,SSN}} = V_{\mathrm{SSN}}\frac{Z_{21}}{Z_{11}} \qquad V_{\mathrm{in,SSN}} = V_{\mathrm{SSN}}\frac{Z_{31}}{Z_{11}}. \tag{32}$$

Fig. 9 graphically shows the power supply noise and the input noise on the chip, and the coupling ratio.

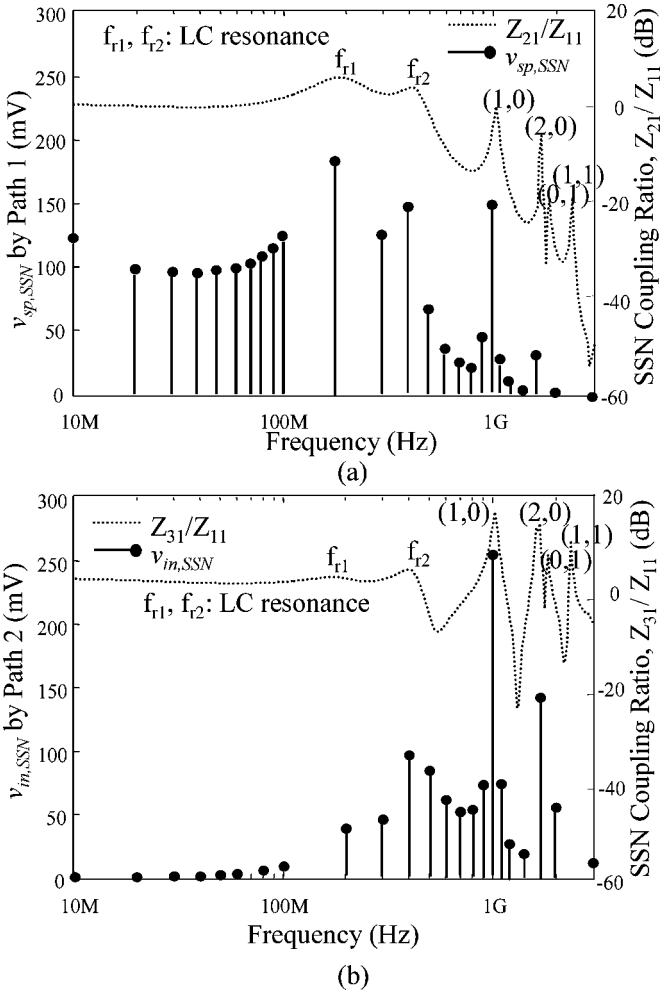


Fig. 9. (a) Stem graph shows the coupled noise to the power supply of the OpAmp on the chip by path 1, as described in Fig. 2(a), and the SSN coupling ratio (Z_{21}/Z_{11}) appears in the dotted line. (b) Stem graph shows the coupled noise to the input of the OpAmp by path 2. The SSN coupling ratio (Z_{31}/Z_{11}) appears in the dotted line.

B. Experimental Verification and Analysis of the Proposed Hybrid Model

In order to verify the hybrid model of the dc output offset voltage, we designed and fabricated a test package and tested a CMOS OpAmp chip, as shown in Fig. 10. Fig. 10 shows the measurement setup. The noise source is imported at the corner of the package substrate using the bias T and the signal generator. The dc output offset voltage is measured using high-Z probe on the pads of the package substrate. We applied a sinusoidal wave source, v_{SSN}, with a 100 $\mathrm{mV_{p-p}}$ amplitude, which mimics a SSN source in a package substrate.

In order to interpret the characteristics of the graph in Fig. 11, we analyze the correlation between the dc output offset voltages, using the curves in Figs. 8 and 9. The SSN coupling coefficient (Z_{21}/Z_{11}) presents the transfer function through the SSN coupling path 1, while the SSN coupling coefficient (Z_{31}/Z_{11}) expresses the transfer function through the SSN coupling path 2, as illustrated in Fig. 2(a). This is because $v_{\mathrm{sp,SSN}}$ and $v_{\mathrm{in,SSN}}$ are related to Z_{21}/Z_{11} and Z_{31}/Z_{11}. The previous

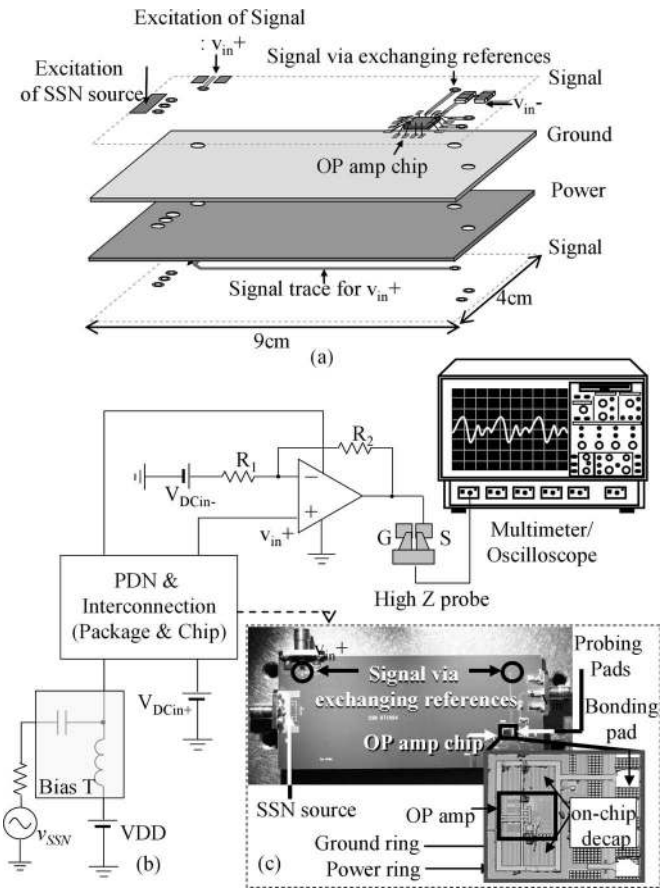


Fig. 10. Test vehicle for the experimental verification. (a) Four-layer design of the package substrate (FR 4). Chip is attached by COB technology. (b) Measurement setup. Voltage source that mimics a noise source is imported at the corner on the package substrate using a signal generator and a bias T. The dc output voltage offset is measured using the high-Z probe. (c) Assembled device under test (DUT). The CMOS OpAmp chip is fabricated using TSMC 0.25 μm process.

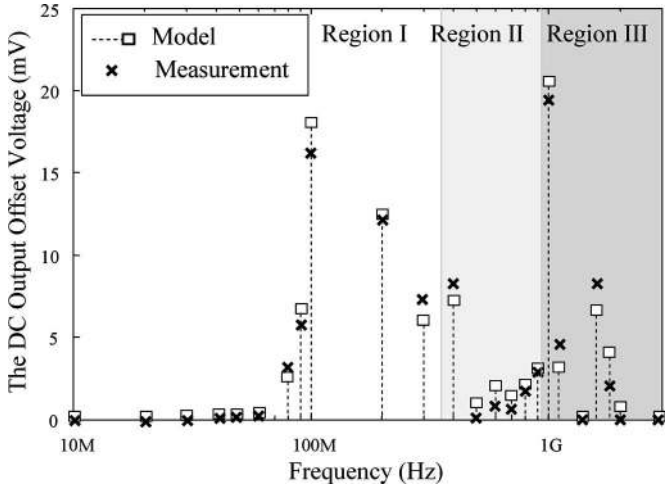


Fig. 11. Estimated and the measured dc output offset voltage depending on SSN frequencies, which is caused by the SSN coupling through the two coupling paths (path 1 and path 2), as shown in Fig. 1.

analysis [10]–[14] of the dc offset voltage of the OpAmp does not include the SSN coupling coefficients of Fig. 9. As a result, the calculated dc offset voltage in Fig. 11 is the reflection of the SSN coupling coefficients in Fig. 9 depending on the structure of the hierarchical PDN and interconnections. In other words, Fig. 11 has explicit footprints of the SSN coupling coefficients of Fig. 9 and the circuit-level analysis of Fig. 8. The SSN coupling coefficients shown in Fig. 9(a) and (b) are acquired using the modeling parameters through the SSN coupling paths 1 and 2, respectively. Meanwhile, the curve in Fig. 11 includes the SSN coupling effect through paths 1 and 2 together.

The remarkable peaks of the dc output offset voltage at 100 and 900 MHz can be explained by the frequency response of the OpAmp in Fig. 8 and the resonance peaks in the SSN coupling coefficients in Fig. 9. In order to interpret Fig. 9, we need to analyze Fig. 11, which is divided into three regions in a similar manner to Fig. 8 in Section IV. As discussed previously regarding Fig. 8, the dominant path up to 400 MHz (region I) is path 1. The maximum coupling noise is at 200 MHz due to a resonance of the hierarchical PDN. However, the dc output offset voltage (only circuit-level analysis) in Fig. 8 has a maximum offset voltage at 100 MHz. According to Fig. 8, when the coupled noises are the same at 100 and 200 MHz, the dc output offset voltage at 100 MHz is remarkably larger than that at 200 MHz. Even if the coupling noise at 200 MHz is larger than that at 100 MHz, the OpAmp filters the coupled noise at frequency greater than 100 MHz. Therefore, the $\Delta V_{\mathrm{dcoffset}}$ at 100 MHz is conspicuous. Both path 1 and path 2 generate the dc output offset voltage from 400 MHz up to 1 GHz. According to Fig. 8 (circuit-level analysis), the dc output offset voltage smoothly increases depending on the frequency of the coupled noises. The coupled SSN at 400 MHz is relatively larger than other frequencies. Therefore, $\Delta V_{\mathrm{dcoffset}}$ has a maximum value at 400 MHz in region II. At the other frequencies in region II, $\Delta V_{\mathrm{dcoffset}}$ increases with a positive slope because of the frequency characteristics of OpAmp, as shown in Fig. 8. Another reason is that there is only one resonance of the hierarchical PDN at 400 MHz in region II. These peaks of the SSN coupling coefficient curves occur at the resonance frequencies of the hierarchical PDN in the chip and package levels. In region III (from 1 to 3 GHz), Fig. 11 shows the peak value at 1 and 1.6 GHz. The dominant path in region III is path 2. $v_{\mathrm{sp,SSN}}$ does not affect the dc output offset voltage any more. According to the circuit-level analysis shown in Fig. 8, the $\Delta V_{\mathrm{dcoffset}}$ smoothly increases in the region III. It is obvious that $\Delta V_{\mathrm{dcoffset}}$ follows the frequency characteristic of the SSN coupling coefficient (Z_{31}/Z_{11}), as shown in Fig. 9(b) in this region. The coupling ratio has a resonance at 1 GHz. In addition, it has another resonance at 1.6 GHz, which is less than the resonance at 1 GHz. Consequently, $\Delta V_{\mathrm{dcoffset}}$ peaks at 1 and 1.6 GHz as it follows the SSN coupling coefficient (Z_{31}/Z_{11}). These peaks of the SSN coupling coefficient curve occur at the resonance frequencies of the PDN in the package levels. In other words, the SSN coupling problems become noteworthy when the SSN frequencies are coincident with the PDN resonance frequencies.

From Fig. 11, it is notable that the dc output offset voltage is determined not only by the frequency response of the OpAmp, as shown in Fig. 8, but also by the coupling coefficient (Z_{21}/Z_{11} and Z_{31}/Z_{11}) of the hierarchical PDN in the chip and package,

as shown in Fig. 9. This fact emphasizes the need for chip–package comodeling and simulation when estimating the effect of the SSN in an SiP.

VI. Conclusion

We proposed and verified a new hybrid modeling method for the efficient chip–package comodeling and cosimulation process. The proposed approach was applied to evaluate the SSN coupling effect onto the input paths and onto the power supplies of the OpAmp circuit in the SiP. It combines an analytical circuit model of the dc output offset voltage in the OpAmp circuit with the on-chip and off-chip PDN and interconnection models in a hybrid manner. Hence, the proposed approach can completely incorporate the interconnection characteristics and interactions of signal paths, power supply paths, and return current paths in both chip-level circuits and package-level structures.

The models and simulations were successfully verified with a series of dc output offset voltage measurements of the OpAmp circuit with respect to the frequency variation of the SSN source. These studies confirmed that the dc output offset voltage is correlated not only to the analysis of the on-chip OpAmp circuit, but also to the frequency dependent SSN coupling coefficients at the package-level PDN and interconnections. Furthermore, we prove that there is a remarkable difference in the simulation results when the PDN and interconnection models are considered compared to the simulation results obtained only using the conventional circuit-level analysis. This further supports the necessity of the chip–package comodeling, simulation, and analysis.

Usually, cosimulation for signal integrity or power integrity analysis of the chip and package together takes a relatively long time and requires extensive computational resources. Accordingly, it has not been feasible to simulate the circuit properties and the characteristics of chip–package PDN simultaneously. The proposed hybrid model successfully enables efficient co-analysis of noise susceptibility, signal integrity, and power integrity of the chips and the package substrate. Additionally, it should be reiterated that this model offers a shorter simulation time and an accurate estimation of the RFI susceptibility. Proposed modeling and analysis approaches can be further applied to the studies on the effect of the SSN coupling on other noise sensitive circuits in the SiP.

Appendix

A. Modeling Parameters for Path 1

The equations for model parameters summarized in Table I are as follows:

$$R = \sqrt{R_{\rm dc}^2 + R_{\rm ac}^2} \quad R_{\rm dc} = 2\frac{\rho}{t_c} \quad R_{\rm ac} = 2\frac{\rho}{\delta_c} \tag{33}$$

$$L = \mu d \tag{34}$$

$$C = \varepsilon_0 \varepsilon_r \frac{Wl}{d} \tag{35}$$

$$G = C\omega \tan\delta \tag{36}$$

$$L_W = 0.2\ell_W \ln\left(\frac{4h}{d}\right) \tag{37}$$

$$C_{f45} = \varepsilon_0 \varepsilon_{\rm IMD} \left[\ln \frac{t_{\rm M45} + t_{m5} + \sqrt{t_{\rm M45}^2 + t_{m5}^2}}{t_{\rm M45}} + \ln \frac{t_{\rm M45} + t_{m4} + \sqrt{t_{\rm M45}^2 + t_{m4}^2}}{t_{\rm M45}} \right] \tag{38}$$

$$R_{\rm ESR} = \frac{1}{12}\left(R_{\rm poly}\left(\frac{W}{L}\right) + \frac{1}{\mu_n C_{\rm ox}(V_G - V_T)}\left(\frac{L}{W}\right)\right) \tag{39}$$

$$C_{\rm MOS} = \varepsilon_0 \varepsilon_{\rm ox} \frac{WL}{t_{\rm ox}}. \tag{40}$$

RM4 and RM5 are derived using (33).

B. Modeling Parameters for Path 2

The equations for model parameters summarized in Table II are as follows:

$$C_s = \varepsilon_0 \varepsilon_r \left[\frac{W_s l_s}{h} + \frac{l_s}{\pi} \ln\left(\frac{h + t_c + \sqrt{t_c^2 + h t_c}}{h}\right)\right]. \tag{41}$$

R_s and L_s can be obtained using (33) and (34), respectively.

$$L_{\rm via} = 5.08d\left[\ln\left(\frac{2d}{r_{\rm via}}\right) + 1\right] \tag{42}$$

$$L_{\rm pad} = 5.08h\left[\ln\left(\frac{2h}{r_{\rm via}}\right) + 1\right] + 5.08t_c\left[\ln\left(\frac{2t_c}{r_{\rm pad}}\right) + 1\right] \tag{43}$$

$$C_{\rm via} = \frac{1.41\varepsilon_0 \varepsilon_r r_{\rm via} t_c}{d_{\rm pad}}. \tag{44}$$

References

[1] C. M. Scanlan and N. Karim, "System-in-package technology, application and trends," in *Technology Paper, Techonline*. Chandler, AZ: Amkor Technol., Jul. 2002.

[2] D. Kam and J. Kim, "Packaging a 40-Gbps serial link using a wire-bonded plastic ball grid array," *IEEE Des. Test Comput.*, vol. 23, no. 3, pp. 212–219, Jun. 2006.

[3] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 284–291, Aug. 1999.

[4] ITRS (International Technology Roadmap for Semiconductor), *Assembly and Packaging*. 2005 edition.

[5] M. Swaminathan, J. Kim, I. Novak, and J. P. Libous, "Power distribution networks for system-on-package: Status and challenges," *IEEE Trans. Adv. Packag.*, vol. 27, no. 2, pp. 286–300, May 2004.

[6] M. Swaminathan and A. E. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Englewood Cliffs, NJ: Prentice-Hall, 2007.

[7] S. G. Rosser, M. K. Kerr, C. S. Chang, J. Fang, Z. Chen, and Y. Chen, "Measurement and simulation of simultaneous switching noise in the multi-reference plane package," in *Proc. Electron. Compon. Technol. Conf.*, 23–31 May 1996, pp. 660–670.

[8] S. B. Dhia, M. Ramadani, and E. Sicard, *Electromagnetic Compatibility of Integrated Circuits*. New York: Springer-SBM, 2006.

[9] M. Douglas, "Integrated circuit electromagnetic susceptibility handbook," McDonnell Douglas Astronautic Co., St. Louis, MO, Tech. Rep. DC E1929, 1978.

[10] F. Fiori and P. S. Crovetti, "Nonlinear effect of radio-frequency interference in operational amplifiers," *IEEE Trans. Circuits Syst., Fundam. Theory Appl.*, vol. 49, no. 3, pp. 367–372, Mar. 2002.

[11] F. Fiori, P. S. Crovetti, and V. Pozzolo, "Prediction of RF interference in operational amplifiers by a new analytical model," in *Proc. IEEE Int. Symp., Electromagn. Compat.*, Aug. 13–17, 2001, vol. 2, pp. 1164–1168.
[12] F. Fiori, "A new nonlinear model of EMI-induced distortion phenomena in feedback CMOS operational amplifier," *IEEE Trans. Electromagn. Compat.*, vol. 44, no. 4, pp. 495–502, Nov. 2002.
[13] F. N. Trofimenkorr, "Noise performance of operational amplifier circuits," *IEEE Trans. Educ.*, vol. 32, no. 1, pp. 12–17, Feb. 1989.
[14] J. Xu, Y. Dai, and D. Abbott, "A complete operational amplifier noise model: Analysis and measurement of correlation coefficient," *IEEE Trans. Circuit Syst.*, vol. 47, no. 3, pp. 420–424, Mar. 2000.
[15] J. Park, H. Kim, Y. Jeong, J. Kim, J. S. Pak, D. G. Kam, and J. Kim, "Modeling and measurement of simultaneous switching noise coupling through signal via transition," *IEEE Trans. Adv. Packag.*, vol. 29, no. 3, pp. 548–559, Aug. 2006.
[16] J. Pak, H. Kim, H. Lee, and J. Kim, "PCB power/ground plane edge radiation excited by high-frequency clock," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Aug. 2004, vol. 1, pp. 197–202.
[17] J. Pak, J. Lee, H. Kim, and J. Kim, "Prediction and verification of power/ground plane edge radiation excited by through-hole signal via based on balanced TLM and via coupling model," in *Proc. Electr. Perform. Electron. Package.*, Oct. 2003, pp. 27–29.
[18] J. Kim, M. D. Rotaru, S. Baek, J. Park, M. K. Iyer, and J. Kim, "Analysis of noise coupling from a power distribution network to signal traces in high-speed multilayer printed circuit boards," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 2, pp. 319–330, May 2006.
[19] H. Park, H. Kim, D. G. Kam, and J. Kim, "Modeling and simulation of IC and package power/ground network," in *Proc. 2006 IEEE Int. Symp. Electromagn. Compat.*, Portland, OR, 14–18 Aug., vol. 3, pp. 659–701.
[20] J.-H. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution planes using transmission matrix method," *IEEE Trans. Adv. Packag.*, vol. 24, no. 3, pp. 334–346, Aug. 2001.
[21] J.-H. Kim and M. Swaminathan, "Modeling of multilayered power distribution planes using transmission matrix method," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 189–199, May 2002.
[22] G. Villar, E. Alarcon, F. Guinjoan, and A. Poveda, "Optimized design of MOS capacitors in standard CMOS technology and evaluation of their equivalent series resistance for power applications," in *Proc. 2003 Int. Symp. Circuits Syst.*, May, vol. 3, pp. III-451–III-454.
[23] S. Sedra and K. C. Smith, *Microelectronic Circuits*, 4th ed. Oxford, U.K.: Oxford Univ. Press.
[24] S. Hall, G. Hall, and J. McCall, *High Speed Digital System Design*. New York: Wiley.
[25] J. M. Rabaey and A. Chandrakasan, *Digital Integrated Circuits: A Design Perspective,* 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 2002.
[26] Y. Shim, J. Park, J. Shim, and J. Kim, "Modeling and verification to analyze effect of power/ground noises on CMOS feedback operational amplifier," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 9–13, Jul. 2007, vol. 2, pp. 1–7.

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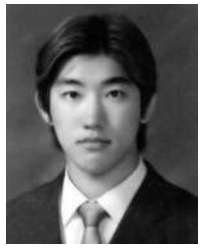

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