Modeling and Characterization of High Frequency Effects in ULSI Interconnects

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ABSTRACT

This paper discusses the accurate modeling of resistance R, inductance L and capacitance C in sub-100nm process node and their impacts on high frequency effects such as delay, crosstalk, and power/ground bounce. Models of interconnect (wire) resistances increase due to electron scattering at the surface and grain boundaries, and coupling capacitance of high aspect ratio interconnects for sub-100nm process nodes are presented. It is observed from test chip measurement that the skin effect and inductive effects of Cu interconnect at high frequencies exhibit different behaviors compared to Al interconnect, presumably because of the presence of CMP dummy metal fills. It is shown that the incorporation of frequency dependent R and L is essential in the modeling and characterization of high frequency effects for high speed ULSI circuits.

Keywords: high frequency effect, on chip interconnect, delay, crosstalk, ground bounce.

1 INTRODUCTION

As the operating speed of ULSI increases beyond a few GHz, higher frequency effects such as delay, crosstalk, ringing, reflection and power/ground bounce start to become limiting factors of ULSI chip performance. As IC process scaling progresses and the high level integration of functional blocks into a single chip continues, the number of metal layers increases, the aspect ratio of the interconnect (wire) becomes higher, and the metal line width and spacing becomes smaller. As a result, high frequency problems including resistance and capacitance (RC) delay and crosstalk are further exacerbated. The frequency-dependent modeling approach for distributed RCL parameters of on-chip interconnects is therefore crucial for the design and validation of high-speed ULSI circuit.

In this paper, we study new physical phenomena that arises in sub-100nm process nodes, namely, increased resistance of Cu interconnect due to electron scattering, coupling capacitance modeling of high aspect ratio Cu interconnects, high frequency skin effects and inductive behaviors of Cu interconnect in the presence of CMP dummy metal fills. We will then discuss their impact in the design and verification of ULSI chips and review various high speed interconnect characterization and measurement techniques.

2 HIGH FREQUENCY SKIN EFFECT

At high operating frequencies, penetrating depth of the electromagnetic field decreases resulting in an increase of wire resistance, so called the skin effect. The skin depth δ is defined as:

$$\delta = 1 \Big/ \sqrt{\pi f \mu \sigma} \tag{1}$$

For a simple Al line, the resistance change due to skin depth can be described as [1]:

$$R = \frac{\rho l}{w\delta\left(1 - \exp\left(t/\delta\right)\right)} \tag{2}$$

However in a real chip, the skin effect of Al interconnect affects the wider lines more than the narrow lines, and it also depends on the surrounding metals and their geometries. An empirical equation for R has been developed based on the measurement of a random test structure that mimics a real chip and is given by [2]:

$$R = \frac{\rho l}{2t\delta\left(1 + w/20\right)\left(1 - \exp\left(-w/2\delta\right)\right)} \tag{3}$$

where w is the width, t is the thickness, l is the length of the metal wire, and δ as shown in (1).

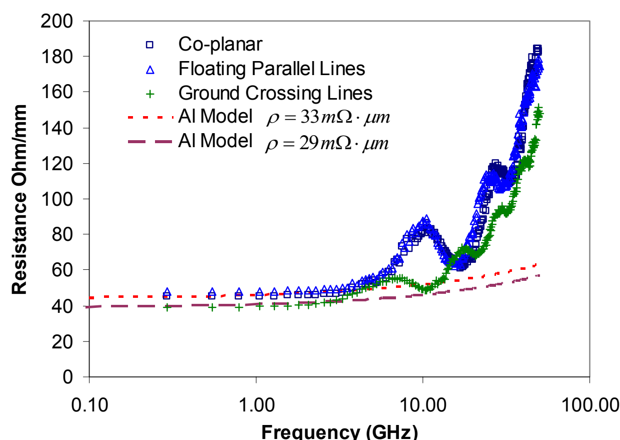

Figure 1: Cu interconnect high frequency skin effects from test chip measurement (90nm Cu process)

The skin depth for a Cu line is around 2µm (vs. 2.8µm for Al) at a frequency of 1GHz. The frequency dependence

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skin effect of a Cu wire in a ULSI design is more severe compared to Al wire based on test structure measurement (Figure 1) [3]. It is believed to be caused by the presence of Cu CMP dummy metal fills. The dummy metal fills are metal blocks that are inserted into empty space post-layout to achieve uniform metal density. These metal blocks surround the Cu wire and cause severe current crowding and higher resistance values at high frequencies.

The skin effect in a transmission line will influence both reflection and signal propagation [4]. Since characteristics impedance is frequency dependent, the reflection at the end of the interconnect will be affected. There will also be an increased attenuation as well as a shift in phase due to the increased resistance at higher frequencies, resulting in extra delay as shown in Figure 2. These results are obtained from SPICE simulation using measured resistance values shown in Figure 1.

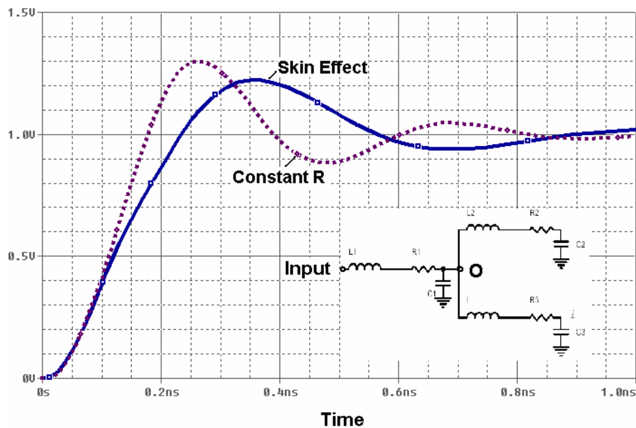

Figure 2: SPICE simulation of resistance with skin effect on delays of a RLC tree's response to a 100ps voltage ramp

3 HIGH FREQUENCY INDUCTANCE

When ULSI operating frequencies increase to multi-GHz range, the impedance contribution by on-chip interconnect inductance (ωL) becomes comparable to the wire resistance [3]. The inclusion of inductive effect in the interconnect modeling not only causes ringing and reflection, thus increases delay, but also causes voltage overshoot and reduces rise time, thus increases crosstalk noise. Furthermore, the switching noise due to inductive voltage drop is an issue for power distribution network.

Inductance, by definition, is for a loop of a wire, the wider the current loop, the higher the inductance. The modeling and calculation of a wire inductance in a ULSI chip requires the knowledge of current return path. Inductance is a frequency dependent component of the interconnect impedance. At low frequency, the resistance component dominates the total impedance. Therefore at low frequencies, current returns through multiple lines and ground lines in order to minimize the resistance. These return loops may not necessarily be the nearest neighbors. However, at high frequency the inductive component of the total impedance begins to dominate, resulting in return loops that are often limited to the nearest neighbors. At even higher frequencies (>50GHz), the inductance value is further decreased due to capacitive coupling of the interconnect to random structures, and current returns to the nearest neighbors through displacement current [2, 4].

Such a reduction of inductance due to proximity effect at higher frequencies for Cu metal wires is shown in Figure 3 for different structures including co-planar structure, co-planar structures with parallel floating lines and grounded crossing lines. These results are from the measurements of a test chip fabricated using a 90nm Cu CMOS process [3]. Similar to Cu skin effect, Cu CMP metal fills also play a role in determining inductive current return loop at high frequency. As can be seen from the figure, the FastHenry simulation indicates that inductance values are relatively constant for co-planar structure, but measurement confirms that the inductance of co-planar structures behave similar to the inductance of the structures with floating parallel lines. This is because of the presence of dummy metal fills in the spacing between the lines. Therefore it is reasonable to believe that Cu dummy metal fills actually provide a current return path at high frequency and limit the current return path to the nearest neighbors (dummy metal blocks in this case) of the signal line.

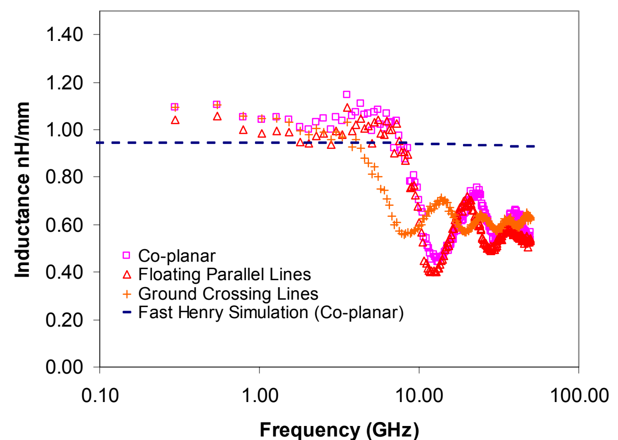

Figure 3 High Frequency inductive effects from test chip measurement (90nm Cu process)

Because of the long range characteristics of inductance coupling, accurate estimation of the delay and the noise for RLC lines is usually time consuming. For N number of signal lines, a full partial and self inductance matrix N x N is physically accurate but computationally expensive. To increase computational efficiency, various effective loop inductance models have been proposed to reduce multiple line condition [5] or structure that consists of a single line over a power grid [6] into a single line model. Figure 4 shows the difference in the output response to a 100ps voltage ramp (see insert) due to the difference in the inductance values calculated using simple loop inductance model ($L_{loop} = L_1 + L_2 - 2L_m$), and the measured inductance (measured inductance is higher than loop inductance). The

inductance value (measurement in this case), is quite different from the case using measured inductance. Therefore an accurate L_{loop} model is essential for efficient timing analysis.

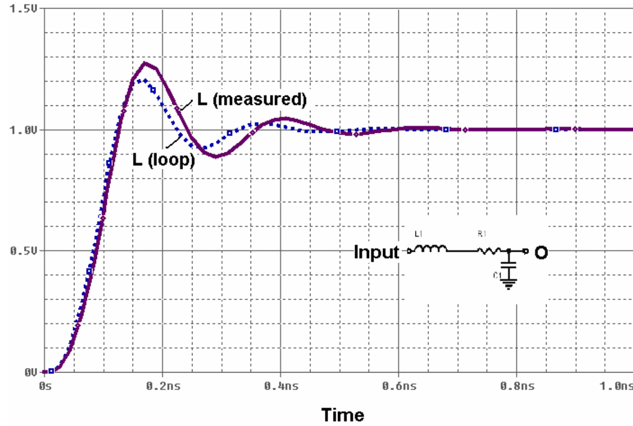

Figure 4: Delay discrepancies due to underestimation by simple loop inductance model

4 HIGH FREQUENCY CAPACITANCE

The capacitance of on-chip interconnect is relatively constant at high frequencies as is evident from test chip measurement shown in Figure 5. The peaks at higher frequencies shown in Figure 5, as well as in Figure 1 and 3 are resonant peaks of the 3mm long interconnect behaving like a transmission line. Due to the presence of adjacent ground lines, the capacitance of the structure with crossing lines is higher, therefore its resonant frequency is also smaller.

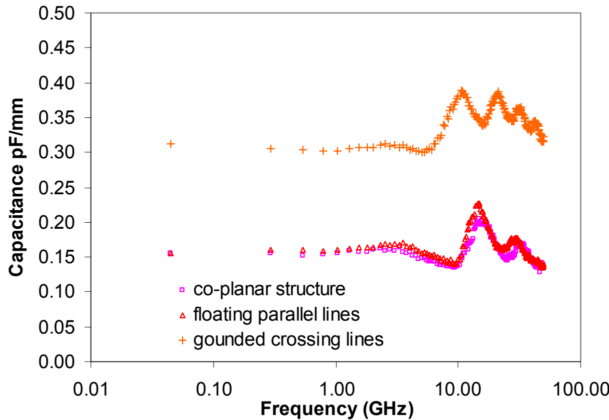

Figure 5 High Frequency capacitance from test chip measurement (90nm Cu process)

5 HIGH FREQUENCY EFFECT CHARACTERIZATION TECHNIQUES

At low frequencies, the DC resistance and coupling capacitance of on-chip interconnect can be measured separately using either passive or active methods, however care must be taken to isolate parasitic effects from the measurements [7].

At high frequency, on-chip interconnect behaves like transmission lines. If a short length of a transmission line is considered, a lumped approximation can be applied to model the interconnect with series resistance R, inductance L, and with shunt capacitance C and conductance G. When losses on a transmission line are small, the complex propagation constant and characteristic impedance are:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$
$$Z = R + jX = \sqrt{(R + j\omega L)/(G + j\omega C)} \quad (4)$$

Using a vector network analyzer, the S parameter matrix of an on-chip interconnect can be measured. The S parameter measurements are carried out by launching waves from both ends of a signal line and measuring the reflected and transmitted network parameters over a frequency range up to 50-100GHz. S parameters are associated with line parameter RLCG by following equation:

$$|S| = \frac{1}{D_s}\begin{bmatrix} (Z^2 - Z_0^2)\sinh(\gamma l) & 2ZZ_0 \\ 2ZZ_0 & (Z^2 - Z_0^2)\sinh(\gamma l) \end{bmatrix}$$
$$D_s = 2ZZ_0\cosh(\gamma l) + (Z^2 + Z_0^2)\sinh(\gamma l) \quad (5)$$

The resistance R, inductance L and capacitance C of the interconnect can then be extracted from γ and Z [3].

Time Domain Reflectometry (TDR) measurement is another high speed interconnect characterization technique. Unlike network analyzer which gives steady state measurement, TDR is a transient measurement and the frequency of measurement is usually much lower compared to the upper range of the S parameter measurement. TDR determines the characteristic impedance by measuring the super-positioned incident and reflected waveform at the source of the interconnect. It provides a good spatial resolution and can easily identify interconnect discontinuity [8].

Ring oscillators can also be used to measure delays and characterize impedance of interconnects. By inserting interconnects into a ring that consists of odd number of inverters, the resonant frequency can be measured and the interconnect delay can then be obtained [9].

6 RC DELAY

The use of Copper (Cu) interconnect has resulted less RC delay due to its lower resistivity. With the incorporation of low k dielectric material, the RC delay has been cut to almost half compared to Aluminum (Al) interconnect with SiO_2 dielectrics in the same process node [10]. However, as scaling continues, resulting in smaller metal line width and spacing, and higher aspect ratio, the RC delay starts to rise again as evident from Table 1. The delay is the time

required for signal to propagate through interconnect and is calculated from the resistance and capacitance of the interconnect. Note that due to increasing ULSI chip operating frequency, on-chip inductance value also increases. Therefore, the inductance effects need to be considered in high frequency interconnect modeling [11].

Since the total wire resistance and capacitance are proportional to wire length, interconnect RC delay can be reduced either by introducing new materials of lower resistance and capacitance or by reducing wire length through a change of design architecture such as X Architecture [12, 13].

Table 1: Typical RC delay values in different process nodes

Process Node (nm)	180	130	90	65	45
Width /Spacing	280	200	140	100	80
Metal Thickness	580	350	320	270	200
Dielectric Thickness	800	360	270	200	140
Dielectric Constant	4.00	3.60	3.10	2.90	2.70
Resistivity (μΩ·cm)	3.70	2.20	2.20	2.60	2.90
R (Ω/μm)	0.246	0.314	0.476	0.815	1.813
C (fF/μm)	0.122	0.083	0.093	0.095	0.080
SoC Freq. (KHz)	500	1000	1500	2000	3000
jwL (/μm)	0.013	0.023	0.033	0.044	0.063
RC delay (fs/μm)	0.030	0.026	0.044	0.077	0.145

6.1 Resistance of Sub-100nm Process Nodes

As scaling of process node reaches below 100nm, the dimensional dependence effects begin to influence the resistivity of Cu interconnect. Since the thickness of the Cu wire barrier layer can not be scaled as fast as Cu wire, the cross section area consumed by high resistivity barrier material becomes proportionally larger. Also electron scatterings at ground boundary and metal surface decrease the mobility of electrons, resulting in higher resistivity compared to bulk Cu material. The combined surface and ground boundary scattering model can be described using electron mean free path l, the average ground boundary distance d, the proportion of electron specularly reflected from the surface p, and the reflection coefficient r that denotes the probability of electron being reflected at the surface [14, 15]:

$$\rho = \rho_0 \left(\frac{1}{3} \Big/ \left(\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right) \right) + 1.2(1-p)\frac{U}{S} l \right) \quad (6)$$

where $\alpha = \frac{l}{d}\frac{r}{1-r}$, U is the perimeter and S is the cross-section area of the wire. Some typical resistivity values calculated for sub-100nm process nodes based on Eq. (6), that are in agreements with measurements, are shown in Table 1.

6.2 Coupling Capacitance Modeling for Sub-100nm Process Nodes

In order to model the RC delay effect of sub-100nm process nodes accurately, not only increased resistance due to electron scattering and barrier layer materials need to be considered, but higher aspect ratio interconnect capacitance modeling also needs to be included. It is also worth mentioning that Cu CMP dummy metal fill impact on interconnect capacitance is among the effects to be modeled precisely. To calculate capacitance values for sub-100nm nodes, a set of empirical equations have been developed for parallel plate interconnect structures [14]. Coupling capacitances shown in Table 1 are obtained by this method. Accurate calculation of resistance and capacitance are not only essential for timing analysis, it is also important for and signal integrity analysis.

7 CROSSTALK NOISE

The signal of one interconnect can affect another interconnect in a ULSI chip through either capacitive coupling or inductive coupling, resulting in a signal noise and discussed in details below.

7.1 Capacitive Crosstalk

When the coupling capacitance of two interconnects are large enough, displacement current can be injected from aggressor to victim lines. The current is spitted evenly in each direction of the victim line. Assuming a weak coupling wherein the secondary crosstalk from victim to aggressor is negligible, the capacitive crosstalk results in a noise at the far end (V_{FE}) and a signal with long pulse at the near end of the victim line. The far end noise (V_{FE}) is a single pulse with width approximately equal to the edge rate of the signal on the aggressor, and it grows in amplitude with longer wires. The near end noise (V_{NE}) however grows in pulse widths with long wire length. The V_{FE} and V_{NE} noise voltages can be described by the following equations [16]:

$$V_{FE} = \frac{1}{2} Z_0 c_c d \frac{dV_s}{dt} \quad (7)$$

$$V_{NE} = \frac{1}{4} \frac{C_c}{C} V_0 \quad (8)$$

where C_c is the coupling capacitance between two interconnects, and C is the self capacitance per unit length.

V_0 is the peak of the signal. Z_0 is the characteristics impedance of the victim line and d is its length.

7.2 Inductive Crosstalk

When two interconnects are coupled by mutual inductance L_m, a crosstalk voltage can be generated on the victim line due to the change in the current on the aggressor line according to $V = L_m dI/dt$. Unlike capacitive coupling, the net change in current of inductive crosstalk is zero. As a result, the forward and backward crosstalks have opposite polarities. A low to high transition on the aggressor line produces a positive backward pulse and a negative forward pulse on the victim line. Similar to capacitive coupling, inductive crosstalk results in a short pulse at the far end and a long pulse at the near end. The far end and near end noise voltages, V_{FE} and V_{NE} respectively, due to inductive crosstalk can be described by the following equation [16]:

$$V_{FE} = -\frac{1}{2}\frac{L_m}{Z_0} d \frac{dV_s}{dt} \tag{9}$$

$$V_{NE} = \frac{1}{4}\frac{L_m}{L} V_0 \tag{10}$$

where L_m is the mutual inductance and L is the self inductance per unit length. Z_0 is the characteristic impedance of the line, d is the length of the line.

7.3 Total Crosstalk

When capacitive and inductive crosstalks are simultaneously present, the noise at the far end is [16]:

$$V_{FE} = \frac{1}{2} d\left(Z_0 c_c - \frac{L_m}{Z_0}\right) d \frac{dV_s}{dt} \tag{11}$$

and the noise at near end is: $V_{NE} = K_{NE} v_0$

where $K_{NE} = \frac{1}{4}\left(\frac{C_c}{C} + \frac{L_m}{L}\right)$ (12)

Note that because of the opposite polarities for capacitive and inductive crosstalk, far end noise can be cancelled out when: $\frac{C_c}{C} = \frac{L_m}{L}$. However, the near-end crosstalk always exists.

In a ULSI chip, there are many closed spaced interconnects thus the crosstalk components are mixed. However, for capacitive crosstalk, the electrical fields are shielded by the nearest neighbors of the signal wire, and coupling capacitance decreases rapidly as distance increases. On the other hand, due to the long range nature of the magnetic field, the mutual inductance decreases slowly with increasing spacing. Therefore couplings to neighbors are both capacitive and inductive, with capacitive crosstalk often dominating, while coupling to farther lines is mostly inductive.

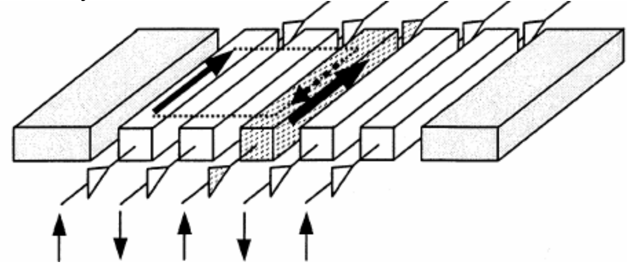

Figure 6: Worst case switching vector

In addition to interconnect geometries, the input vector for multiple signal lines also significantly affects the delay and the noise amplitude on central signal lines. If the simple RC model is applied, it is known that the opposite switching pattern of the first neighbors to the victim line generates the worst delay and largest noise. When capacitive coupling dominates, the maximum noise happens when the first neighbors switch oppositely as shown in Figure 6. However, with the inclusion of long-range inductive coupling, the maximum noise happens when all the higher-order neighbors, which are only coupled inductively to the victim, switch in the same direction as the victim. [15].

8 POWER OR GROUND BOUNCE

As the operating frequencies of ULSI chips increase, the inductive effects of the power/ground lines or planes become significant. As time-changing voltage propagates down the signal line, crosstalk arises through the energy being coupled from one conductor to another either capacitively (through electric field coupling) or inductively (through magnetic field coupling). Furthermore, dI/dt noise (also known as power/ground bounce) also appears in the power/ground lines. This voltage fluctuation is proportional to the inductance of the power/ground lines and the rate of the current change:

$$\Delta V = L dI/dt \tag{13}$$

When the logic cells in a circuit are switched on and off, the voltage levels at the power distribution lines of the circuit or the reference levels of the ground lines vary, resulting in a false triggering and timing failure. Such an effect worsens as multiple cells are switching at the same time, thus it is also called Simultaneous Switching Noise (SSN).

Equivalent circuit models that consider the distributed nature of the power/ground bounce are often used to analyze the circuit. Thus the accurate estimations of the inductance of signal lines and power or ground distribution lines are important. Figure 7 shows the simulation results (FastHenry) of inductance values as functions of frequency for either a Manhattan line or an X Architecture line (diagonal line) in the presence of X Architecture power

grid, in which one layer of the power is diagonal. Compared to Manhattan signal line, the inductance of a diagonal line is insensitive to the placement relative to the power grid because the current return loop through power grid is relatively constant.

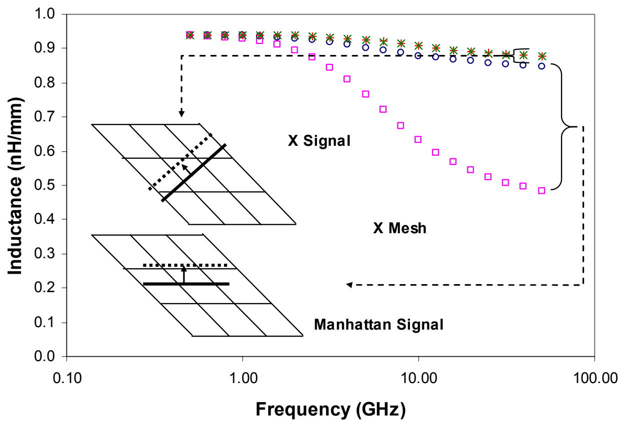

Figure 7: Inductance of a signal line with return loop through X Architecture power grid.

Since on-chip decoupling capacitors force the same fluctuations to appear on both power and ground plane, hence they are often used to reduce power/ground bounce problem. However precise estimations of the decoupling capacitance values are required since overestimation is costly from the chip area point of view, whereas underestimation may lead to noise margin problem. Another way to minimize the peak ground bounce amplitude is to delay the switching time of the output buffers and thereby prohibit all the buffers from switching simultaneously. This is done by inserting a chain of buffers in the signal path to the output drivers. Based on a special property of the ground bounce waveform, one can propose an optimum skew time for switching of output buffers under which the ground bounce is attenuated up to 65% of its original values [17].

9 CONCLUSION

Accurate modeling and characterization of high frequency effects of sub-100nm process nodes Cu interconnects are studied. Resistance increase due to electron scattering, higher coupling capacitance due to higher aspect ratio, skin effect and high frequency inductive behaviors, as well as their impact on delay, crosstalk and power/ground bounce are discussed. High frequency interconnect characterization techniques are also reviewed.

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