Modeling and circuit design for three-terminal memristors

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Abstract: In this paper, a three-terminal memristor model is developed in order to improve the anti-interference performance of the memristor and address the issue that the resistance value of the conventional two-terminal memristor is readily impacted by voltage. In order to simulate and validate the function of the three-terminal memristor, the logic circuit and multiplication circuit are developed using this model in this work using the cadence ic617 program. According to the findings, the three-terminal memristor multiplication circuit uses less energy than the typical conventional multiplier circuit, consuming only 0.335 uW. The memristor offers the benefits of low power consumption, compact size, and great integratability as a nanoscale device. The use of three-terminal memristors can dramatically reduce the number of chip components and improve chip integration when Moore's law approaches a limit.

Keywords: memristor; multiplication circuit; logic circuit; cadence ic617 simulation

Ⅰ.INTRODUCTION

Prof. Shaotang Cai initially put up the memristor idea in the 1970s[1], and it wasn't until 2008 when TiO2 thin-film devices at HP Laboratories[2] provided the first evidence of its reality. A new class of electrical devices called memristors include features including high integration, low power consumption, and non-volatility. Memristors are used in a variety of neural network [3][4] , Chaotic circuits [5][6] and logic circuit design[7] applications. One of the current research areas for logic circuits is the development of novel logic circuits for memristors [8].

Memristors can be divided into charge-controlled and magnetically-controlled memristors. The resistance value of a memristor is determined by the magnitude, direction, and duration of the voltage applied to its terminals, and it has a memory function to remember the amount of charge or flux flowing through it. It is also non-volatile and can maintain the resistance value at the time of power failure until the power is turned on again. 2008 HP Labs discovered a charge-controlled memristor that consists of two metal Pt electrodes with two TiO2 films sandwiched between them, with one TiO2 film containing oxygen vacancies, the doped layer, and the other pure TiO2 film, the undoped layer，As shown in Figure 1.

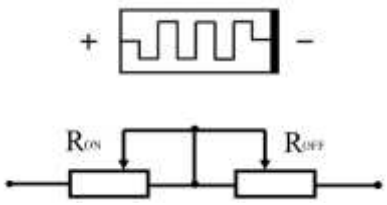


Fig.1 HP two-terminal memristor equivalent circuit

The resistance value of the charge-controlled memristor changes as the boundary between the doped and non-doped layers moves. The magnetically controlled memristor is derived on the basis of the charge-controlled memristor, and according to the literature[9], the resistance value of the charge-controlled memristor is given by.

$$M(t)=\begin{cases} R_{OFF} & q(t)<c_1 \\ M(0)+kq(t) & c_1,\ q(t)<c_2 \\ R_{\mathrm{ON}} & q(t)..c_2 \end{cases} \tag{1}$$

ROFF and RON are the ultimate resistance values of TiO2 films with all undoped layers and all doped layers, respectively. M(0) is the initial resistance of the memristor. $k=\frac{(R_{ON}-R_{OFF})\mu_v R_{ON}}{D^2}$, μ_V is the ion mobility and D is the thickness of the TiO2 thickness of the TiO2 film; $c_1=\frac{R_{OFF}-M(0)}{k}$, $c_2=\frac{R_{ON}-M(0)}{k}$.

The expression of the magnetron memristor conductance is .

$$dv=Mdi \tag{2}$$

$$d\varphi=vdt \tag{3}$$

$$\varphi(t)=\int_0^t M(t)i(t)\mathrm{d}t=\int_{q(0)}^{q(t)}M(t)\mathrm{d}q(t) \tag{4}$$

$$\mathrm{d}i=W\mathrm{d}v \tag{5}$$

$$W(\varphi)=\begin{cases} \dfrac{1}{R_{OFF}} & \varphi(t)<c_3 \\ \dfrac{1}{\sqrt{2k\varphi(t)+M^2(0)}} & c_3,\ \varphi(t)<c_4 \\ \dfrac{1}{R_{ON}} & \varphi(t)..c_4 \end{cases} \tag{6}$$

Where: $c_3=\frac{R_{\mathrm{OFF}}^2-M^2(0)}{2k}$; $c_4=\frac{R_{\mathrm{ON}}^2-M^2(0)}{2k}$

Memristors have a special non-volatile property that prevents their resistance value from changing until the voltage does. Nevertheless, in certain circuits that substitute memristors for MOS transistors, the property of the resistance value changing with voltage restricts the usage of memristors and occasionally necessitates the inclusion of extra peripheral circuitry to guarantee the correct execution of the function. This, however, makes the circuit design more complicated and negates the goal of employing memristors to achieve a higher level of integration.

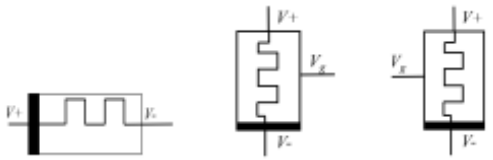
Conventional two-terminal memristors are vulnerable to interference from external magnetic fields in industrial generation, and a change in resistance value would impact the performance of the circuit stability[10]. A three-terminal memristor model is suggested to accomplish anti-interference protection for stored data in order to strengthen the stability of the memristor and protect it from outside interference when data input to it happens and when data storage is to be done.

Compared to two-terminal memristors, three-terminal memristors have the following performance and application advantages by adding a port to control the shielding from external electromagnetic interference:

1. Better immunity to interference: Three-terminal amnesic resistors can control external electromagnetic interference through an additional control port, thus being able to resist the influence of external electromagnetic interference to a certain extent, improving their stability and reliability. In contrast, two-terminal memristors may be more sensitive in the face of external electromagnetic interference.
2. Higher controllability: The control port of the three-terminal memristor can be used to control the internal resistance value of the memristor, thus enabling control of the memristor. By adjusting the voltage or current at the control port, it is possible to change the state of the three-terminal memristor, including the transition from high to low resistance and vice versa, thus providing greater controllability.

Ⅱ. THREE-TERMINAL MEMRISTOR MODEL DESIGN

The three-terminal memristor adds a vertical port to the two-terminal memristor, as seen in Figure 1. The vertical port Vg serves as the control terminal to switch on or off the horizontal channel, while the horizontal ports V+ and V- are utilized to regulate the memristor's resistance change. When the voltage of Vg has to be greater or lower than a specific value to turn on or off the vertical channel, it can construct PMOS-like and NMOS-like structured memristors, respectively. The voltage of Vg is equivalent to the gate voltage of a MOS tube.



a.two-terminal memristor b.PMOS memristor c.NMOS memristor

Fig.2. Two-terminal memristor and two types of three-terminal memristor

The memristor model of Gul F[11]is used to develop a three-terminal memristor model in this research. This model has a straightforward and compact circuit topology, and its corresponding circuit is displayed in Figure 2.

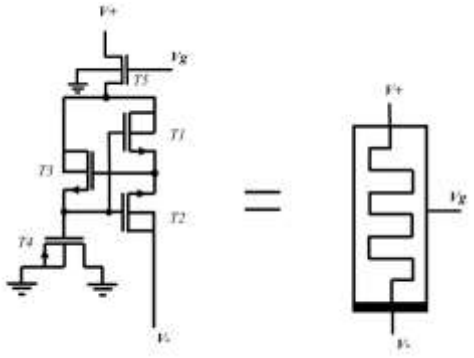


Fig.3. Equivalent circuit of three-terminal memristor

There are just five CMOS transistors in the memristor circuit model. The source and drain terminals of the T4 transistor are grounded, so T4 transistor can be seen as a capacitor to provide storage memory function for the entire circuit, and T5 acts as the input control of memristors. T1 and T2 transistors are driven by the input conduction voltage and can be seen as two nonlinear resistors. T3 transistor acts as a regulating switch to regulate the charging and discharging of the capacitor to change the resistance value of T1 and T2. This memristor modulation's R_{off} and R_{on} values are approximately 100K and 10K, respectively.

ⅠⅠⅠ.SIMULATION OF THREE-TERMINAL MEMRISTOR CIRCUIT

TSMC18rf process characteristics and the Cadence ic617 Environment were used to develop the circuits discussed in this study. This memristor equivalent circuit can possibly implement the memristor function based on the prior study. In this study, a sinusoidal AC signal is employed as the input, and it is discovered through experimental analysis that a more complete

hysteresis curve graph can be generated by providing five CMOS transistors with a proper aspect ratio, as shown in Figure 3. Table 1 lists the MOS tube specifications needed to construct the memristor.

Table1.Transistor parameters

Mos	$W/\mu m$	$L/\mu m$
T1	8.6	2.85
T2	18	1.4
T3	0.42	5.25
T4	24.4	0.245
T5	12	6.45

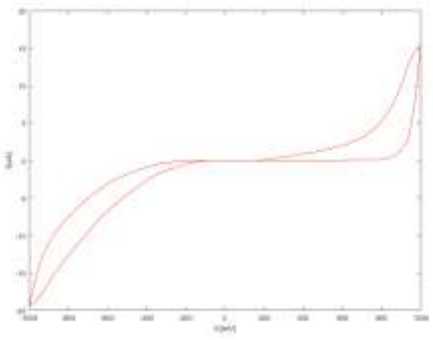


Fig.4.I-V hysteresis curve of the Three-terminal memristor

The memristor's I-V characteristic curve shows that when the input sinusoidal voltage signal behaves as a positive voltage, the forward charge flowing through the device increases. This is equivalent to increasing the doping concentration or speeding up the migration of hole charge in the HP model, which causes the thickness of the undoped region to decrease and lowers the memristor's resistance value. The forward charge flowing through the memristor declines and the reverse charge grows when the input positive selective voltage signal is inverted, which causes the memristor's resistance value to progressively rise.

Ⅳ.Three-terminal memory resistors build logic gate circuits

Figure 4 depicts the layout of the three-terminal Memristor logic "with" gate circuit.

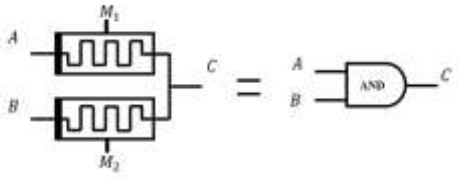


Fig.5 Three-terminal Memristor "with" gate circuit

Attach the memristors M_1 and M_2's positive terminals, using the negative terminals A and B as inputs and the terminal C as the output terminal. Assume that the voltage at the output terminal C is V_C and the voltages at the input terminals A and B are V_A and V_B, respectively. The memristors M_1 and M_2 have resistances of R_{M1} and R_{M2}, respectively. R_M equals R_{on} when the memristors are forward biased, and R_{off} when they are reverse biased. Then.

$$V_C = \frac{R_{M2}}{R_{M1}+R_{M2}} \cdot V_A + \frac{R_{M1}}{R_{M1}+R_{M2}} \cdot V_B \quad (7)$$

Low voltage denotes logic "0," whereas high voltage denotes logic "1." When both input voltages are 0, it is computed; when just one is 0, it may be determined by inserting into equation (1). Figure 5 displays the simulation outcomes for the Three-terminal memristor "with" gate circuit. The relationship between the input and output voltages of the "with" gate circuit built by the three-terminal memristor is shown in Table 2.

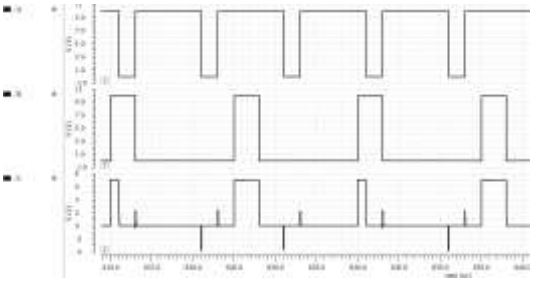


Fig.6. Simulation results of Three-terminal memristor "with" gate circuit

Table2.Three-terminal memristor "with" gate input and output voltage results

V_A/V	V_B/V	V_C/V
0	0	0
0	10	0
10	0	0
10	10	10

A=B="1", C="1" when both A and B input high level 10V; C="0" in all other circumstances. The simulation findings and the with-gate logic are consistent. Figure 6 depicts the three-terminal memristor logic "or" gate circuit's physical layout.

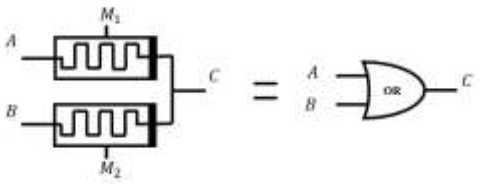


Fig.7. Three-terminal Memristor "or" gate circuit

Link the memristors M_1 and M_2's negative terminals together, using the positive terminals A and B as inputs and the C

terminal as an output. The answer to equation (1) can also be derived by assuming that the voltages of the A and B inputs are V_A and V_B, the voltage of the C output is V_C, and the memristors' M_1 and M_2 resistances are R_{M1} and R_{M2}, respectively. The simulation outcome for the Three-terminal Memristor "or" gate circuit is displayed in Figure 7. The relationship between the input and output voltages of the "or" gate circuit built by the three-terminal memristor is shown in Table 3.

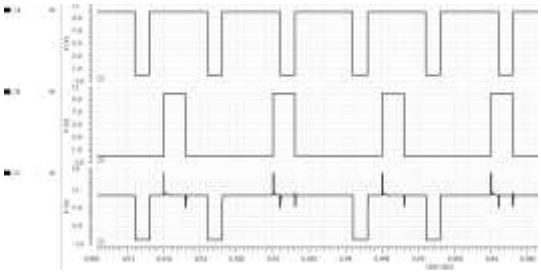


Fig.8. Simulation results of Three-terminal memristor "or" gate circuit

Table3. Three-terminal memristor "or" gate input and output

V_A/V	V_B/V	V_C/V
0	0	0
0	10	10
10	0	10
10	10	10

A=B="0", C="1" when both A and B input high level 10V; C="0" in all other circumstances. The simulation findings and the with-gate logic are consistent.

Figure 8 depicts the amnestic logic "non" gate's circuit layout.

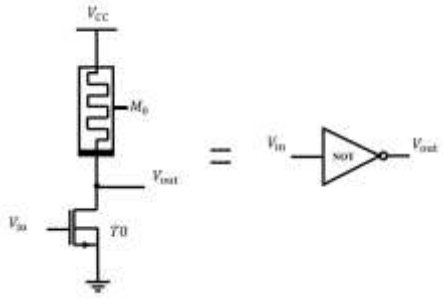


Fig.9. Three-terminal Memristor "non" gate circuit

The inverter circuit structure of the MOS tube is used by the logic "non" gate of the memristor. The "non" gate circuit is created by swapping out the fixed resistor in the inverter circuit for the memristor, which can be thought of as a variable resistor.

The CMOS tube's source is linked to ground, and the circuit pulls up the memristor M_0's positive side while connecting its negative side to the tube's drain. The drain voltage of the T_0 tube serves as the output Vout while the gate voltage of the "non" gate circuit serves as the input. The three-terminal memristor "non" gate circuit simulation result is shown in Figure 9. The working concept is similar to that of an inverter.

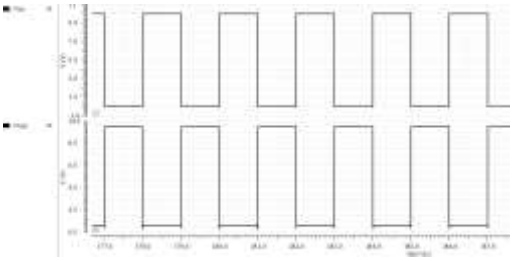


Fig.10. Simulation results of Three-terminal memristor "non" gate circuit

The vin and vout are reversed everywhere, as can be seen from the image, enabling the memristor circuit in Figure 8 to implement the logic "non" function proposed in this study.

The forward terminal of the memristor is pulled up while designing the memristor "non" gate circuit using a CMOS inverter circuit construction. The "non" gate depicted in Figure 8 is de-sourced because if the designed logic "non" gate is used to construct other circuit modules directly, the designed circuit will include a DC pull-up voltage source and additional logic circuits will be needed for synthesis, increasing the number of memristor. The circuit in Figure 8 can be improved by de-sourcing to obtain the source-free "non" gate circuit in Figure 10.

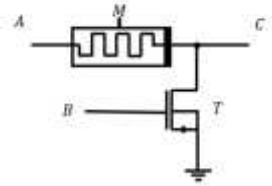


Fig.11. Three-terminal Memristor "non" gate circuit after de-sourcing

The A and B terminals are used as inputs and the C terminal is an output terminal. A high level of 10V means logic "1" and a low level of 0V means logic "0". Assume that the voltage at the input of A and B are, respectively, and the voltage at the output of C is, the resistance of the memristor M is, and the drain resistance of the MOS tube is, the working principle is analyzed as follows:

① When the input voltage V_A = 0V, V_B = 0V, MOS tube cutoff, regardless of the previous M memristor value, the output

voltage V_C = 0V.

②When the input voltage V_A=10V and V_B=0V, the MOS tube is cut off, M is positively biased, R_M=R_{ON}, R_T>>R_{ON}, and the output voltage V_C=10V.

③When the input voltage V_A=0V, V_B=10V, MOS tube is on, M is reverse biased, R_M=R_{OFF}, R_{OFF}>>R_T, and the output voltage V_C=0V.

④When the input voltage V_A=10V, V_B=10V, MOS tube is on, M is reverse biased, R_M=R_{OFF}, R_{OFF}>>R_T, and output voltage V_C=0V.

Input a square wave signal with a high level of 10V, a low level of 0V, a period of 10 μs and a pulse width of 3 μs to terminal A of this circuit, and input a square wave signal with a high level of 10V, a low level of 0V, a period of 20 μs and a pulse width of 4 μs to terminal B. The simulation results are shown in Figure11.

The input signal at A and B are both square wave signals with amplitude 10V, but the difference is that the pulse width at A is 3us and the period is 10us, while the pulse width at B is 4us and the period is 20us.

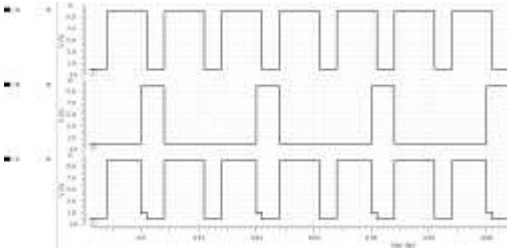


Fig.12. Simulation results of Three-terminal memristor "non" gate circuit after de-sourcing

Table4.Three-terminal memristor "non" gate circuit after de-sourcing input and output voltage results

V_A/V	V_B/V	V_C/V
0	0	0
0	10	12μ
10	0	10
10	10	0.8

Three-terminal memristor logic's "xor" gate may be built using the "with," "or," and "non" gates that were previously created. Here is a quick explanation of the principle: Let A, B, and C be the three variables; the "x-or" operation relation indicates that there are.

$$C = A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B = (\overline{A} + \overline{B}) \cdot (A + B) \quad (8)$$

Based on this logic relationship, the Three-terminal memristor logic "xor" gate circuit can be designed, as shown in Figure 12.

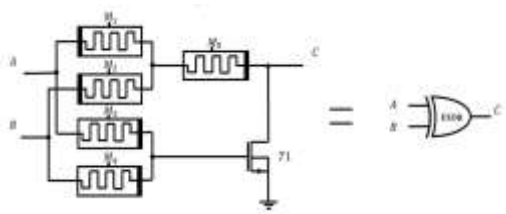


Fig.13.Three-terminal memristor "xor" gate circuit

A and B serve as the inputs, M_1–M_5 as the Three-terminal memristors, T1 as the MOS transistor, and C as the output. The "xor" gate logic connection may be used to characterize the logic function as "same as 0, different as 1". Figure 13 displays the simulation results. The relationship between the input and output voltages of the "xor" gate circuit built by the three-terminal memristor is shown in Table 4.

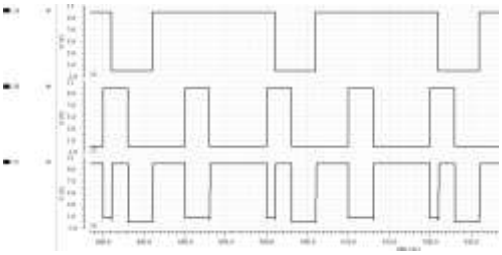


Fig.14.Simulation results of Three-terminal memristor "xor" gate circuit

Table5.Three-terminal memristor "xor" gate input and output voltage results

V_A/V	V_B/V	V_C/V
0	0	0
0	10	10
10	0	10
10	10	0

The graphic shows that when levels of the same kinds are input to A and B, C="0," and when levels of different kinds are supplied to A and B, C="1." The memristor circuit depicted in Figure 12 may implement the logic "xor" function since the simulation result also matches the "xor" gate.

Ⅳ Construction of multiplication circuit with three-terminal memristor

A functional circuit that multiplies two uncorrelated analog

input signals is known as a multiplier. Integrated circuit design applications and digital logic circuits both often employ multiplication circuits at the moment. The size, power consumption, and speed of the multipliers used in particular digital signal processing system algorithms can have a significant impact on the cost, power consumption, and system execution time of the hardware system. One of the urgent circuit architectures is the multiplication circuit, which uses three-terminal memristors to produce fast speed and low power consumption.

Suppose that the two-bit binary multiplication circuit's inputs are represented by A_1, A_0, B_1, and B_0, while its outputs are represented by Y_3, Y_2, and Y_0. The input-output relationship of the multiplication circuit may be determined from a study of its working principal as follows.

$$\begin{aligned} Y_0 &= A_0 B_0 \\ Y_1 &= A_1 B_0 \oplus A_0 B_1 \\ Y_2 &= A_1 B_1 \oplus A_1 A_0 B_1 B_0 \\ Y_3 &= A_1 A_0 B_1 B_0 \end{aligned} \tag{9}$$

According to the result of equation(9), the logical framework of the multiplication circuit is shown in Figure 14 and the circuit diagram is shown in Figure 15.

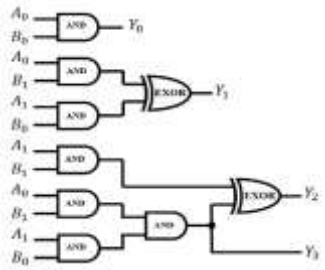


Fig.15.Multiplication circuit logic diagrams

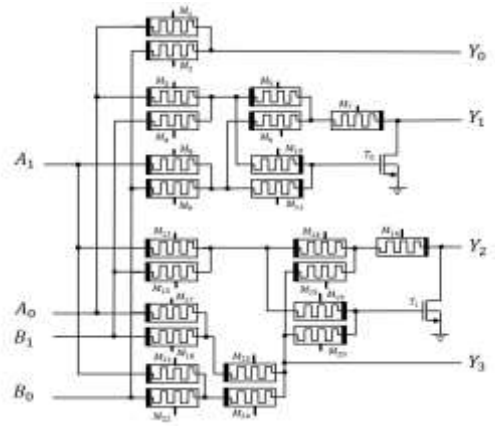


Fig.16.Three-terminal memristor multiplication circuit

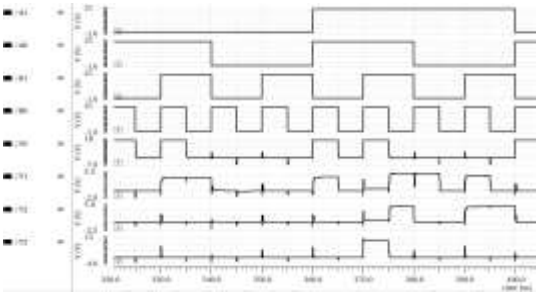


Fig.17.Simulation results of Three-terminal memristor multiplication circuit

In the multiplication circuit M_1-M_{24} represents the Three-terminal memristor selected in this paper, while T0 and T1 represent CMOS transistors. After the analog input signal is given, the simulation results are shown in Figure 15. From the figure, it can be seen that the input-output relationship conforms to equation (3) and meets the design requirements, and the circuit shown in Figure 14 can realize the multiplication circuit function.

A three-terminal memristor and transistor hybrid is used to create a two-bit binary multiplication circuit. Just 2 CMOS transistors and 24 memristors make up the straightforward multiplication circuit. As shown in Table 2, the number of transistors, memristors, and power consumption of two-bit binary multiplication circuits created using various techniques are compared.

Table 6 Comparison of multiplication circuits.

	Transistors	memristor	Electricity consumption/μW
Transistors	62	—	0.347
Literature[12]	50	22	1.09
Literature[13]	2	16	0.89
This paper	2	24	0.335

As can be seen in Table 6, the multiplication circuit designed in this paper has a greater advantage in terms of the number of transistors used compared to the other two multiplication circuits. Although the number of memristor elements used in this paper is more than that of the literature[12], in terms of component size and cost effectiveness, the memristor has a greater advantage over the process size and its manufacturing cost that can be achieved by current CMOS transistors, and at the same time the memristor is compatible with CMOS transistors[14].

This paper uses a larger number of memristor elements to

build the circuit than in the literature[13], because the stability of the circuit system and the efficiency of the signal transfer are taken into account, and because of the inconsistency of the chosen base memristor model circuit, the memristor circuit designed in this paper still has the advantage of power consumption, which can be used for other more complex circuit systems in logic applications. The proposed memristor circuit still has power consumption advantages and can provide operational benefits for other more complex circuit systems in logic applications.

Declarations

Ethical Approval

No ethical Approval required

Competing interests

This article has no competitive interest

Authors' contributions

Xianyan kuang presents the main research of this paper and the proposed circuit structure. Xianglan Huan performed the main simulation test and parameter adjustment of the circuit of the article, and Hongbiao Xiao analyzed and compared the simulation results of the circuit.

Funding

No funding.

Availability of data and materials

This paper uses the TSMC18rf process library as the basis for simulation testing on the candence software platform.

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