

# Modeling and Control of Three-Port DC/DC Converter Interface for Satellite Applications

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**Abstract**—This paper presents the control strategy and power management for an integrated three-port converter, which interfaces one solar input port, one bidirectional battery port, and an isolated output port. Multimode operations and multiloop designs are vital for such multiport converters. However, control design is difficult for a multiport converter to achieve multifunctional power management because of various cross-coupled control loops. Since there are various modes of operation, it is challenging to define different modes and to further implement autonomous mode transition based on the energy state of the three power ports. A competitive method is used to realize smooth and seamless mode transition. Multiport converter has plenty of interacting control loops due to integrated power trains. It is difficult to design close-loop controls without proper decoupling method. A detailed approach is provided utilizing state-space averaging method to obtain the converter model under different modes of operation, and then a decoupling network is introduced to allow separate controller designs. Simulation and experimental results verify the converter control design and power management during various operational modes.

**Index Terms**—DC–DC converters, digital control, mode transition, multi-input multi-output (MIMO), multiport, small-signal modeling, state-space averaging.

## I. INTRODUCTION

THE INTEGRATED multiport converter, instead of several independent converters, has advantages such as less component count and conversion stage because resources like switching devices and storage elements are shared in each switching period. As a result, the integrated system will have a lower overall mass and more compact packaging. In addition, some other advantages of integrated power converters are lower cost, improved reliability, and enhanced dynamic performance due to power stage integration and centralized control. Besides, it requires no communication capabilities that would be necessary for multiple converters. Therefore, the communication delay and error can be avoided with the centralized control structure. Instead of one control input for traditional

two-port converter, N-port converter has N-1 control inputs, which requires more modeling effort. Moreover, since the multiport converter has integrated power stage and, thus, multi-input multi-output (MIMO) feature, it necessitates proper decoupling for various control-loops design. Table I gives a comparison of the two different system structures.

Due to the advantages of multiport converter, recently there have been extensive researches that result in a wide variety of topologies. One simple approach is to interface several converter stages to a common dc bus with independent control for each converter stage. A multiinput boost-type converter [1] was designed for hybrid electric vehicles using such loose structure. But, it is widely accepted that an integrated topology specially tailored for multiport conversions will be more compact in size and lower in mass since switches and passive components are shared. A buck-based topology was used to interface spacecraft front-end power systems [3]. But the battery port is unidirectional and cannot be charged from solar port. Modeling of this converter was further discussed in [4], but plenty of interacting control loops were neither analyzed nor decoupled. A multiinput buck–boost-topology-based converter was proposed to accommodate various renewable sources [5]. But there is neither bidirectional port nor isolated power port to interface battery and comply with safety requirement for certain applications. A triple-voltage half-bridge topology is developed for automotive application in 14-V/42-V/high-voltage bus system [10], which has one isolated high-voltage port. Its power flow management is based on a combined duty ratio and phase shift control, and it can achieve soft-switching with four main switches, but soft-switching range is limited when the phase shifts between two very different voltage levels to have large current swing. Another half-bridge-based topology has also been proposed for vehicle application [18]. It has three fully isolated power ports, but utilizes six switches and many components, which is overqualified for our application that requires only one isolated port. Similarly, isolated-bidirectional multiport converters can also be constructed out of full-bridge topology for relatively high-power applications [19]–[23], since they apply full voltage to the transformer and adopt more switches to process power. But full-bridge-based topologies utilize a lot of switches with complicated driving and control circuitry that counteracts the size benefit of integrated topologies. Recently, a three-port topology with only one middle branch added to the traditional half-bridge converter has been reported in [16], which can achieve zero-voltage switching (ZVS) for all three main switches, adopts a high-frequency transformer to interface an isolated distribution bus, and has a

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TABLE I  
COMPARISON OF CONVENTIONAL STRUCTURE AND INTEGRATED STRUCTURE

	Conventional multi-converter structure	Integrated multi-port structure
Conversion stage	more than one	one
Component count	high	low
Overall mass	high	low
Control design	conventional and well-known	complicated and little-reported
Control structure	separated (require communication)	centralized (no communication)
Control input	one	N-1
Control loop decoupling	not required	necessary

\*N denotes the port numbers of N-port integrated converter.

bidirectional port to interface battery. To sum up, the multiport topologies can be classified into two categories: nonisolated topologies [1]–[9] and isolated topologies [10]–[23]. Nonisolated multiport converters usually take the form of buck, boost, buck–boost, etc., featuring compact design and high-power density; isolated multiport converters using bridge topologies have the advantages of flexible voltage levels and high efficiency since high-frequency transformer and soft-switching techniques are used; besides, isolation may be required for certain critical applications.

However, most reports focus on converter’s open-loop operation and lack of investigation on control strategy such as system-level power management for different operational modes and various interacting control-loops’ design, which are unique features of multiport converters and difficult to be dealt with. Therefore, it is interesting to solve problems like how to deal with different operational modes and let them transit between each other smoothly and seamlessly, and how to decouple control loops and design optimized compensators to minimize interactions of the MIMO converter system.

This paper is organized as follows. Section II introduces three-port converter’s principle of operation, which includes three parts: 1) four stages in satellite’s one-orbit cycle to generate two basic modes of operation; 2) system control structure to realize various control loops while achieving maximum power-point tracking (MPPT) for solar panel, battery charge control for battery, and bus regulation for output port; 3) an alternative approach to achieve autonomous mode transitions through a minimum function competition instead of complicated judgment-based algorithms. Section III utilizes state-space averaging method to derive three-port converter’s small-signal model under all operational modes. Then, the small-signal model is compared to circuit model to verify its effectiveness. Because multiport system contains multiple interacting control variables, one decoupling network is introduced to enable separate controller designs. In Section IV, experimental results for mode transitions are provided with a 200-W prototype, bode plots of various control loops are measured and compared to simulation results, load step tests show three different ports’ transient response, and at last, the system operation imitating different conditions in satellite’s one-orbit cycle is carried out to prove the validity of design concept for space application. Section V offers the conclusion.

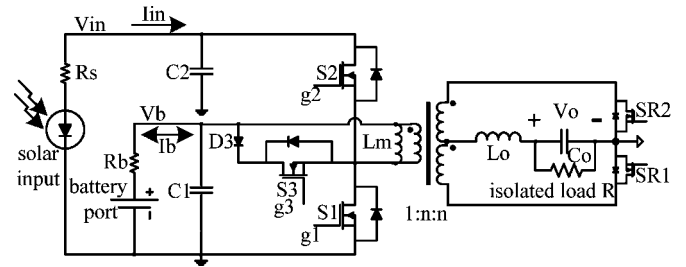


Fig. 1. Three-port modified half-bridge converter topology, which can achieve ZVS for all three main switches (S1, S2, and S3) and adopt synchronous rectification for the secondary side to minimize conduction loss.

## II. PRINCIPLE OF OPERATION

This section introduces the three-port topology and control structure. As shown in Fig. 1, it is a modified version of pulsewidth-modulated (PWM) half-bridge converter that includes three basic circuit stages within a constant-frequency switching cycle to provide two independent control variables, namely, duty-cycles  $d_1$  and  $d_2$  that are used to control S1 and S2, respectively. This allows tight control over two of the converter ports, while the third port provides the power balance in the system. The switching sequence ensures a clamping path for the energy of the leakage inductance of the transformer at all times. This energy is further utilized to achieve ZVS for all primary switches for a wide range of source and load conditions. The circuit operation and dc analysis have been reported in [16], and detailed ZVS analysis can be found in [28].

### A. Operational Modes

Having different operational modes is one of the unique features for three-port converters. As illustrated in Fig. 2, orbital satellite’s power platform experiences periods of insolation and eclipse during each orbit cycle, with insolation period being longer. Since MPPT can notably boost solar energy extraction of a photovoltaic (PV) system, the longer insolation period means that MPPT is more often operated to allow a smaller solar array while managing the same amount of load. Two assumptions are made to simplify the analysis: 1) load power is assumed to be constant and 2) battery overdischarge is ignored because PV arrays and batteries are typically oversized in satellites to provide

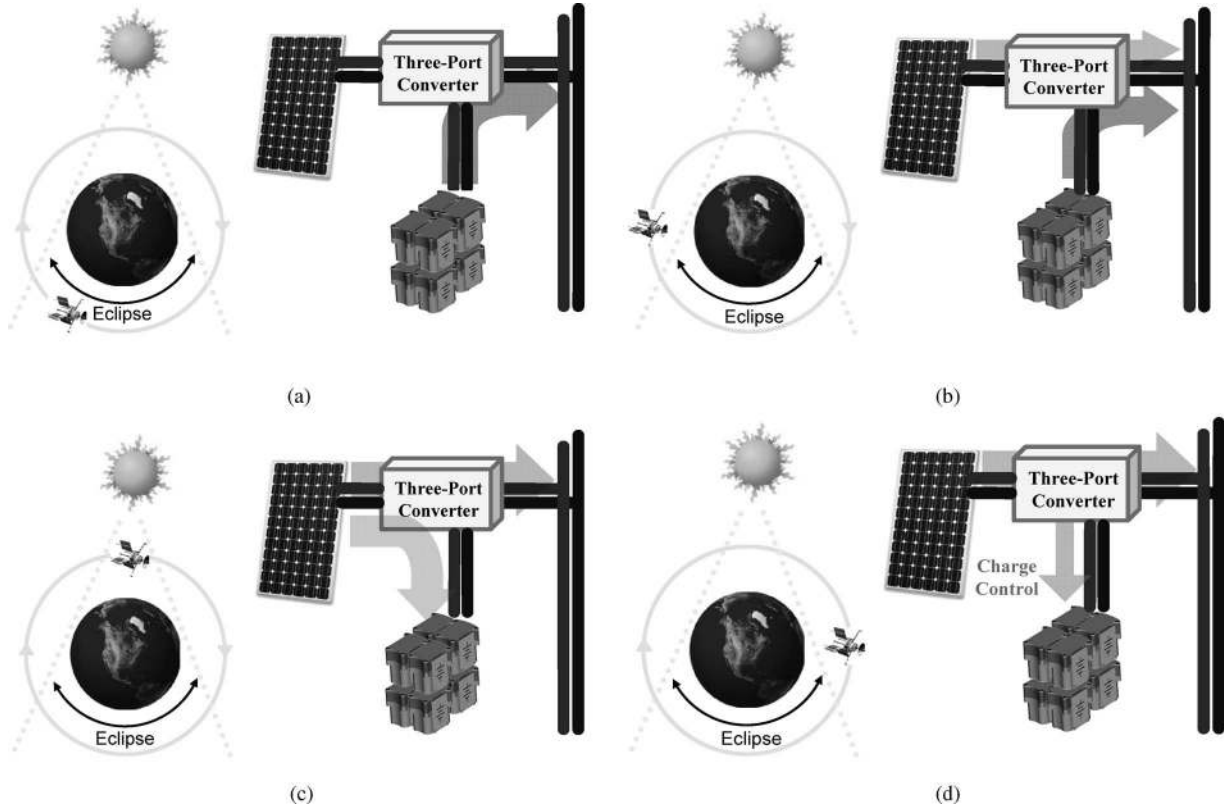


Fig. 2. Different operational modes in satellite’s one-orbit cycle. Three-port converter can achieve MPPT, battery charge control, and load regulation depending on available solar power, battery state of charge, and load profile. In stage I, battery acts as the exclusive source during eclipse period. In stages II and III, solar power is maximized to decrease battery state of discharge in stage II for initial insolation period, and then to increase battery state of charge in stage III for increased insolation period. In stage IV, battery charge control is applied to prevent battery overcharging and extend battery service life. (a) Stage I operation (eclipse period). (b) Stage II operation (initial insolation). (c) Stage III operation (increased insolation). (d) Stage IV operation (battery charge control).

some safety margins. Four stages in satellite’s one-orbit cycle yield two basic operational modes as follows.

In battery-balanced mode (mode 1), the load voltage is tightly regulated, and the solar panel operates under MPPT control to provide maximum power. The battery preserves the power balance for the system by storing unconsumed solar power or providing the deficit during high-load intervals. Therefore, the solar array can be scaled to provide average load power, while the battery provides the deficit during peak power of load, which is attracting to reduce solar array mass.

In battery-regulation mode (mode 2), the load is regulated and sinks less power than is available, while the battery charge rate is controlled to prevent overcharging. This mode stops to start mode 1 when the load increases beyond available solar power, i.e., battery parameter falls below either maximum voltage setting or maximum current setting.

**B. Control Structure**

The multiobjective control architecture that aims to regulate different power ports is shown in Fig. 3, control loops are named as follows: input voltage regulation (IVR), output voltage regulation (OVR), battery voltage regulation (BVR), and battery current regulation (BCR).

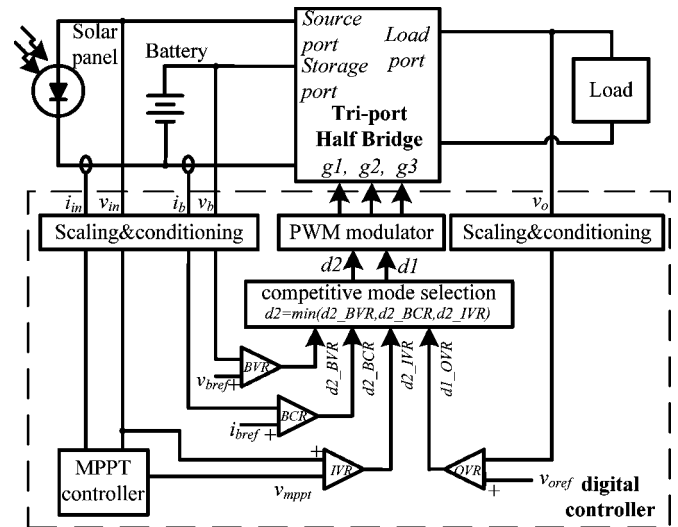


Fig. 3. Three-port converter’s control architecture to achieve MPPT for solar port, battery charge control for battery port, and meanwhile, always maintaining voltage regulation for output port. OVR is to control  $d_1$ , and the rest of control loops (BVR, BCR, and IVR) are competing the minimum value to control  $d_2$ .

The output-port loop is simply a voltage-mode control loop, closed around the load voltage, and duty cycle  $d_1$  is used as its control input. According to the dc circuit equation

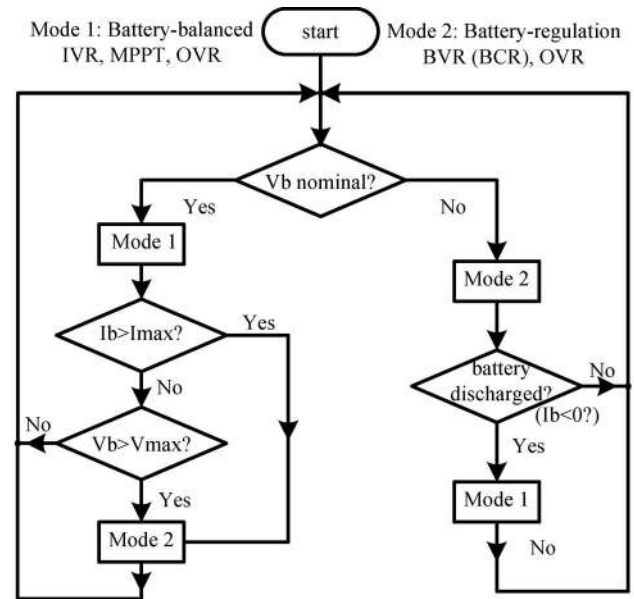
$V_o = 2V_b D_1 n$ , output voltage  $V_o$  can only be controlled by  $d_1$ , since battery voltage  $V_b$  is almost constant and transformer turn's ratio  $n$  is fixed. As a result,  $d_2$  is assigned to control either input port or battery port.

The IVR loop is used to regulate the solar panel voltage to its reference value. The reference is provided by an MPPT controller [29] using perturb and observe algorithm, and represents an estimate of the optimal operating voltage, duty cycle  $d_2$  is used as the control input when realizing the IVR loop. Otherwise,  $d_2$  can be decided by battery control loop that has two controllers: BVR and BCR. It should be mentioned that BCR is used to prevent battery overcurrent, and therefore, it can be considered as a protection function. Under normal operation, only one of two loops (IVR or BVR) will be active depending on the battery state of charge. Therefore, whether  $d_2$  is commanded by IVR, BVR, or BCR depends on the mode it is in.

### C. Autonomous Mode Transitions

The mode of operation is determined according to the present operating conditions such as available solar power, battery state of charge, and load profile. Fig. 4(a) gives flow chart for traditional mode transition algorithm. Mode 1 will be the default mode, where converter will spend most of the time. Mode 1 is desirable because it enables maximum solar power input. When the converter is in mode 1, controller will continually check the battery parameter, and then switch to mode 2 if the maximum setting voltage or current is reached. Once the converter is in mode 2, it stays there until load increases beyond available power. Although this algorithm is straightforward, without careful design of mode transitions, system oscillation will occur due to duty cycle's instant change. In a simulation, as shown in Fig. 4(b), when battery voltage reaches its maximum setting  $V_{b_{max}}$ , it switches to mode 2 suddenly, i.e.,  $d_2$  is switched from a nominal value to  $d_{2\_BVR}$ , which is saturating at that moment, causing a battery voltage spike. But when the spike of  $V_b$  reduces below  $V_{b_{max}}$ , it will force the converter to switch back to mode 1 and cause  $d_2$  another step change to introduce another voltage spike, and thus, this process continues for a long time. Besides, small battery voltage spike can cause huge current spike, which is usually large enough to break the circuit because of small battery internal resistance.

In order to avoid the sudden transition between modes, the autonomous mode transition is proposed in a competitive manner, as shown in Fig. 5. BVR, BCR, and IVR run in parallel to compete for minimum value in order to win control over  $d_2$ . Again, BCR will not be active during normal operation. Therefore, battery control is mainly BVR-loop operation. For example, when converter is in mode 1 with MPPT to maximize solar power,  $d_2$  will be determined by IVR loop, while BVR output is saturated at its upper limit because battery voltage does not reach its maximum setting. BVR will start to take control over  $d_2$  when battery maximum setting  $V_{b_{max}}$  is reached and BVR output goes down to win the minimum function. It should be noted that if IVR loop loses control, MPPT function needs to be disabled accordingly because of MPPT algorithm's inherent noise issue [33]. The experimental results in Section VI demonstrate that this method



(a)



(b)

Fig. 4. (a) Conventional mode transition algorithm flow chart that is inclined to cause oscillation. (b) Oscillation between modes 1 and 2 because of instant switching of duty-cycle value.

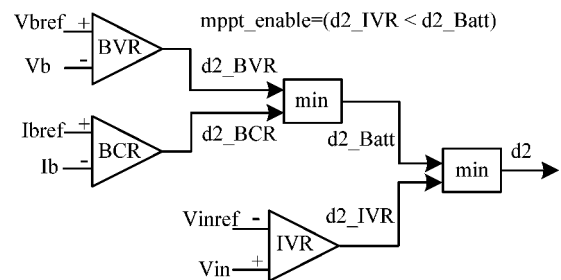


Fig. 5. Proposed minimum function competitive method to allow smooth transition of modes.

can achieve smooth and seamless transition between different modes.

### III. MODELING AND CONTROL DESIGN

Small-signal model is the basis for optimized controller design. Especially for such a complicated MIMO system of

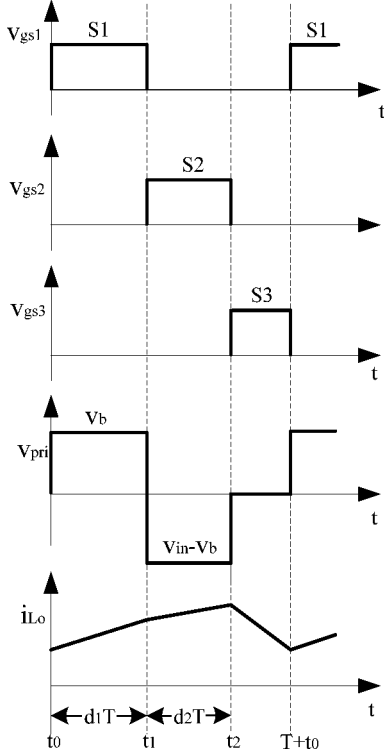


Fig. 6. Basic waveforms of the three-port converter. Variables  $v_{pri}$  and  $i_{L_o}$  represent transformer primary-side voltage and output inductor current, respectively.

three-port converter, an effective model will be helpful to realize closed-loop control, and furthermore, to optimize the converter dynamics. Since there are two modes of operation for the three-port converter, small-signal models in both modes need to be obtained separately. Unlike conventional two-port converter, multiport converter is a high-order system, and the symbolic derivation of these plant transfer functions is fairly tedious; therefore, it is difficult to obtain values of poles and zeros for analysis. Alternatively, the dynamics of the plant can be described in a matrix form; therefore, computer software is used to plot the Bode graph of different transfer functions. A common problem about MIMO system is the existence of various interacting control loops that complicate compensator designs; therefore, a decoupling network is introduced to allow separate controller designs for each of the three power port.

### A. Three-Port Converter Modeling During Battery-Regulation Mode

Before deriving for small-signal transfer functions of the converter, state equations for four energy storage element during each circuit stage are developed. For battery-regulation mode, these include the battery capacitor  $C_1$ , the transformer magnetizing inductance  $L_m$ , the output inductance  $L_o$ , and the output capacitance  $C_o$ . There are three main circuit stages, as illustrated in Fig. 6.

*Stage I ( $t_0-t_1$ ):* In stage I, S1 is gated ON, applying a positive voltage to the transformer primary side, while output inductor is charging. Synchronous Switch SR1 is gated ON to allow current flow through output inductor  $L_o$ . Current of battery-port filter capacitor is equal to the sum of battery current, transformer magnetizing inductor current, and reflected secondary-side current. The state equation in this stage is as follows:

$$\begin{cases} \frac{C_1 dv_{C_1}}{dt} = \frac{-v_{C_1}}{R_b} + i_{L_m} - ni_{L_o} \\ \frac{L_m di_{L_m}}{dt} = -v_{C_1} \\ \frac{L_o di_{L_o}}{dt} = v_{C_1} n - v_o \\ \frac{C_o dv_o}{dt} = i_{L_o} - \frac{v_o}{R} \end{cases} \quad (1)$$

*Stage II ( $t_1-t_2$ ):* In stage II, S2 is gated ON, a negative voltage is applied to the transformer primary side, and output inductor is still charging. Synchronous switch SR2 is gated ON to allow a current flow path through  $L_o$ . The transformer primary voltage is the input voltage that subtracts battery voltage, and thus, output inductor charging rate changes accordingly. The state equation in this stage is as follows:

$$\begin{cases} \frac{C_1 dv_{C_1}}{dt} = \frac{-v_{C_1}}{R_b} + i_{L_m} + ni_{L_o} \\ \frac{L_m di_{L_m}}{dt} = v_{C_2} - v_{C_1} \\ \frac{L_o di_{L_o}}{dt} = (v_{C_2} - v_{C_1})n - v_o \\ \frac{C_o dv_o}{dt} = i_{L_o} - \frac{v_o}{R} \end{cases} \quad (2)$$

*Stage III ( $t_2-T+t_0$ ):* In stage III, S3 is gated ON, zero voltage is applied to the transformer primary side due to middle branch (S3 and D3 path)'s clamping, and output inductor is discharging. This allows both the magnetizing and output inductor currents to free-wheel. Both SR1 and SR2 are turned on, thus output inductor current distributes into both of rectifying paths. The state equation in this stage is as follows:

$$\begin{cases} \frac{C_1 dv_{C_1}}{dt} = \frac{-v_{C_1}}{R_b} \\ \frac{L_m di_{L_m}}{dt} = 0 \\ \frac{L_o di_{L_o}}{dt} = -v_o \\ \frac{C_o dv_o}{dt} = i_{L_o} - \frac{v_o}{R} \end{cases} \quad (3)$$

Before we perform the averaging to three different state equations, we consider that the state variables have a perturbation  $\hat{x}$

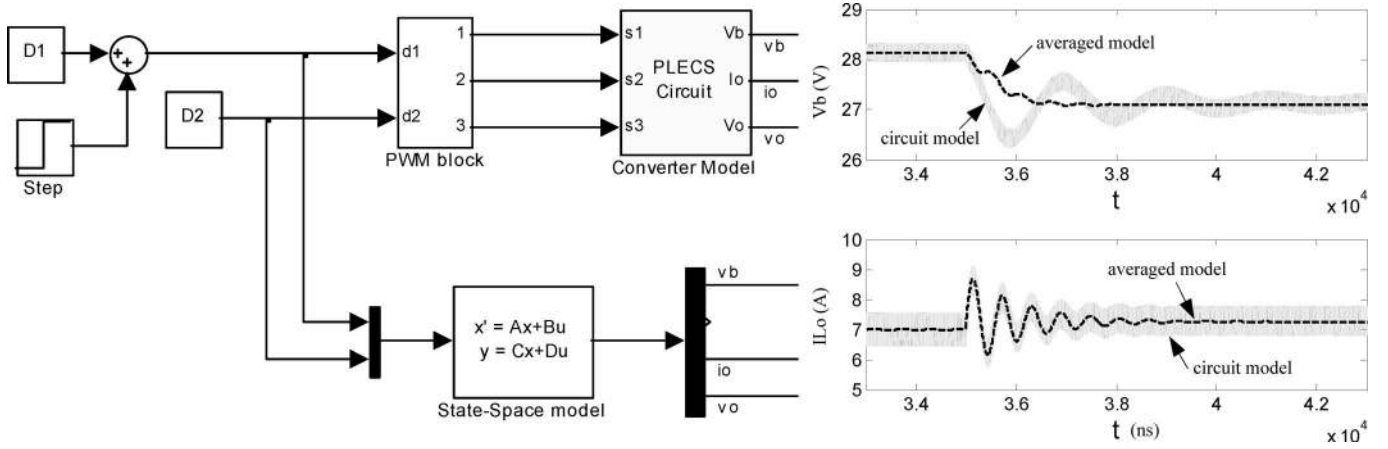


Fig. 7. (a) Model comparison due to duty-cycle step. (b) Averaged model and circuit model comparison for battery-regulation mode.

superimposed to the dc value  $X$

$$x = X + \hat{x} \quad (4)$$

And similarly,  $d = D + \hat{d}$  and  $v = V + \hat{v}$ .

To obtain the small-signal model, we assume that the perturbations are small, i.e.,  $\hat{d} \ll D$ ,  $\hat{v} \ll V$ , etc. We also assume that the perturbations do not vary significantly during one switching period, which means that the dynamic models that will be obtained are valid for frequencies much smaller than the switching frequency. If we substitute (4) into (1)–(3), apply the averaging to three state equations multiplied with corresponding duty-cycle value, and then, neglect second-order terms, we obtain small-signal equations that are demonstrated as follows:

$$\begin{cases} \frac{C_1 d\hat{v}_{C_1}}{dt} = \frac{-\hat{v}_{C_1} C_1}{R_b} + \hat{i}_{L_m} (D_1 + D_2) + n \cdot \hat{i}_{L_o} \\ \quad (D_2 - D_1) + I_{L_m} \cdot (\hat{d}_1 + \hat{d}_2) + \frac{nV_o(\hat{d}_2 - \hat{d}_1)}{R} \\ \frac{L_m d\hat{i}_{L_m}}{dt} = -\hat{v}_{C_1} (D_1 + D_2) - \frac{(\hat{d}_1 + \hat{d}_2) D_2 V_{in}}{(D_1 + D_2)} + \hat{d}_2 V_{in} \\ \frac{L_o d\hat{i}_{L_o}}{dt} = \hat{v}_{C_1} n(D_1 - D_2) - \hat{v}_o + \frac{(\hat{d}_1 - \hat{d}_2) n D_2 V_{in}}{(D_1 + D_2)} + \hat{d}_2 n V_{in} \\ \frac{C_o d\hat{v}_o}{dt} = \hat{i}_{L_o} - \frac{\hat{v}_o}{R} \end{cases} \quad (5)$$

Therefore, the system can be represented in a matrix form using a state-space model after converting (5) into frequency domain. The state-space model takes the following form:

$$\frac{dX}{dt} = AX + BU \quad Y = IX \quad (6)$$

where  $X$  is a matrix containing the state variables  $v_{C_1}$ ,  $i_{L_m}$ ,  $i_{L_o}$ , and  $v_o$ ,  $U$  is a matrix containing the control inputs  $d_1$  and  $d_2$ ,  $Y$  is a matrix containing the system outputs, and  $I$  is the identity matrix. For this model, the four state variables are also the system outputs. Filling in the  $A$  and  $B$  matrices using the state

equations gives the following result:

$$A = \begin{bmatrix} -\frac{1}{R_b C_1} & \frac{(D_1 + D_2)}{C_1} & \frac{n(D_2 - D_1)}{C_1} & 0 \\ -\frac{(D_1 + D_2)}{L_m} & 0 & 0 & 0 \\ \frac{n(D_1 - D_2)}{L_o} & 0 & 0 & -\frac{1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix}$$

$$X = \begin{bmatrix} \hat{v}_{C_1} \\ \hat{i}_{L_m} \\ \hat{i}_{L_o} \\ \hat{v}_o \end{bmatrix} \quad B = \begin{bmatrix} \frac{I_{L_m} - nV_o/R}{C_1} & \frac{I_{L_m} + nV_o/R}{C_1} \\ -\frac{D_2 V_{in}}{(D_1 + D_2) L_m} & \frac{D_1 V_{in}}{(D_1 + D_2) L_m} \\ \frac{nD_2 V_{in}}{(D_1 + D_2) L_o} & \frac{nD_1 V_{in}}{(D_1 + D_2) L_o} \\ 0 & 0 \end{bmatrix}$$

$$U = \begin{bmatrix} d_1 \\ d_2 \end{bmatrix} \quad (7)$$

In order to verify the derived state-space averaged model, MATLAB's Simulink is used to compare the averaged model at the bottom with the actual switching converter model on the top, as shown in Fig. 7(a). The converter model is realized by actual switches and passive components, while the averaged model is expressed by state-space matrices such as  $A$  and  $B$ . Then a small-signal perturbation in the form of a small step change is applied to one of the duty cycles. Fig. 7(b) shows that the averaged model correctly approximates the battery voltage and output inductor current for battery-regulation mode.

The feedback control loops of OVR and BVR are then designed based on the state-space models. Using the model, transfer functions for output and battery voltage to different duty-cycle values can be extracted according to the small-signal

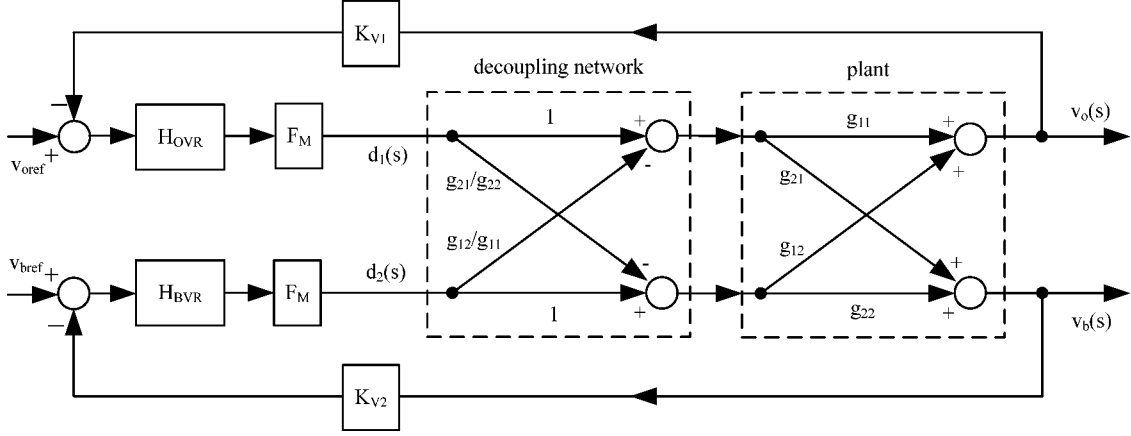


Fig. 8. Small-signal model of battery-regulation mode, control inputs and outputs are decoupled to enable separate controller design.  $V_{oref}$  and  $V_{bref}$  are the references for output voltage and battery voltage, respectively.  $H_{OVR}$  and  $H_{BVR}$  are the compensators that need to be designed.

diagram shown in Fig. 8. For example,  $G(s)(4, 1)$  represents the fourth state variable  $V_o$  and the first control variable  $d_1$ , which, thus, equals to open-loop transfer function of  $V_o/d_1$ . Therefore, the row number denotes the sequence of state variable, and column number denotes that of control input. The values such as  $g_{11}$  and  $g_{12}$  are not expressed because the symbolic derivation of these transfer functions is fairly tedious. Alternatively, a computer software like MATLAB can be used to calculate the desired transfer functions, and then plot out the Bode plots for analysis in the frequency domain as

$$G(s) = (sI - A)^{-1} B$$

$$\frac{v_o}{d_1} = g_{11} = G(s)(4, 1) \quad \frac{v_b}{d_1} = g_{21} = G(s)(1, 1)$$

$$\frac{v_o}{d_2} = g_{12} = G(s)(4, 2) \quad \frac{v_b}{d_2} = g_{22} = G(s)(1, 2). \quad (8)$$

In Fig. 8, PWM modulator gain  $F_M$  is calculated using the following equation:

$$F_M = \frac{2^M f_s}{f_{PWMclock}}. \quad (9)$$

Where  $f_{PWMclock}$  is the clock frequency of the PWM counter,  $f_s$  is the switching frequency, and  $M$  is chosen to allow the logical value in the compare register of the PWM to be between 0 and 1.

The gains  $K_{v1}$  and  $K_{v2}$  actually take into account both sensing gain and analog-to-digital conversion gain, and the latter is dependent on the resolution of the analog-to-digital converter.

As mentioned earlier, it is difficult to design close-loop compensators for each control loop without proper decoupling method. Therefore, a decoupling network, as in Fig. 8, is introduced so that the control loops can be designed independently with different bandwidth requirement. Since output-port voltage regulation requirement is the stringiest of the three and battery characteristics are relatively slower, the BVR loop is designed to have a one decade lower bandwidth than that of OVR. The derivation of decoupling network  $G^*$  is described as follows. The state vector matrix  $X$  can be written as  $X = GU^*$ , where

$U^*$  is the modified input vector made up of duty cycles  $U$ ,  $U^* = G^*U$ . Therefore,  $X = GG^*U$ . According to the modern control theory, our goal is to make  $GG^*$  a diagonal matrix to allow one control input to determine one output independently. Therefore, based on  $G^* = XU^{-1}G^{-1}$ ,  $G^*$  can be derived and simplified as

$$G^* = \begin{bmatrix} 1 & -g_{12}/g_{11} \\ -g_{21}/g_{22} & 1 \end{bmatrix}. \quad (10)$$

Since  $g_{11}$  and  $g_{21}$  are already known, the OVR controller can then be designed with the following equation:

$$v_o(s)/d_1(s) = g_{11} - g_{12} \cdot g_{21}/g_{22}. \quad (11)$$

Similarly, the BVR-loop design utilizes the BVR-loop equation

$$v_b(s)/d_2(s) = g_{22} - g_{12} \cdot g_{21}/g_{11}. \quad (12)$$

With the open-loop control objects of  $v_o(s)/d_1(s)$  and  $v_b(s)/d_2(s)$  are available, now it is possible to explore the close-loop compensators design. In order to design OVR-loop compensator  $H_{OVR}$  so that a stable and high-bandwidth output-loop gain can be obtained, the open Bode plot of OVR loop before compensation has been plotted in Fig. 9(a). The Bode shape implies that it has two main poles at around  $L_oC_o$  resonance, which causes a  $-40$  dB/decade slope. Therefore, the design objective is to boost up the low-frequency gain to minimize steady-state error and make it pass 0 dB line at  $-20$  dB/decade slope, while maintaining a sufficient phase margin. A tradition PI controller will be able to handle this, but if two poles are close to cause sharp phase drop as in this case, a PID controller is recommended to boost up the phase. After compensation, the crossover frequency for the OVR loop is set at 4.1 kHz with a phase margin of  $78^\circ$ .  $H_{OVR}$  takes the following form:

$$H_{OVR} = 80(s/2\pi \cdot 400 + 1)(s/2\pi \cdot 800 + 1) \times /s/(s/2\pi \cdot 4000 + 1)/(s/2\pi \cdot 4000 + 1). \quad (13)$$

For the BVR loop, as shown in Fig. 9(b), the open-loop Bode also shows a two-main-pole feature that is easy to compensate,

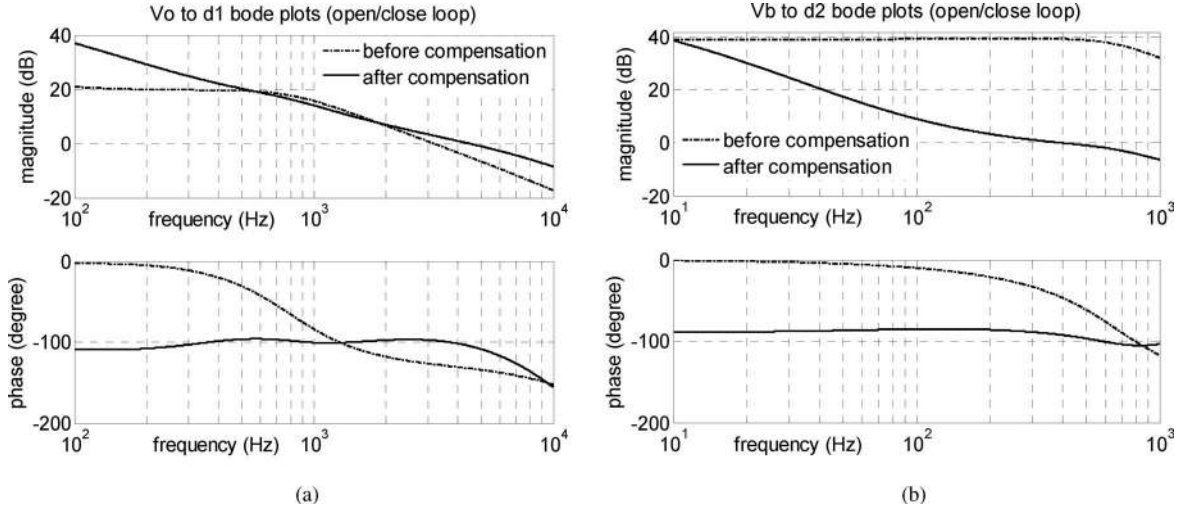


Fig. 9. Simulated Bode plots for battery-regulation mode. (a)  $v_o(s)/d_1(s)$ . (b)  $v_b(s)/d_2(s)$ . Dashed line denotes open-loop plant transfer function before applying the compensator, solid line denotes close-loop transfer function after applying the compensator. BVR-loop bandwidth is set to be one-tenth of that of OVR.

but in order to comply with the bandwidth assumption that is one decade lower than OVR loop, a low-gain PI controller is adopted to deliberately shape it to cross 0 dB line at the desired frequency range, and the pole will be placed in front of zero to force a sharp drop of the gain curve, but it should be noted that phase margin should be sufficiently large to allow this kind of zero-pole placement. If one set of zero and pole is not enough, two sets of zero and pole (PID controller) may be utilized. The crossover frequency of the BVR loop is set at 390 Hz, and phase margin of BVR is set at  $88^\circ$ . The compensator of  $H_{BVR}$  used is as follows:

$$H_{BVR} = 0.7(s/2\pi \cdot 1000 + 1)(s/2\pi \cdot 1000 + 1) \times /s/(s/2\pi \cdot 200 + 1)/(s/2\pi \cdot 300 + 1). \quad (14)$$

### B. Three-Port Converter Modeling During Battery-Balanced Mode

The same method is followed for battery-balanced mode. In this mode, the input-port voltage  $v_{C_2}$  is considered as a state variable instead of the battery-port voltage  $v_{C_1}$ . Averaged model is derived by state-space representation. The state matrix  $X$  contains the four state variables  $v_{C_2}$ ,  $i_{L_m}$ ,  $i_{L_o}$ , and  $v_o$ , and the input matrix  $U$  remains the two control variables  $d_1$  and  $d_2$ . The  $A$  and  $B$  matrices take the following form:

$$A = \begin{bmatrix} -\frac{1}{R_S C_2} & -\frac{D_2}{C_2} & -\frac{nD_2}{C_2} & 0 \\ \frac{D_2}{L_m} & 0 & 0 & 0 \\ \frac{nD_2}{L_o} & 0 & 0 & -\frac{1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix}, \quad X = \begin{bmatrix} \hat{v}_{C_2} \\ \hat{i}_{L_m} \\ \hat{i}_{L_o} \\ \hat{v}_o \end{bmatrix}$$

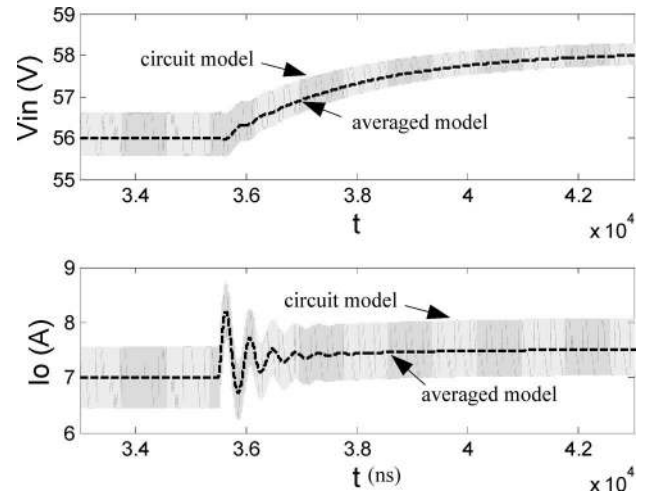


Fig. 10. Averaged model and circuit model comparison for battery-balanced mode.

$$B = \begin{bmatrix} 0 & -\frac{1}{C_2} (I_{L_m} + nV_o/R) \\ \frac{V_b}{L_m} & \frac{D_1 V_b}{D_2 L_m} \\ \frac{nV_b}{L_o} & \frac{nD_1 V_b}{D_2 L_o} \\ 0 & 0 \end{bmatrix}, \quad U = \begin{bmatrix} d_1 \\ d_2 \end{bmatrix}. \quad (15)$$

Again, it can be seen from Fig. 10 that the averaged model correctly approximates the input voltage and output current according to the simulation. Since matrices  $A$  and  $B$  are derived, transfer functions for output and input voltage to duty-cycle values can be extracted from the small-signal model, as shown in Fig. 11.

The same decoupling network is adopted here as the battery-regulation mode. In fact, the design of OVR is exactly the same,



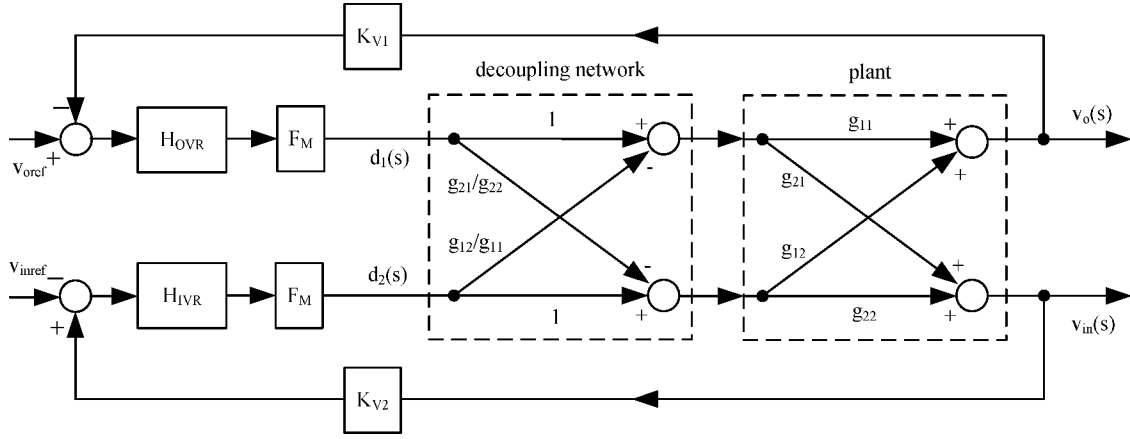


Fig. 11. Small-signal model of battery-balanced mode, control inputs and outputs are decoupled to enable separate controller design.  $V_{oref}$  and  $V_{inref}$  are the references for output voltage and input voltage, respectively.  $H_{OVR}$  and  $H_{IVR}$  are the compensators that need to be designed.

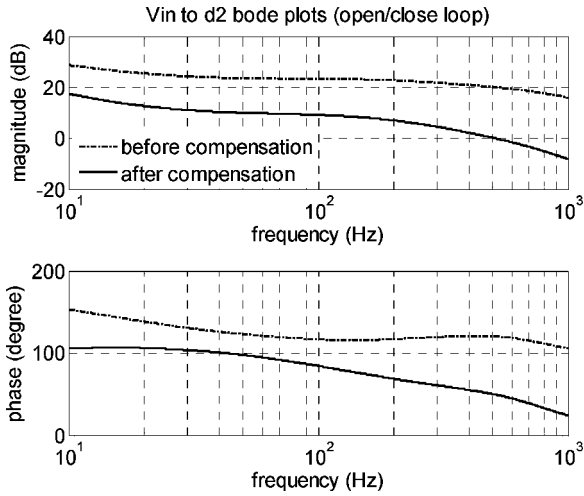


Fig. 12. Simulated Bode plots of  $v_{in}(s)/d_2(s)$ . Dashed line denotes open-loop plant transfer function before applying the compensator and solid line denotes close-loop transfer function after applying the compensator.

because no matter in which mode, the transfer function of  $v_o/d_1$  should be the same even though different approaches are applied, and therefore, Bode plot of  $v_o/d_1$  before and after compensation in this mode should be the same as the battery-regulation mode.

Then, according to  $v_{in}(s)/d_2(s) = g_{22} - g_{12}g_{21}/g_{11}$ . The  $v_{in}(s)/d_2(s)$  Bode plot before compensation is plotted in Fig. 12, which has high bandwidth and  $100^\circ$  of phase margin. IVR compensator  $H_{IVR}$  is then designed to enforce relatively low control-loop bandwidth with some phase drop. Therefore, a PI controller with extremely low gain, and one set of zero and pole is adopted to achieve this design goal. The bandwidth of IVR loop is designed at 500 Hz, which is about one decade lower than OVR bandwidth. The phase margin is set at  $61^\circ$  in this case

$$H_{IVR} = 0.08(s/2\pi \cdot 10 + 1)/s/(s/2\pi \cdot 200 + 1). \quad (16)$$

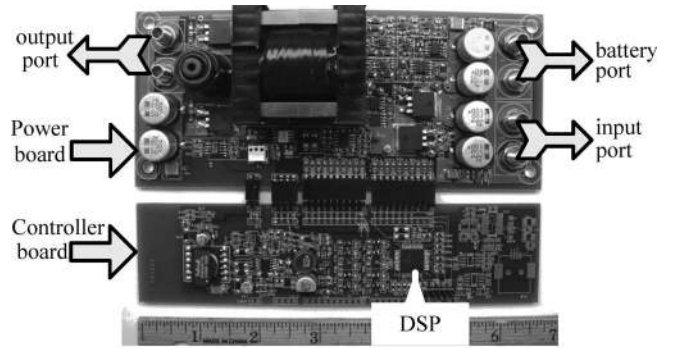


Fig. 13. Prototype photograph of three-port converter that consists of one controller board and one power board.

#### IV. EXPERIMENTAL RESULTS

The mode transition and control structure for both operational modes are tested through a 200-W prototype, as illustrated in Fig. 13. Power stage's input port, battery port, and output port are marked as in the prototype photograph. It consists of two boards: power stage board and controller board. All feedback control loops' compensators are implemented by a direct digital design method [27].

The values of circuit parameters used in the simulation and experimental circuit are listed in Table II.

Fig. 14(a) shows mode transition from battery-balanced mode (mode 1) to battery-regulation mode (mode 2) when battery maximum-voltage setting of 29 V is reached. Solar panel first works under IVR control with MPPT to maximize the solar power, then it is forced to operate in solar panel's voltage-source region when IVR loses control and BVR takes control over  $d_2$ ; therefore, the input port provides power balance after the transition into battery regulation mode. It can be seen that the transition of the proposed competitive method is smooth and causes no oscillation that is experienced with the sudden transition of duty cycles mentioned in Section IV. The battery voltage has 0.5 V overshoot, and input voltage has 2.5 V overshoot, both are within acceptable range according to specifications.

TABLE II  
VALUES OF CIRCUIT PARAMETERS

output inductor	$L_o$	65 $\mu\text{H}$	output voltage	$V_o$	28V
magnetizing inductor	$L_m$	45 $\mu\text{H}$	input voltage	$V_{in} (V_{c_2})$	60 V
output filter capacitor	$C_o$	680 $\mu\text{F}$	battery voltage	$V_b (V_{c_1})$	28 V
battery port filter capacitor	$C_1$	680 $\mu\text{F}$	input port filter capacitor	$C_2$	210 $\mu\text{F}$

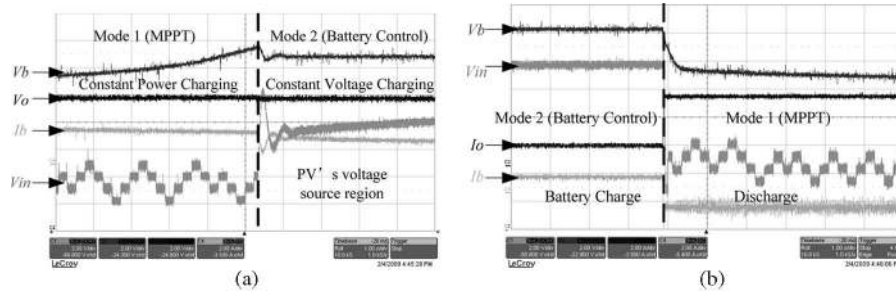


Fig. 14. Autonomous mode transition. (a) Mode 1–mode 2. (b) Mode 2–mode 1.

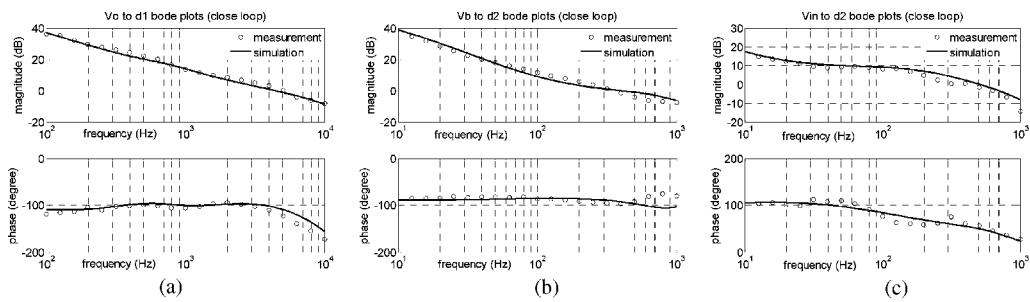


Fig. 15. Simulated and measured Bode plots. (a)  $V_o/d_1$ . (b)  $V_b/d_2$ . (c)  $V_{in}/d_2$ .

Fig. 14(b) gives mode 2 to mode 1 transition when load level suddenly increases to force the battery to source instead of sink. Since battery voltage setting cannot be met during discharging,  $d_2$  will be controlled by IVR since BVR quickly loses control, and solar panel quickly reacts to work under MPPT control so as to harvest maximum available solar power, and battery becomes to provide the power balance in mode 1.

Frequency analyzer is used to verify the control-loop design. Close-loop Bode plots of three control loops are tested, respectively, as shown in Fig. 15, and the dotted Bode plot measurement agree with the previous simulation in the form of solid lines.

Fig. 16(a) shows the input voltage, battery voltage, and output voltage response to a load step between 1 and 3 A in battery-regulation mode. Output voltage transient response of 500  $\mu\text{s}$  settling time is much faster than battery voltage settling time of 40 ms because OVR bandwidth is ten times larger than that of BVR. Input voltage changes according to load level changes because input port provides power balance. Fig. 16(b) demonstrates the system transient response in battery-balanced mode when MPPT is active. The load step is from 1 to 5 A. Input voltage response to load transient of 20 ms settling time is much slower than output voltage settling time of 500  $\mu\text{s}$  because IVR crossover frequency is set at one-tenth of that of OVR. Input voltage remains uninterrupted at around MPP, even during load changes, which is the unique feature of three-port con-

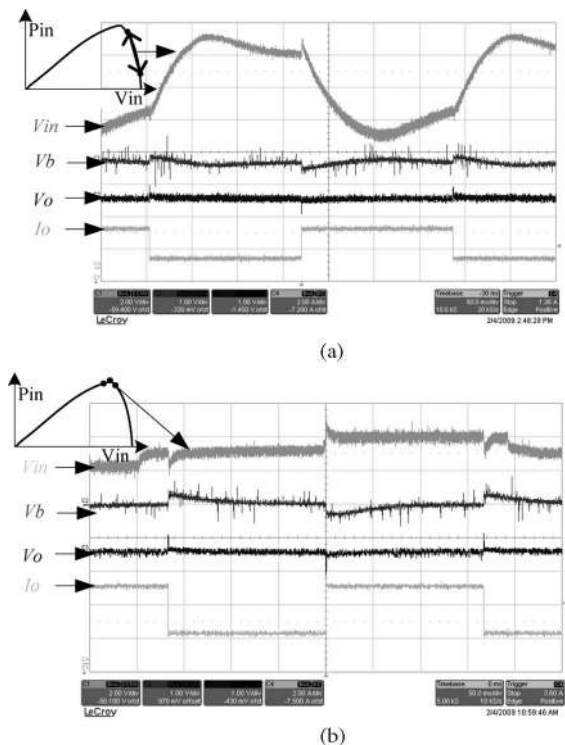


Fig. 16. (a) Battery-regulation-mode load step response. (b) Battery-balanced-mode load step response.

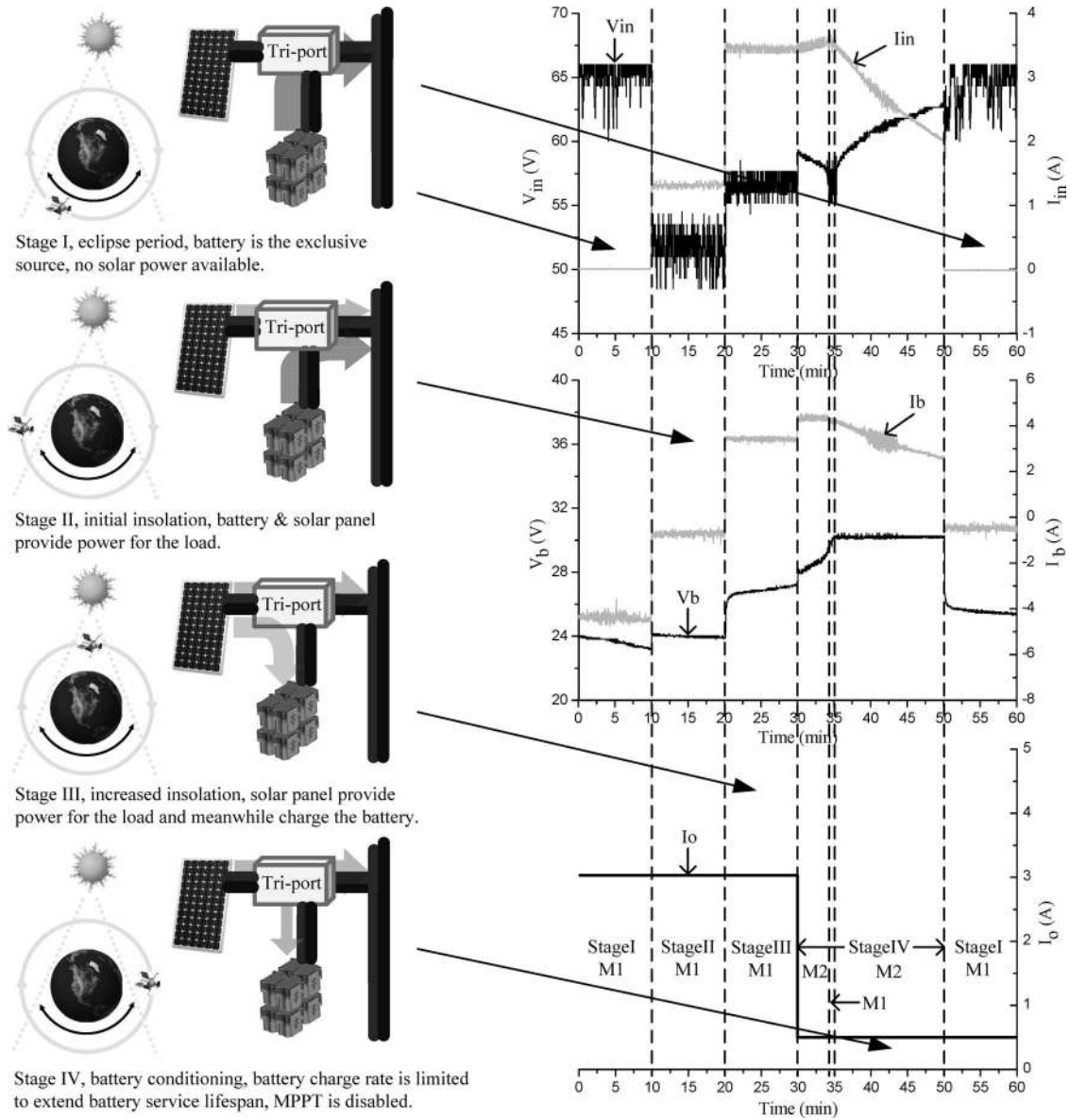


Fig. 17. Different mode operations based on available solar power, battery state of charge, and load profile; left column shows four stages in satellite’s one-orbit cycle; for the right column, top one shows input solar panel voltage and current, middle one represents battery voltage and current, and the bottom one shows output-port load level, while its voltage is regulated all the time.

verters, because MPPT and load regulation cannot be achieved simultaneously by conventional two-port converter.

Fig. 17 presents the typical experimental results of three different ports’ voltage and current imitating for satellite’s one-orbit cycle that includes four orbiting stages to verify the control design for space applications. The output voltage is regulated all the time, while output load level is commanded to change deliberately from 3 to 0.5 A to allow for mode transitions. As mentioned in Section II, in stage I of satellite cycling, no solar power is available due to eclipse, and therefore, input current  $I_{in}$  is zero and battery discharges to supply for full load. In stage II of initial insolation, solar panel operates in MPPT to maximize power input, but it is still not enough to support full load, and therefore, the battery still discharges, but with less discharging current, while  $I_{in}$  is 1.3 A. In stage III, solar in-

solation level increases, and solar power at this point not only supplies for full load, but also has extra power to charge the battery, meanwhile battery current  $I_b$  becomes positive. At the 30-min point, load requirement is suddenly reduced from 3 to 0.5 A. As a result, the power deficit goes to charge battery and triggers BCR to prevent overcurrent, and therefore, BCR takes control over  $d_2$  from previous IVR commanding, and MPPT is disabled accordingly. During this period (30–34 min), because input power and output power is fixed, battery power is fixed as well, more specifically, battery current reduces due to increase of battery voltage. So, it eventually goes out of current protection and BCR loses control when IVR takes control back over  $d_2$  again to operate in MPPT. Then, battery voltage setting is quickly reached, and BVR wins control over  $d_2$ , and thus, battery voltage is regulated, meanwhile  $I_b$  drops gradually.

When satellite enters into eclipse again, the system will go through another similar cycling period.

## V. CONCLUSION

The control strategy and modeling of the three-port dc/dc converter for satellite application that interfaces a solar input panel, a rechargeable battery port, and an isolated output port were presented in this paper. The converter has three circuit stages to allow two control inputs that are used to regulate two of the three ports. The output voltage is regulated at any given time, but either input port or battery port can be regulated depending on which is most urgently needed according to available solar power and battery state of charge. The control design for multiport converter is challenging and needs to manage power flow under various operating conditions. Therefore, the control strategy must be “powerful” and “intelligent” enough to realize complicated control tasks, and should have different operational mode transition control. A competitive method was utilized to realize autonomous mode transitions. Basically, there are no modes from controller point of view, which simplifies the control algorithm and avoids possible system oscillations due to elimination of instant duty-cycle value change. This paper also presented a general modeling procedure specially tailored for three-port converters. Since there are many control inputs and state variables for multiport converter, converter model derivation adopts matrix-based averaged state-space method. Moreover, the small-signal models for different operational modes were obtained separately, while the model derived for each mode includes two ports’ dynamic characteristics other than one for two-port converters. Then, a decoupling network was adopted to solve the problem of control-loop interdependence, so that each port can be treated as an independent subsystem. With proper decoupling, it is then possible to analyze each port’s control loop separately. Control-loop design examples in all operational modes were presented in detail. Operation of this converter for satellite application was experimentally verified using a 200-W prototype.

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