Modeling and Design for a Novel Adaptive Voltage Positioning (AVP) Scheme for Multiphase VRMs

Martin Lee, Dan Chen, *Fellow, IEEE*, Kevin Huang, Chih-Wen Liu, *Senior Member, IEEE*, and Ben Tai

***Abstract*—Adaptive voltage positioning (AVP) has been used in multiphase voltage regulator module (VRM) applications. A novel scheme, called AVP+, is analyzed in this paper. Small signal model is used to look into the control performance issues such as output impedance and stability. The model has been verified in the experiments and simulations. Compared to a conventional AVP schemes, the present scheme provides better stability margin and output-impedance performance. This is especially true for the prevailing trend of using ceramic output capacitors and high switching frequency. The focus of the present paper is the small-signal modeling for control loop design using the AVP+ scheme which was never analyzed before. And the comparisons were made between AVP+ and AVP− on the stability and output impedance performance.**

***Index Terms*—Adaptive voltage positioning (AVP)+ control, constant output impedance, stability, voltage regulator.**

I. Introduction

AN ADAPTIVE voltage positioning (AVP) scheme has been used in multiphase synchronous rectifier buck converter topology for satisfying the power requirements of Intel's CPUs [1], [2]. The use of such a scheme normally leads to lower power dissipation in the CPU and smaller output capacitors required in the power converter circuit.

It has been pointed out that to achieve AVP, the closed-loop small-signal output impedance of the converter circuit should be a constant value which is specified by Intel's requirements [3]–[6]. The goal of the feedback design is therefore to perform a desirable output impedance characteristic while still maintaining feedback stability margin and good line regulation.

Fig. 1 shows a simplified diagram of an AVP control scheme commonly used to realize active droop control [7]–[9]. In the diagram, the load current signal is fed back and summed with the output voltage to be fed through Z_2 into the inverting input of the error amplifier. Most existing schemes employ this control strategy [10], [11]. This general scheme will be called the AVP− scheme for the fact that the feedback signal is connected to the inverting side of the error amplifier. Another scheme, called AVP+ in the present paper, was used in [12] and [13]

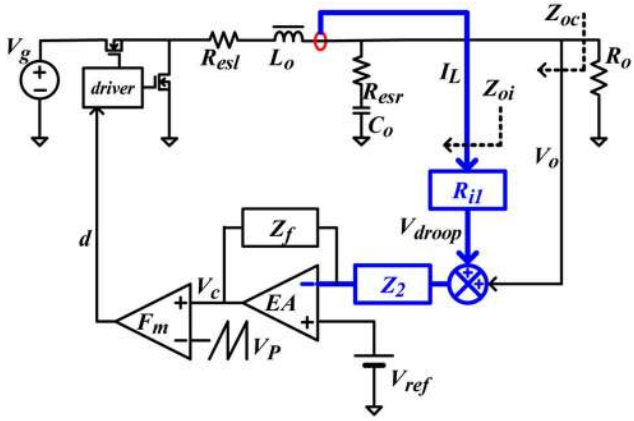

Fig. 1. VRM buck controller with AVP− control.

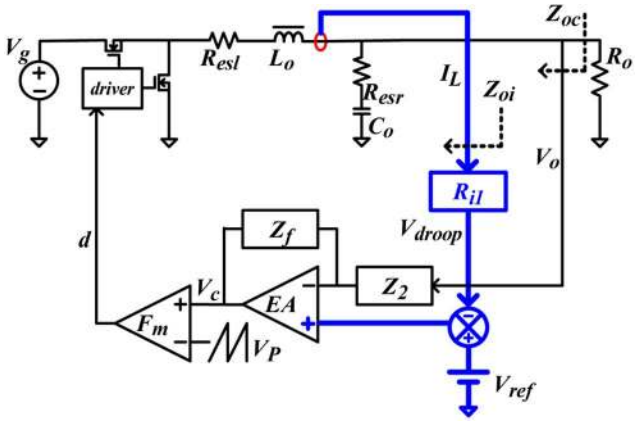

Fig. 2. VRM buck controller with AVP+ control.

but was never analyzed. The focus of this paper will be on the modeling and the design of the feedback for such a scheme. Fig. 2 shows the block diagram of the AVP+ control scheme. In the diagram, the sensed output inductor current information is subtracted from the reference voltage and fed into the non-inverting terminal of the error amplifier EA. And the output voltage signal is fed into the inverting terminal. This scheme also allows the converter characteristic of output voltage declining with increasing load current as AVP requires. There is a subtle difference between the two control schemes that favors AVP+ scheme, especially when ceramic capacitors are used in the output capacitors of the VRMs.

In this paper, the small-signal average model of buck converter circuit will be reviewed first. A model will then be developed for the AVP+. Both simulation and experimental results will be used to verify the model for a three-phase VRM.

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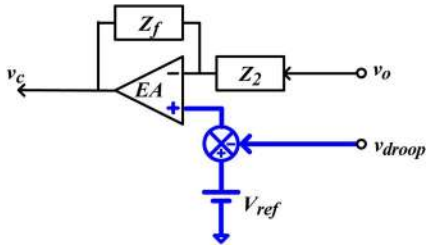

Fig. 3. Compensator circuit diagram.

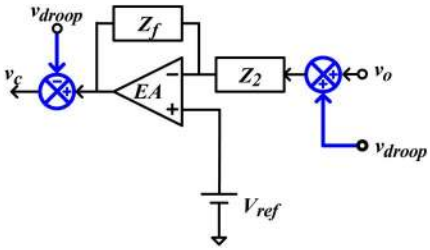

Fig. 4. Equivalent circuit diagram of that shown in Fig. 3.

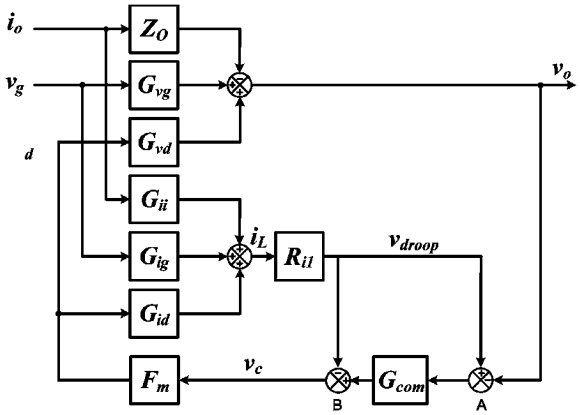

Fig. 5. Small-signal control block diagram of the AVP+ circuit shown in Fig. 2.

A comparison of the proposed AVP+ with conventional AVP− is given at the end. The focus of the present paper is the small-signal modeling for control loop design using the AVP+ scheme which was never analyzed before. And the comparisons were made between AVP+ and AVP− on the stability and output impedance performance.

II. Control Block Diagram

It has been pointed out that by proper switching frequency and component scaling, the control behavior of a multiphase converter can be represented by a simplified single-phase control circuit as shown in Fig. 2 [14].

A. Compensator Transfer Functions

From Fig. 2, the diagram around the error amplifier EA is isolated and redrawn in Fig. 3. From this figure, one can derive that

$$v_c = \frac{Z_f}{Z_2} \cdot (v_o + v_{\text{droop}}) - v_{\text{droop}}. \tag{1}$$

TABLE I
Transfer Functions of the Control Block Diagram of Fig. 4

Transfer Functions
Output current to inductor current: $G_{ii}(s) = \frac{i_L(s)}{i_O(s)} = \frac{1 + \frac{s}{\omega_{esr}}}{\Delta}$
Duty cycle to inductor current: $G_{id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_g}{R_O} \cdot \frac{1 + \frac{s}{\omega_R}}{\Delta}$
Input voltage to output voltage: $G_{vg}(s) = \frac{v_o(s)}{v_g(s)} = D \cdot \frac{1 + \frac{s}{\omega_{esr}}}{\Delta}$
Duty cycle to output voltage: $G_{vd}(s) = \frac{v_o(s)}{d(s)} = V_g \cdot \frac{1 + \frac{s}{\omega_{esr}}}{\Delta}$
Input voltage to inductor current: $G_{ig}(s) = \frac{i_L(s)}{v_g(s)} = D \cdot \frac{s \cdot C_O}{\Delta}$
Output current to output voltage: $Z_O(s) = \frac{v_o(s)}{i_O(s)} = R_{esl} \cdot \frac{\left(1 + \frac{s}{\omega_{esr}}\right) \cdot \left(1 + \frac{s}{\omega_L}\right)}{\Delta}$
Voltage loop gain: $T_v(s) = F_m \cdot G_{vd}(s) \cdot G_{com}(s)$
Current loop gain: $T_i(s) = F_m \cdot G_{id}(s) \cdot R_{il} \cdot (1 + G_{com}(s))$
Compensator gain: $G_{com}(s) = \frac{-Z_f(s)}{Z_2(s)}$
Modulator gain: $F_m = \frac{d(s)}{v_c(s)} = \frac{1}{V_P}$, where V_P is the peak value of the saw-tooth waveform.
Parameters
$\omega_O = \sqrt{\frac{R_O}{L_O \cdot C_O \cdot (R_O + C_O)}}$ $\quad$ $\omega_R = \frac{1}{R_O \cdot C_O}$
$\omega_{esr} = \frac{1}{R_{esr} \cdot C_O}$ $\quad$ $\omega_L = \frac{R_{esl}}{L_O}$
$Q = \frac{1}{\omega_O} \cdot \frac{1}{R_{esr} \cdot C_O + \frac{L_O}{R_O}}$ $\quad$ $\Delta = 1 + \frac{s}{Q \cdot \omega_O} + \frac{s^2}{\omega_O}$
R_{esr} : output capacitor ESR.
R_o : load resistance.
R_{esl} : output inductor resistance.
Z_{oi} : output impedance with T_i closed and T_v opened.
Z_{oc} : output impedance with both T_i and T_v closed.
f_{zc} : frequency of compensation zero.
f_{pc} : frequency of switching-noise-suppressing compensation pole.

From this equation, the equivalent circuit of the error amplifier compensation circuit is shown in Fig. 4. The voltage droop caused by changing the V_{ref} voltage has been represented by adding the two v_{droop} inputs in the circuit shown in Fig. 4.

B. Control Block Diagram

The control scheme shown in Fig. 2 can be represented by the small-signal block diagram shown in Fig. 5. In the lower-right corner of the figure, the v_{droop} signal is fed into Sumers A and B. This is to incorporate the equivalent circuit shown in Fig. 4 into the overall block diagram in Fig. 5. G_{com} (s) is the transfer function of the compensator gain in Fig. 4, which is equal to $-Z_f$ (s)/Z_2 (s). With the exception of the lower-right corner, the block diagram in Fig. 5 is similar to that of a conventional

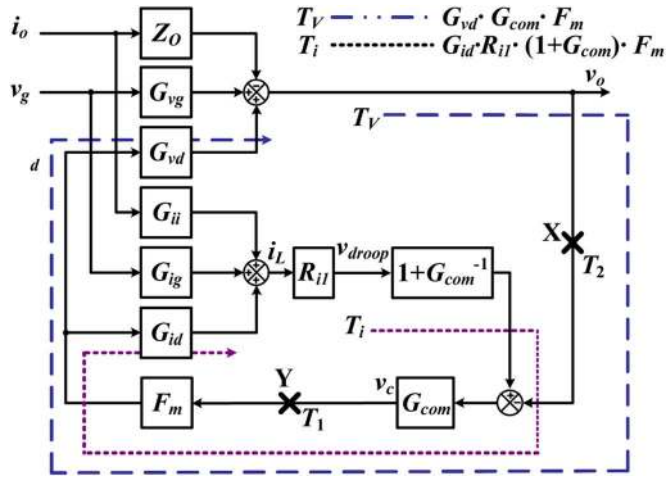

Fig. 6. Equivalent control block diagram of that shown in Fig. 5.

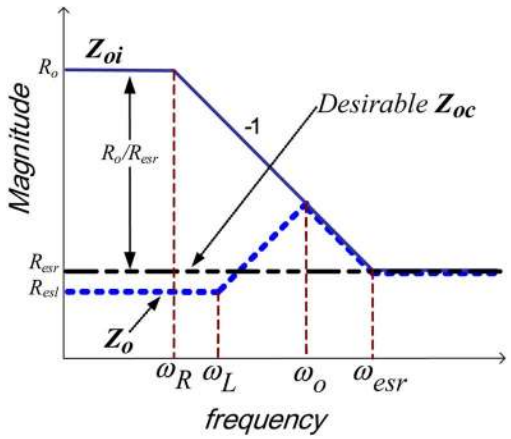

Fig. 7. Plots of $|Z_o|$, $|Z_{\rm oi}|$, and $|Z_{\rm oc}|$.

current-mode control buck converter which has been commonly used [15]. All the transfer functions are listed in Table I.

The diagram in Fig. 5 is further simplified into that in Fig. 6, where $1+G_{\rm com}^{-1}$ is the equivalent transfer function when Sumer B in Fig. 5 is eliminated.

C. Useful Equations

Loop gains: From Fig. 6, two loop gain functions, T_i (s) and $T_v(s)$, are defined as follows:

$$T_v(s) \equiv F_m \cdot G_{vd}(s) \cdot G_{\rm com}(s) \quad (2)$$

$$T_i(s) \equiv F_m \cdot G_{id}(s) \cdot R_{il} \cdot (1 + G_{\rm com}(s)). \quad (3)$$

By applying the Mason's gain formula, the two loop gains, T_1 (s) and T_2 (s), evaluated at points X and Y respectively, are shown as follows.

Converter output impedance transfer functions:

$$T_1(s) = T_1(s) + T_v(s) \quad (4)$$

$$T_2(s) = \frac{T_v(s)}{1 + T_i(s)}. \quad (5)$$

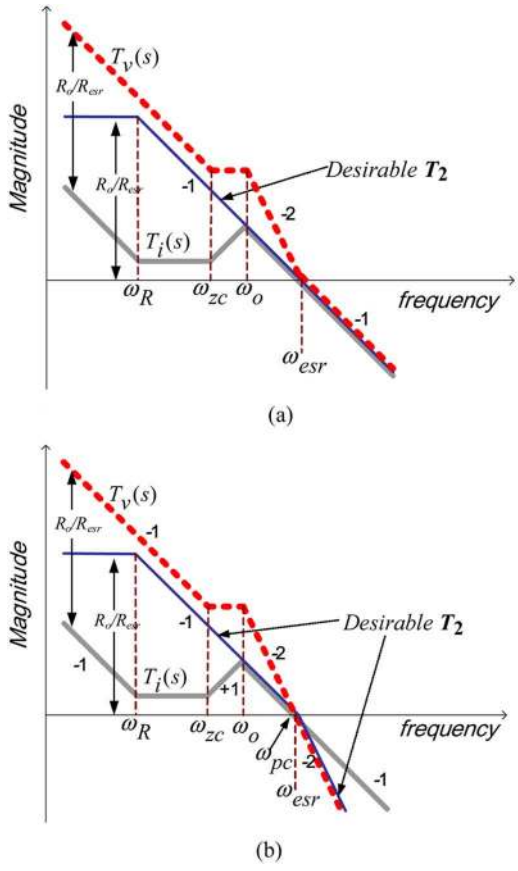

Fig. 8. Plots of $|T_i|$, $|T_v|$, and $|T_2|$. (a) Noise-suppression pole $\omega_{\rm pc}$ is much larger than $\omega_{\rm esr}$. (b) Noise-suppression pole $\omega_{\rm pc}$ is placed at $\omega = \omega_{\rm esr}$.

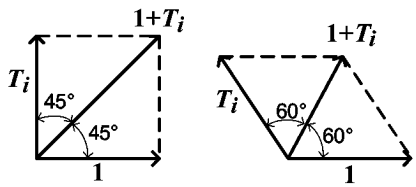

Fig. 9. Vector summation of 1+T_i.

The output impedance transfer function with current loop closed but voltage loop opened is expressed as

$$Z_{oi}(s) = \frac{Z_o(s)(1 + T_i(s)) + F_m \cdot G_{ii}(s) G_{vd}(s) \cdot R_{il}}{1 + T_i(s)}. \quad (6)$$

The output impedance transfer function with both the current- and the voltage-loop closed is expressed as

$$Z_{oc}(s) = \frac{Z_o(s)(1 + T_i(s)) + F_m \cdot G_{ii}(s) G_{vd}(s) \cdot R_{il}}{1 + T_i(s) + T_v(s)}. \quad (7)$$

Fig. 7 shows the comparison plots of $|Z_o|$, $|Z_{\rm oi}|$, and $|Z_{\rm oc}|$. It can be seen the current loop alone actually increases the output impedance. Only when the voltage loop is also closed will the output impedance be brought down. Based on (8), the output

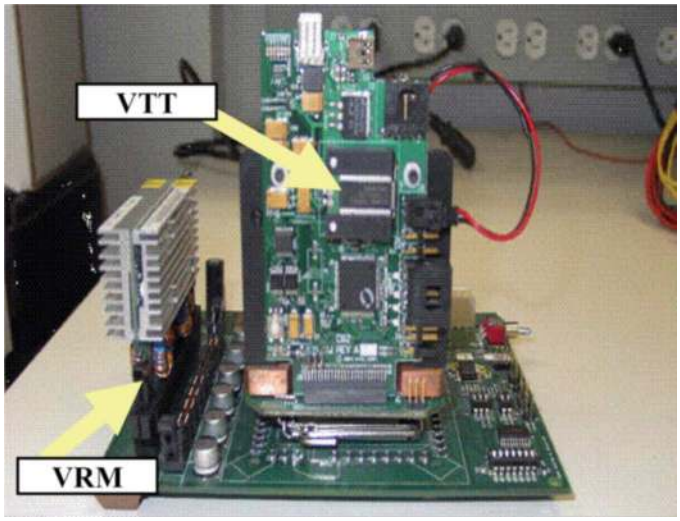

Fig. 10. Experimental hardware with VTT tool.

impedance $Z_{\rm oc}$ can be brought to constant output impedance shown by the "desirable $Z_{\rm oc}$," if a proper T_2 is used [7].

III. Design for a Constant Output Impedance for AVP+

It has been pointed out that constant output impedance is required to accomplish AVP. In this section, discussion will be given to feedback design to accomplish such a goal. As results of accomplishing this goal, other converter performances such as converter stability and audio-susceptibility are affected. These performances will be taken into considerations in the discussion.

The relationships between $Z_{\rm oc}(s)$ and $Z_{\rm oi}(s)$ can be derived as

$$Z_{\rm oc} = \frac{Z_{\rm oi}(s)}{1 + T_2(s)}. \tag{8}$$

A. Desirable $T_2(s)$ to Accomplish a Constant Output Impedance

Using (2), (3), and (5), if $|T_i| \gg 1$ and $|G_{\rm com}| \gg 1$, T_2 is approximated as follows:

$$T_2(s) \cong \frac{R_o}{R_{i1}} \cdot \frac{1 + \frac{s}{\omega_{\rm esr}}}{1 + \frac{s}{\omega_R}}. \tag{9}$$

To achieve a constant $Z_{\rm oc}$ as shown in Fig. 7, T_2 must satisfy the following two conditions:

1) R_{i1} is set to be $R_{\rm esr}$ in (9).
2) $|T_2| \gg 1$ for $f < f_{\rm esr}$.

It can be seen that T_2 is independent of $G_{\rm com}$ as long as the two assumptions, $|T_i| \gg 1$, and $|G_{\rm com}| \gg 1$, hold. Therefore, one can design the compensation function $G_{\rm com}$ to achieve a good T_2 stability margin and retain a constant output impedance performance. The two assumptions, $|T_i| \gg 1$ and $|G_{\rm com}| \gg 1$, are generally true for frequency much lower than $f_{\rm esr}$ because a compensating pole is normally placed at dc frequency. This will be explained later in Section III-B.

B. Compensation Design for AVP

Beside output impedance, two other key issues, i.e., the stability and the audio-susceptibility, need to be taken into considerations. As described previously, T_2 is unchanged by the compensation $G_{\rm com}$ as long as $|G_{\rm com}|$ and $|T_i|$ are both much greater than 1. Therefore, a low-frequency compensation pole (integrator) can be used in $G_{\rm com}$ to boost the low-frequency gain of

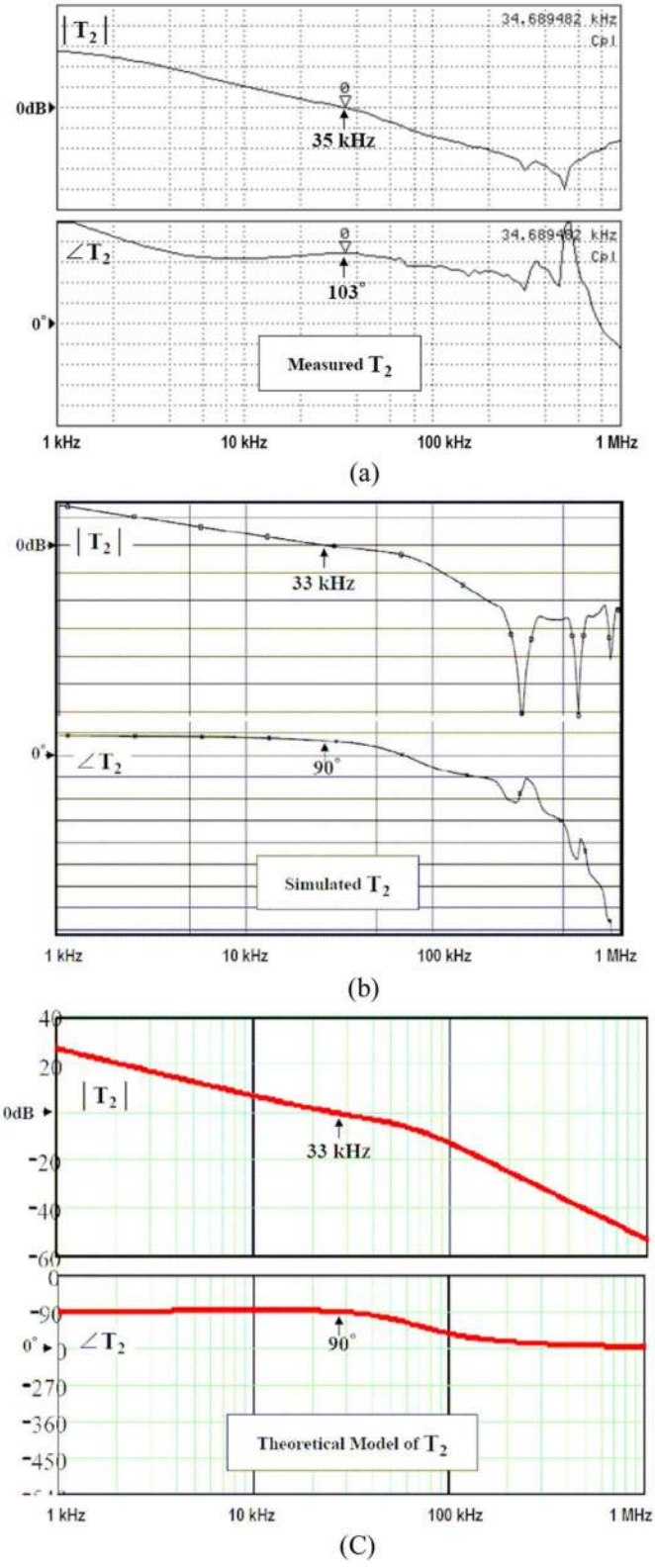

Fig. 11. Utter loop gain. (a) Measured T_2, (b) simulated T_2, and (c) theoretical model of T_2

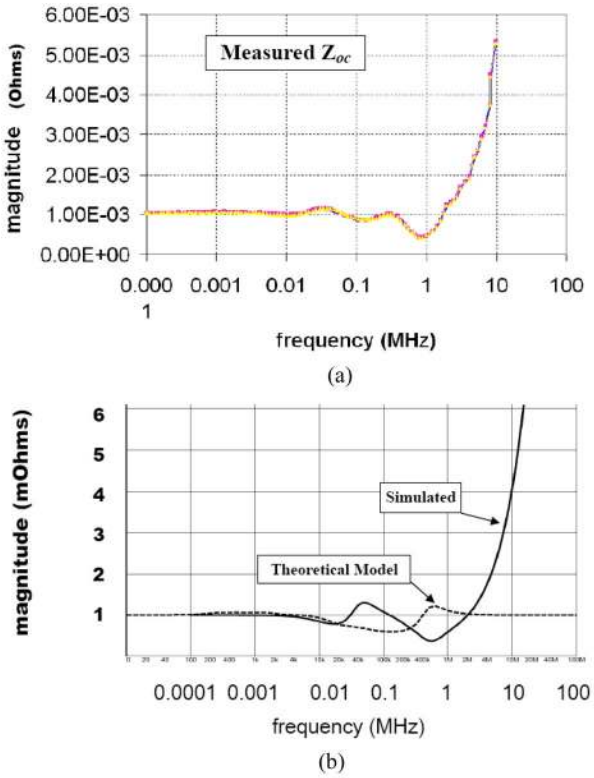

Fig. 12. Closed-loop output impedance. (a) Measured $|Z_{\rm oc}|$ and (b) theoretical model of $|Z_{\rm oc}|$ and simulated $|Z_{\rm oc}|$ plot including parasitic inductance of 100 pH.

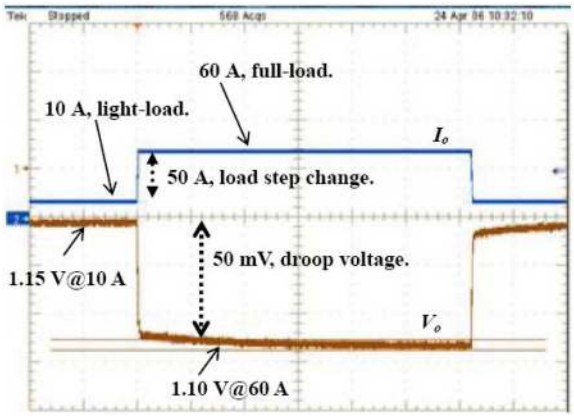

Fig. 13. Measured waveforms of output voltage and output current for AVP+.

TABLE II
KEY COMPONENT PARAMETERS FOR EXPERIMENT

Circuit Parameters
C_o : Oscon, (560 μF/ 7 mΩ) x10,
f_{esr} : 40.62 kHz,
L_o : 320 nH, *per-phase*,
f_{sw} : 300 kHz
Controller: RT8800 by Richtek Inc.,
MOSFETs: FAN0N9B

TABLE III
KEY COMPONENT PARAMETERS FOR SIMPLIS SIMULATION

Circuit Parameters
CASE I. *using large capacitor type*
C_o :Oscon, (820 μF/ 12 mΩ) x12 → 9,840 μF/ 1 mΩ, f_{esr}=16.17 kHz.
L_o :470 nH, *per-phase*
f_{sw} :300 kHz
f_{pc} :100 kHz
CASE II. *using ceramic capacitors*
C_o :Ceramic, (100 μF/ 1.5 mΩ) x2 → 200 μF/ 0.75 mΩ, f_{esr}=1.1 MHz.
L_o :100 nH, *per-phase*
f_{sw} :1 MHz
f_{pc} :300 kHz
L_o : output inductance
C_o : output capacitance
R_{esr} : capacitance ESR

T_i and T_v and consequently T_1 so that audio-susceptibility performance can be improved without much affecting T_2 characteristics and the close-loop output impedance performance $Z_{\rm oc}$. A compensation zero $f_{\rm zc}$ should also be placed near the resonance frequency f_o to stabilize the loop gain T_1. Finally, a compensation pole $f_{\rm pc}$ is normally used to suppress switching-frequency noise. Placement of $f_{\rm pc}$ is flexible, depending on the amount of the noise attenuation required [7], [16]. However, if $f_{\rm pc}$ is too close to $f_{\rm esr}$, then $f_{\rm pc}$ may have noticeable effects on the T_1 and T_2 stability margin, and $Z_{\rm oc}$ may spike near $f_{\rm esr}$. This will be discussed in detail in Section III-D.

C. Crossover Frequency

From the discussion in the last section, T_2 crosses over at $f_{\rm esr}$ as shown in Fig. 8. As a result, T_i and T_v must also cross over at $f_{\rm esr}$. Because of (5), the T_2 value for frequency beyond $f_{\rm esr}$ can be decreasing with -1 slope or -2 slope depending on whether a noise-suppressing pole is placed near $f_{\rm esr}$. Fig. 8 shows the plots for both cases. In either case, $Z_{\rm oc}$ is essentially the same except for frequency near $f_{\rm esr}$. $|Z_{\rm oc}|$ is more likely to exhibit a spike near $f = f_{\rm esr}$ for the case in Fig. 8(b). The T_2 stability margin will also be affected by the crossover slope of T_2.

A quick explanation of T_2 behavior is given below. From (5), for low frequency when $|T_i| \gg 1, T_2 \approx T_v/T_i$, for frequency when $|T_i| \ll 1, T_2 \approx T_v$. Near the cross over frequency of T_i, where $|T_i| \approx 1, T_2$ behavior depends on the phase angles of T_i and T_v at that frequency. This affects the T_2 stability phase margin. And according to (8), the T_2 phase margin affects the $Z_{\rm oc}$ behavior near $f_{\rm esr}$. Spiking of $|Z_{\rm oc}|$ characteristics may show up near $f_{\rm esr}$ because of low T_2 stability margin. This will be explained in Section III-D.

D. Behavior of $Z_{\rm oc}, T_2$, and T_1 Near $f_{\rm esr}$

Near $f_{\rm esr}$, the amplitude of T_i is nearly unity. However, because of vector summation, $|1 + T_i|$ can vary from 0 to 2. Fig. 9 shows the vector summation of $|1 + T_i|$ for the phases of T_i are 90° and 120°, respectively. If T_i is close to 180°, then $|T_2|$ frequency response would have a peaking near $f_{\rm esr}$, according to (5). By the same argument, the T_2 phase angle at $f = f_{\rm esr}$ affects $Z_{\rm oc}$ near $f_{\rm esr}$ also according to (8).

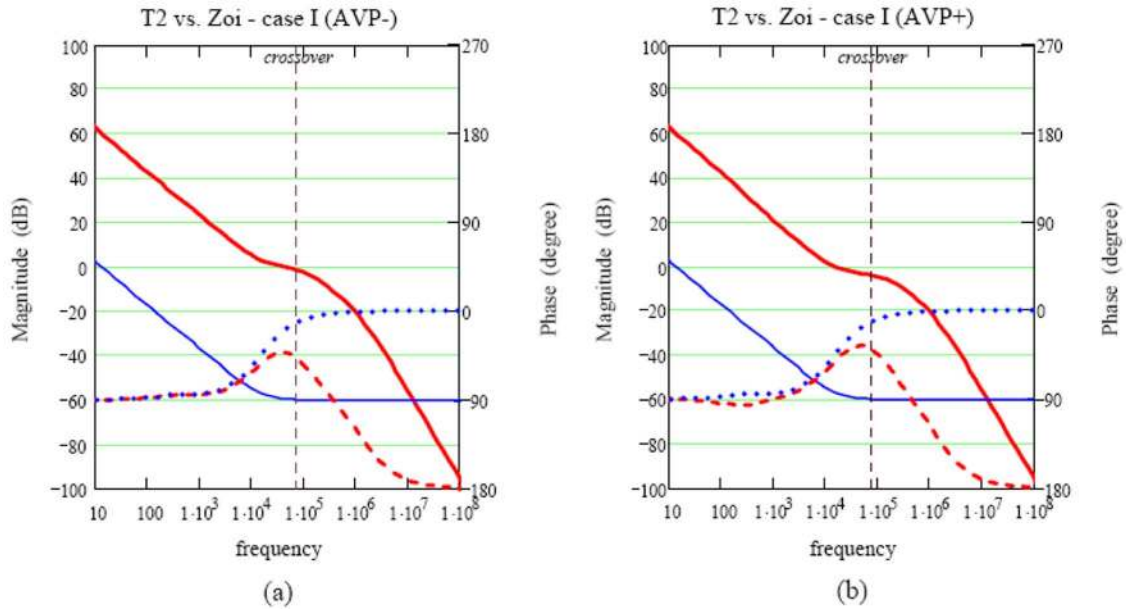

Fig. 14. Theoretical T_2 plots for case I (a) AVP$-$ and (b) AVP$+$, when $f_{\rm pc} \gg f_{\rm esr}$.

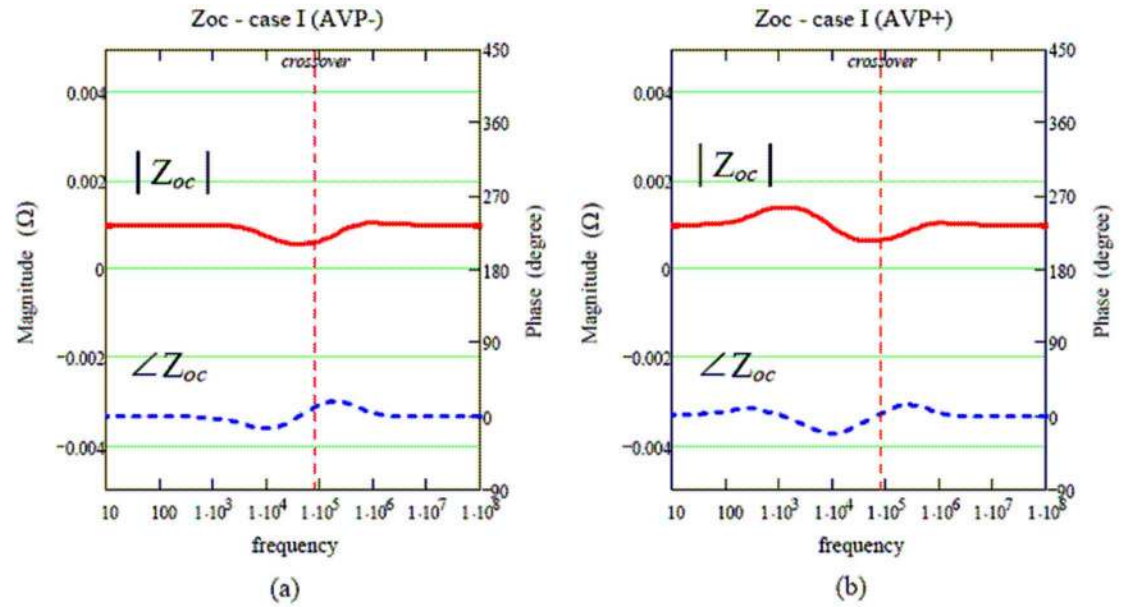

Fig. 15. Theoretical $Z_{\rm oc}$ plots for case I (a) AVP$-$ and (b) AVP$+$, when $f_{\rm pc} \gg f_{\rm esr}$.

Based on the design concerns given in this subsection, a converter was built for experimental verification to be explained in Section IV.

IV. Experimental Results

A three-phase interleaved buck converter was designed and tested to verify the model described above. Table II shows the circuit operating conditions and component values. A Cascade Systems Technology's Voltage Transient Tool (VTT) as a CPU load equipment was used to test the various circuit functions [17]. Fig. 10 shows the hardware. Fig. 11 not only shows the measured and the theoretical utter loop gain T_2 but also the simulation results of this magnitude. Fig. 12(a) shows the measured closed-loop output impedance $Z_{\rm oc}$ versus the frequency. It agrees well with the model at frequency below 1 MHz. The derivation at high frequencies was attributed to the parasitic inductance of the breadboard circuit trace. When a 100-pH parasitic inductor was used, both agree well. This is also confirmed by the SIMPLIS simulation results shown in Fig. 12(b). The load step change waveforms of the breadboard are shown in Fig. 13.

V. Comparison of AVP$+$ and AVP$-$

The design and analysis of AVP$-$ are well discussed and developed in papers. For control loop design, the major difference between AVP$-$ and AVP$+$ is the expressions for the current loop transfer function $T_i(\rm s)$. The equations for $T_i(\rm s)$ are as

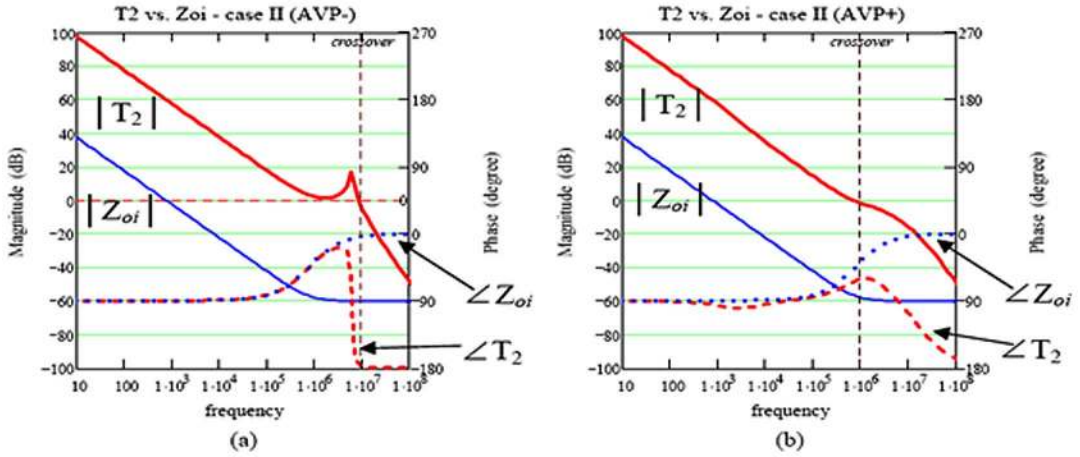

Fig. 16. Theoretical T_2 plots for case II (a) AVP$-$ and (b) AVP$+$, when $f_{\rm pc}$ is near or less than $f_{\rm esr}$.

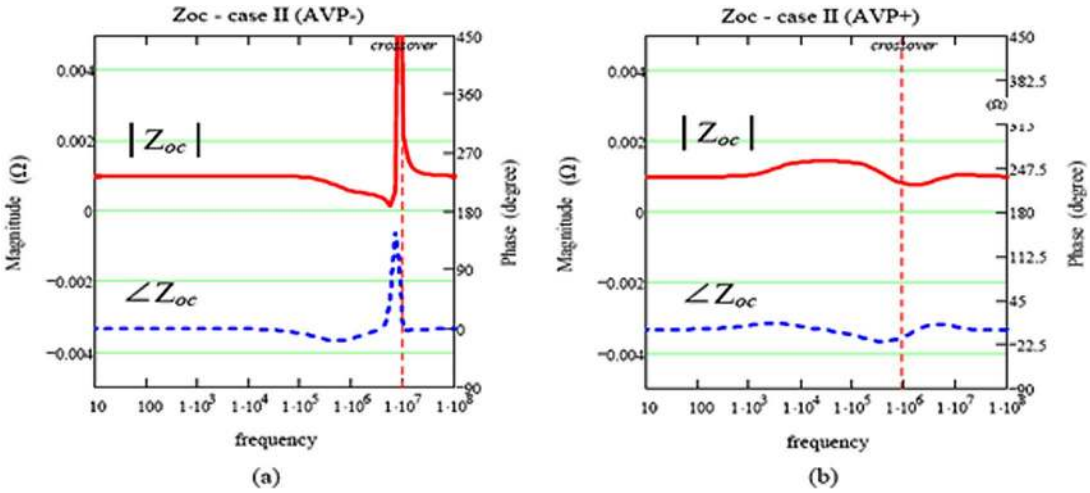

Fig. 17. Theoretical $Z_{\rm oc}$ plots for case II (a) AVP$-$ and (b) AVP$+$, when $f_{\rm pc}$ is near or less than $f_{\rm esr}$.

follows:

$$T_i(s) \equiv F_m \cdot G_{id}(s) \cdot R_{i1} \cdot (1 + G_{\rm com}(s)), \quad \text{for AVP} + \tag{10}$$

$$T_i(s) \equiv F_m \cdot G_{id}(s) \cdot R_{i1} \cdot (1 + G_{\rm com}(s)), \quad \text{for AVP} - . \tag{11}$$

T_2 and $Z_{\rm oc}$ functions will be plotted for two practical cases using the model and the expression given above. In case I, large OSCAN capacitors were used in which $f_{\rm esr}$ is relatively small compared to switching frequency. In case II, small ceramics capacitors were used in which $f_{\rm esr}$ is close to the switching frequency.

In both cases, a noise-suppression compensation pole $f_{\rm pc}$ was used. To be effective, $f_{\rm pc}$ must be significantly below switching frequency. The exact component values of the two cases are listed in Table III.

As mentioned in Section III-B, a compensation pole $f_{\rm pc}$ may be used to suppress hardware switching-frequency noise in the circuit. To be effective, $f_{\rm pc}$ must be significantly lower than the switching frequency. If $f_{\rm pc} \gg f_{\rm esr}$, as case I, then there is very little difference between AVP$+$ and AVP$-$. Figs. 14 and 15 show the T_2 and $Z_{\rm oc}$ plots for the two schemes. However, if $f_{\rm pc}$ is close to or even less than $f_{\rm esr}$, then that significantly degrades the T_2 stability margin, and $Z_{\rm oc}$ exhibits a spike near $f_{\rm esr}$ for the AVP$-$ but not AVP$+$, as shown in Figs. 16 and 17. This is because $f_{\rm pc}$ significantly affects T_i phase angle at $f = f_{\rm esr}$. As can be seen from Fig. 18(a), $\angle T_i$ is near -180° at $|T_i|$ zero crossovers for AVP$-$. From the discussing given in Section III-D, this means T_2 is near instability and $|Z_{\rm oc}|$ shows a spike. However, in Fig. 18(b), the AVP$+$ case, T_i still has about an 80° phase margin which means large $|T_2|$ stability phase margin and little $|Z_{\rm oc}|$ spike near $f_{\rm esr}$. For the cases shown in Fig. 19, both AVP$-$ and AVP$+$ exhibit a large margin at $|T_i|$ crossover frequency. This explains why there is very little difference between AVP$+$ and AVP$-$ for this condition.

Simulation results: The simulations were run for a practical three-phase VRM to compare the two schemes, AVP$+$ and AVP$-$, under both cases I and II using SIMPLIS simulation tool [18]. For case I, there is a little difference between the two schemes. However, there are significant differences for case II as shown by the T_2 and $|Z_{\rm oc}|$ plots shown in Figs. 20–22. Simulation results confirm the theoretical predictions. Fig. 23 shows the load-step response of AVP$+$ and AVP$-$ for case II. It can be seen that AVP$+$ gives a better step response because of absence of output voltage and inductor current ringing which

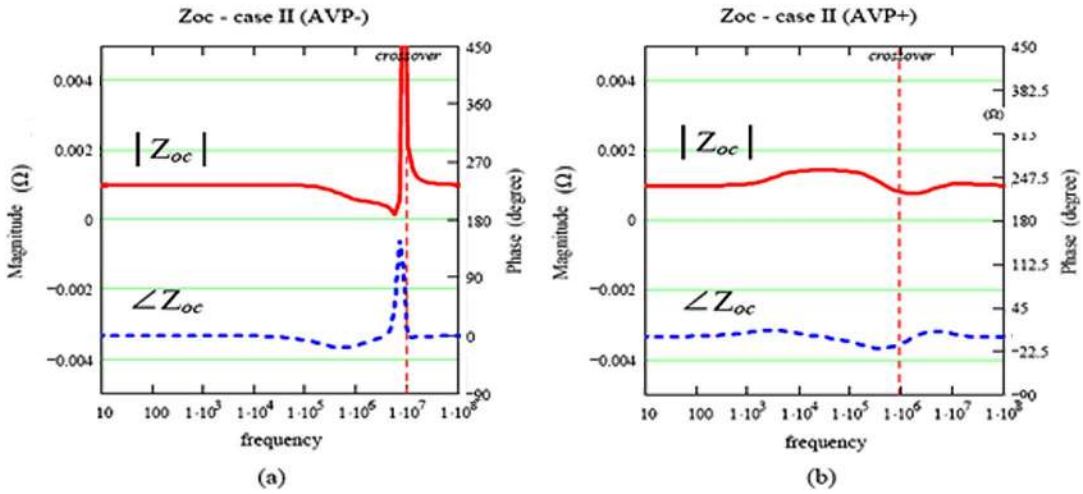

Fig. 18. Theoretical T_i plots for case II (a) AVP− and (b) AVP+, when $f_{\rm pc}$ is near or less than $f_{\rm esr}$.

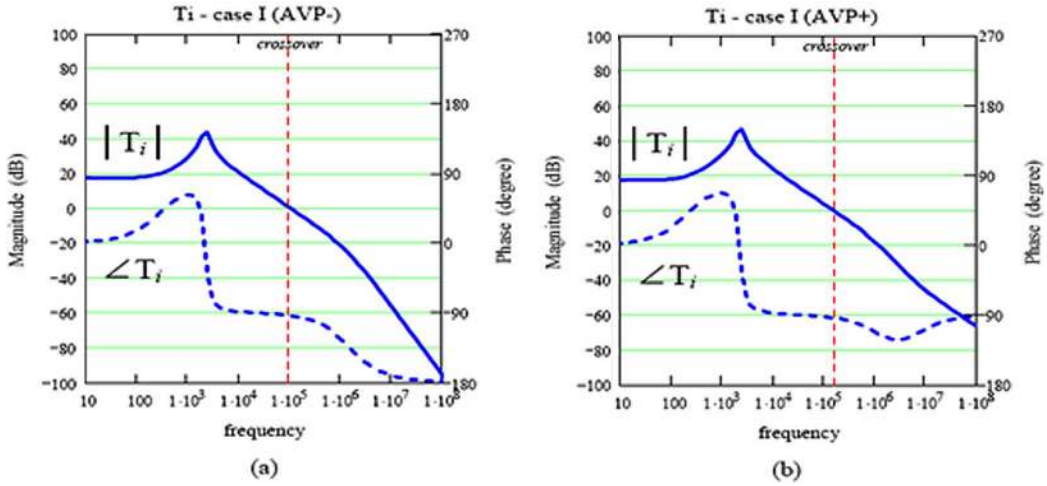

Fig. 19. Theoretical T_i plots for case I (a) AVP− and (b) AVP+, when $f_{\rm pc} \gg f_{\rm esr}$.

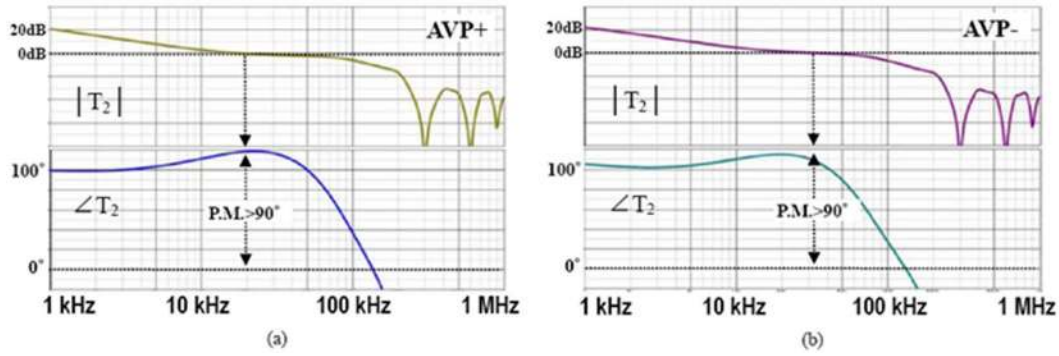

Fig. 20. Simulated T_2 of (a) AVP+ and (b) AVP− for case I.

occurs for AVP− starting to oscillate. The instability resulted in oscillation of the voltage and current waveforms.

VI. Conclusion

An AVP+ control scheme was proposed and implemented for multiphase synchronous buck converter applications. A small-signal model was also developed for converters using this scheme. Based on the model, various compensation design issues were explored. The results are compared to a common-used AVP− scheme.

Depending on the relative location of the noise-suppressing compensation pole frequency with respect to the capacitor ESR-zero frequency, the performance of converter output impedance $Z_{\rm oc}$ and stability margin near the crossover frequency may vary a great deal. If the two frequencies are closer to each other, the

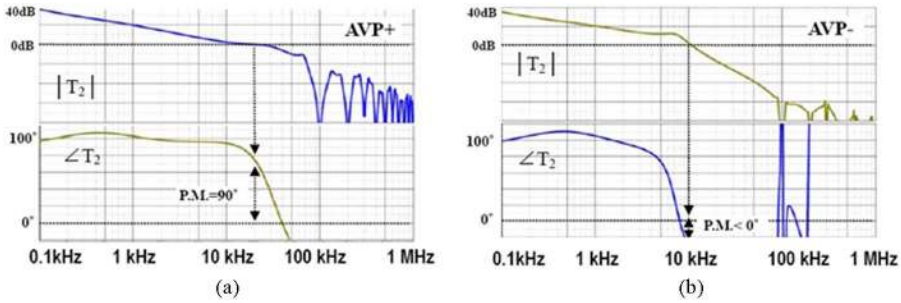

Fig. 21. Simulated T_2 of (a) AVP+ and (b) AVP− for case II.

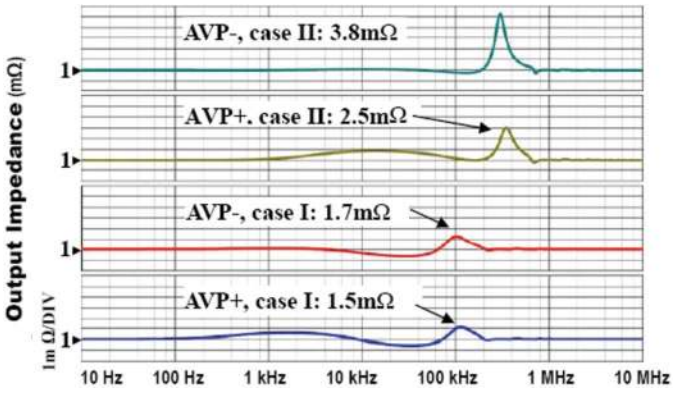

Fig. 22. Comparisons of $Z_{\rm oc}$ in SIMPLIS.

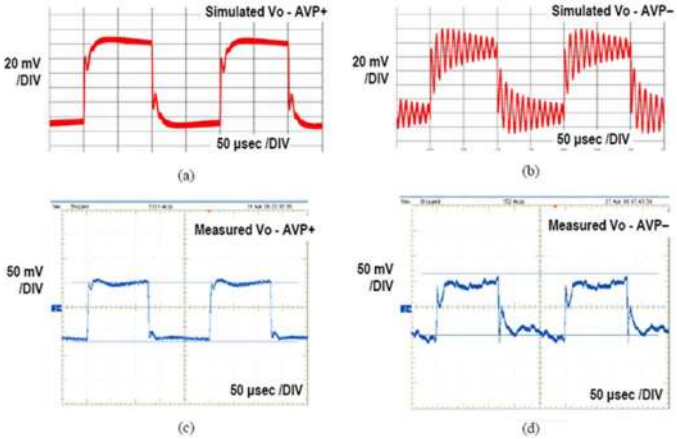

Fig. 23. Transient response waveforms for case II. (a) Simulated V_o for AVP+, (b) simulated V_o for AVP−, (c) measured V_o for AVP+, and (d) measured V_o for AVP. Test conditions: VID = 1.0 V, load current step changed between 10 and 110 A.

stability margin get smaller, and $Z_{\rm oc}$ is more likely to exhibit a spike/dip at the ESR frequency and step-load response gets overshoot. Compared to a conventional AVP− scheme, the proposed AVP+ shows superior performance especially when ceramic output capacitors are used. This is a significant advantage considering the trend of using ceramic capacitors in many future VRM applications.

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