Modelling and Design of High-Order Phase Locked Loops

Brian Daniels, Gerard Baldwin, Ronan Farrell, Sean McLoone
Department of Electronic Engineering, National University of Ireland Maynooth

ABSTRACT

In this paper a new stable high order Digital Phase Lock Loop (DPLL) design technique is proposed. This technique uses linear theory to design the DPLL. The stability of the DPLL is guaranteed by placing a restriction on the system gain. This stability boundary is found by transforming the system transfer function to the Z-domain and plotting the root locus of the LPLL for values of gain where all the system poles lie inside the unit circle. The max value of gain where all the poles lie inside the unit circle is the stability boundary. It is shown that the stability boundary of the LPLL is comparable to the stability boundary of the DPLL. Finally where the above Bessel filter system produces slow lock, gear shifting of the DPLL components is considered. This allows the DPLL to start off with a wide loop bandwidth and switch to the narrow bandwidth once the system has locked.

INTRODUCTION

In this paper, the modelling and design of digital phase locked loops (DPLL) is considered. Firstly the differences between the Linear Phase Locked Loop (LPLL) and the DPLL are considered, the difference is mainly in the non-linear Charge Pump and the Phase Frequency Detector (CP-PFD). Therefore only simulation of the DPLL needs to accurately model the non-linearity introduced by these. In the second section of this paper the techniques used to model and simulate the LPLL and DPLL are explained. Both the DPLL simulation and LPLL model estimate the phase error of each system. Using these techniques, the third section compares the LPLL model response to the response of the DPLL. In the forth section, a novel technique is introduced to design stable high order DPLLs. The filter poles of the DPLL are placed using Bessel filter design, stability is guaranteed by placing the poles inside the Z domain unit circle. This is achieved by plotting the root locus of the system poles in the Z domain, and finding the stability boundary of the system. The stability boundary being the largest value of system gain K_{SYS} for which all the poles lie inside the unit circle. Finally in the last section, gear shifting of the loop parameters in order to achieve faster lock is considered.

DPLL NON-LINEARITIES

The LPLL continuous time model is generally used to model the DPLL, however the DPLL is non-linear. Two vital components of the DPLL have non-linearities, namely the charge pump and the phase frequency detector, and the voltage controlled oscillator (VCO). The VCO non-linearity is due to saturation.

The CP-PFD non-linearity is due to the switching nature of the PFD. The PFD switches between the three states,

1. UP – signal R in figure 1 below leads signal V,
2. DOWN – signal R lags signal V, or
3. NULL – signal R and V correspond.

The PFD switches between these three states, in effect acting as a Quantizer. It has an output of $+I_p$, 0 or $-I_p$ depending on the state of the PFD, where I_p is the current gain of the CP. Because the CP-PFD operates as a switch, the DPLL system of figure 1 is varying with time. This quantization and time varying nature is the non-linearity.

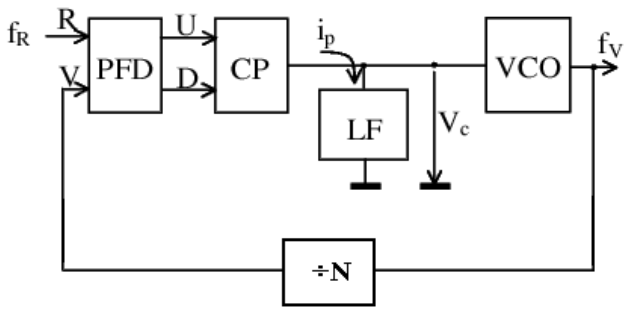

Figure 1: DPLL system

The PLLs non-linear operation as illustrated in figure 2. For a Digital PLL the inputs R and V will be square waves. The output of the PFD will be Up, Down or Null depending on whether the signal R leads, lags, or is incidental with the fed back signal V. The output of the charge pump will then be $+I_p$, $-I_p$ or zero respectively.

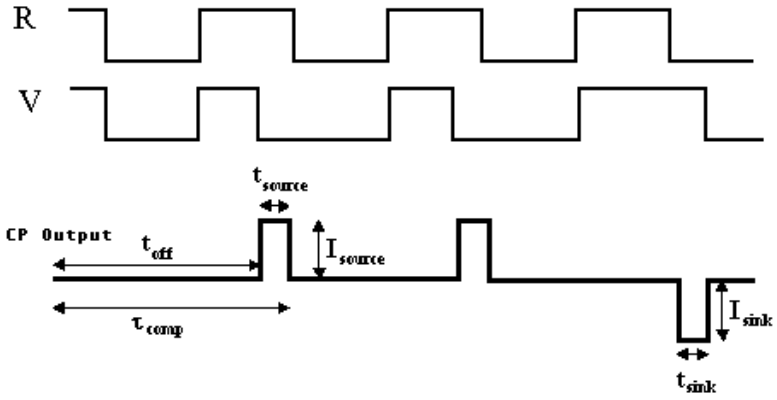

Figure 2: PFD input and Output signals

In order to analysis this system, the following assumptions are made [1]:

1. The PFD can be modelled as a subtractor if the assumption is made that the phase error of the DPLL is small. The linear PFD output corresponds to $\theta_e = \theta_R - \theta_V$.
2. By averaging over time, the time-varying operation can be bypassed. If each cycle has a duration of $\frac{2\pi}{\omega_i}$ seconds, where ω_i is the frequency of the input signal, then the average error current over a cycle is $i_d = \frac{I_p \theta_e}{2\pi}$ amps (This also corresponds to the averse error current over many cycles).

PLL MODELING AND SIMULATION

Linear System Response Estimation

The LPLL block diagram shown in figure 3 is traditionally used to model and design the DPLL. This system has all linear components with a subtractor and a gain K_C replacing the CP-PFD and an integrator and a gain K_V replacing the VCO blocks of figure 1. The charge pump gain K_C is equal to the charge pump current I_p divided by 2π. The control voltage of the linear PLL system can be estimated as

$V_c(s) = I_P(s)F(s)$, where F(s) is the transfer function of the loop filter, and the VCO output phase is $\theta_e(s) = \frac{K_V V_c(s)}{s}$. With this equation the overall linear system transfer function can be calculated.

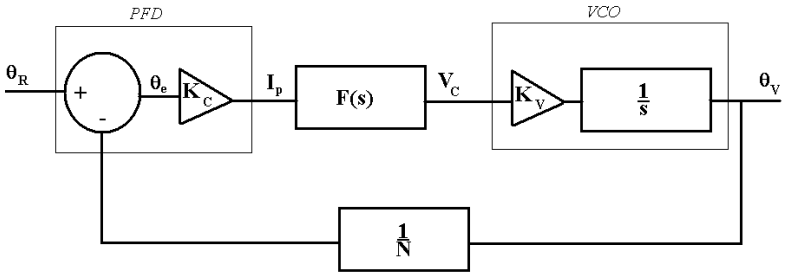

Figure 3: Linear PLL system

Traditionally [2] higher order (4th, 5th,6th, etc) DPLL systems are designed by using Gardner's technique [1] to design a stable 3rd order DPLL, and then adding higher order poles at a location in the S-Domain much greater then the filter cut-off frequency, the intention is to insure that the system stability is dependent on only 3 system poles and that any higher order poles placed out of band will have little or no effect on the stability of the system. These systems are designed to reduce the noise in out of band frequencies, but the loop filter cut-off rate is still that of a third order system. This pole placement procedure reduces the number of poles that need to be considered when optimising the system, making this analysis simpler. For example it is possible to design a 7th order stable PLL system [2] with three dominant poles, the stability of this system depends only on the effects of these three poles.

Digital System Response Simulation

The DPLL non-linearity in the VCO can be linearised by operating within a maximum and minimum control voltage restriction. The CP-PFD non-linearity exists because of the switching nature of the PFD. The CP-PFD operates linearly in any one state, the non-linearity occurs when the CP-PFD changes state. So the operation of the DPLL between state changes can be described by linear differential equations. The DPLL can be accurately modeled if the changing states of the PFD are considered. Using the charge approximation model [4] of a second order DPLL system the control voltage can be estimated using equation (1) below:

$$V_C(t_n) = I_{CP}R + \frac{Q(t_{n-1}) + I_{CP}\Delta t}{C} \qquad (1)$$

Where R and C are the resistor and capacitor values of the loop filter, Q is the charge on the loop filter capacitor, Δt is the discrete time step, and I_{CP} is the current output of the CP-PFD. The value of I_{CP} is dependent on the present state of the CP-PFD. The technique used to model the changing state of the CP-PFD is to use an event driven state machine model. This assumes that the PFD will always operate in one of the following three states:

1. Up (Reference Phase leads the VCO Phase)
2. Down (VCO Phase leads the Reference Phase)
3. Null (Neutral)

If the CP-PFD is in the Up state then the charge pump output I_{CP} is equal $+I_p$, where I_p is constant gain value. Likewise if the state is Down there is a $-I_p$ current out, finally if the state is Null there is no current out from the CP-PFD. The state machine transitions are visually illustrated in figure 4 below, where R↓ and V↓ are the reference and VCO falling edge events.

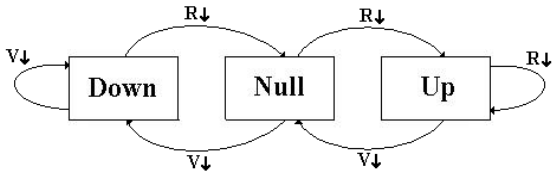

Figure 4: PFD State Diagram

The state changes after each new event detected in the system. For high order systems the DPLL difference equations cannot be solved in closed form. The solution is to numerically integrate the DPLL difference equation (2) to calculate the control voltage response V_c over time.

$$\int_0^{\Delta t} V_c(t')dt = \Delta t V_c(t_n) + \frac{\Delta t\left(V_c\left(t_{n+1}\right) - V_c\left(t_n\right)\right)}{2} \qquad (2)$$

This introduces an approximation error into the model that can be minimised by using a small value of the time step Δt. An important parameter of this event driven model is the phase of the VCO and reference signals. These parameters determine the instant at which events occur in the PFD and hence the current state and output value of the CP-PFD. The VCO and reference phase are calculated using the difference equations (3) and (4) below, where f_r is the reference frequency.

$$\varphi_v(t_{n+1}) = \varphi_v(t_n) + 2\pi\left(K_v\left(\Delta t V_c(t_n) + \frac{\Delta t\left(V_c(t_{n+1}) - V_c(t_n)\right)}{2}\right) + \Delta t f_{v0}\right) \qquad (3)$$

$$\varphi_r(t_{n+1}) = \varphi_r(t_n) + 2\pi f_r \Delta t \qquad (4)$$

The CP-PFD detects falling edge events of the VCO and reference signals. The VCO signal falling edge occurs when the VCO phase is equal to 2πN, where N is the feedback divider ratio, as shown in Figure 1 earlier. Similarly the reference falling edge occurs when the reference phase is equal to 2π.

LINEAR/DIGITAL COMPARISON

Estimation of phase error from CP-PFD data in the DPLL

In the linear PLL the phase error is a continuous time representation of the phase difference between the reference and VCO signals. The CP output signal shown in figure 2 is not continuous time, therefore in order to compare the linear and digital PLL a continuous time representation of the above DPLL phase difference must be found.

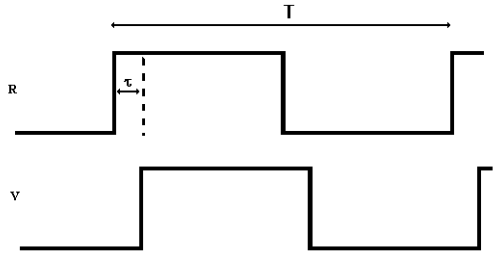

Figure 5: CP-PFD input signals

To find the continuous time phase error between the reference and VCO signals of the DPLL, consider the two square wave signals in figure 5, the top one representing the reference and the bottom one representing

the VCO or feedback signal. The frequency of the reference signal is equal to 1/T. If we consider the rising edges of both signals, then the time difference from the rising edge of one signal to the other is τ. The continuous time phase difference between these two signals is equal to $\phi_{error} = \frac{2\pi\tau}{T}$ radians/s.

Calculation of the Linear PLL step responses

As mentioned earlier the non-linear CP-PFD can be approximated as a subtractor and a gain component, and the VCO as an integrator and a gain component. From figure 3 the closed loop error transfer function for this system can be calculated as:

$$H_e(s) = \frac{Ns}{Ns + K_V K_C F(s)} \qquad (5)$$

The transient response of this transfer function ideally should represent the response of the DPLL phase/frequency error. Using linear theory the phase step response of the above $H_e(s)$ is $\Theta_e(s) = H_e(s)\frac{\Delta\Phi}{s}$, where ΔΦ is the change in phase. Therefore the phase step response of the LPLL is:

$$\Theta_e(s) = \frac{\Delta\Phi Ns}{Ns^2 + K_V K_C F(s)s} \quad (6)$$

Similarly the frequency step response of the LPLL for a frequency step of Δω is:

$$\Theta_e(s) = \frac{\Delta\omega . Ns}{Ns^3 + K_V K_C F(s)s^2} \quad (7)$$

Finally for a frequency ramp of Δϖ over a time period of t, the system response is:

$$\Theta_e(s) = \frac{\Delta\varpi . Ns}{Ns^4 + K_V K_C F(s)s^3} \quad (8)$$

Comparison between the Linear and Digital Responses

In the following example the LPLL and DPLL are modelled and simulated respectively and the response of both systems are compared. The system component values for this example are filter capacitor C_1 = 20pF, filter resistor R_1 = 9kΩ, VCO gain $K_V = 10^6$, and charge pump gain $K_C = 10^{-6}$. In figure 6 a plot of the DPLL and LPLL phase step responses for a phase step of π is shown.

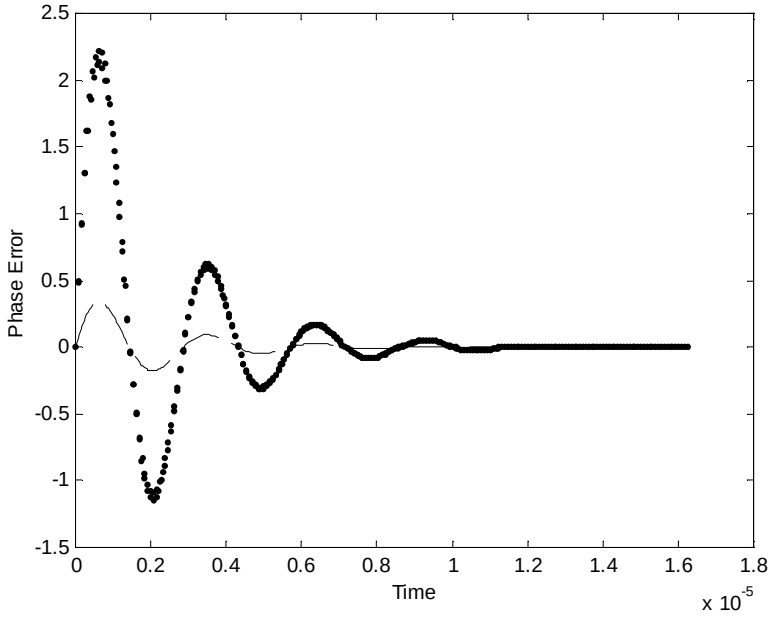

Figure 6: Phase error responses of LPLL(--) and DPLL(..)

Because of the non-linear nature of the DPLL the simulations show a difference in response, it is clear that this non-linearity causes the DPLL to be less stable. The difference in response of both signals in figure 6 is shown in figure 7 below. As the PLLs approach the locked state the phase difference between the DPLL and the LPLL is reduced. This is expected as the DPLL is assumed to be linear for a small phase error.

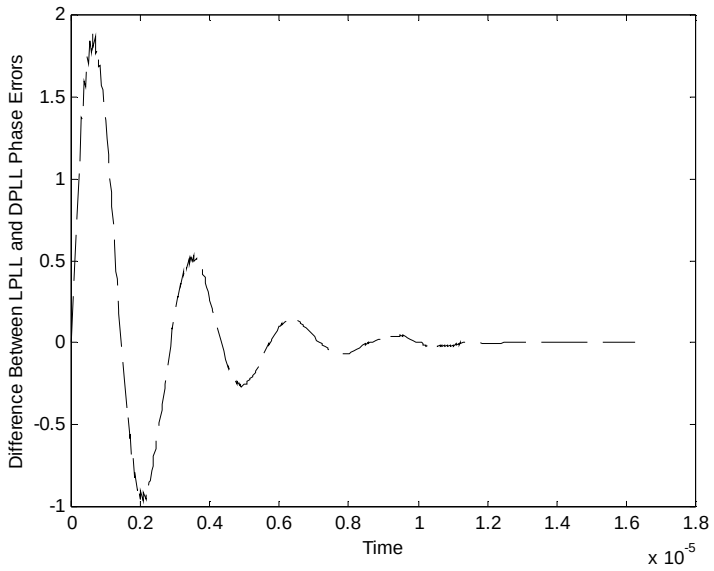

Figure 7: LPLL and DPLL phase error difference

The above simulation is extended to vary the phase step. Figure 8 shows the responses for the various phase step inputs as it varies from $\frac{\pi}{12}$ to π. As expected the difference between the LPLL and DPLL increases as the phase step is increased.

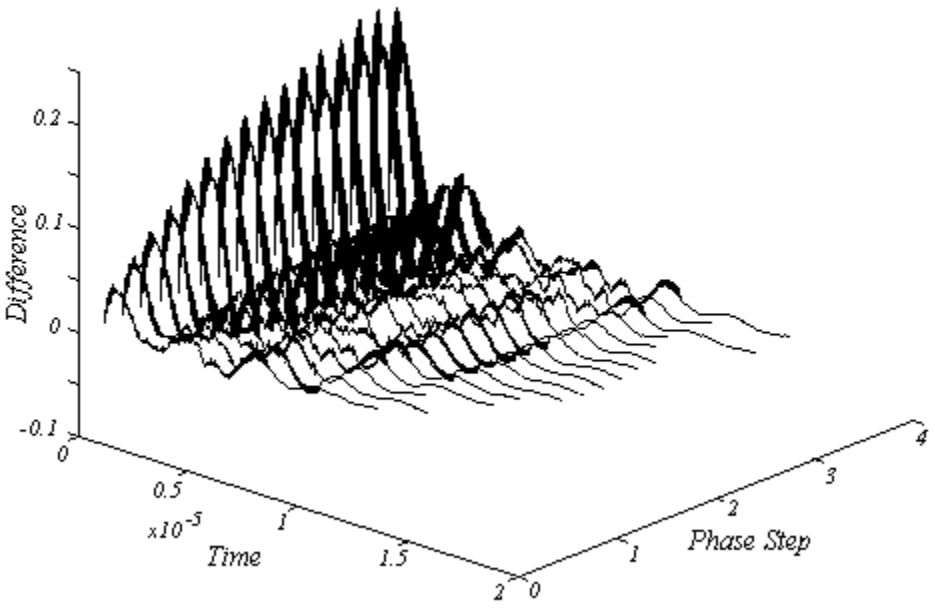

Figure 8: Difference for range of phase steps

Frequency step response

Similarly, the difference between the DPLL and the LPLL frequency step responses is increased as the frequency step size is increased. This is shown in figure 9 below.

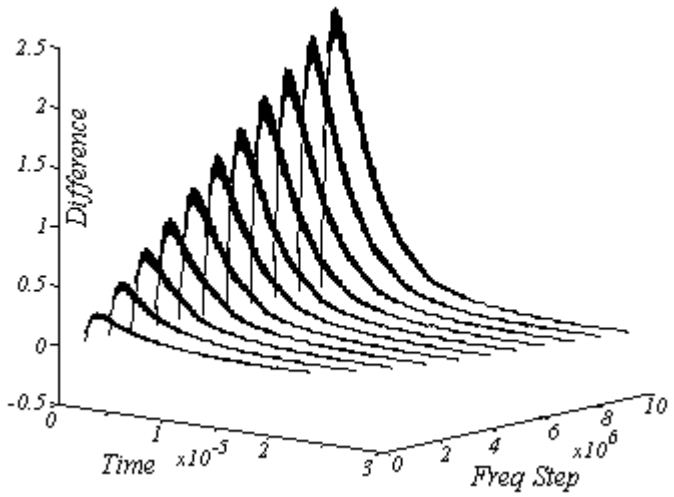

Figure 9: Difference for Variation of Frequency steps

From figure 8 and 9 it is clear that the difference between the DPLL and LPLL phase error response increases as either the phase step or frequency step sizes are increased. So the DPLL is more linear if it operates within a small region and does not deviate outside this region. In the next section the difference between the LPLL and DPLL as the reference frequency and the system bandwidth are increased is considered.

FILTER POLE PLACEMENT DIGITAL PLL DESIGN TECHNIQUE

In this section the Bessel filter design technique is used to design a stable high order digital PLL by optimally placing the poles of the PLL loop filter. In [1] the linear PLL model is used to design the digital PLL. The system is stable if the z-domain transfer function poles lie inside the unit circle. The poles of this system are placed using the Bessel filter design technique, and using the aforementioned root locus technique to obtain the maximum gain of the stable system. It is shown that a stable high order digital PLL with a sharp cut-off frequency can be designed.

The Bessel filter design technique optimally places the poles of the low pass filter system in an arc as shown in figure 10 below. This produces a sharp cut-off frequency at the desired frequency, in this case at a normalised cut-off frequency of $\omega_c = 1$.

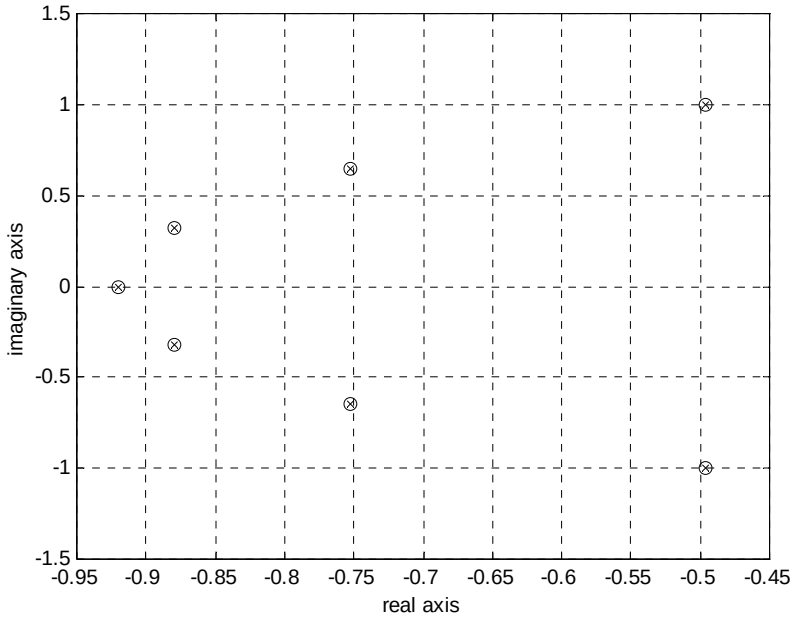

Figure 10: Plot of Bessel Filter Poles with normalised cut-off frequency

Figure 11 shows the magnitude responses of low pass filters, designed using standard PLL rules of thumb and various orders of Bessel filters, for a cut-off frequency of 10^6 rad/sec.

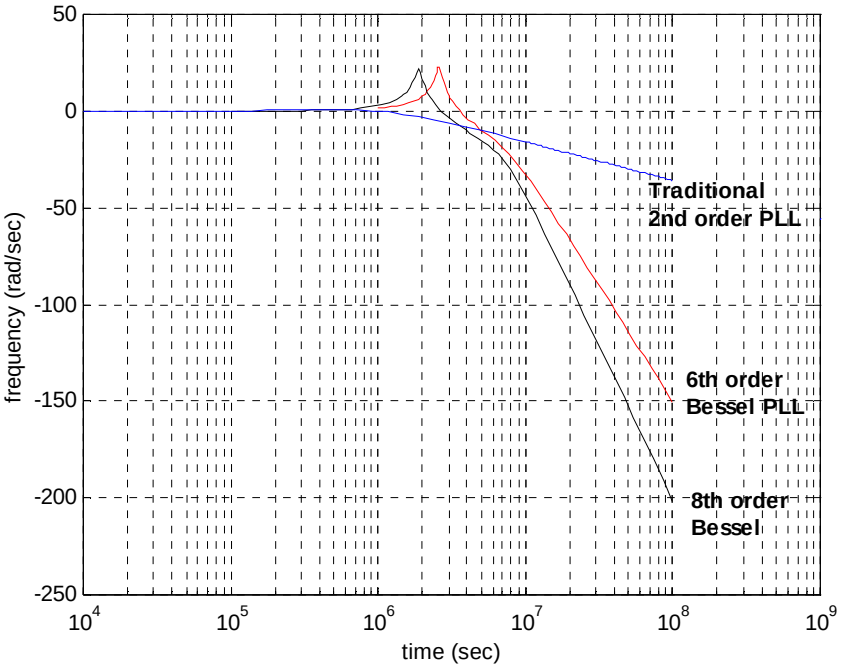

Figure 11: Plot of Traditional 2nd order PLL, 6th order PLL with Bessel filter
And an 8th order PLL with Bessel filter

It is obvious from the above plot that the Bessel filters have a much sharper cut off then the standard PLL filter.

Stability Criterion

The transfer function of the above Bessel filter is F(s), using this filter as the loop filter of the PLL, the transfer function of the closed loop PLL system is $H(s) = \frac{K_V K_C F(s)}{s + K_V K_C F(s)}$. A restriction on the value of K_{SYS} can be estimated using a root locus plot of the system poles as K_{SYS} increases. Where K_{SYS} is the sum of all gains in the DPLL system, these are the charge pump gain, the filter gain and the VCO gain, therefore $K_{SYS} = K_C * K_F * K_V$.

Using linear theory, in the z-domain the system is stable if all the poles lie inside the unit circle. The z-domain transfer function is found from H(s) using the bilinear transform, from this a root locus plot of the system poles as the gain increases from 0 up to K_{SB} is plotted. K_{SB} is the value of gain for the PLL with a pole on the unit circle this is illustrated in figure 12 as the stability boundary limit. It is intuitive that if the above stabilisation technique works then the system should be stable for values of $K_{SYS} < K_{SB}$ and unstable for values of $K_{SYS} >= K_{SB}$.

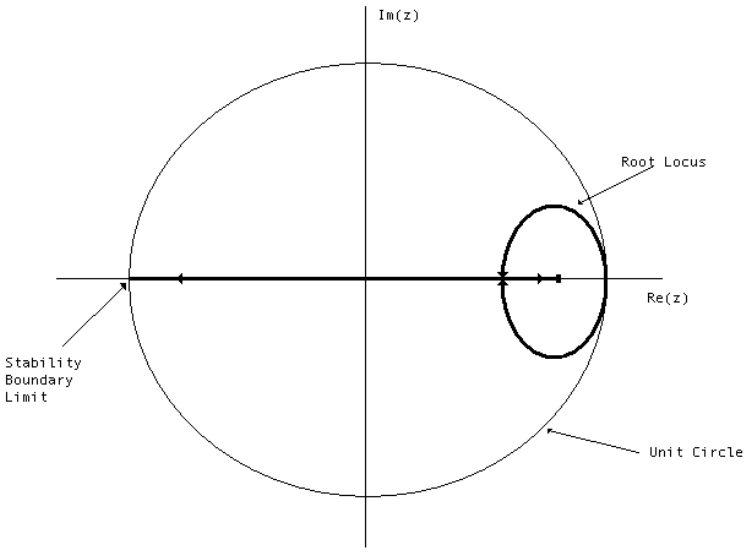

Figure 12: Root Locus Plot for a Second order PLL system

In the previous section, it was shown that by placing the poles of the PLL loop filter using the Bessel design technique, a sharper cut-off frequency is achieved. In this section it was shown that for any order of PLL system the stability is assured by placing a constraint on the gain K_{SYS} of the system by keeping all the poles inside the unit circle. An example of the root locus plot for a fifth order PLL is shown in figure 13. In the next section, both these techniques are used to design a stable high order PLL with a sharp cut off frequency.

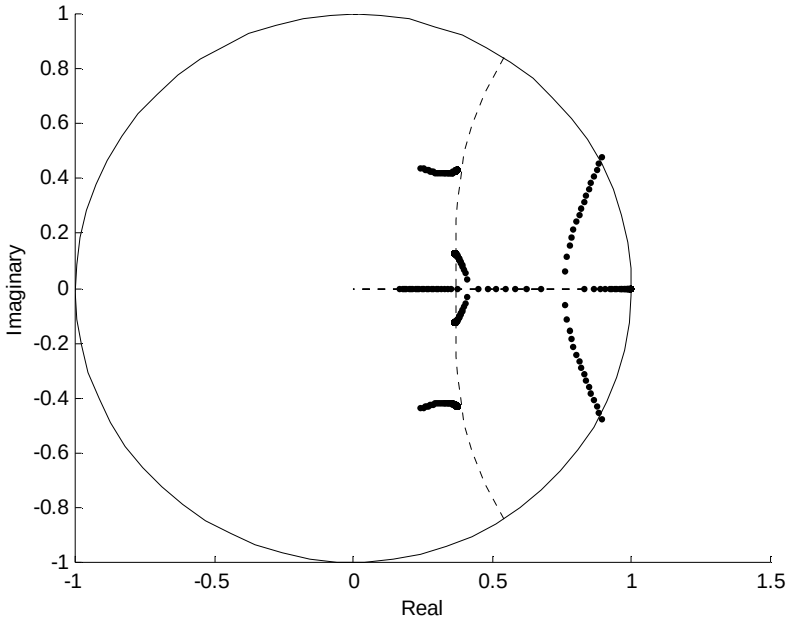

Figure 13: Root Locus Plot for a fifth order PLL system

High order PLL design using pole placement

For a PLL with a given frequency cut-off requirement of ω_c, the poles of the loop filter are optimally placed to achieve a sharp cut-off using the Bessel technique. The linear PLL system is then converted to the Z-domain using the bilinear transform. The root locus of this system is plotted while all the poles lie inside

the unit circle. K_{SB} is the gain at which a pole of the system lies on the unit circle. The required digital PLL can then be designed using the Bessel loop filter transfer function and a choice of gain that is stable and meets the transient requirements of the system.

The stability boundary of the Digital PLL is where the transient response of the system reaches a limit cycle, ie where the system oscillates about a point, this is illustrated in figure 14 below. The gain of this system K_{SYS} is equal to the gain at the stability boundary K_{SB}, therefore the system never decays to a stable point, and never expands to infinity.

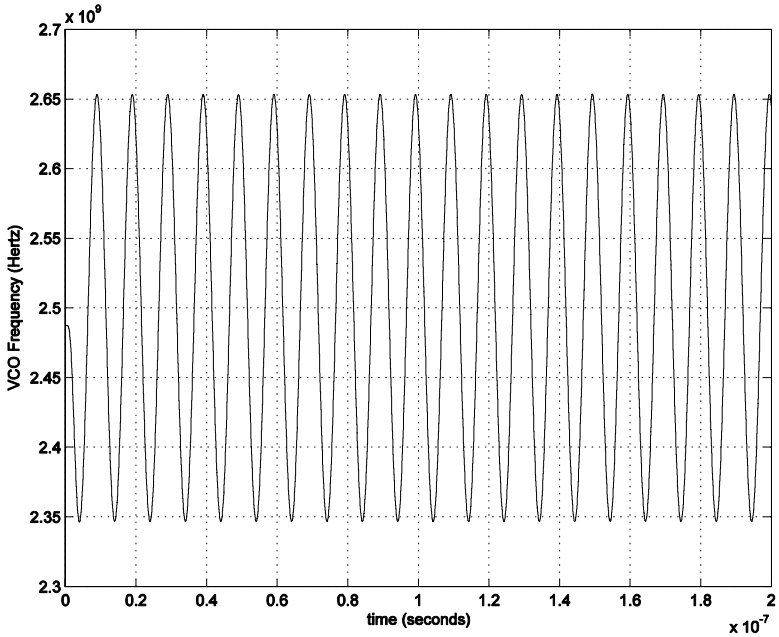

Figure 14: Asymptotically stable system response

Table 1 below shows the value K_{SB} for both the linear and digital PLL, for a range of frequencies from 1GHz up to 5GHz, estimated using the above definitions of the stability boundaries.

Frequency (GHz)	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5	5.0
K_{SB} of LPLL	2.88E+08	4.33E+08	5.77E+08	7.21E+08	8.65E+08	1.01E+09	1.15E+09	1.30E+09	1.44E+09
K_{SB} of DPLL	2.88E+08	4.33E+08	5.77E+08	7.21E+08	8.65E+08	1.01E+09	1.15E+09	1.30E+09	1.44E+09
% difference	0.012	0.017	0.021	0.023	0.032	0.036	0.042	0.045	0.052

Table 1: LPLL and DPLL stability boundaries

A plot of the percentage difference, figure 15 and 16, shows that the difference between the K_{SB} of the LPLL and the DPLL increases as the cut-off frequency of the system increases and as the filter cut-off frequency or system bandwidth increases. Therefore it is clear that the DPLL is more linear the lower the reference frequency and the smaller the bandwidth. This is as expected as the non-linearity of the CP-PFD is due to the switching of the CP-PFD state, the more frequent the switching period, during tracking or high frequency, the more non-linear the system becomes, and the linear approximation of the DPLL becomes less accurate.

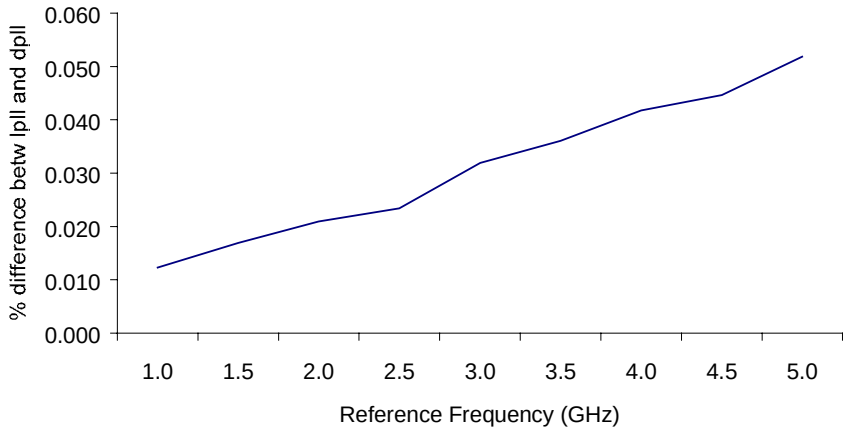

Figure 15: Plot of percentage difference between LPLL and DPLL stability boundaries as Frequencies increases

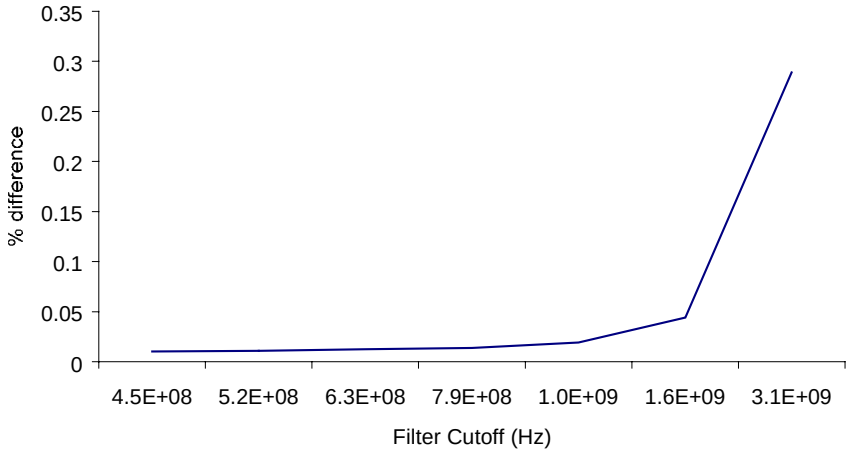

Figure 16: Plot of percentage difference between LPLL and DPLL stability boundaries as bandwidth increases

Figure 17 shows a plot of the Gain limit K_{SYS} for 4^{th}, 5^{th}, 6^{th}, and 7^{th} order linear PLLs. Any value of K_{SYS} chosen beneath the line will result in a stable system. Figure 17 shows that the gain limit increases as the linear PLL order is decreased.

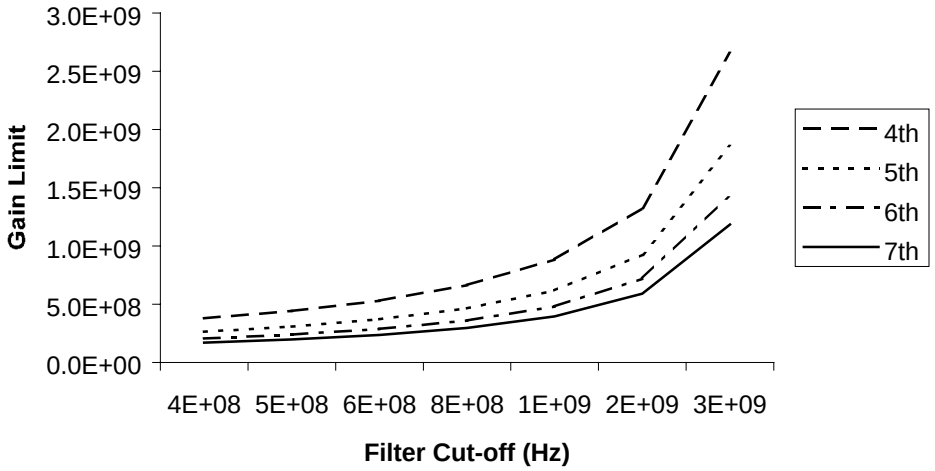

Figure 17: Plot of gain stability boundary for LPLL

The above case is for the LPLL, figure 18 shows the gain stability boundary of the DPLL for the same 4th to 7th order systems.

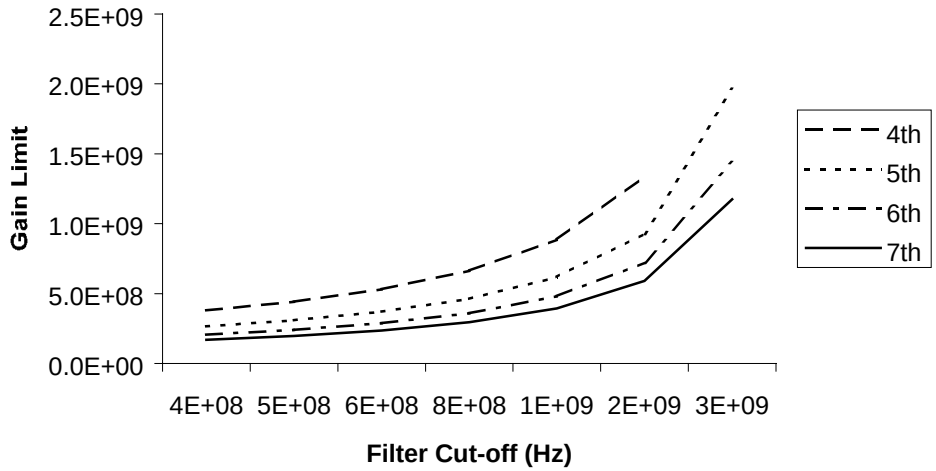

Figure 18: Plot of gain stability boundary for DPLL

Figure 18 is a plot of the DPLL systems of 4th order up to 7th and operating at a frequency of 1GHz. As the bandwidth of each system is increased the stability gain boundaries is increased. Similar to the linear PLL the boundary is increased as the order is decreased. The average difference between the LPLL gain boundary and the DPLL gain boundary is shown in figure 19 below. This shows that the difference between the boundaries is small, less then 0.02% for a cut-off frequency of a typical PLL with loop bandwidth of 1/10th the reference frequency. But this difference increases as the filter cut-off frequency (loop bandwidth) is increased.

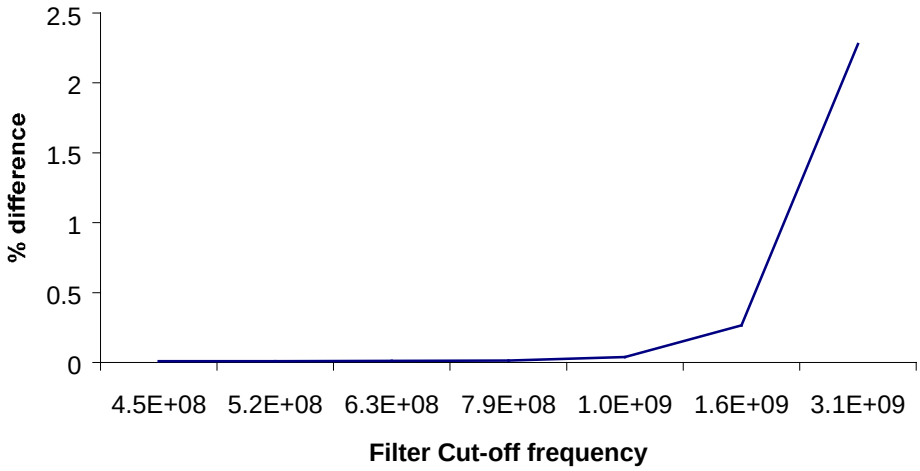

Figure 19: Plot of difference between the LPLL and DPLL gain boundaries
Against filter cut-off frequency

Similarly the difference between the LPLL and DPLL gain boundaries increases as the frequency is increased, this is shown in figure 20 below where the frequency is increased from 1GHz up to 5GHz.

Consider a 5th order PLL with a reference frequency of 12 MHz. In this example the Bessel filter design technique is used to place the poles of the DPLL loop filter. Using the root locus technique from above, K_{SB} for this system is estimated to be of magnitude 4.4e6. Therefore the system should be stable for values less then K_{SB} and unstable for values greater then $K_{SB.}$ In figure 20 below, the left hand plot is the system with a gain K_{SYS} of 4e6, this is stable. The plot on the right hand side is for a system of gain K_{SYS} = 4.5e6, and as expected it is unstable.

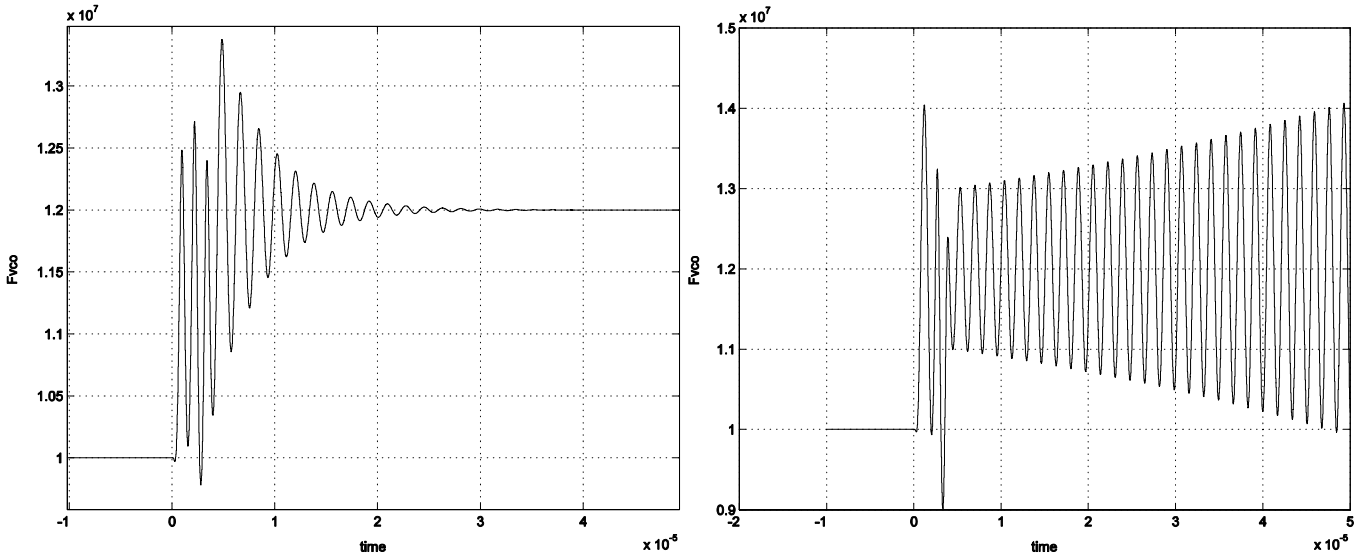

Figure 20: Plots of stable and unstable PLL either side of the boundary K_{SB}

Similarly for a 7th order PLL with a reference frequency of 1 GHz, K_{SB} is estimated to be 2.5e8. So plots of the system response to a gain of 2e8 and 2.6e8 are shown on the left and the right respectively, in figure 21.

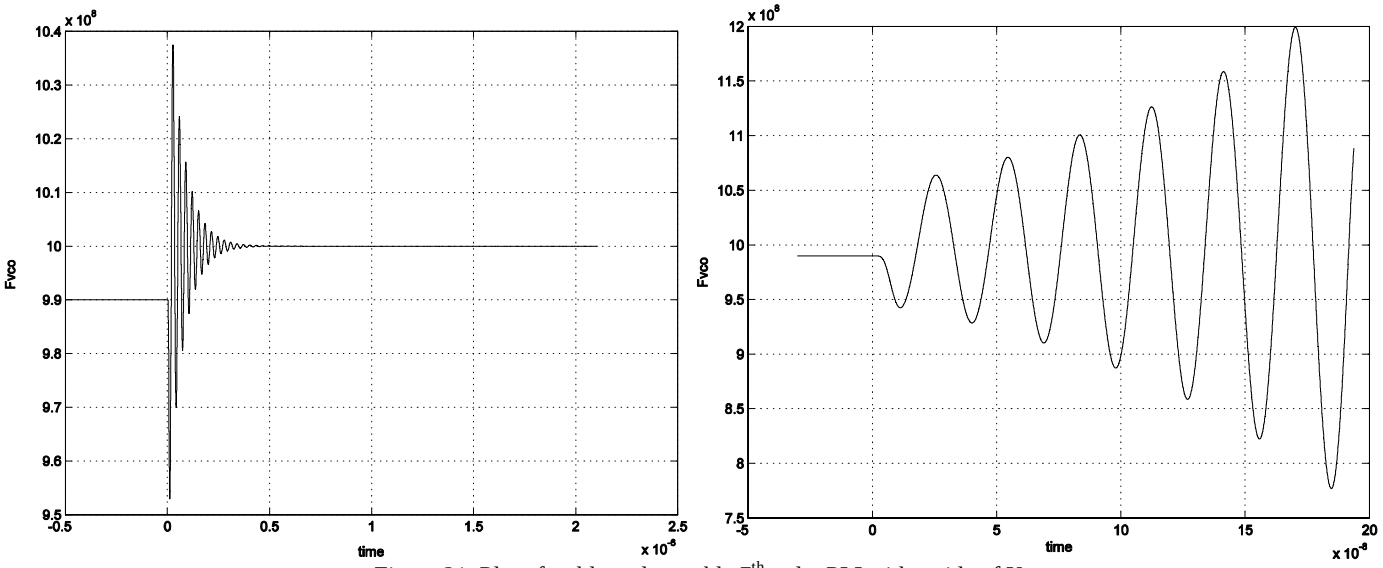

Figure 21: Plot of stable and unstable 7th order PLL either side of K_{SB}

In the above example it is clear that simulating the root locus of the PLL to find the stability boundary K_{SB} is an efficient method of designing a high order DPLL. By choosing the maximum stable gain a DPLL system can be designed that has the widest loop bandwidth or fastest lock time while ensuring stability. Some systems may require faster lock time and therefore values of K_{SYS} greater then K_{SB}, to achieve this it is possible to use a wide bandwidth DPLL initially to obtain lock and then to switch in the above narrow bandwidth DPLL once the system is locked. This technique is known as gear shifting and is covered in the next section.

GEAR SHIFTING OF THE SYSTEM BANDWIDTH

It has been shown that the DPLL is stable if all the poles of the equivalent LPLL lie inside the unit circle in the Z domain, however for values of K_{SYS} where the gain is too small the system will not produce fast lock. Adaptive PLLs are generally used to provide both fast-lock and low-jitter [5] by adjusting the loop bandwidth accordingly. This section proposes adapting the PLL parameters with the purpose of achieving high orders while maintaining stability. In the previous section it was shown that the DPLL has a similar response to the LPLL when the system bandwidth is small. For this reason it is feasible to design the DPLL using linear analysis as long as the DPLL bandwidth is small. However it is known that for fast lock time the DPLL bandwidth must be large. This introduces a performance trade off. The solution is adaptive PLLs or 'gear shifting'.

To obtain simultaneous fast lock and low jitter an adaptive PLL is used to dynamically adjust the bandwidth of the DPLL. The bandwidth of the DPLL is directly proportional to the closed loop gain of the system, the resistance of the loop filter, and is indirectly proportional to the divide ratio of the PLL. So the bandwidth may be adjusted by changing one of the following parameters:

1. Gain can be increased. This can be achieved by adaptively changing the charge pump current [6-9, 10,11,12].
2. Simultaneously decreasing the main divider N and the reference divider R [13]. In the out of lock state if the reference and feedback divide ratios are decreased and the reference frequency increased by factors of Q, an additional Q-fold bandwidth and settling speed enhancement can be achieved [4].
3. Loop filter bandwidth increased by adjusting the filter time constants [11,14,16]. This method requires a lock detector to control the switch.

In this case the system will initially have a large bandwidth which will produce a fast lock of the DPLL. However with a large bandwidth the output of the locked DPLL will have significant jitter. To reduce this a high order DPLL with poles optimally placed using Bessel filter theory is designed. This filter is then switched in once the DPLL has locked.

The filter structure is adapted by switching in or out either a new filter system, or filter components. In such a system, pre-charging of the switched-in components is necessary. Switching in an uncharged capacitor will cause the control voltage to drop sharply. This voltage drop will knock the PLL system away from lock causing either prolonged settling time or even instability.

CONCLUSION

In this paper it has been shown that a stable high order digital PLL using a Bessel filter can be designed. This technique uses the Bessel filter design criterion to choose a filter with an optimum cut-off frequency. Using standard linear theory, the PLL transfer function is converted from the s to the z-domain using the bilinear transform. The trajectory of the z-domain poles are then plotted for values of gain from zero up to the stability boundary K_{SB}. Using this stability boundary an optimum gain can be chosen to ensure the stability of the system. The results found show that the system operates as expected, displaying unstable transients for gains outside the stability boundary, and stable gains inside the stability boundary.

It has been shown that the response of the linear PLL is different to that of the DPLL. This is due to the non-linearity of the CP-PFD in the DPLL. However it was also shown that difference between the LPLL and the DPLL is proportional to the bandwidth – for narrow bandwidth DPLLs, filter cut-off of less then $1/10^{th}$ of the reference frequency, the DPLL can be accurately modelled using the linear theory. Similarly it was shown that the difference is proportional to the reference frequency.

REFERENCES

[1] F.M. Gardner, "*Charge pump phase lock loops*", IEEE Trans. Commun., vol. COM-28, pp. 1849-1858,Nov 1980.

[2] Teresa M. Almeida, and Moises S. Piedade, "*High Performance Analog and Digital PLL design*", IEEE 1999

[3] Yao Puqiang, Zhang Juesheng, Du Wulin, "*Research about LL-DPLL Changing Order Automatically*", International conference on Circuits and Systems, 1991

[4] Brian Daniels, Ronan Farrell, Gerard Baldwin, '*Arbitrary Order Charge Approximation Event Driven Phase Lock Loop Model*', ISSC 2004

[5] Minoru Kamata, Takashi Shono, Takahiko Sabo, Iwao Sasase, and Shinsaku Mori, "*Third-Order Phase-Locked Loops using Dual Loops with Improved Stability*", IEEE J Solid-State Circuits 1997

[6] Joonsuk Lee, Boemsup Kim, "*A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control*", IEEE J Solid-State Circuits 2000

[7] G Roh, Y Lee, B Kim, "*Optimum Phase-Acquisition Technique for Charge-Pump PLL*", IEEE Trans. On Circuits and Systems 1997

[8] C Vaucher, "*An Adaptive PLL Tuning System Architecture Combining High Spectral Purity and Fast Settling Time*", IEEE J Solid-State Circuits 2000

[9] J Maneatis, J Kim, I McClatchie, J Maxey, M Shankaradas, "*Self-Biased High-Bandwidth Low-Jitter 1-to-4096 Multiplier Clock Generator PLL*", IEEE DAC 2003

[10] J Lee, B Kim, "*A 250MHz Low Jitter Adaptive Bandwidth PLL*", IEEE ISSCC 1999

[11] S Sidiropoulos, D Liu, G Wei, M Horowitz, "*Adaptive Bandwidth DLLs and PLLs using Regulated Supply CMOS Buffers*", IEEE Symposium on VLSI 2000

[12] K Nagaraj, R Shariatdoust, "*Adaptive Charge Pump for Phase-Locked Loops*", US Patent 5,208,546 1993

[13] D Nelson, L Sun, "*Low-Noise, Fast-Lock Phase-Lock Loop with "gearshifting" Control*", US Patent 6,504,437 2003

[14] Yiwu Tang, Yingjie Zhou, Steven Bibyk, Mohammed Ismail, "*A Low-Noise Fast Settling PLL With Extended Loop Bandwidth Enhancement By New Adaptation Technique*", IEEE J Solid-State Circuits 2001

[15] Takao Tsukutani, Yasuaki Sumi, Masami Higashimura, Yutaka Fukui, "*Electronically Tunable Low-Pass Filter in PLL Frequency Synthesizer*", IEEE J Solid-State Circuits 2001

[16] Yao Fuqiang, Zhang Juesheng, Du Wulin, "*Research About LL-PLL Changing Order Automatically*", IEEE International Conference on Circuits and Systems 1991

[17] M Toyama, S Dosho, N Yanagisawa, *"A Design of a Compact 2GHz-PLL with a New Adaptive Loop Filter Circuit"*, IEEE Symposium on VLSI 2003