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# Modeling and Layout Optimization of Differential Inductors for Silicon-Based RFIC Applications

Choon Beng Sia, Beng Hwee Ong, Wei Meng Lim, Kiat Seng Yeo, and Tariq Alam

*Abstract*—A scalable RF differential inductor model has been developed, enabling device performance versus layout size trade-offs and optimization as well as accurate circuit predictions. Comparing inductors with identical inductance values up to an operating frequency of 10 GHz, large conductor width designs are found to yield good performance for inductors with small inductance values. As differential inductance or operating frequency increases, interactions between metallization resistive and substrate losses discourage the use of large widths as it consumes silicon area and degrades device performance.

*Index Terms*—Common mode rejection ratio (CMRR), differential, differential amplifier, ground-signal (GS), ground-signal-ground (GSG), ground-signal-signal-ground (GSSG), inductance, inductor, layout, mixed-mode *S*-parameter, optimization, quality factor.

## I. INTRODUCTION

**D**IFFERENTIAL modulation schemes for low cost transceivers have motivated strong research interest in silicon-based on-chip differential inductors [1]–[5]. Interwinding two coils together, differential inductors consume a smaller silicon area, thus reducing the overall chip size. They also exhibit a higher quality factor over a broader range of frequencies, making them essential device components for radio frequency integrated circuit (RFIC) design. Despite these advantages, such inductors are not readily available in silicon-verified device libraries but only offered by established semiconductor foundries. Reliable techniques to optimize the physical design of differential inductors are also not well established in the literature. Impacts of each inductor physical design parameters such as core diameter and width, methodologies to optimize these parameters, and availability of silicon-verified inductor libraries having small incremental steps of inductance values are crucial criteria for one-pass circuit design success and optimization. In short, circuit designers must have accurate and scalable device models, empowering them with full flexibilities and freedom to choose and tradeoff between device performance and device size conveniently. This paper, an extension of the work from [6] and [7] presents an accurate and scalable differential inductor model to address the growing demands of differential design trends for RFICs, allowing physical layout of differential inductors to be optimized either for small area-driven or high performance-driven circuit designs.

## II. TEST STRUCTURE DESIGN CONSIDERATIONS AND EXPERIMENTAL SETUP

An extensive set of differential inductor test structures, fabricated using 0.18 $\mu$m RFCMOS processing technology, has been designed to extract a scalable differential inductor model and allow for application-specific performance optimization. Fig. 1(a) shows the die photo of a circular differential inductor. Its two spiral coils consist mainly of thick top metal 6 with metal 5 as underpasses to avoid shorting the two coils. The center-tap, a common ac ground where the two coils are connected, is routed out from the center of the differential inductor with metal 4. The test element group in this paper consists of two, four, six, and eight even-turn differential inductors with core diameters ranging from 30 to 180 $\mu$m in steps of 30 $\mu$m. The metal-to-metal spacing of the differential inductors is kept constant at 3 $\mu$m. Metal width, varies from 4 to 28 $\mu$m for two and four-turn inductors and 4 to 12 $\mu$m for six and eight-turn inductors, with both sets spaced in steps of 4 $\mu$m.

Several objectives are to be achieved designing the test element group in this manner. One important goal is to have small incremental inductance steps within the library of differential inductors. Changing the inductor's number of turns will result in inductors with quarter, half or three-quarter turns having big inductance steps in between these turns. On the contrary, incrementing the core diameter in small $\mu$m steps offers small and gradual change in its differential inductance, essential in facilitating efficient circuit optimization, managing circuit postlayout interconnect effects as well as swift design migrations for circuits with conventional spiral inductors to differential inductors. In addition, this approach also allows input/output leads of differential inductors to be established in a fixed orientation, making the overall chip floor-planning a convenient task for IC layout engineers. Inductors with large core diameters are usually preferred because they have a high quality factor due to a small conductor eddy current effect [7]. Inductors having small core diameters, however, cater for situations for which circuit performance can be compromised to achieve area-efficient chips. Finally, permutations of conductor width enable performance optimization for a wide range of inductance values over various application frequencies.

The Agilent 8510C Vector Network Analyzer and Cascade Microtech Infinity probes (which offer low and stable contact resistance) are used to characterize the differential inductors. Wafer and RF probes are shielded within the Microchamber of the semiautomated probe station when measuring two-port $S$-parameters of the inductors up to 20 GHz. P+ taps near the inductors are included to ensure effective grounding of
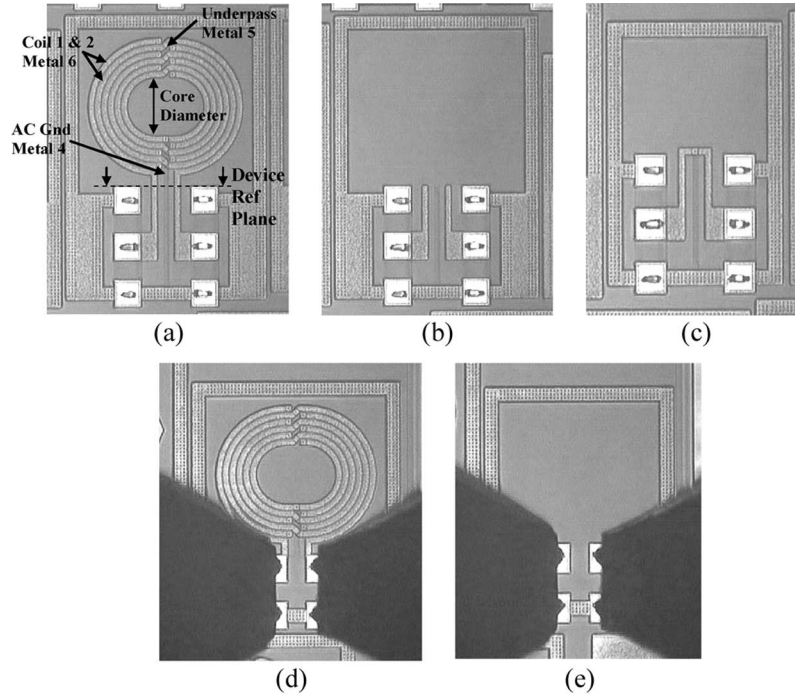
Fig. 1.   Die photos showing differential inductor layouts in GSG configuration [inductor (a) open (b) and short calibration structures (c)] and in GS configuration [inductor (d) and open calibration structure (e)].

the substrate. The ground-signal-ground (GSG) configuration shown in Fig. 1 is the popular technique to layout full turn differential inductors for on-wafer RF characterization. Two deembedding structures, open [Fig. 1(b)] and short [Fig. 1(c)] remove pad capacitive parasitic, test leads parasitic resistance and inductance, respectively, moving the device/measurement reference plane to the inductor input/output leads shown in Fig. 1(a). With an extra set of ground pads and additional short calibration structure, such method of characterizing the inductor requires more silicon real estate. Also, the short deembedding procedure has high tendencies of introducing over deembedding errors, leading to deceivingly high quality factor if high contact resistance is experienced during probing of the short calibration structure. For this paper, a ground-signal (GS) configuration approach [in Fig. 1(d)] without the need for a short deembedding structure is used. Capacitive parasitics of the test pads are accurately deembedded by subtracting $Y$-parameters of the open calibration structures from test structures with the inductors [8]. Fig. 2 shows excellent correlations between deembedded intrinsic characteristics of differential inductors for the GSG and GS layout schemes. More importantly, the proposed GS layout approach minimizes deembedding errors and yielded a significant 44% reduction in test chip size.

## III. FIGURE OF MERITS AND RF SUBCIRCUIT MODEL

Differential inductors' figure of merits, differential inductance, $L_{\text{DIFF}}$ and differential quality factor, $Q_{\text{DIFF}}$ used in this paper are obtained from the deembedded $S$-parameters shown in (1)–(4) [9]. The differential one-port $S$-parameter
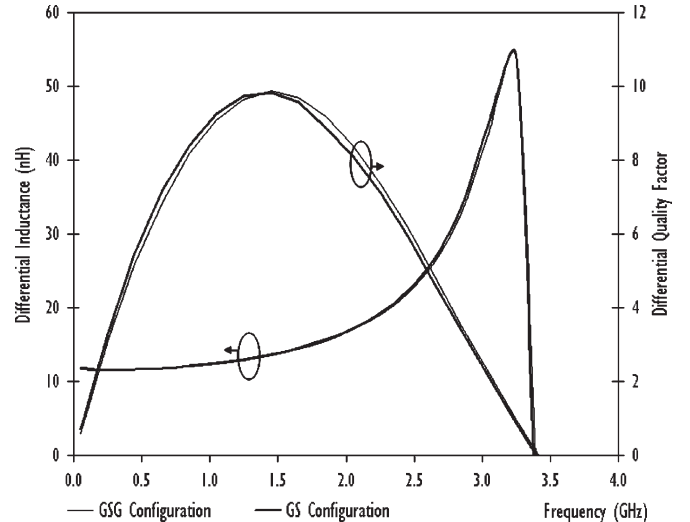


Fig. 2.   Differential inductance and quality factor versus frequency for the same differential inductor in GSG and GS layout configurations.

is first obtained from the deembedded $S$-parameters as follows:

$$S_{\text{DIFF}} = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2}. \quad (1)$$

With $Z_o$ as the differential system impedance, the differential $Z$-parameter is derived as

$$Z_{\text{DIFF}} = \frac{2Z_o(1 + S_{\text{DIFF}})}{1 - S_{\text{DIFF}}}. \quad (2)$$

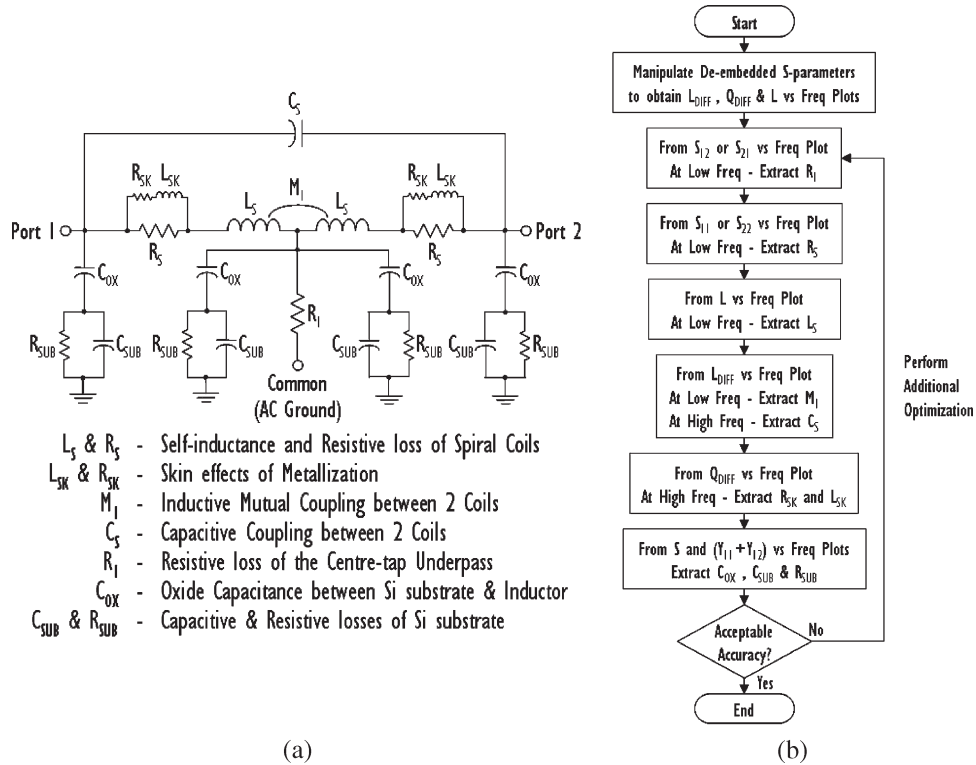(a)                                                                     (b)

Fig. 3.   (a) SPICE-compatible RF subcircuit model and its (b) model extraction strategy for differential inductor.

Differential inductance and quality factor are evaluated from the differential $Z$-parameter as

$$L_{\text{DIFF}} = \frac{\text{Imag}(Z_{\text{DIFF}})}{2 \times \pi \times \text{Frequency}} \qquad (3)$$

$$Q_{\text{DIFF}} = \frac{\text{Imag}(Z_{\text{DIFF}})}{\text{Real}(Z_{\text{DIFF}})}. \qquad (4)$$

The inductance related to single-ended excitation (at Port 1) to decouple the inductive mutual coupling effects between the two spiral coils can be evaluated as

$$L = \frac{\text{imag}\left[Z_o \times \left(\frac{1+S_{11}}{1-S_{11}}\right)\right]}{2 \times \pi \times \text{Frequency}}. \qquad (5)$$

Fig. 3 depicts the proposed scalable differential inductor lumped-element RF subcircuit model and its extraction strategy for this paper. In the suggested extraction methodology, $R_S$, $L_S$ and $R_1$ must first be determined to ensure that subsequent model parameters obtained are physical and accurate. This is particularly so for $L_S$ because the measured $L_{\text{DIFF}}$ is a contribution of both self-inductance from individual coils as well as mutual coupling effect from both spiral coils. To accurately resolve the amount of mutual coupling $M_1$, $L_S$ must be established first from the $L$ versus frequency plot and then $M_1$ from $L_{\text{DIFF}}$ plot. Elements such as $R_{\text{SK}}$ and $L_{\text{SK}}$, which model the skin effects can be extracted focusing on the high frequency portion of $Q_{\text{DIFF}}$ versus frequency plot. In contrast to techniques that model skin effects using resistive elements described by frequency-dependent equations, this approach develops device models that are compatible with SPICE simulators.
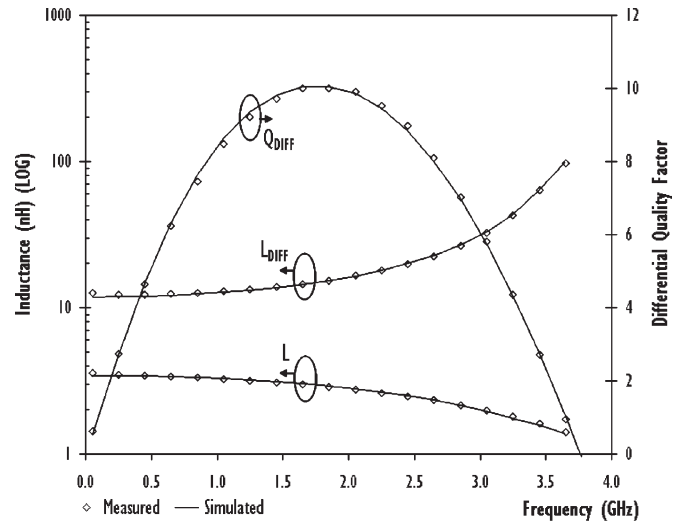


Fig. 4.   Simulated versus measured inductance due to single-ended excitation, $L$, differential inductance $L_{\text{DIFF}}$ and quality factor $Q_{\text{DIFF}}$ for six-turn differential inductor with core diameter and width of 180 and 12 $\mu$m, respectively.

The differential inductor model and its extraction methodology set forth in this paper are both physical and simple to understand. Most published subcircuit models are complex, lacking clear procedures for precise extraction of the mutual coupling coefficient $M_1$ [10]–[12]. Accurate determination of $M_1$ and $L_S$ is very important particularly for one-turn differential inductors with small core diameters as they have negative coupling coefficients for $M_1$. Also, the proposed modeling methodology has been tested extensively with a total of 120 differential inductors. On the contrary, in the literature, limited test structures with small physical design parameter variations
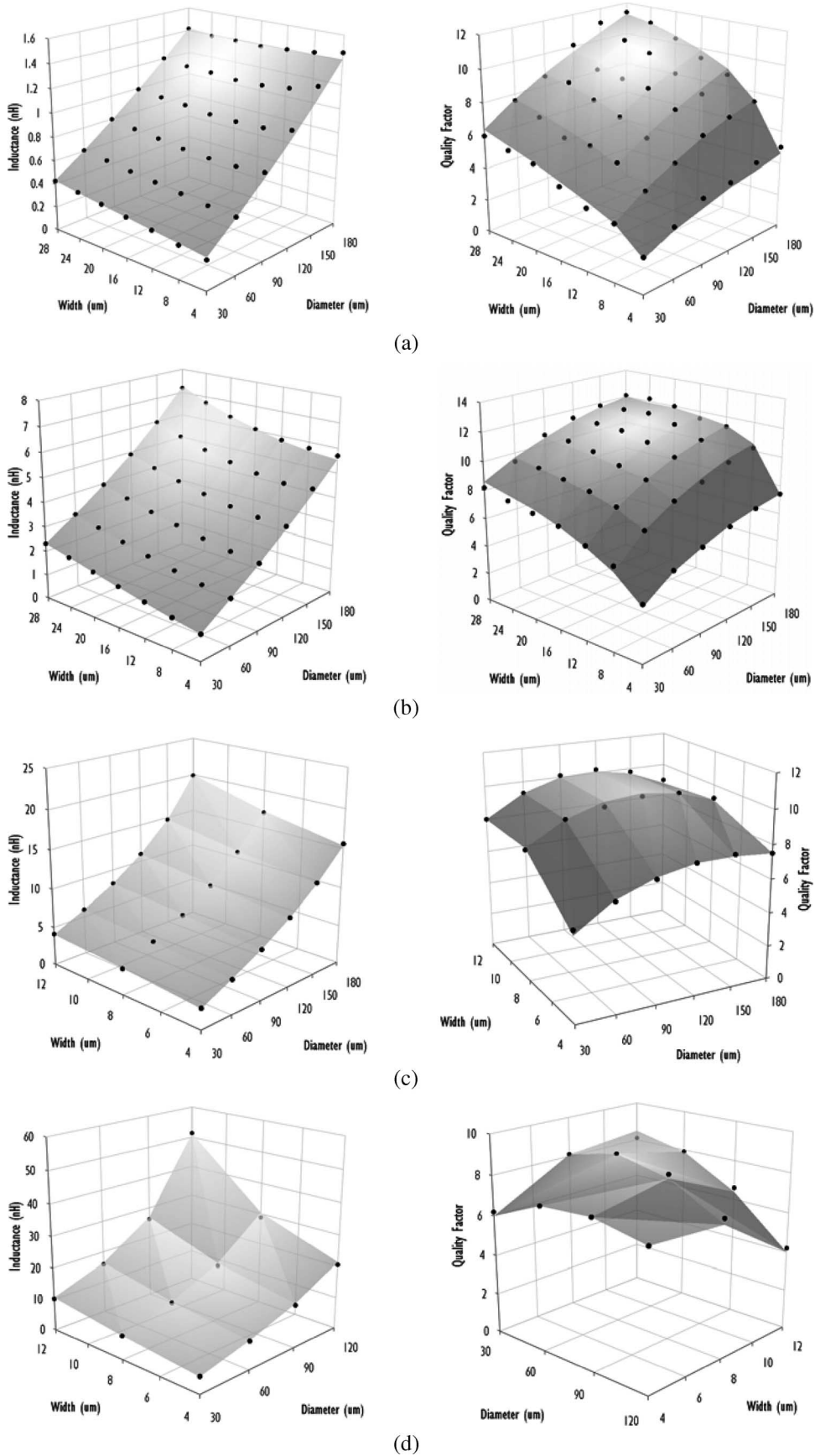
Fig. 5.   RF differential inductor model continuity–simulated (surface) and measured (dots) differential inductance and quality factor versus diameter and width at 2.45 GHz for (a) two-turn, (b) four-turn, (c) six-turn, (d) eight-turn differential inductors.

are often used to qualify model validity, accuracy and even scalability [12]–[14].

## IV. MODEL ACCURACY, CONTINUITY AND DESIGN TRADE-OFFS

Automated full map on-wafer RF measurements with die alignment and wafer thickness corrections are performed to determine the "golden die." Consistent "skating" of the RF probes on the test pads to achieve good ohmic contact is vital to ensure that deviations in the measured device characteristics across the wafer are predominantly due to process variations. Such full wafer map analysis assures that measurement data for device modeling are obtained from a typical die and this helps prolong validity of device models as processing technology matures along with the implementation of yield enhancement techniques. The subcircuit elements in the scalable RF model are extracted using IC-CAP, Agilent's device characterization and modeling software. These model parameters are then each formulated with empirical functions that best emulate (with the smallest error) their relationships with respect to the inductors' turns, core diameter and width. Fig. 4 shows how well this model can match the measured $L$, $L_{\mathrm{DIFF}}$, and $Q_{\mathrm{DIFF}}$ for a six-turn differential inductor. With the extraction methodology of first determining $L_S$ using the $L$ plot, $M_1$ is found to be 0.81 when fitting $L_{\mathrm{DIFF}}$ at low frequency. To maintain a reasonable paper length for this paper, 2.45 and 5.05 GHz are selected to scrutinize the model accuracy. It has been found that at 2.45 and 5.05 GHz, for majority of useful inductors in the test element group that have yet to operate beyond their self-resonant frequencies, model deviations between the measured and simulated differential inductance and quality factor are within $-3\%$ to 4% and $-4\%$ to 8% correspondingly. This differential inductor model has clearly demonstrated outstanding predictability and accuracy.

Fig. 5 shows that at 2.45 GHz, the scalable RF model is accurate and continuous within all the test structures having various turn, core diameter, and conductor width. A huge device library with 5436 differential inductors can be derived from this scalable RF model when the core diameter and conductor width are swept in steps of 1 and 2 $\mu$m, respectively. Excellent linear change in inductance has been observed for the differential inductors when their core diameter increases from 30 to 180 $\mu$m (except for eight-turn inductors with diameter $> 120$ $\mu$m which experience self-resonance). This reaffirms the fact that a library of inductors with fine inductance steps is achievable when the diameter is swept at 1 $\mu$m step.

Fig. 6 shows the differential inductance and quality factor versus frequency plots for 1 and 5 nH inductors at 2.45 GHz. From these two graphs, varying and optimizing the core diameters in 1 $\mu$m steps allow inductors of different conductor widths to have identical inductance values and hence, nonbiased performance comparisons. The overall conductor lengths for 1 nH inductors with widths of 4, 8, 12, 16, 20, 24, and 28 $\mu$m are evaluated to be 1004, 1092, 1180, 1269, 1351, 1433, and 1508 $\mu$m, respectively, reiterating the fact that the per unit length inductance of the metal line is inversely proportional to its conductor width. On the other hand, 5 nH differential
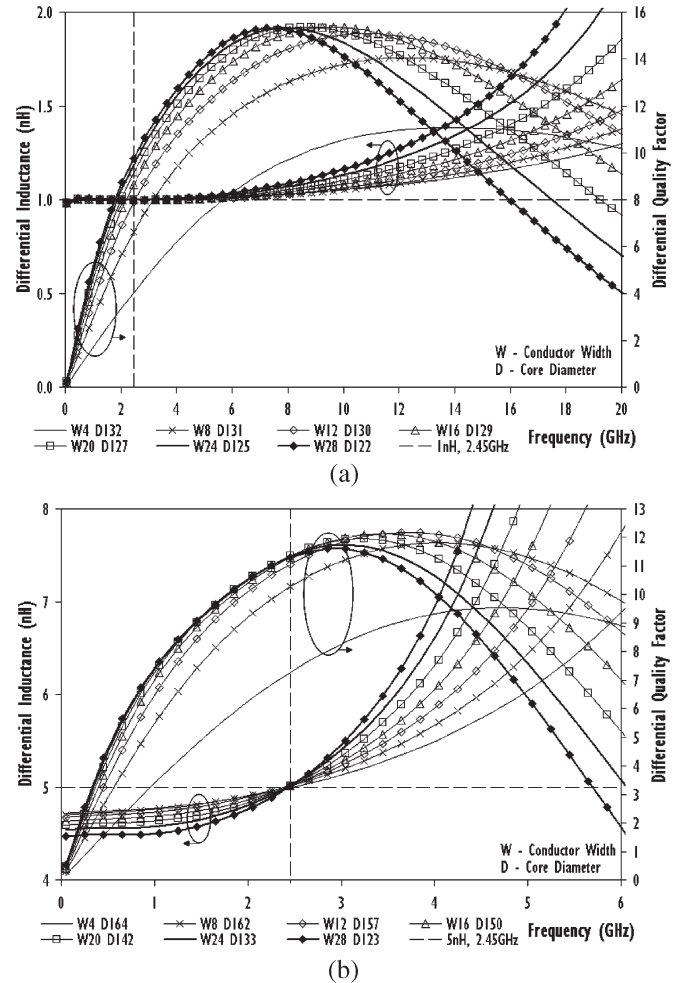


Fig. 6. Differential inductance and quality factor versus frequency for (a) 1.0 nH and (b) 5.0 nH differential inductors at 2.45 GHz.

inductors with widths larger than 12 $\mu$m are designed to have smaller low-frequency inductances, taking into consideration self-resonance and substrate loss effects to ensure that they would have exactly 5 nH at 2.45 GHz, making fair device performance comparisons possible. This is the first time such experimental studies and comparisons, particularly at frequencies of more than 2 GHz, are performed through the use of an accurate scalable differential inductor model.

Fig. 6 concludes that at 2.45 GHz, wider conductor width for differential inductors reduces the resistive loss at low frequencies, thereby improving $Q_{\mathrm{DIFF}}$. Although implementing such design approach trades off substantial chip area for better device performance, an optimal width exists beyond which any further use of larger width and silicon real estate would render this technique ineffective. To demonstrate this, using a conductor width of 16 $\mu$m instead of 4 $\mu$m for 1 nH inductors, improves $Q_{\mathrm{DIFF}}$ significantly from 4.0 to 8.7 (115%) with a corresponding 73% increase in the device size. However, an increase in width from 4 to 28 $\mu$m leads to a 142% $Q_{\mathrm{DIFF}}$ improvement but expands the inductor overall size enormously by more than 158%. For 1 nH inductors, the optimal width at 2.45 GHz is therefore 16 $\mu$m and that for 5 nH inductors is determined to be 12 $\mu$m. Large-inductance inductors generally require huge total conductor length and therefore, a sizeable
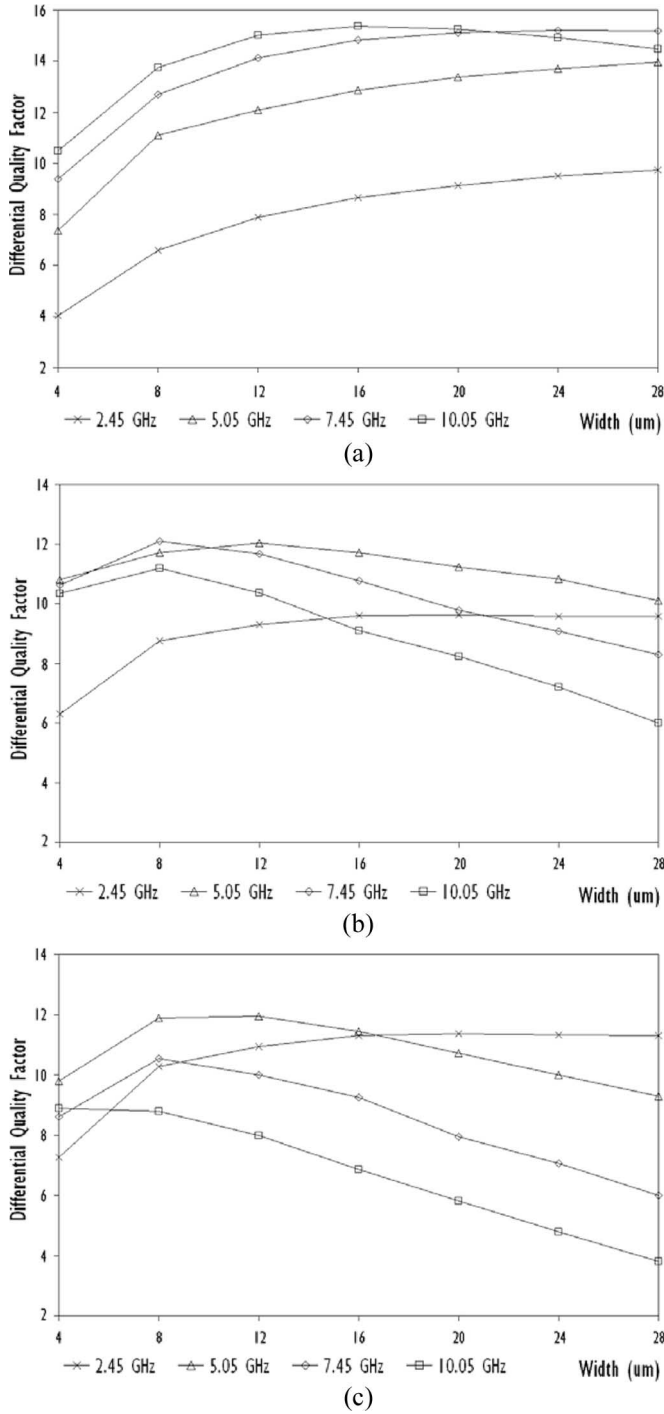
(a)



(b)



(c)

Fig. 7. Differential quality factor versus conductor width for (a) 1.0 nH, (b) 3.0 nH, and (c) 5.0 nH differential inductors at various operating frequencies of 2.45, 5.05, 7.45, and 10.05 GHz.
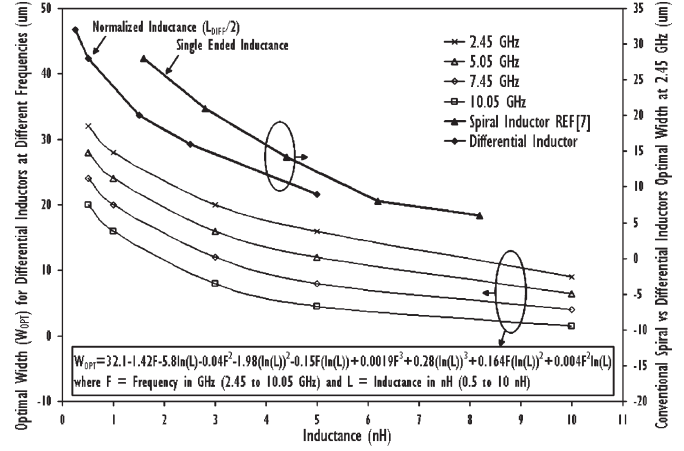


Fig. 8. Optimal width for differential inductors at operating frequencies of 2.45, 5.05, 7.45, and 10.05 GHz and comparing optimal width for conventional spiral and differential inductors at 2.45 GHz.

small-inductance differential inductors, large conductor width improves $Q_{\mathrm{DIFF}}$ tremendously, apparent for 1 nH inductors up to 10.05 GHz. Such phenomenon as explained earlier on is attributed to the reduction in resistive loss at the expense of chip area, which for these small inductors, do not significantly degrade their high frequency performance since their total conductor lengths are still fairly short. Meanwhile, as differential inductance increases, particularly at higher operating frequencies, tradeoffs between resistive and substrate loss results in the existence of optimal widths such that beyond these widths, any further use of larger conductor width do not improve $Q_{\mathrm{DIFF}}$ but waste expensive silicon area. This is evident for 5 nH inductors in Fig. 7(c) which show degradations in $Q_{\mathrm{DIFF}}$ for operating frequencies of 5.05, 7.45, and 10.05 GHz when conductor width of more than 8 $\mu$m is used. The left $y$-axis on Fig. 8 summarizes the three graphs in Fig. 7, describing the optimal widths versus inductance values at various operating frequencies. For a particular application frequency and required inductance, one can make use of the equation in Fig. 8 to determine the optimal width to be used for the differential inductor.

The right $y$-axis on Fig. 8 compares, for the first time, optimal width between conventional spiral inductors in [7] and the differential inductors in this paper at 2.45 GHz through normalization of the differential inductance ($L_{\mathrm{DIFF}}/2$). At the same inductance value, differential inductors have the huge advantage of requiring 30% smaller optimal conductor width compared to conventional spiral inductors, suggesting further device size reduction when using and optimizing differential inductors for RF circuits. The results in this section highlighted the great potential of building device libraries with application-specific differential inductors having optimized layouts which will save model development time and test chip cost.

## V. MODEL VERIFICATION USING DIFFERENTIAL GIGAHERTZ AMPLIFIER

Accuracy of the scalable differential inductor model is evaluated using a 2.4 GHz amplifier with an expected gain of about 15 dB in the same 0.18 $\mu$m RFCMOS technology as shown in Fig. 9(a) and (b). Adopting inductive source degeneration

chip area is necessary to generate the required self inductance. Employing narrower conductor width and thus shorter total conductor length (narrow width conductor have larger per unit length inductance) attractively results in smaller inductor size, lower substrate loss and better device performance all at the same time.

Comparing 1, 3, and 5 nH at 2.45, 5.05, 7.45, and 10.05 GHz, again ensuring that inductors with identical inductance values are compared, plots of differential quality factor at these frequencies versus conductor width are consolidated in Fig. 7. For
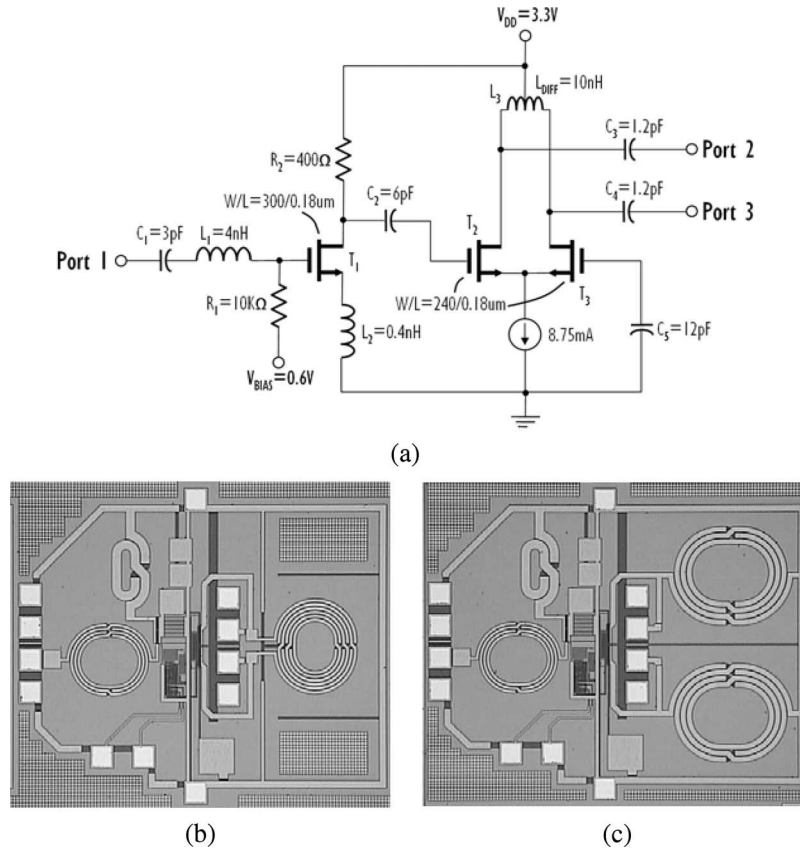
(a)

(b)          (c)

Fig. 9. (a) Circuit schematic and (b) die photo of a 2.4 GHz single-ended-to-differential amplifier with differential inductor. (c) Die photo for differential amplifier with conventional spiral inductor.

input matching technique, the input transistor $T_1$ is matched to the external 50 $\Omega$ system at 2.4 GHz with $L_1$, $L_2$, and $C_1$. $V_{BIAS}$ provides the gate biasing to $T_1$ and $R_1$ isolates the RF input signal. $T_2$ and $T_3$ make up the second stage differential transistor pair with $C_2$ and $C_5$ as the dc blocking and ac grounding capacitors, respectively. The differential inductor $L_3$, together with $C_3$ and $C_4$, provides 50 $\Omega$ load matching at the output ports. An optimal conductor width of about 8 $\mu$m has been selected for $L_3$ ($L_{DIFF} = 10$ nH), a tradeoff between size and $Q_{DIFF}$ performance at 2.4 GHz.

Pad capacitances have been taken into account during circuit simulations and hence, pad parasitic deembedding is not required. RF interconnect model is utilized to evaluate and tackle the postlayout effects contributed by metal interconnects routed between devices [15]. Typical dies for circuit tests are selected based on full wafer map device characteristics obtained from RF scribe-line process monitoring test structures [16]. Cascade Microtech Dual Infinity GSSG probes, Agilent four-port performance network analyzer and hybrid calibration technique [17] are used for performing the on-wafer circuit characterization. Source power selection of $-17$ dBm on the network analyzer ensures that the differential amplifier is in the linear mode of operation. Fig. 10 shows the simulated versus measured three-port $S$-parameters of the amplifier. Acceptable circuit predictions of measured matching characteristics have been achieved at all input and output ports. Deviations for gain predictions at 2.4 GHz are kept within 2.7% for both $S_{21}$ and $S_{31}$. Excellent correlations between measured and simulated amplifier charac-
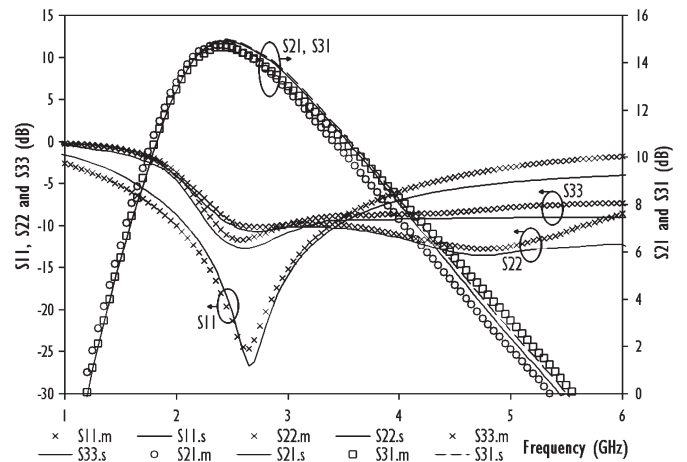


Fig. 10. Simulated (.s) and measured (.m) three-port $S$-parameters versus frequency characteristics for a gigahertz amplifier with differential inductor.

teristics endorse the reliability, scalability and accuracy of the proposed differential inductor model in this paper.

A second differential amplifier [die photo in Fig. 9(c)] with two spiral inductors instead of a differential inductor is also fabricated. Adopting the design methodology in [7], these two spiral inductors are optimized to have exactly 5 nH and peak quality factor at 2.4 GHz. The two amplifiers are benchmarked with $S_{DS21} = S_{21} - S_{31}/\sqrt{2}$, $S_{CS21} = S_{21} + S_{31}/\sqrt{2}$, and CMRR $= S_{DS21}/S_{CS21}$, which refer to the differential mode to single-ended gain, common mode to single-ended gain and
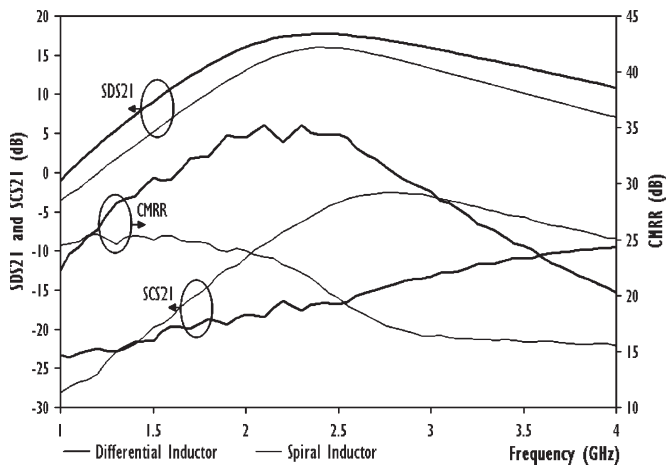
Fig. 11. Comparing measured performance of gigahertz amplifiers using a differential inductor or spiral inductor as the output matching load inductor.

common mode rejection ratio, respectively [18]. Fair circuit assessment as shown in Fig. 11 is possible based on the fact that both amplifiers have identical peak $S_{DS21}$ at 2.4 GHz and there is no shift in frequency response when the differential inductor is replaced by two spiral inductors. The use of differential inductors offers a chip size reduction of more than 20%. In addition, larger differential mode to single-ended gain of more than 2 dB over the entire frequency spectrum and superior common mode rejection ratio of 13.5 dB at 2.4 GHz have both been observed for the amplifier with differential inductors. On-wafer high frequency noise characterization also revealed that the use of differential inductors reduces the noise figure of the amplifier, $NF_{50}$ at 2.4 GHz from 3.43 to 2.85 dB. Huge improvements in circuit performance can be attributed to two key reasons: better ac grounding and higher quality factor for differential inductors. The layout of differential inductors promotes substantial amount of inductive mutual coupling. As such, the required total conductor length for differential inductors as compared to using two conventional spiral inductors for generating the same amount of inductance is much shorter, resulting in smaller resistive loss and higher quality factor, leading to circuit level gain and noise improvements.

## VI. CONCLUSION

In this paper, a streamlined set of differential inductor test structures for developing a scalable RF SPICE model is designed and fabricated in the 0.18 $\mu$m RFCMOS technology. Test structure layout in GS configuration allows on-wafer differential inductor characterization with high level of accuracy and reliability, having great benefits of minimizing both test chip size and deembedding errors compared to the GSG layout configuration. Model validations with a gigahertz differential amplifier revealed good correlations between SPICE simulated and on-wafer measured circuit characteristics. The scalable RF model has enabled ground-breaking analysis of tradeoffs between inductor performance and design layout. These findings together with the aggressive downscaling of feature size in silicon-based transistors continue to bolster silicon technologies as preferred design platforms for cost-sensitive mobile communication products.

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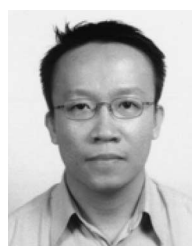
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