Modeling and Measurement of Simultaneous Switching Noise Coupling Through Signal Via Transition

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***Abstract*—The signal via is a heavily utilized interconnection structure in high-density System-on-Package (SoP) substrates and printed circuit boards (PCBs). Vias facilitate complicated routings in these multilayer structures. Significant simultaneous switching noise (SSN) coupling occurs through the signal via transition when the signal via suffers return current interruption caused by reference plane exchange. The coupled SSN decreases noise and timing margins of digital and analog circuits, resulting in reduction of achievable jitter performance, bit error ratio (BER), and system reliability. We introduce a modeling method to estimate SSN coupling based on a balanced transmission line matrix (TLM) method. The proposed modeling method is successfully verified by a series of time–domain and frequency–domain measurements of several via transition structures. First, it is clearly verified that SSN coupling causes considerable clock waveform distortion, increases jitter and noise, and reduces margins in pseudorandom bit sequence (PRBS) eye patterns. We also note that the major frequency spectrum component of the coupled noise is one of the plane pair resonance frequencies in the PCB power/ground pair. Furthermore, we demonstrate that the amount of SSN noise coupling is strongly dependent not only on the position of the signal via, but also on the layer configuration of the multilayer PCB. Finally, we have successfully proposed and confirmed a design methodology to minimize the SSN coupling based on an optimal via positioning approach.**

***Index Terms*—Noise coupling, power/ground noise, printed circuit board (PCB), reference plane change, simultaneous switching noise (SSN), system-on-package (SoP), via.**

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I. Introduction

THE semiconductor industry strives to decrease the size and cost of semiconductor-integrated systems to facilitate the growth of markets and to meet user demands for low-cost and high-functionality system solutions. To meet the growing needs for these system solutions, system-on-chip (SoC) has been the focus of integrated circuit manufacturers for several years. Even though SoCs have many advantageous attributes, productivity and reliability of SoCs are impeded by the limitations of single-wafer processes, high cost, large die size, and slow time-to-market [1].

Recently, as an alternative solution for the low-cost and highly integrated system with multiple functionalities, system-on-package (SoP) technology has emerged [2], [3]. The SoP brings multiple semiconductor dies of various semiconductor processes and materials, and passive devices such as termination resistors, decoupling capacitors, inductors, waveguide, filters, and antennas into a three-dimensional package, to create highly integrated products with optimized cost, size, and performance. Markets for the SoP solution include wireless communication, networking, computing, and sensor and storage system applications. To integrate these multiple dies and passive devices into a tiny three-dimensional (3-D) SoP, adoption of high-density multilayer substrate design is a common approach to mount the multiple dies on a substrate with the embedded passives, which are laterally or vertically integrated onto the package substrate.

Thus, the SoP has countless closely spaced metallic interconnection structures such as traces, vias, pads, leads, partial planes, and plane cavities in a small package. These densely spaced interconnection structures become sources of high-frequency noise generation and noise coupling, imposing serious signal and power integrity issues as well as electromagnetic interference (EMI)/electromagnetic compatibility (EMC) problems [3].

Obviously, these noise problems are crucial concerns when designing the SoP substrate and interconnections. Similar problems arise with high-speed and high-density multilayer PCBs, where many radio frequency (RF), analog, and digital devices are integrated into a densely populated PCB. The noise at the SoP or the PCB worsens noise and timing margin of digital and analog circuits, resulting in reduction of achievable jitter performance, bit error rate (BER), and system reliability. The coupled noise from fast switching digital devices can also affect phase noise and signal to noise ratio (SNR) performance in RF and wireless communication circuits.

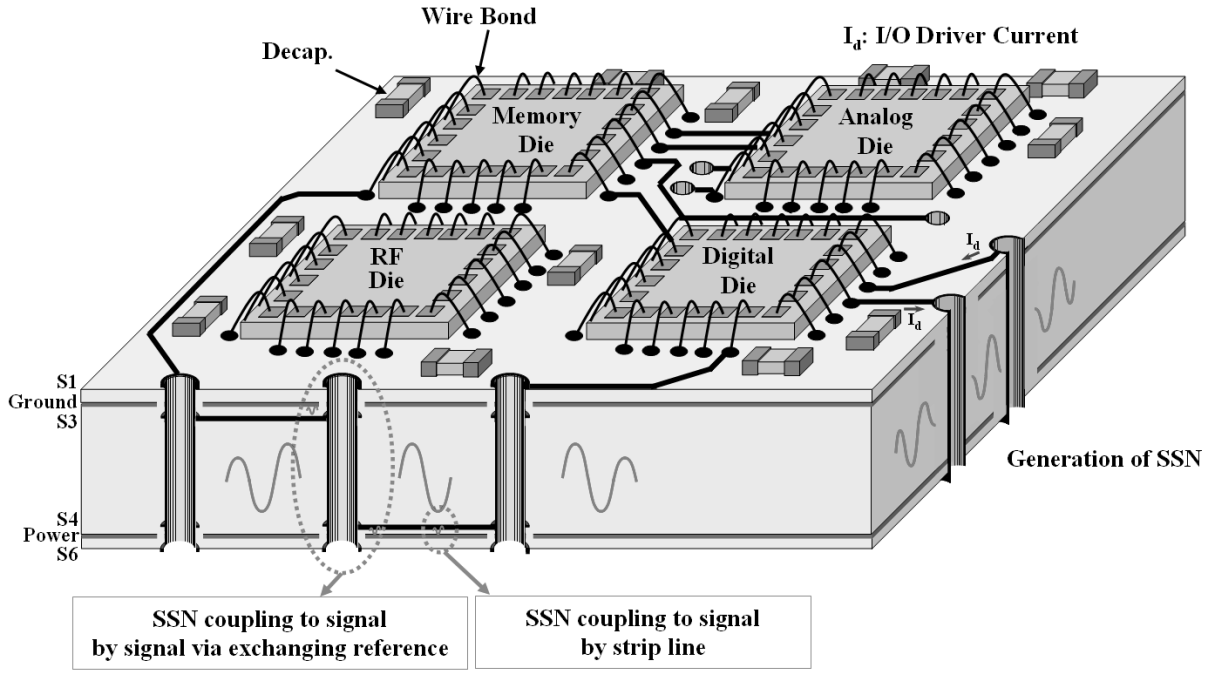

Fig. 1. SSN coupling into a signal via with reference plane exchange through a power/ground plane pair in an SoP.

In high-speed and high-density SoPs and PCBs, a major element of the high-frequency noise is simultaneous switching noise (SSN) from fast-switching digital circuits, as clock frequencies and the amount of switching current are significantly increased.[1] There have been numerous studies of design and analysis methodologies to reduce the SSN by using discrete on-chip and off-chip decoupling capacitors, and by implementing embedded capacitors inside the multilayer PCB [4]–[10]. There has been always a tradeoff between the reduction effect and the necessary cost and manufacturing complexity to realize the solution.

The generated SSN could be transmitted to noise-sensitive circuits such as I/O interface interconnects, phase-locked loops (PLLs), and RF circuits through power delivery and ground return current paths as well as through signal traces and vias. Among the SSN coupling paths at signal interconnections, the signal via is the most significant noise coupling structure, especially when the signal path is exchanging its reference planes. Fig. 1 illustrates the coupling mechanism between the SSN and a signal via with reference plane exchange through a power/ground plane pair in an SoP [11]–[13]. The signal via is the heavily utilized interconnection structure in high-density SoPs and PCBs and enables complicated routing between the many active and passive devices mounted on or embedded inside the multilayer structure. To minimize radiated emission from such signal traces as microstrip lines, strip lines are used and the signal via is necessary to make a transition from the microstrip line to the strip line. Unless the two reference planes are tied together using an electrically shorted circuit with minimal inductance, the signal interconnect encounters a very large signal reflection and the SSN noise coupling caused by the disrupted return current path at the reference plane transition [14]. When one of the reference planes is a power plane and the other reference plane is a ground plane, it is not possible to connect them with a low-inductance via. The signal reflection and the noise coupling are maximal at resonance frequencies of the power/ground planes.

Meanwhile, allowable noise and timing margins have been considerably reduced in advanced serialized I/O interface signaling schemes with gigahertz-range data rates, such as serial advanced technology attachment (SATA), fiber channel (FC), and peripheral component interconnect express (PCI-Express), while the supply voltage has been scaled down and signal frequency has been increased [15]. As a result, clarifying and modeling the SSN coupling mechanism at signal vias in multilayer SoP substrates and PCBs is very necessary.

Several papers have been published to analyze and accurately simulate SSN on power/ground planes and noise in signal lines caused by the interaction between the power and the signal distribution systems [16]–[22]. A general model of interaction between currents in signal vias and SSN voltage was presented and has been implemented in a full-wave simulation tool, Sigrity PowerSI [17], [18].[2] A SPICE-type circuit model is proposed in this paper and compared with the full-wave simulation tool. Further, various modeling methodologies have been proposed, including analytical approaches such as the method of moments and finite-difference time–domain methods [17]–[22]. The SSN coupling phenomena to signal via have been also analyzed by using the superposition principle and the transmission line theory in a simple equivalent circuit model [17]. In this paper, the similar approaches are used and further a simple equation is proposed to predict the amount of the SSN coupled to signal via. It is also a valuable research to investigate efficient and practical methods to minimize the SSN coupling to the signal via. One suggested reduction method is the use of a split power plane [21].

[1]International Technology Roadmap for Semiconductors, 2003.

[2]SIGRITY PowerSI. Sigrity, Inc. [Online]. Available: www.sigrity.com.

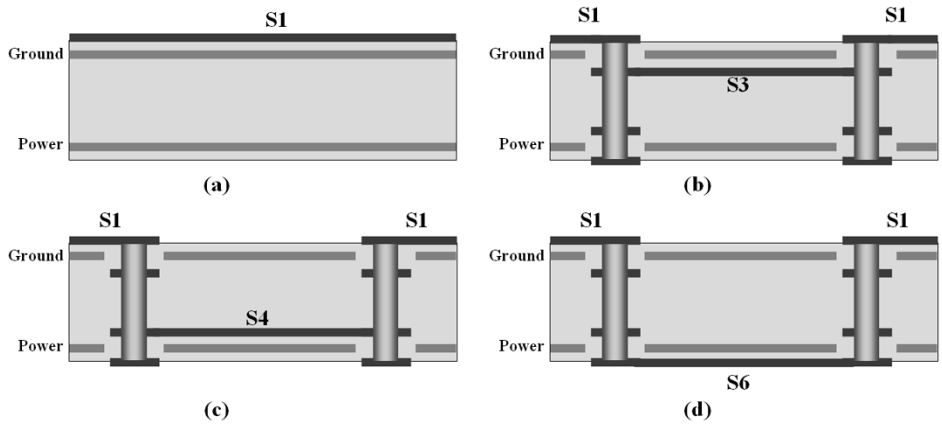

Fig. 2. Four different interconnection structures in a six-layer package or PCB to study the effect of the signal transition through the via. (a) Microstrip line with ground plane reference (Type-1). (b) Microstrip line to strip line transition without reference plane exchange (Type-2). (c) Microstrip line to strip line transition with reference plane exchange to power plane (Type-3). (d) Microstrip line with reference plane exchange to power plane (Type-4).

In this paper, we first introduce a modeling and analysis method to describe and estimate the SSN coupling to signal vias. We have used a SPICE-type circuit model based on a transmission line matrix (TLM) method [23]. In a previous publication, we reported the balanced TLM modeling approach to predict the SSN generation and PCB edge radiation excited by a through-hole signal via, when the signal trace is exchanging reference planes [24], [25]. By using the balanced TLM method, we present the noise coupling mechanism in a multilayer plane structure with microstrips, strip lines, and signal vias. Then, the proposed modeling and analysis method are verified by a series of time–domain and frequency–domain measurements using four different signal layer configurations. Finally, we propose several practical methods to reduce the noise coupling, and demonstrate the usefulness of the proposed methods through simulations and measurements. The measurements show good agreement with the predictions based on the model and its analysis. Based on the modeling and the measurements, we show that the signal via is the interconnection structure most susceptible to the power/ground SSN coupling when a signal line exchanges reference planes. We also show that the SSN coupling causes a considerable amount of waveform distortion in signal lines and that the major spectrum component of the coupled noise is the plane pair resonance frequency of the power/ground planes. Finally, we have successfully proposed and confirmed a design method to minimize the SSN coupling based on optimal via positioning. We also demonstrated that the amount of the SSN noise coupling is strongly dependent not only on the position of the signal via, but also on the layer configurations.

II. Frequency–Domain Modeling and Analysis of Simultaneous Switching Noise Coupling Through Signal Vias

A. Test Layer Structures With Via Transitions

A signal trace on a package substrate or PCB requires a reference plane or a pair of reference planes to guarantee return current paths and to maintain transverse electromagnetic (TEM) wave propagation with uniform impedance and propagation velocity over a frequency range. Usually, a ground plane, a power plane, or a pair of power/ground planes can serve as the reference plane. However, when the signal trace exchanges its reference plane though a via, the return current path can be severely disrupted, and the disrupted return current can cause considerable signal integrity problems. The obstructed return current then excites SSN in the power/ground. As a result, the via becomes a source of SSN, or could be a receptor of SSN. To investigate the effect of the signal trace transition through the via with a series of simulations and measurements, we have considered four structures of layers, as illustrated in Fig. 2.

As shown in Fig. 2, the four test layer structures are classified according to transmission line structure such as strip line or microstrip line, as well as whether the signal trace exchanges reference planes. Even when the number of stacking layers is more or less than six, most signal transition structures through vias will fall into one of the four categories. The four layer structures in Fig. 2 are called Type-1, Type-2, Type-3, and Type-4, respectively. The signal trace in each layer is symbolized as S1 (microstip line in layer 1), S3 (strip line in layer 3), S4 (strip line in layer 4), and S6 (microstrip line in layer 6). In Type-1 and Type-2 layer structures, the signal traces maintain the same reference plane (ground plane of layer 2) even after the via transition. In the Type-2 layer structure, the return current path changes from the top surface of the ground plane (layer 2) to the bottom surface of the same ground plane (layer 2). Therefore, the generation of the SSN and the noise coupling through the via transition may be less serious than with the layer structures of Type-3 and Type-4. On the other hand, the reference plane is switched from the ground plane (layer 2) to the power plane (layer 5), in the layer structures Type-3 and Type-4. The two reference planes are capacitively coupled to each other, and the return current is severely disrupted to produce displacement current between the two reference planes. This displacement current and the associated high-frequency field distribution inside the plane pair give rise to SSN generation as well as noise coupling problems. In this study, we have investigated these mechanisms using careful modeling, simulation, and measurement.

The dimensions and the stack-up of the four test vehicles are depicted in Fig. 3. Each test vehicle is 80 $\times$ 190 mm, with a six-layer stack-up. Similar stack-ups are commonly used in

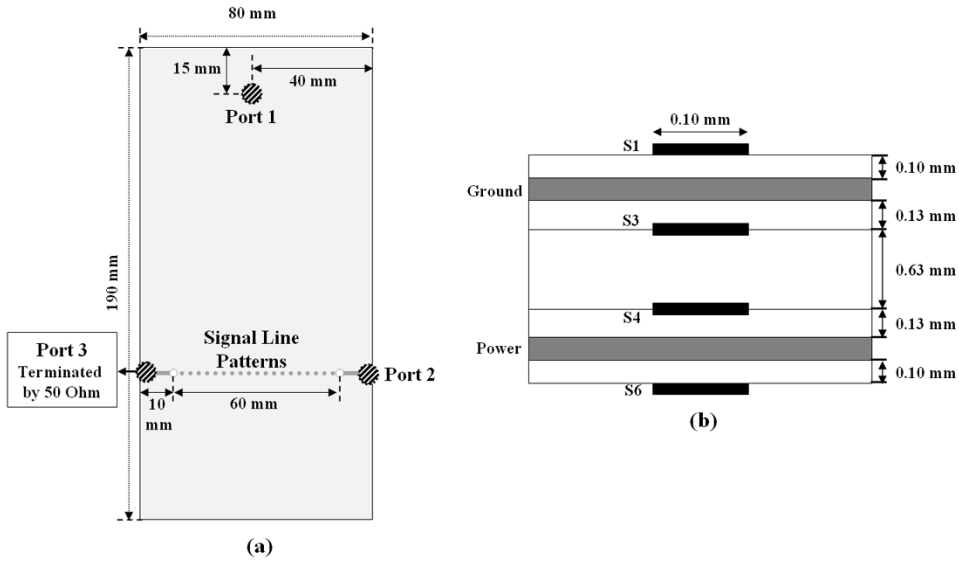

Fig. 3. (a) Top view and (b) Stack-up of the device under test (DUT). For frequency– and time–domain measurements, port 1 is located at a position on the PCB and connected to the power plane and ground plane, while port 2 is located at the end of the signal trace after the signal trace transition through the via.

commercial DDR memory modules. We have executed a series of time–domain and frequency–domain analyses and measurements using these test vehicles. Port 1 is located at an upper position on the PCB and is connected to the power plane (layer 5) and the ground plane (layer 2). Port 2 is connected to one end of the signal trace after a pair of via transitions. Port 1 is used to generate the SSN between the power and ground planes and to measure the frequency-dependent coupling coefficient between ports 1 and 2. To generate the SSN, a clock generator chip (CDCVF2310, Texas Instruments) is mounted at the same position as port 1, and the time-domain coupled noise is measured at port 2.

B. Via Coupling Model and Balanced TLM Method

To simulate and analyze the SSN generation and coupling mechanism through the signal via transition, we have used a via coupling model combined with a balanced TLM model [23]–[26]. The via coupling model is shown in Fig. 4 for the Type-4 layer structure. The electrical model of the metallic via column is expressed as an inductor (L_{Via}), while the capacitive coupling between the via and the adjacent reference planes is modeled by coupling capacitors (C_{Via}) surrounding the metallic via column. The signal via is coupled equally to both the power plane (layer 5) and the ground plane (layer 2) of the plane pair in a balanced manner. Further, the via neck effect is added to the model by adding an inductor (L_{Neck}). This effect is induced by the absence of the reference plane under the signal trace at the via clearance [24]. The model parameters of the via coupling model were extracted by fitting the calculated S-parameters from the model to the measured S-parameters. Table I lists the extracted model parameters. The detailed modeling procedure was introduced in previous publications [24].

The signal trace and the multilayer reference planes are described by the balanced TLM modeling method. First, the signal trace is modeled by a distributed lumped circuit model of a transmission line. The distributed transmission line model has a unit mesh of a balanced circuit schematic, as shown in Figs. 5 and 6.

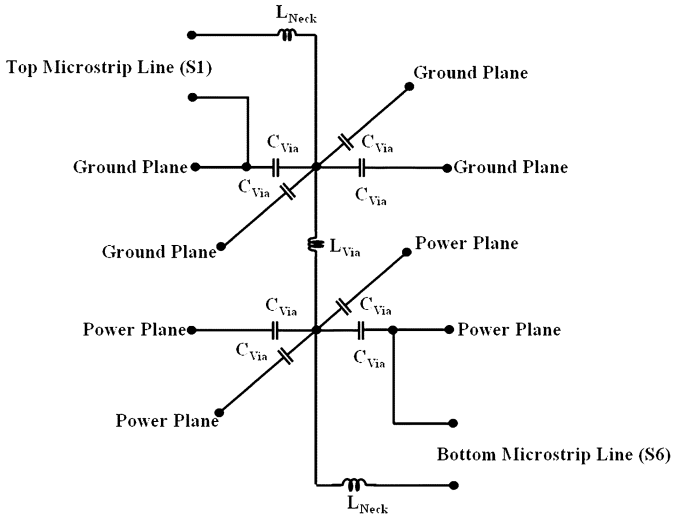

Fig. 4. Via coupling model used for analysis of the signal transition through a via in the Type-4 layer structure.

TABLE I
MODEL PARAMETERS OF THE VIA COUPLING MODEL

Notation	Total Value
C_{Via}	123 fF
L_{Via}	752 pH
L_{Neck}	622 pF

In the balanced TLM model of the signal trace, the total line inductance in a mesh is divided into two inductors, while the two line inductors are allocated to the line and the reference plane. The inductance at the reference plane describes the inductance of the return current path through the reference plane. In a layer structure with multiple reference planes as the test vehicles, the balanced TLM is an effective and useful modeling method. It is not necessary to assign a single plane as a common reference plane for all the signal traces in layers 1, 3, 4, or 6, which is not

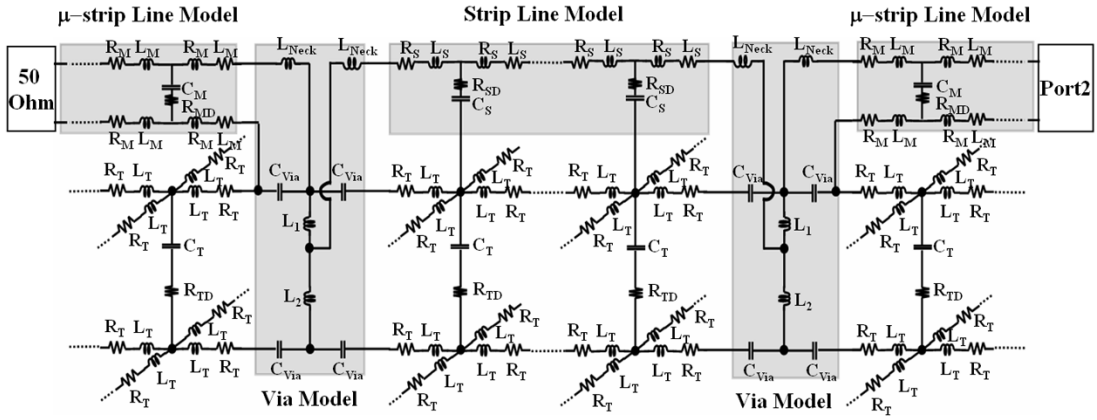

Fig. 5. Balanced TLM model for a Type-2 layer structure ($L_{Via} = L_1 + L_2$).

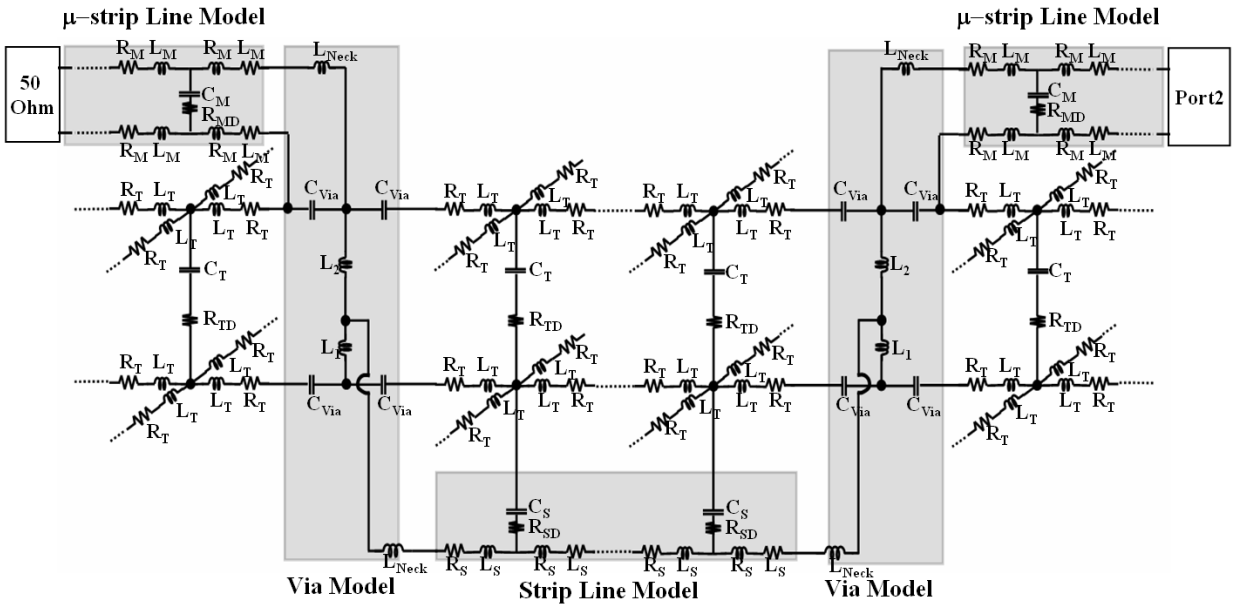

Fig. 6. Balanced TLM model for a Type-3 layer structure ($L_{Via} = L_1 + L_2$).

the case for the test vehicles. When a metal plane provides the return current path for a signal trace, the plane becomes a reference plane for the signal trace. By using the balanced modeling approach, any plane can be used as a reference plane, even if it is a power plane. The balanced TLM is based on a SPICE-type circuit model, so the modeling method can be easily embedded into conventional SPICE-type circuit simulators, and the simulation time can be considerably reduced compared to full 3-D simulation methods. Furthermore, various passive and active device models can be readily inserted into the balanced TLM circuit schematics by including commonly used component models.

In a similar way, the plane pair formed by the ground plane (layer 2) and the power plane (layer 5) is described by a two-dimensional (2-D) balanced TLM modeling approach. In this plane pair, the electromagnetic fields are confined inside the pair by the charge and the current at the surfaces of the two planes. The modeling circuit schematics of the Type-2 layer structure and the Type-3 layer structure are shown in Figs. 5 and 6. Along with the plane pair, both the microstrip line and the strip line are modeled by the balanced TLM in Figs. 5 and 6. As described in the balanced TLM schematic in Fig. 5, the microstrip line signal trace uses the top metal surface of the ground plane (layer 2) for the reference return current path, while the strip line (layer 3) uses the bottom surface of the ground plane (layer 2). Thus, the strip line and the power/ground plane pair share one metal surface (the bottom surface of layer 2) for the return current path and the ground plane. On the other hand, the strip line in Fig. 6 employs the top surface of the power plane (layer 5) for its reference return current path. It means that the line model and the plane pair models share one plane (the top surface of layer 5) for the return current path and the power plane.

It is also assumed that the strip line has as its reference plane either the ground plane (layer 2) or the power plane (layer 5) for simplicity of modeling. In Fig. 5, the distance from the strip line to the ground reference plane is much less than the distance to the power reference plane. The dimensions of the test vehicles are shown in Fig. 3(b). Similarly, the strip line in Fig. 6 is modeled as a microstrip line with a power reference plane. The validity of this assumption is proved when comparing the simulation to measurements in the following sections. The modeling parameters were extracted by fitting the simulated S-parameters to the measured S-parameters, and are listed in Table II. Be-

TABLE II
MODEL PARAMETERS OF THE BALANCED TLM MODEL

Notation	Total Value	Notation	Total Value
R_T	2.5 mΩ / Cell	R_S	2.5 mΩ / Cell
L_T	0.28 nH / Cell	L_S	0.48 nH / Cell
C_T	963 fF / Cell	C_S	534 fF / Cell
R_{Td}	2 Ω / Cell	R_{Sd}	2 Ω / Cell
R_M	2.5 mΩ / Cell	L_1	110 pH
L_M	0.27 nH / Cell	L_2	642 pH
C_M	473 fF / Cell	L_{Neck}	622 pH
R_{Md}	2 Ω / Cell	C_{Via}	123 fF

* $L_{Via}=L_1+L_2$

cause the strip line begins at a specific height of the metallic via column, L_{Via} is divided into L_1 and L_2, which are proportional to the distance from the strip line to the upper and lower via column. By using the combined via coupling model, the signal balanced TLM model, and the 2-D balanced plane pair TLM model, we are able to simulate the SSN generation and the SSN coupling mechanism in the test multilayer PCB vehicles.

C. Frequency–Domain Analysis and Measurement

Figs. 7 and 8 show the simulated and measured SSN coupling coefficient, S_{21}, obtained to evaluate the SSN coupling effect. S_{21} is the high-frequency electromagnetic coupling coefficient between port 1 and 2. Port 1 is connected between the power plane (layer 5) and the ground plane (layer 2), while port 2 is connected to one end of the signal trace after the signal via transition. The other end of the signal trace is terminated with a 50-Ω termination resistor to avoid signal reflection at the end of the signal trace. The port assignment and the terminations are explained in Fig. 3(a): port 1 is used to excite the SSN at the power/ground plane, and port 2 is used to measure the coupled SSN to the signal line and via.

As shown in Fig. 7, the calculated coupling coefficient from the balanced TLM model agrees well with the measurement and full-wave simulation using Sigrity PowerSI, demonstrating the validity and usefulness of the modeling. However, The accuracy of the balanced TLM model is better than that of Sigrity PowerSI tool. Further, solving the problem using the numerical approach required approximately 1 min, whereas the proposed model required less than 10 s, with the same computing resources.

In the simulation, the coupling coefficient of the Type-1 layer structure is neglected because the signal trace does not have a via transition in the Type-1 layer structure. In the simulation of the Type-1 layer structure, the signal line TLM model and the power/ground TLM model are completely isolated from each other. The modeling is evidently valid when the skin depth is less than the metal thickness of layer 2 [12]. However, as observed in Fig. 8, the measured S_{21} of the Type-1 layer structure has a minute amount of SSN coupling. The measured coupling coefficient of the Type-1 layer structure has a range below −50-dB scale. We believe that the measured coupling could be caused by radiated coupling between ports 1 and 2 through the air because of imperfect connector and cable shielding.

From the simulation and measurements, it is noted that the Type-3 and Type-4 layer structures have much higher SSN coupling than the Type-1 and Type-2 layer structure. The measured

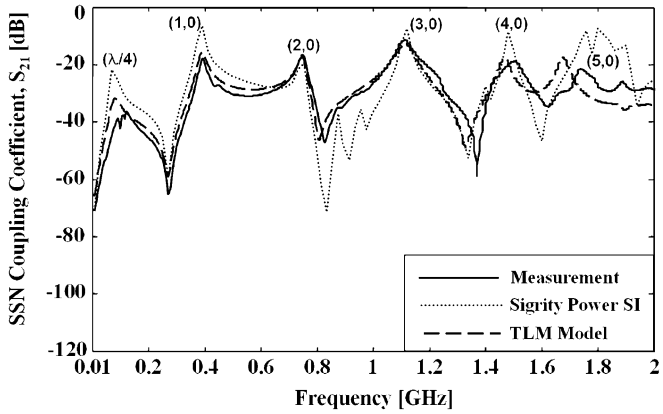

Fig. 7. Comparison of the measurement, the full-wave simulation, and balanced TLM model of the S_{21} parameter, SSN coupling coefficient, for test vehicle Type-3 up to 2 GHz. The solid line represents the coupling coefficient obtained from the measurement, and the dotted line represents the coupling coefficient obtained from Sigrity PowerSI, whereas the dashed line represents the coupling coefficient calculated using the balanced TLM model.

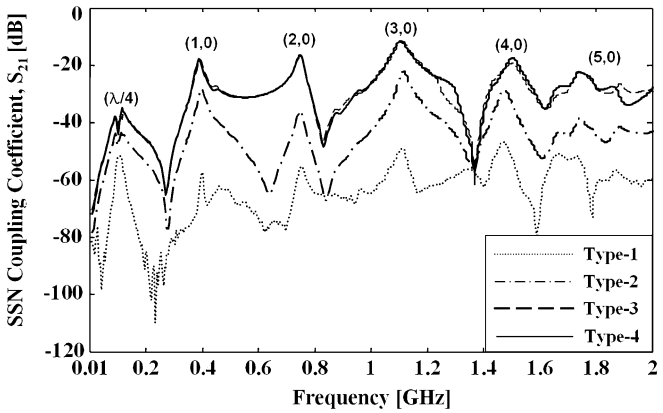

Fig. 8. Measured coupling coefficient S_{21} to evaluate the coupling of power/ground noise to the signal trace. Port 1 is placed between the power and ground planes, and port 2 is located at the end of the signal trace.

S_{21} of the Type-1 layer structure shows the fact that there is little SSN coupling to microstrip line because of the skin effect. Therefore, it is obvious that microstrip line does not affect the amount of SSN coupling in Type-3 and Type-4 so that the significant receptors of Type-3 layer structure are either the strip line or the reference change via. From the measured S_{21} of the Type-2 layer structure, the strip line causes just a little SSN coupling. In conclusion, it is clear that the reference change via is a significant receptor of SSN coupling. In addition, since microstrip line has nothing to do with SSN coupling, the significant receptor of Type-4 layer structure is the reference change via.

It is also observed that slightly more SSN is coupled to the strip line in the Type-3 layer structure than to the microstrip line in the Type-4 layer structure. This slight difference of the two curves in Fig. 8 is caused by the small differences in the amount of SSN coupling to the strip line in the plane pair and to the microstrip line on layer 6. The Type-3 layer structure suffers slightly higher SSN coupling, because the strip line is inside the power/ground plane, while the SSN is generated inside the plane pair at port 1. On the other hand, the SSN coupling at the strip line is still much less than that at the via transitions. The distance

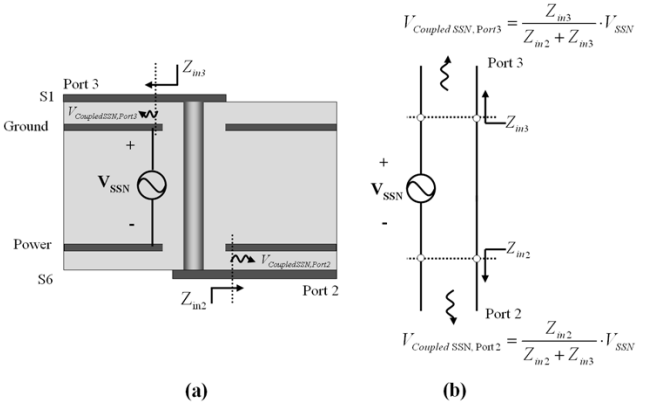

Fig. 9. SSN coupling through a signal via transition with exchange of reference planes. (a) Signal via structure exchanging the reference plane and SSN coupling mechanism. (b) Equivalent circuit model to describe the SSN coupling at the signal via transition.

from the signal trace to the reference plane is much shorter than the power/ground dielectric thickness. Hence, the contribution of the SSN coupling to the strip line is not significant compared to the coupling to the signal via transition with the reference plane exchange.

The SSN coupling coefficient becomes maximal at the resonance frequencies of the power/ground pair. The SSN coupling coefficient reaches above -20 dB at the plane pair resonant frequencies. These frequencies are determined by the dimensions of the plane pair, the dielectric constant of the insulator, and the resonance mode number [27]. In Figs. 7 and 8, the mode numbers are recorded at the coefficient peaks of the resonance frequencies. The $\lambda/4$ resonance mode is a parallel resonance mode excited by the equivalent serial inductance (ESL) of a bulk decoupling capacitor and the power/ground plane capacitance between layers 2 and 5.

The SSN coupling analysis and modeling in electronics packaging has been done by Fan [16]–[18]. Using the similar analysis, the SSN coupling phenomena through the signal via transition are further interpreted by the conceptual diagram of Fig. 9(a) and the circuit schematic of Fig. 9(b). When the SSN is applied near the reference change via of the plane pair, the time-varying SSN voltage ($V_{\rm SSN}$) is built up between the power plane and the ground plane. As a result, $V_{\rm SSN}$ is developed across the two planes at the via position. The amplitude and the phase of $V_{\rm SSN}$ at the via location are dependent on the resonance mode number and the location of the via [28]. Then, $V_{\rm SSN}$ becomes a voltage source between the two reference planes at the via location, resulting in the injection of electromagnetic waves into ports 2 and 3 simultaneously. The SSN coupling mechanism is also depicted in the circuit schematic of Fig. 9(b). The incident wave at port 3 is absorbed by the 50-Ω termination resistor, while the incident wave to port 2 is measured by an oscilloscope or a spectrum analyzer with a matching 50-Ω input impedance. The coupled SSN voltages to ports 2 and 3 are expressed in (1) and (2):

$$V_{\rm Coupled\cdot SSN,Port2} = \frac{Z_{\rm in2}}{Z_{\rm in2}+Z_{\rm in3}} \cdot V_{\rm SSN} \quad (1)$$

$$V_{\rm Coupled\cdot SSN,Port3} = \frac{Z_{\rm in3}}{Z_{\rm in2}+Z_{\rm in3}} \cdot V_{\rm SSN}. \quad (2)$$

As indicated, the coupled SSN voltage is related to the characteristic impedances of the two transmission lines, $Z_{\rm in1}$ and $Z_{\rm in2}$. In the test vehicles, $Z_{\rm in1}$ and $Z_{\rm in2}$ are both 50 Ω. The coupled SSN can then be calculated using the above equations with the given characteristic line impedances. Because $Z_{\rm in1}$ and $Z_{\rm in2}$ are the same, half of $V_{\rm SSN}$ is coupled to the signal line through the via transition.

The above frequency domain modeling, analysis, and measurement confirm that the proposed via coupling model and balanced TLM model can be effectively used to predict the SSN coupling at via transitions. The expectation agrees well with the measurements. It is noted that, while the SSN is built up between the power plane and the ground plane near the via location, 50% of the SSN can be coupled to the signal via, causing considerable degradation of noise and jitter performance in high-speed serial data transmission systems.

III. Time Domain Analysis and Measurement of SSN Coupling Through Signal Vias

A. Verification by Time–Domain Analysis and Measurement

To verify the SSN coupling mechanism based on time–domain analysis and measurement, we have designed and tested a series of test vehicles with Type-1, Type-2, Type-3, and Type-4 layer structures, the same as those shown in Figs. 2 and 3. Fig. 10 shows the PCB dimensions, chip position, and cable connections to measurement instruments. To generate the SSN, we mounted a clock driver chip (CDCVF2310, Texas Instruments) at the port 1 location, and the output drivers consume totally about 200-mA simultaneous output driver current with a 200-MHz clock frequency. A precisely controlled 200-MHz clock source signal was supplied to the clock driver chip from a port of a two-channel pulse pattern generator. The power pins and the ground pins of the clock driver chip were connected to the power plane (layer 5) and the ground plane (layer 2) through power and ground vias, respectively, to generate the SSN in the power/ground pair. Accordingly, this group of power vias and ground vias served as a SSN current source at port 1. At the same time, another output port of the two-channel pulse pattern generator was connected to port 3, supplying a 400-mV, 200-MHz clock signal or a 500-mV, 200-Mb/s pseudorandom bit sequence (PRBS) signal. Because a single pulse pattern generator with the two output ports was used to generate the SSN as well as to supply the clock or the PRBS signal, the signal (clock or PRBS signal at port 3) and the SSN in the plane pair were synchronized. Port 2 was connected to an oscilloscope to monitor distorted clock waveforms or PRBS eye patterns caused by the SSN coupling.

First, we simulated and measured the SSN waveform at the driver chip location (port 1) using a high-impedance probe, as shown in Fig. 11(a). The simulated SSN waveform was obtained by using the via coupling model and the balanced TLM model as explained in the previous section. Because the model does not include an output driver and package model, there are small differences between the measurements and simulations. Fig. 11(b) shows the spectrum of the simulated and the measured SSN

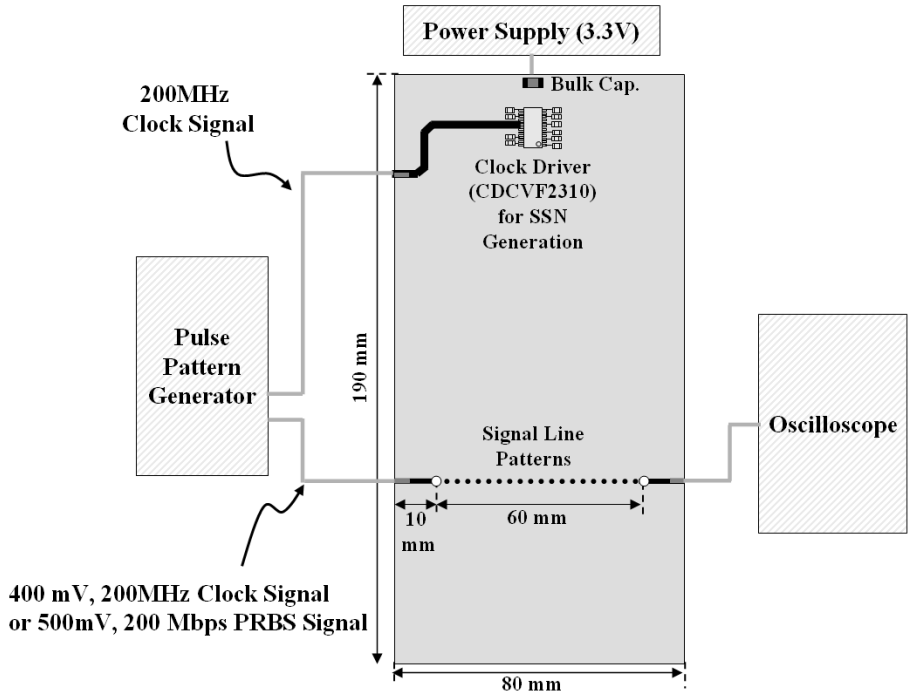

Fig. 10. Test vehicle and cable connections for the time domain analysis and measurement. A clock signal and pseudorandom bit sequence (PRBS) signal were supplied by a pulse pattern generator and a clock driver chip. The clock driver chip consumes about 200-mA output driver switching current with 200-MHz frequency.

with the measured power/ground network impedance curve at the center of the clock driver chip.

As demonstrated in Fig. 11(a), the predicted SSN waveform (dotted line) is very similar to the measured waveform (solid line) considering SSN amplitude, noise period, and small high-frequency ripples. It is evident that the modeling and simulation method has demonstrated meaningful accuracy and can effectively evaluate SSN generation in high-speed multilayer package substrates or boards. The peak-to-peak SSN amplitude is about 600 mV, while the voltage level of the clock driver chip's power supply is 3.3 V. The major period of the SSN waveform is 2.5 ns, corresponding to 400 MHz. The 400-MHz frequency component of the SSN waveform corresponds to the second harmonic frequency of the simultaneous switching current driven by the clock driver chip with 200-MHz clock frequency. At the same time, the 400-MHz frequency component of the SSN waveform is the resonance frequency of the power/ground plane pair with the resonance mode number of TM(1, 0). As a result, it is confirmed that when one of the clock harmonic frequencies is coincident with or close to one of the plane pair resonance mode frequencies, the SoP or the system can suffer significant signal integrity problems because of the huge SSN amplitude and subsequent radiated emission at the resonance mode frequency of the plane pair. Meanwhile, the small voltage ripples at the SSN waveform in Fig. 11(b) have a noise frequency corresponding to the higher harmonics of the clock frequency. Fig. 11(b) shows the spectrum components of the simulated and measured SSN waveforms. It also plots the measured power/ground network impedance curve (dotted line) to show the impact of the peak power/ground network impedance at the plane pair resonance frequencies on the increased spectrum intensity of the SSN.

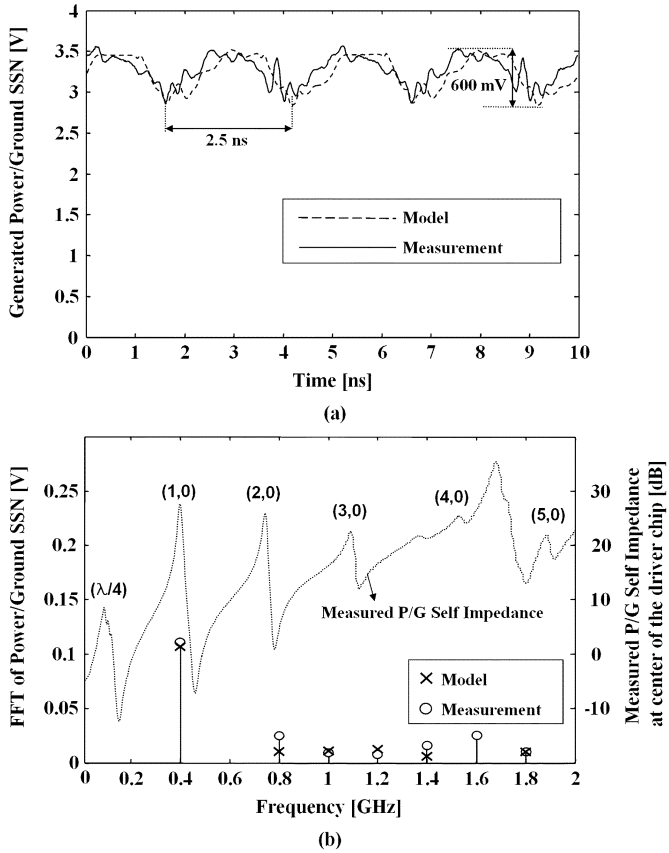

Fig. 11. (a) Measured and the simulated SSN waveforms at the center of the clock driver chip. (b) Spectrum of the simulated and the measured SSN waveform at the center of the clock driver chip. The measured power/ground network impedance curve at the center of the clock driver chip is shown.

To complete the series of time–domain measurements, we monitored the distorted clock waveforms and eye patterns af-

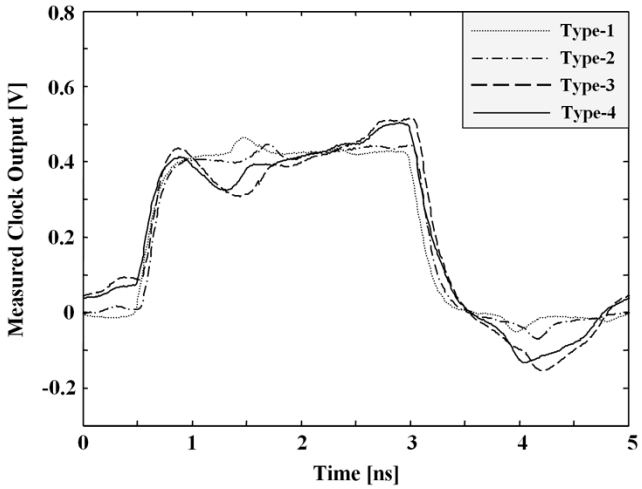

Fig. 12. Measured output clock waveforms at port 2 with 200-MHz input clock and 400-mV peak-to-peak voltage, depending on the layer structure when a 600-mV SSN exists at the power/ground pair, excited at port 1.

fected by the SSN coupling at the via transitions and the strip line inside the plane pair for each of the four different layer structures of Type-1, Type-2, Type-3, and Type-4 as illustrate in Fig. 10. The SSN of a 600-mV peak-to-peak voltage was produced at the port 1 location by the clock driver chip. The distorted waveforms were measured at port 2, and are displayed in Fig. 12, depending on the layer structures. It is manifest again that the Type-3 layer structure produces the worst waveform distortion, where the strip line has a reference plane of the power plane (layer 5) inside the plane pair, and has a via transition with reference plane exchange from the ground plane (layer 2) to the power plane (layer 5). The SSN coupling occurs not only at the via transition with the reference plane exchange, but also at the strip line inside the plane pair. However, the SSN coupling at the via transition is the major coupling mechanism compared to that for the strip line. Therefore, the Type-4 layer structure has almost the same amount of the SSN coupling as the Type-3 layer structure, even though the Type-4 layer structure has a microstrip line outside the plane pair. On the other hand, the Type-1 and the Type-2 layer structures have less SSN coupling because both layer structures maintain the same reference plane, the ground plane (layer 2). It is evident that the time–domain and measurement results and analysis are quite consistent with the understanding and interpretation of the SSN coupling mechanism obtained during the frequency–domain measurement and analysis in the previous sections.

B. Reduction of SSN Coupling by Via Positioning

As discussed in the previous frequency- and time–domain analysis and measurement, it is well confirmed that both Type-3 and Type-4 layer structures are very sensitive to SSN coupling. Unfortunately, we commonly encounter designs in which the reference plane exchange found in Type-3 and Type-4 layer structures is inevitable to enable efficient trace routings in high-density multilayer package substrates and boards. To mitigate the SSN coupling problem, we suggest a design methodology based on optimal via positioning. When an electromagnetic SSN field is developed at a plane pair resonance frequency, the SSN field distribution follows the same spatial function as the power/ground network impedance. The peak magnitude of the power/ground network impedance varies as a function of the via position in the plane pair. However, the plane pair resonance frequencies and the field distributions are not altered by the presence of the via, unless the number of vias in a small area is high enough. Accordingly, by locating a via at an optimal position that possesses the minimum power/ground network impedance, the amount of SSN coupling at the via transition can be significantly reduced.

To demonstrate our design approach for suppressing SSN coupling based on via positioning, we designed and tested a series of test PCB vehicles as described in Fig. 13, which depicts the size of the test PCBs and the positions of the vias. The cross-sectional view and the dimensions are identical to the test vehicles shown in Fig. 3. As we observed in the previous section, the primary frequency component of the SSN is 400 MHz, which is the TM(1,0) mode of the plane pair resonance frequency. Then, the field and the power/ground network impedance functions follow the solid curve plotted at the right of Fig. 14. It shows that the SSN voltage is maximal at the upper or bottom edges of the test PCB, while it is minimal at the center of the test PCB along the vertical axis of the PCB. In other words, if we locate the via at the center of the y-axis on the PCB, the SSN coupling can be significantly suppressed. PCB edges should usually be avoided when placing vias, unless the PCB edge is properly terminated with resistors or capacitors. To validate the proposed design approach, we measured coupling coefficients, distorted clock waveforms, and noise margin of PRBS eye patterns, depending on the via position along the vertical axis of the test PCB.

Fig. 14 shows the measured SSN coupling coefficient S_{21}. As expected from the previous discussion, it is evident that via position 4 has the worst SSN coupling because the via is located at the edge of the PCB along the y-axis. On the other hand, via position 1 has the least SSN coupling. The order of the SSN coupling coefficient is correspondingly equivalent to the order of the power/ground network impedance curve of the TM(1.0) mode, as plotted in Fig. 13. This observation supports the basic argument of the proposed design methodology. Fig. 15(a) and (b) shows the measured clock waveforms and their frequency spectra, respectively. It is demonstrated that the test PCB with the via at the position 1 has the lowest coupled SSN as in Fig. 15(b) and has the smallest component of the TM(1,0) mode spectrum components at 400 MHz. However, the spectrum component at 600 MHz, the third harmonic frequency of the clock signal, is not altered noticeably.

In summary, the first design approach to lower the SSN coupling through the signal via transitions at resonance frequencies is to locate the via at a specific location in such a way that the SSN field intensity and voltage amplitude are minimal at the designed via position with the resonance mode frequency [12], [28]. Similarly, the SSN generation intensity and frequency spectrum are also dependent on the location of the SSN source. Usually, the digital clock frequency or its harmonics should not be coincident with the plane resonance frequencies. Otherwise, the via and the SSN source positioning approach could be an effective design solution. In the case that the signal via cannot

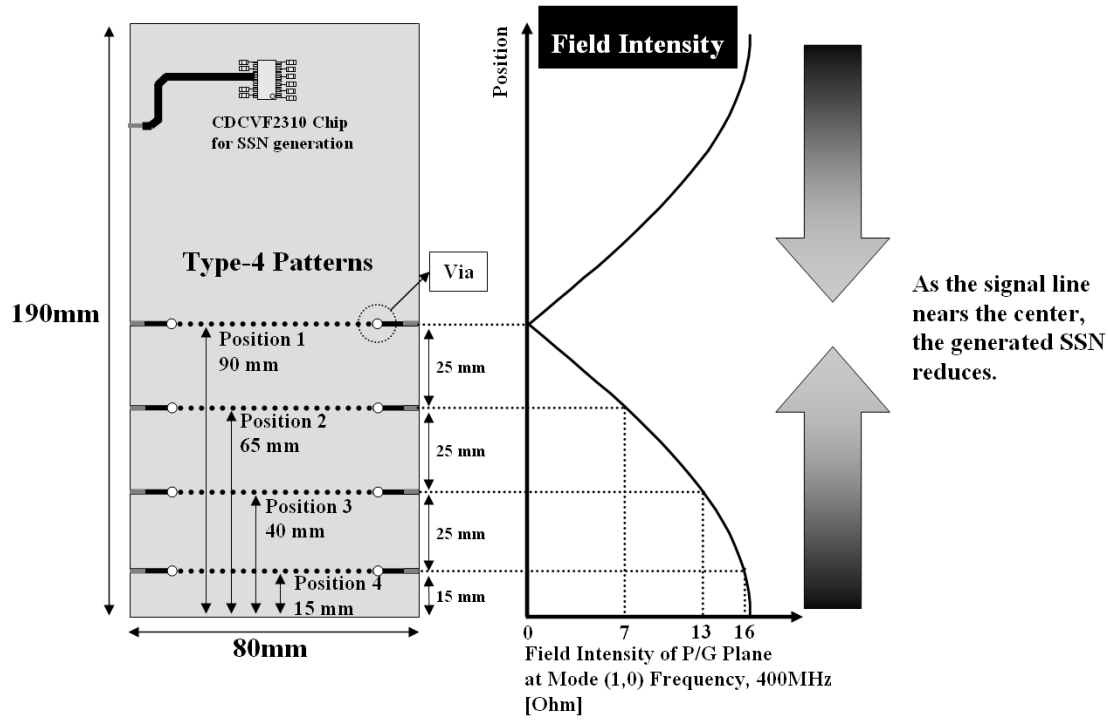

Fig. 13. Test PCB with various via positions and the spatial distribution of the SSN voltage of the TM(1,0) power/ground plane pair resonance mode.

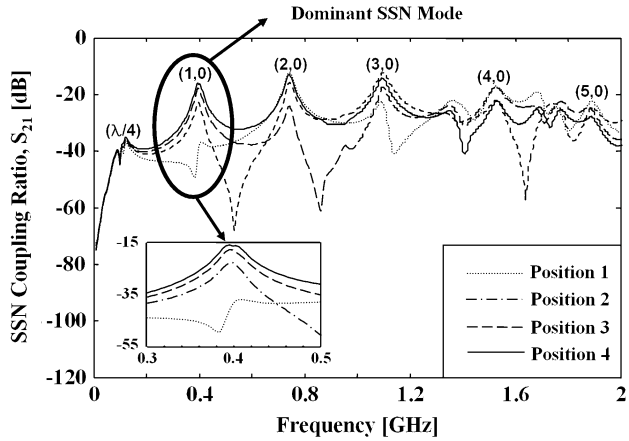

Fig. 14. Measured coupling coefficient S_{21} to evaluate the SSN coupling effect depending on the via position.

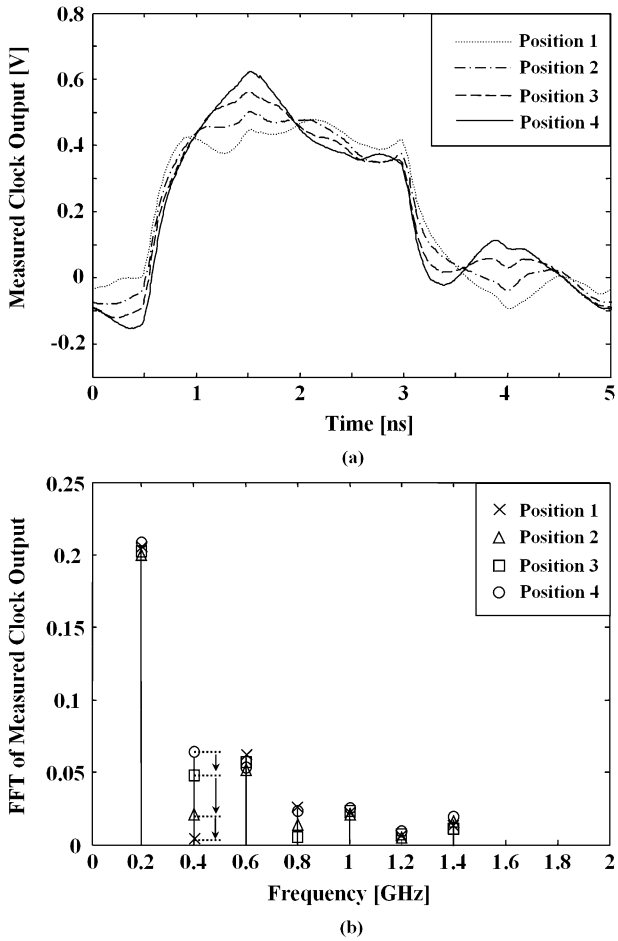

Fig. 15. (a) Distorted clock waveforms depending on the via positions. (b) Frequency spectrum of the measured clock waveforms depending on the via position. In particular, the spectrum component of the TM(1,0) mode is strongly affected by the via position.

be placed at where we want due to design constraint, the design approach to lower the SSN coupling is to surround the signal transition via with ground vias. If the two planes of the pair are both ground planes, we can connect the two planes with a group of ground vias circling the signal via. When the ground via inductance is negligible, a return current path with a low ground inductance can be provided, avoiding serious SSN coupling problems. A similar design methodology with ground via shielding can be applied to the SSN source. However, when one of the planes in a pair is a power plane and the other plane is a ground plane, we cannot use ground vias in this way. Then, to provide the return current path and to reduce the SSN coupling, we can put a group of decoupling capacitors with a low ESL. If the ESL of each decoupling is high, we cannot achieve a low-impedance ground return current path. If we have a decoupling capacitor with an extremely small ESL, a single decoupling capacitor may work. It should be remembered that

the design adoption of ground vias or decoupling capacitors occupies considerable surface area of the package substrate or the PCB.

Dielectric loss and skin effect loss of the power/ground plane pair at the resonance frequencies could help to lower the Q-factor of the resonance modes, reducing the SSN voltage and the SSN coupling. The dielectric loss and the skin effect loss increase as the frequency increases. Hence, loss is a useful mechanism to reduce SSN coupling at gigahertz frequencies. The last and most promising design solution is to use differential signaling schemes. We can use a pair of differential vias to support a high-speed differential signaling interconnection with lower noise generation and higher immunity [14]. The two vias in a differential pair should be placed close enough to each other that a virtual ground plane is built between the two vias, and return current is provided by the opposite via in the same pair.

IV. Conclusion

In modern high-speed, high-density SoP and PCB design, SSN from fast-switching digital circuits becomes a major concern, as the clock frequency and amount of switching current are increased. The SSN seriously affects the performance of noise-sensitive devices such as I/O interface interconnects, PLLs, and RF circuits. The SSN can be coupled into these noise sensitive circuits through common power delivery and ground return current networks as well as through signal traces and vias. In particular, a significant amount of SSN coupling occurs when a signal via suffers return current interruption from reference plane exchanges. With the limited number of ground planes and ground vias in densely populated multilayer interconnection structures, it is quite common to encounter vias with reference plane changes for critical signal paths such as clock distribution networks. The SSN coupling produces clock waveform distortion as well as increased jitter and noise margin reduction in the PRBS eye patterns. Therefore, it is useful to develop an efficient model and to suggest a suppression method with experimental verifications.

To validate the proposed modeling method and the interpretation of the SSN coupling mechanism, we have introduced a series of time–domain and frequency–domain measurements with various via transition structures. We also have introduced a balanced TLM method to predict the SSN generation and the SSN coupling. We have proved that the SSN coupling causes considerable clock waveform distortion and also increases jitter and reduces noise margin. Unless the SSN coupling is carefully considered, an SoP or PCB may fail to work with acceptable operating margins. In particular, for critical signal paths such as clock delivery nets or high-speed serial interconnections, special attention must be paid to provide satisfactory eye and jitter specifications. We have also validated that the major frequency spectrum component of the SSN coupling is decided not only by the plane pair resonance frequency of the power/ground plane pair, but also by the SSN voltage distribution on the surface of the power/ground plane pair. Hence, the amount of SSN coupling is heavily dependent on the via positions at a specific plane pair resonance frequency. Finally, we have successfully proposed and confirmed a design methodology that minimizes SSN coupling based on an optimal via positioning approach.

This study can be extended to cases where numerous RF passive devices, filters, or even antennas are embedded in an SoP substrate or a PCB. These design trends meet a strong requirement from the market to provide tiny, light-weight wireless communication systems to conventional customers. These embedded RF devices can suffer similar SSN coupling problems, because the devices are usually made of 3-D metal interconnections inside the power/ground plane pair, in which SSN resonance is produced by digital switching devices. Our research will also be valuable for the study of design methods to isolate the SSN from noise sensitive RF devices.

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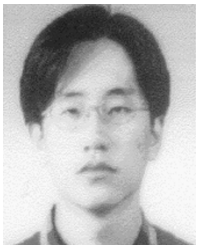

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