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Modeling and Optimization of Plasmonic Detectors for Beyond-CMOS Plasmonic Majority Logic Gates

Samantha Lubaba Noor, *Member, IEEE,* Kristof Dens, Patrick Reynaert, Francky Catthoor, *Fellow, IEEE*, Dennis Lin, Pol Van Dorpe, and Azad Naeemi, *Senior Member, IEEE*

***Abstract*—In this work, we report the modeling and design of a high-speed Ge-based plasmonic detector coupled with a Metal-Insulator-Metal (MIM) plasmonic majority gate. The detector is designed to distinguish between multiple output levels of the integrated majority gate. Through numerical analyses we predict the proposed plasmonic detector has an intrinsic bandwidth beyond $220GHz$ at an applied bias of only $100mV$. An asymmetric Metal-Semiconductor-Metal (MSM) configuration of the plasmonic detector ensures a dark current of a few nA which results in high sensitivity. The high electric field generated by the electrode asymmetry enables effective separation of the photogenerated carriers resulting in high photocurrent even at few mVs of applied bias. The low capacitance of less than $1fF$ arising from the small detector dimensions results in a high RC-limited bandwidth. Moreover, the narrow plasmonic Ge slot of the photodetector provides a short drift path and fast transit time for carriers. Unlike previously reported plasmonic detectors that use noble metals as electrodes, our proposed detector employs Al and Cu to meet CMOS compatibility requirements and thus can be a potential candidate for high-speed computational systems in industry-level applications. Additionally, the findings presented in the paper will be helpful for the future realization of an integrated plasmonic system.**

***Index Terms*—Integrated optics, majority logic devices, plasmons, photodetectors.**

I. Introduction

OPTICAL computing has attracted a great deal of interest as electronic integrated circuits rapidly approach fundamental scaling limits, and interconnect delay and thermal management in CMOS circuits have become issues of major concern [1], [2], [3], [4]. However, light cannot be confined beyond the diffraction limit of $\lambda_0/2n$ where λ_0 is free space wavelength of light and n is the material refractive index. Hence, the required size of the conventional photonic devices and circuits is on the order of λ_0. Due to size mismatch, on-chip integration of optical components and nm-sized electronic components has become a challenging issue. Surface Plasmon Polariton (SPP), which is an electromagnetic wave propagating at a metal-dielectric interface combines the strong localization of electrons, thanks to its subwavelength confinement, with the fast propagation of photons. Because of these major advantages, plasmonic logic devices and circuits have become subjects of extensive studies [5], [6], [7], [8], [9].

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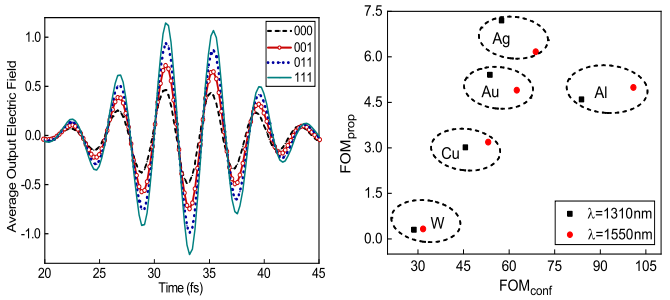
A plasmonic logic gate can operate at the THz frequency range. However, it lacks gain and the signal level decays as more stages are added. Hence, converting plasmonic signals to electrical signals will be an essential part of any plasmonic circuit. The operation bandwidth of the detector and its sensitivity will determine the overall circuit throughput as well as the number of cascadable plasmonic logic stages for a given input power budget. In recent years, there has been a surge of research on plasmonic detectors addressing various aspects such as responsivity, quantum efficiency, speed, and footprint. A plasmonic Ge waveguide detector with an active area of $0.16\mu m \times 10\mu m$ operating at $\lambda = 1310nm$ has been demonstrated to have $100GHz$ of bandwidth [10]. However, a high voltage of $7.5V$ is used to achieve this bandwidth and the associated dark current is relatively high ($I_{dark} = 2\mu A$). Another work has presented a Ge detector based on long range dielectric loaded surface plasmon polariton (LRDLSPP) with a bandwidth of $150GHz$ at a bias voltage of $4V$ [11]. Additionally, plasmonic detectors based on graphene have been demonstrated to have a bandwidth greater than $110GHz$ at applied biases of $1V$ [12] and $1.6V$ [13]. These plasmonic detectors and a number of other reported detectors [14], [15], [16] use the noble metal Au as electrode which is not compatible with CMOS fabrication processes.

All these previous works mainly focus on the detector alone and do not consider the interaction between the logic gate and the detector and associated design trade-offs. In a plasmonic majority gate, information is encoded in both phase and amplitude. However, direct detection of the phase of a plasmonic signal with a frequency of hundreds of THz is very challenging if not impossible. An additional reference signal can be used to convert phase information to signal amplitude [17]. With this approach, various input combinations result in different output levels. Hence, the plasmonic detector needs to distinguish between these levels rather than choosing between signal and no signal as all previous works have studied. In this work, we study a Ge-based asymmetric MSM plasmonic detector which is optimized for detecting the output levels of a plasmonic MIM majority gate. The MSM configuration is used because of its simple fabrication process and compatibility with the preamplifier circuits [18]. The monolithic integration of MSM detectors with Field Effect Transistors (FET) is simple because the electrodes of the MSM photodetector and the gate fingers of a FET can be defined with the same photolithographic step and then deposited with the same metallization [19]. An MSM detector also offers much lower capacitance per unit area compared to p-i-n photodiode and as a result, can operate



(a) (b)

Fig. 1. (a) Spatial average of the transverse component of the electric field at the output of Al-SiO2-Al majority gate for four out of eight possible input combinations. The other four combinations are repetitive, and hence redundant. (b) Comparison of figures of merit for propagation and confinement of the MIM waveguide for different metals.

at a higher bandwidth. Ge is chosen as the active material of the detector because of its large absorption coefficient at communication wavelengths, low cost, and compatibility with CMOS fabrication processes.

Our proposed plasmonic detector is predicted to attain a bandwidth above $220GHz$ at only $100mV$ of applied bias. The detector's active region footprint is only $0.9\mu m \times 2\mu m$. Additionally, the dark current is predicted to be as low as $2nA$. Moreover, we used Cu and Al as electrode metals which are CMOS process compatible. The proposed high-speed plasmonic detector can be used in high-end server system applications where high speed, small area and streaming data are the most important criteria.

II. MIM Plasmonic Logic Gate

The 3-input majority gate, proposed by Dutta *et al.* [17], is based on plasmonic slot waveguides with a SiO2 slot sandwiched between two Ag surfaces. We are going to summarize the structure and logic operation of the majority gate using Al as the metal layer and $\lambda_0 = 1310nm$ as the wavelength of operation. The identical SPP modes at the two individual Al-SiO2 interfaces are coupled and generate a gap-SPP mode in the SiO2 slot with effective index, $n_{eff} = 1.594 + j0.018$.

The gate consists of three regions: input, combiner, and output. Plasmon waves from the three input waveguides traverse the same path length and interfere at the combiner region. The phase of the three signals have to be controlled before the combiner section. Input region is $200nm$ long, while the length of the combiner region depends on the bending angle $(35°)$ of the bent waveguides. To provide reasonable on-chip packing density and cross-talk noise, a $360nm$ pitch (center-center distance) is maintained between the input waveguides [17]. Moreover, the output waveguide is made wider ($W_{out} = 120nm$) compared to the input waveguides ($W_{in} = 60nm$) to match the waveguide impedance and to improve transmission.

For the logic operation, the phase of the plasmonic wave is considered as the computational state variable. For instance, phase π and 0 represent logic 0 and logic 1 respectively. At the combiner output, both amplitude and phase of the field contain the signal information. For example, input combinations 000 and 111 produce the same amplitude at the combiner output but maintain a π phase difference. A reference signal is added to convert the phase information into signal intensity which circumvents the challenging task of THz phase-detection of the SPP waves. One can get different output field amplitudes to distinguish among the four possible cases: strong majority 1 (111), weak majority 1 (011/101/110), strong majority 0 (000), and weak majority 0 (001/010/100) as shown in Fig. 1a. Including the reference waveguide, the logic gate footprint is $1.57\mu m \times 1.2\mu m$, which is much smaller than other proposed plasmonic logic gates [20], [21].

Two important parameters for plasmonic-based devices are propagation length (L_p) and confinement (δ). L_p is the characteristic length after which the intensity of field decreases to $1/e$ of its initial value due to loss, and δ is a measure of field confinement in the transverse direction inside the metal. The two figures of merit for the MIM plasmonic waveguide for confinement and propagation respectively can be described as [17]:

$$FOM_{conf} = \frac{\lambda_0}{\delta}, \quad FOM_{prop} = \frac{L_p}{\lambda_{spp}} \tag{1}$$

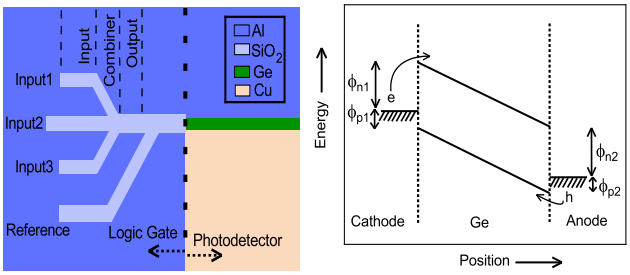
Here, λ_{spp} is the SPP wavelength which is smaller than the free space wavelength, λ_0.

The performance of different metals used in the MIM waveguide with SiO2 core is summarized in terms of FOM_{prop} and FOM_{conf} in Fig. 1b. The majority of works on plasmonic devices are based on Au or Ag due to their low loss at optical frequencies. However, these noble metals are not compatible with standard silicon manufacturing processes as they act as contaminants [22]. Besides, Drude-damping in the noble metals increases greatly due to imperfections such as roughness and grain boundary scattering [23]. Recently, Al has become a promising substitute for the noble metals in plasmonic structures [24], [25], [26]. It is low-cost, mass-producible, and most importantly, compatible with standard CMOS process. Al provides better confinement, while its FOM_{prop} value is comparable to Au or Ag, as shown in Fig. 1b. For these reasons, in this work, we use Al for the MIM structure instead of Ag which was used in the previously proposed plasmonic majority gate [17].

III. Plasmonic Detector Structure

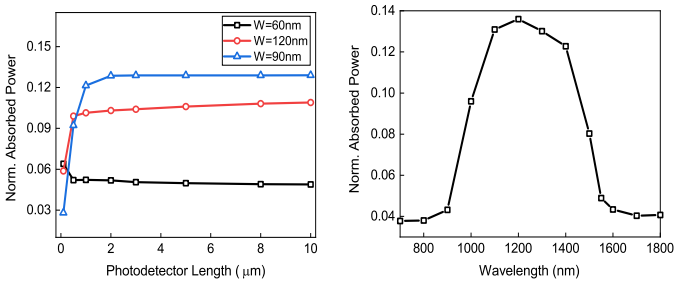
An MSM plasmonic detector with Ge as absorbing semiconductor and Al and Cu as lateral claddings is designed and coupled with the MIM logic gate in butt-coupling configuration as shown in Fig. 2a. Plasmons from the MIM waveguide are evanescently coupled to the MSM waveguide and absorbed while propagating in the Ge core, thereby generating electron-hole pairs. These photogenerated carriers are separated by the applied electric field and drift towards the metallic claddings, generating photocurrent. Coupling efficiency is determined by reflection from the coupling interface and transmission in the MSM waveguide.

The detector consists of two back-to-back Schottky diodes, formed by the metal and semiconductor interfaces. Thickness (t) of the active region of the detector is $100nm$ to



(a) (b)

Fig. 2. (a) MSM plasmonic detector integrated to MIM plasmonic logic gate. Inset shows the materials used in the coupled structure (b) Band diagram of an MSM photodetector. ϕ_n and ϕ_p represent SBH for electron, e and hole, h respectively at the electrodes.



(a) (b)

Fig. 3. Absorbed power variation in Ge with (a) varying width and length of the MSM detector (b) varying operating wavelength for $W = 90nm, L = 5\mu m$.

ensure dimension compatibility with the logic gate, while length (L) and width (W) are optimized in a later section. Optimization of these values depends on coupling efficiency with the MIM waveguide, plasmon absorption in Ge, and the transient performance of the device. Although MSM detectors are not intentionally doped conventionally, Ge films show p-type behavior due to structural imperfections [10], [27]. To mimic this, a uniform p-doping with $N_a = 5 \times 10^{16} cm^{-3}$ is considered for the Ge layer.

One issue with Ge-based MSM detectors is that they suffer from high dark current due to carrier injection over small Schottky barrier that results from Fermi level pinning at the metal-Ge junction [28]. Using amorphous Ge [29], insertion of higher bandgap interlayer of doped a-Si:H or TiO2 between Ge and metal [30], dopant segregation process [31], and using asymmetric electrode metal contacts [32], [33] can increase the SBH. In this work, we have applied the concept of asymmetrical metal electrodes proposed in earlier works [32], [33] to reduce the dark current of the plasmonic detector.

Fig. 2b shows a generalized band diagram of an MSM photodetector. When same metal is used for both electrodes, an increase in the barrier height for electrons in the cathode (ϕ_{n1}) reduces the barrier height for holes in the anode (ϕ_{p2}) since, $\phi_{n1} + \phi_{p2} = E_g$. By using two different metals for electrodes, barrier height can be tailored independently as $\phi_{n1} + \phi_{p2} \geq E_g$ [34]. We have chosen Al and Cu for the detector electrodes. Although Cu is known to be lossy, it has been demonstrated that it is possible to fabricate truly nanoscale ultra-low-loss copper plasmonic components [35] and unlike Au and Ag, an industry standard process can be used.

IV. Simulation Method

The MIM-MSM structure is simulated using Lumerical's commercially available 'DEVICE Multiphysics Simulation Suite'. The 3D Finite Difference Time Domain (FDTD) method is used to solve Maxwell's equations and calculate the electric and magnetic fields on a spatio-temporal grid. The classical Maxwell's equations are sufficient for our structure since plasmons can be accurately described by classical Maxwell's equations when the feature size of a structure is not less than $10nm$ [36]. An absorbing boundary condition based on perfectly matched layers (PML) is used in the FDTD solver. The refractive indices of Al and Cu in our simulations are obtained from Palik's Handbook of optical constants [37].

A standard mode source injects the fundamental guided mode in the form of Gaussian pulse into the input MIM waveguide. From electric field distribution (E) and permittivity data (ε) inside the Ge layer, the absorption profile (P_{abs}) and optical generation rate (G) are calculated under the assumption that each absorbed photon excites an electron-hole pair:

$$G = \frac{P_{abs}}{\hbar\omega} = -\frac{0.5|E|^2 Im(\varepsilon)}{\hbar} \tag{2}$$

The photogeneration rate data from FDTD solver is imported as input for the 'Device Charge Transport' solver of Lumerical to perform the electrical simulations. The 3D optical generation rate from FDTD solver is averaged along the length since the detector is relatively uniform along its length. This allows 2D electrical simulation reducing the simulation time significantly. Default workfunction values for the metals have been used with $\phi_{Cu} = 4.65eV$ and $\phi_{Al} = 4.28eV$. Scattering dependent mobility model, field dependent mobility model, doping dependent Shockley-Read-Hall (SRH) recombination model, and surface recombination models are incorporated during simulation.

V. Results

A. Power Absorption in Ge

An important metric for plasmonic circuits is the fraction of the plasmons that are lost in the waveguides or not absorbed by the detector. To study the loss in the majority gate, a $2\mu m \times 1\mu m$ frequency domain power monitor in the FDTD simulation tool is used, with the three inputs set to logic 1. We found that 35% of the total input power is transmitted through the MSM waveguide and delivered to the detector. This significant loss is due to the inherent losses in metals, bending losses in the plasmonic MIM waveguides, and coupling loss between the MIM and MSM waveguides. The absorption of plasmons inside the Ge film depends on the detector dimensions and operating wavelength.

The absorbed power in the Ge layer normalized to the majority gate input power for 111 input is shown in Fig. 3(a). From electric field and index data, absorbed power at each 3-D point is calculated and integration is performed over the

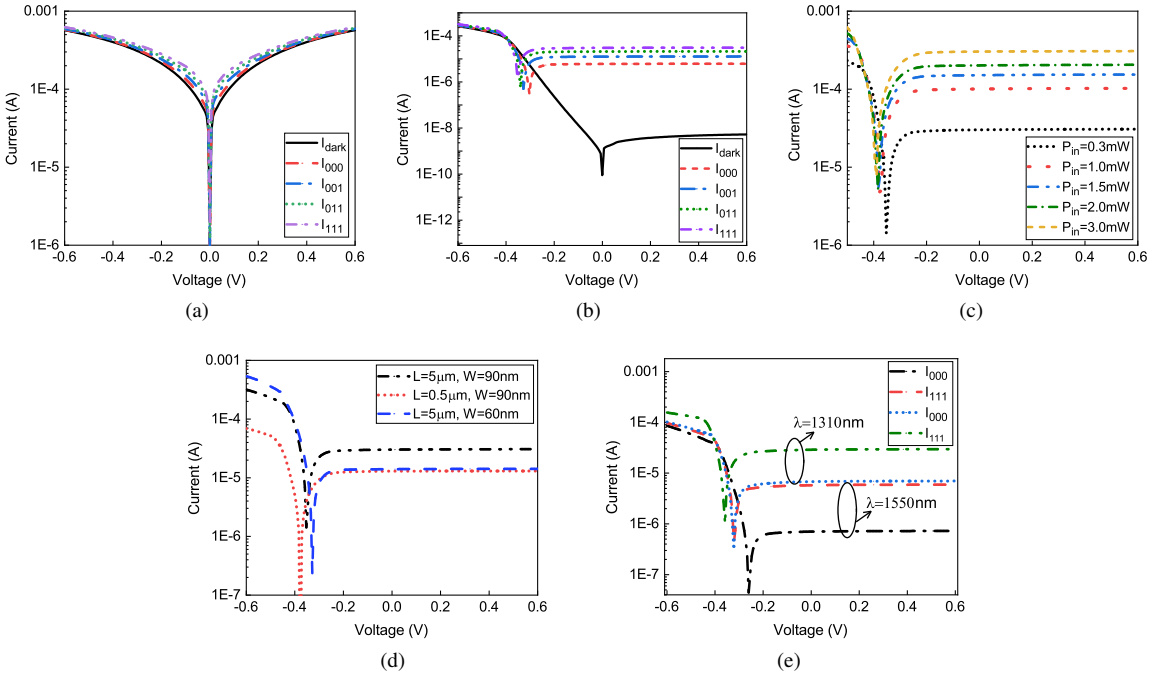


Fig. 4. I-V characteristics for different input logic levels and dark condition for (a) Al-Ge-Al symmetric MSM detector (b) Al-Ge-Cu asymmetric MSM detector. For the Al-Ge-Cu detector, on-state current variation is shown for (c) different input power levels (d) different detector dimensions, and (e) different operating wavelengths. $W = 90nm, L = 5\mu m$.

volume of the Ge layer. The values are normalized to the overall input power of the majority gate. For $W = 90nm$, there is a sharp increase in absorption from $L = 100nm$ to $1\mu m$ and little change for $L > 2\mu m$ which indicates that most plasmons are absorbed within the first $1\mu m$. Absorption is also a strong function of the Ge slot width. Due to mode mismatch, there is reflection when the MIM and MSM waveguides are coupled. When the slot widths in the detector and output MIM waveguide are same $(W = 120nm)$, there is considerable reflection resulting in less absorption compared to the $W = 90nm$ case, even though it provides a larger area for plasmon absorption. For $W = 60nm$, absorption is much smaller because of higher reflection from the MIM-MSM waveguide coupling interface as well as increased absorption in the metal since more power is squeezed out of the narrow Ge core.

Fig. 3b shows absorption in Ge versus free space wavelength of the input signal at the MIM logic gate. Maximum absorption occurs at $\lambda = 1200nm$. For $1100nm < \lambda < 1450nm$, absorption is within 90% of the maximum value. For simulation, we are considering the wavelengths of $1310nm$ and $1550nm$ which are global standards for optical communication systems. Moreover, it is evident from Fig. 3b that absorption at $\lambda = 1550nm$ is significantly smaller than absorption at $\lambda = 1310nm$.

B. Steady State Analysis

The integrated MIM-MSM structure is simulated in the 'Device Charge Transport' solver of Lumerical to evaluate steady state operation. In the case of an asymmetric MSM detector, the lower workfunction metal (Al) is used as the anode, where the positive bias is applied (forward bias condition). This helps to get the same level of semiconductor depletion and internal electric field at a lower bias voltage compared to the symmetric case and enables low voltage operation.

Fig. 4 shows steady state performance of the detector for dark as well as various input logic conditions. An overall input power (P_{in}) of $0.3mW$ is assumed unless otherwise specified. For the Al-Ge-Al symmetric MSM detector, at $V = 0.1V$, the dark current (I_{dark}) is only 1.2 times smaller than the lowest logic current, I_{000} as shown in Fig. 4a. The high value of I_{dark} in a symmetric MSM detector can become an issue for detecting the weakest signal, I_{000}. However, in the asymmetric case shown in Fig. 4b, I_{dark} becomes 3 orders of magnitude smaller than I_{000} and the logic levels are more distinguishable at forward bias. At reverse bias, I_{dark} increases rapidly due to small SBH for carriers at the electrodes (ϕ_{p1}, ϕ_{n2}). For this reason, we are particularly interested in the forward bias region. Moreover, when $V = 0V$, photocurrent is high due to the built-in potential resulting from the electrode asymmetry.

Fig. 4c shows that as the input power level decreases, there is a linear drop in the detector current. Next, we study the impact of various detector dimensions. The trends for the impact of the detector length and width on current are similar to those for absorption, which were shown in Fig. 3a. It is seen in Fig. 4d that $W = 90nm$ and $L = 5\mu m$ result in a higher photocurrent compared to $L = 0.5\mu m$ due to more absorption in Ge. In addition, when L is fixed at $5\mu m$, current decreases as W is changed from $90nm$ to $60nm$ due to the increase in coupling reflection and metal absorption. Fig. 4e compares the detector output for the two different wavelengths mostly used in optical communications. For the same input

power level, at V=0.1V, $I_{000}(\lambda = 1310nm)$ is almost an order of magnitude larger than $I_{000}(\lambda = 1550nm)$. Although FOM_{conf} and FOM_{prop} degrade at $\lambda = 1310nm$ as shown in Fig. 1b, due to higher current level, $\lambda = 1310nm$ is chosen as the wavelength of operation for the coupled MIM-MSM configuration.

C. Transient Analysis

In the previous section we analyzed the static performance of the detector, this section will focus on the dynamic behavior of the plasmonic detector. Due to subwavelength confinement of SPP, the width of the active region of the proposed detector is less than $100nm$ which ensures short transit times for the photogenerated carriers in Ge. In addition, due to the asymmetry in the electrode workfunctions, a strong internal electric field exists in the plasmonic Ge slot region even without any applied voltage. The transit-time-limited bandwidth can be estimated from the carrier saturation velocity (v_{sat}) and electrode spacing (W) as [38],

$$f_t = \frac{0.45 v_{sat}}{W} \tag{3}$$

Assuming a carrier saturation velocity of $6 \times 10^6 cms^{-1}$ in Ge, a transit-time-limited bandwidth of $300GHz$ can be achieved for $W = 90nm$.

To investigate the RC-limited bandwidth of the device, the detector capacitance is calculated next. A variable frequency small signal is superimposed on a fixed bias and applied to the detector. The admittance is calculated and capacitance is extracted using,

$$Y(w) = \left(R_{pd} + \frac{1}{jwC_{pd}} \right)^{-1} \tag{4}$$

where R_{pd} is the series resistance of the detector equivalent circuit. For the detector with $W = 90nm$ and $L = 5\mu m$, the calculated value of capacitance including contact capacitance is, $C_{pd} = 0.9fF \approx 1fF$. This small value of capacitance arises from the small dimensions of the plasmonic detector. Less than $1ps$ is needed to charge up the capacitor to a voltage of $5mV$ even when the weakest majority logic signal (000) is present. Moreover, a metallic waveguide has a small resistance and metallic lateral claddings of the detector can be used as low resistive contacts [10]. This leads to an RC-limited bandwidth of few THz if a 50Ω purely resistive load is connected to the detector. Hence, the intrinsic bandwidth of a device like this would be transit-time-limited ($\sim 300GHz$).

To confirm these results, we also investigated the dynamic behavior of the plasmonic detector by running transient simulations and performing a Fourier transform of the impulse current response. The high-field mobility model is especially important for transient analysis to avoid overestimation of the bandwidth. Fig. 5a shows the normalized frequency response of the detector with $W = 90nm$ and four different bias voltages. We can see that the bandwidth is $220GHz$ at $100mV$, which is close to the estimated value of $300GHz$. As the applied positive voltage is increased, it aids the downward band tilting at the anode which results in a stronger electric field inside the Ge slot and therefore a higher bandwidth.

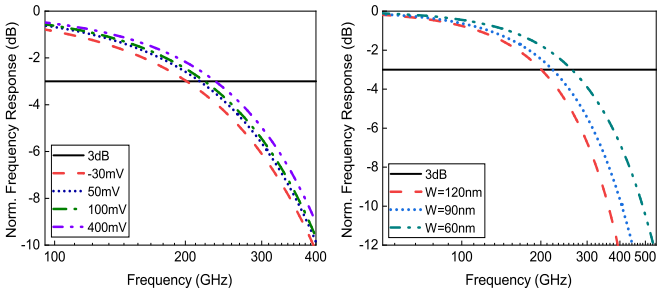


Fig. 5. Detector intrinsic bandwidth for (a) varying applied voltage with $W = 90nm$ (b) varying detector width with $V = 100mV$. $L = 5\mu m$.

When a negative voltage ($V = -30mV$) is applied, it causes the band to move upward at the anode end which decreases the device bandwidth.

The transient behavior is also simulated for different detector widths. As the width of the active region decreases, the carrier drift path gets smaller resulting in shorter transit time and higher bandwidth as shown in Fig. 5b. It is possible to get very high bandwidth by using a very narrow active region. However, as the Ge width is reduced, more energy enters into the metallic layer and absorption in the metal dominates. Although $W \leq 60nm$ provides an intrinsic bandwidth of over $250GHz$, considering the metal absorption issue, $W = 90nm$ is the selected optimized width which offers a good balance between current and bandwidth. Moreover, for $W = 90nm$, although $L = 5\mu m$ is used in simulations, the detector length can be decreased to $L = 2\mu m$ with negligible change in the absorbed power and hence current as shown in Fig. 3a. Additionally, since the detector is transit-time-limited, bandwidth is not affected as well. So, $L = 2\mu m$ is the selected optimized length of the detector. Detector bandwidth is also a function of Ge doping level, increasing in value when a lower doping level is used.

D. Design Considerations for the Detector's Load Circuit

The weak current signal generated by the detector needs to be amplified using a transimpedance amplifier (TIA). A large TIA resistor improves the transimpedance gain but degrades the overall RC-limited bandwidth of the detector. The input capacitance of the amplifier is also an important factor that can be larger than the intrinsic capacitance of the detector depending on the size of transistors and the technology node. In this section, we quantify the impact of the TIA resistance and capacitance on bandwidth and overall performance and determine the maximum load capacitance for a target bandwidth. This will allow to dimension the full system once also the CMOS circuit design stage is worked out in more detail. We believe that independent of the specific direction of circuit optimization, the analysis below remains valid and useful.

Fig. 6a shows the equivalent circuit of the detector with TIA and a capacitive load (C_L). The shunt resistance, R_p can be calculated from the slope of the I-V curve at $V = 0V$ and it is $60M\Omega$ for the proposed detector. As TIA resistance and load capacitance increase, RC bandwidth decreases below

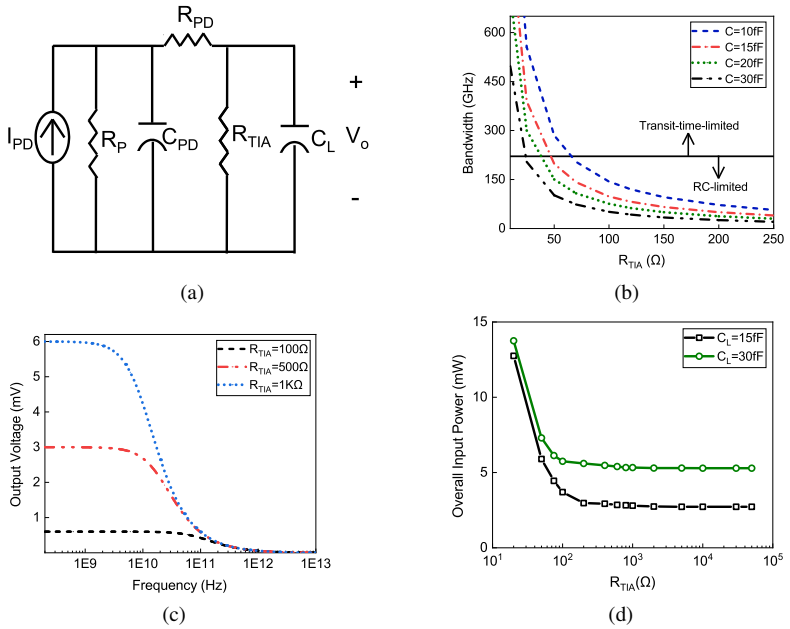


Fig. 6. (a) Equivalent circuit of the detector with a resistive TIA in parallel with a capacitive load (b) Effect of TIA resistor on the overall bandwidth of the detector. Arrows indicate the regions where RC-limited and transit-time-limited bandwidths are dominant (c) Output voltage, V_o variation with R_{TIA} when 000 is applied at the logic gate input. $C_L = 15fF$ (d) Variation of the required overall input power for getting $V_o = 5mV$ at $100GHz$.

$220GHz$ and the detector changes from transit-time-limited to RC-limited as shown in Fig. 6b. For calculating the bandwidth, we assumed a detector series resistance, $R_{pd} = 50\Omega$. So, if we want to take advantage of the high intrinsic bandwidth of the detector, R_{TIA} and C_L need to be designed accordingly. For example, if $R_{TIA} = 50\Omega$ is used, we need to ensure the capacitive load associated with the CMOS circuit is less than $15fF$ to reach an overall bandwidth of $220GHz$.

The voltage swing required at the TIA output depends mainly on noise and offset of the comparator which restores the sampler output signal to digital voltage levels. The input referred noise of state-of-the-art comparators is around $1mV$ root mean square (rms) [39], so a few mV's of signal swing are required to have a large signal-to-noise ratio (SNR) ensuring a low bit-error-rate. Since, I_{000} is the lowest current level, the voltage corresponding to I_{000} needs to be above the noise level. Fig. 6c shows how R_{TIA} affects the output voltage (V_o) swing when 000 logic is applied at the majority gate input. Fig. 6d shows the overall input power requirement for getting $V_o = 5mV$ at $100GHz$ when $100mV$ bias voltage is applied to the detector. As R_{TIA} is increased, V_o increases and less input power is required to have the same level of output. Increasing R_{TIA} also decreases the RC bandwidth resulting in attenuation of voltage at high frequency. For this reason, required input power decreases very little when $R_{TIA} > 500\Omega$ is used. Moreover, as C_L increases, the input power requirement increases as shown in Fig. 6d.

It is important to highlight that the proposed $220GHz$ bandwidth of the detector is higher than the experimentally observed bandwidth of a plasmonic Ge detector [10]. However, as shown in Fig. 4a of Ref. [10], measured frequency response was flat up to $100GHz$. Higher frequency measurements were not done due to instrumental limitations as losses in the cable, connectors, and probe result in low SNR values. Moreover, the fabricated detector had symmetric metal electrode and wider active region compared to our proposed detector. Therefore, the proposed detector attains higher electric field, and hence improved speed performance for the same applied bias compared to the fabricated detector. Moreover, the prediction of the $220GHz$ bandwidth of a Ge-based plasmonic detector with a narrower waveguide is in agreement with similar simulations of Fig. S2(b) in Ref. [10].

The majority gate structure under consideration can implement all Boolean functionality also. Additionally, the MIM waveguide structure with some extension can realize the so-called threshold logic and can then be used as a building block for counters and multipliers, which we discussed in another work [40]. However, the logic structure cannot operate alone and the optical output needs to be converted to the electrical domain for data interpretation. This work highlights guidelines regarding the co-optimization of the logic gate-detector structure, design considerations of the receiver circuit, and trade-off between speed and gain performance of the detector. This information is critical to know before fabricating a fully functional device demonstrator. While the exact value of the bandwidth might turn out to be lower or higher than $220GHz$ in reality, we believe the general trends and trade-offs are going to be valid and of interest to researchers working on beyond-CMOS plasmonic circuits.

E. Noise in the Detector

Noise in the detector is an essential parameter for consideration. For a photodetector, Noise Equivalent Power (NEP) is a metric to quantify the minimum detectable signal power [41]:

$$NEP = P_{in,d}\frac{i_n}{I_{ph}} \tag{5}$$

Where i_n is the noise current, $P_{in,d}$ is the detector's input power, and I_{ph} is the photocurrent. In a photodetector, two types of noise mainly affect the detection performance: shot noise due to generation of carriers in dark condition and thermal noise due to the random motion of carriers. Total noise of the detector is [41],

$$i_n^2 = \left(2qI_{dark} + \frac{4K_BT}{R_p}\right) B \tag{6}$$

Here, I_{dark} is the dark current, K_B is Boltzmann constant, and B is detector's bandwidth. Using the values of I_{dark} and I_{ph} at $V = 100mV$, calculated R_P from section $V(D)$, the calculated noise current and NEP of the proposed detector are $35fAHz^{-1/2}$ and $0.12pWHz^{-1/2}$, respectively. For reference, NEP value of a commercially available high-speed InGaAs p-i-n photodetector (UPD-15-IR2-FC, ALPHALAS GmbH) with a bandwidth $> 25GHz$ is $1fWHz^{-1/2}$. For the bandwidth of $220GHz$, the NEP value of the proposed device refers to a noise power level of $56.2nW$. As discussed in section $V(A)$, 35% of the input power is transmitted to the MSM detector; so noise imposes a limit of $0.16\mu W$ on the total input power of the majority gate.

In addition to the noise of the detector itself, the CMOS load circuit introduces noise. For instance, input-referred noise current of a TIA is inversely proportional to $\sqrt{R_{TIA}}$. Therefore, a large TIA resistor will be needed for good noise performance which reduces the overall bandwidth of the detector. So, there is a trade-off between noise performance and overall detection speed while choosing the value of R_{TIA}.

VI. Conclusion

In this work, we have studied a plasmonic Ge MSM detector which is designed to detect the outputs of a coupled MIM plasmonic majority gate. The detector has a narrow active region of $W = 90nm$ and suppressed dark current of a few nA with a photocurrent to dark current ratio of $I_{photo}/I_{dark} > 10^3$ at forward bias. The high internal electric field helps in fast transit of the photogenerated carriers leading to an intrinsic bandwidth of more than $220GHz$. In addition, the proposed detector can operate at a low bias voltage of $100mV$ or less. We also considered the load circuit of the detector and analyzed how a transimpedance amplifier with a capacitive load affects the output voltage swing as well as overall bandwidth of the device.

Appendix
Proposed Fabrication Method of the Detector

To understand the feasibility of the proposed device, here we discuss a possible technology and steps that can be followed to fabricate the asymmetric MSM structure.

At first, SiO2 will be grown on Si substrate by high-temperature oxidation, which opens a Si seeding window in the oxide. Amorphous Ge with a thickness of $100nm$ will be deposited using low-pressure CVD. The deposited Ge will be patterned and aligned subsequently to the Si seeding window. To encapsulate the deposited Ge, a thin layer of low-temperature SiO2 will be deposited. Rapid thermal annealing will then be used to melt the Ge. Crystalline Ge will start growing from the Si/Ge interface, and this will propagate laterally through the Ge liquid on top of SiO2. After etching the oxide, Focused Ion Beam milling process will be used to fabricate the active area of the detector. The same process has been used in [42] to deposit crystalline Ge on SiO2. The process can be visualized from Fig. 3 of Ref. [42].

Once the Ge active area is fabricated, asymmetric metals can be deposited using different technologies. The e-beam evaporation, patterning, and lift-off process can be used for metal electrode deposition, as demonstrated in [10]. However, for the asymmetric MSM structure, we will need two sequential lift-off processes: one for Al and one for Cu. Moreover, we can use the directional deposition technique for two metals, which has been demonstrated for fabricating a Si-based asymmetric MSM photodetector with an electrode spacing of only $75nm$ [15]. The process can be visualized from Fig. S2 of Ref. [15]. In this case, an oxide layer grown on Ge acts as a hard mask for metal evaporation. Metal evaporation will take place from both sides of Ge at a grazing incidence to the plane of the chip. The metals will be deposited on the oxide hard mask also. Metal lift-off followed by oxide etching will create the final MSM structure with different metal electrodes.

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References

[1] C. M. Santori, J. Pelc, R. Bose, C. Li, and R. G. Beausoleil, "Optical logic gates," U.S. Patent 10 386 698, Aug. 20, 2019.
[2] S. C. Xavier, B. E. Carolin, A. P. Kabilan, and W. Johnson, "Compact photonic crystal integrated circuit for all-optical logic operation," *IET Optoelectron.*, vol. 10, no. 4, pp. 142–147, Aug. 2016.
[3] H. Yang, V. Khayrudinov, V. Dhaka, H. Jiang, A. Autere, H. Lipsanen, Z. Sun, and H. Jussila, "Nanowire network–based multifunctional all-optical logic gates," *Sci. Adv.*, vol. 4, no. 7, p. eaar7954, Jul. 2018.
[4] Z. Cheng, C. Ríos, N. Youngblood, C. D. Wright, W. H. Pernice, and H. Bhaskaran, "Device-level photonic memories and logic applications using phase-change materials," *Adv. Mater.*, vol. 30, no. 32, p. 1802435, Aug. 2018.
[5] X. Yang, X. Hu, H. Yang, and Q. Gong, "Ultracompact all-optical logic gates based on nonlinear plasmonic nanocavities," *Nanophotonics*, vol. 6, no. 1, p. 365, Aug. 2017.
[6] W. Huang, Y. Zhou, J. Du, Y. Deng, and Y. He, "Versatile visual logic operations based on plasmonic switching in label-free molybdenum oxide nanomaterials," *Anal. Chem.*, vol. 90, no. 3, pp. 2384–2388, Jan. 2018.
[7] D. Pan, H. Wei, and H. Xu, "Optical interferometric logic gates based on metal slot waveguide network realizing whole fundamental logic operations," *Opt. Express*, vol. 21, no. 8, pp. 9556–9562, Apr. 2013.
[8] Z. Liu, L. Ding, J. Yi, Z. Wei, and J. Guo, "Design of a multi-bits input optical logic device with high intensity contrast based on plasmonic waveguides structure," *Opt. Commun.*, vol. 430, pp. 112–118, Jan. 2019.
[9] D. Dragoman and E. Vlădescu, "Ring-shaped plasmonic logic gates," *Plasmonics*, vol. 14, no. 1, pp. 71–78, Feb. 2019.
[10] Y. Salamin, P. Ma, B. Baeuerle, A. Emboras, Y. Fedoryshyn, W. Heni, B. Cheng, A. Josten, and J. Leuthold, "100 GHz plasmonic photodetector," *ACS Photonics*, vol. 5, no. 8, pp. 3291–3297, Jun. 2018.
[11] J. Gosciniak and M. Rasras, "High-bandwidth and high-responsivity waveguide-integrated plasmonic germanium photodetector," *J. Opt. Soc. Am. B*, vol. 36, no. 9, pp. 2481–2491, Sep. 2019.
[12] P. Ma, Y. Salamin, B. Baeuerle, A. Josten, W. Heni, A. Emboras, and J. Leuthold, "Plasmonically enhanced graphene photodetector featuring 100 Gbit/s data reception, high responsivity, and compact size," *ACS Photonics*, vol. 6, no. 1, pp. 154–161, Nov. 2018.

[13] Y. Ding, Z. Chen, X. Zhu, K. Yvind, J. Dong, M. Galili, H. Hu, N. Mortensen, S. Xiao, and L. Oxenløwe, "Ultra-compact integrated graphene plasmonic photodetector with bandwidth over 110 GHz," *Nanophotonics*, vol. 9, no. 2, pp. 317–325, Feb. 2020.

[14] M. Tanzid, A. Ahmadivand, R. Zhang, B. Cerjan, A. Sobhani, S. Yazdi, P. Nordlander, and N. J. Halas, "Combining plasmonic hot carrier generation with free carrier absorption for high-performance near-infrared silicon-based photodetection," *ACS Photonics*, vol. 5, no. 9, pp. 3472–3477, Aug. 2018.

[15] S. Muehlbrandt, A. Melikyan, T. Harter, K. Köhnle, A. Muslija, P. Vincze, S. Wolf, P. Jakobs, Y. Fedoryshyn, W. Freude *et al.*, "Silicon-plasmonic internal-photoemission detector for 40 Gbit/s data reception," *Optica*, vol. 3, no. 7, pp. 741–747, Jul. 2016.

[16] P. Neutens, P. Van Dorpe, I. De Vlaminck, L. Lagae, and G. Borghs, "Electrical detection of confined gap plasmons in metal–insulator–metal waveguides," *Nat. Photonics*, vol. 3, no. 5, p. 283, May 2009.

[17] S. Dutta, O. Zografos, S. Gurunarayanan, I. Radu, B. Soree, F. Catthoor, and A. Naeemi, "Proposal for nanoscale cascaded plasmonic majority gates for non-Boolean computation," *Sci. Rep.*, vol. 7, no. 1, p. 17866, Dec. 2017.

[18] K. C. Saraswat, C. O. Chui, P. C. McIntyre, and B. B. Triplett, "Novel germanium technology and devices for high performance mosfets and integrated on-chip optical clocking," in *Silicon Nitride and Silicon Dioxide Thin Insulating Films: Proc. Int. Symp.* Electrochemical Society., 2003, p. 55.

[19] P. R. Berger, "Metal-semiconductor-metal photodetectors," in *Testing, Reliability, and Applications Optoelectronic Devices*, vol. 4285. International Society for Optics and Photonics, 2001, pp. 198–207.

[20] Y. Fu, X. Hu, C. Lu, S. Yue, H. Yang, and Q. Gong, "All-optical logic gates based on nanoscale plasmonic slot waveguides," *Nano Lett.*, vol. 12, no. 11, pp. 5784–5790, Nov. 2012.

[21] J. Doevenspeck, O. Zografos, S. Gurunarayanan, R. Lauwereins, P. Raghavan, and B. Sorée, "Design and simulation of plasmonic interference-based majority gate," *AIP Adv.*, vol. 7, no. 6, p. 065116, Jun. 2017.

[22] A. Lefebvre, D. Costantini, I. Doyen, Q. Lévesque, E. Lorent, D. Jacolin, J. Greffet, S. Boutami, and H. Benisty, "CMOS compatible metal-insulator-metal plasmonic perfect absorbers," *Opt. Mater. Express*, vol. 6, no. 7, pp. 2389–2396, Jul. 2016.

[23] A. S. Baburin, A. M. Merzlikin, A. V. Baryshev, I. A. Ryzhikov, Y. V. Panfilov, and I. A. Rodionov, "Silver-based plasmonics: golden material platform and application challenges," *Opt. Mater. Express*, vol. 9, no. 2, pp. 611–642, Feb. 2019.

[24] D. Gérard and S. K. Gray, "Aluminium plasmonics," *J. Phys. D: Appl. Phys.*, vol. 48, no. 18, p. 184001, Dec. 2014.

[25] J. Martin and J. Plain, "Fabrication of aluminium nanostructures for plasmonics," *J. Phys. D: Appl. Phys.*, vol. 48, no. 18, p. 184002, Dec. 2014.

[26] M. W. Knight, L. Liu, Y. Wang, L. Brown, S. Mukherjee, N. S. King, H. O. Everitt, P. Nordlander, and N. J. Halas, "Aluminum plasmonic nanoantennas," *Nano Lett.*, vol. 12, no. 11, pp. 6000–6004, Oct. 2012.

[27] M. Mäenpää, T. Kuech, M.-A. Nicolet, S. Lau, and D. Sadana, "The heteroepitaxy of Ge on Si: a comparison of chemical vapor and vacuum deposited layers," *J. Appl. Phys.*, vol. 53, no. 2, pp. 1076–1083, Feb. 1982.

[28] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. Evangelou, "Fermi-level pinning and charge neutrality level in germanium," *Appl. Phys. Lett.*, vol. 89, no. 25, p. 252110, Dec. 2006.

[29] J. Oh, S. K. Banerjee, and J. C. Campbell, "Metal-germanium-metal photodetectors on heteroepitaxial Ge-on-Si with amorphous Ge Schottky barrier enhancement layers," *IEEE Photonics Technol. Lett.*, vol. 16, no. 2, pp. 581–583, Feb. 2004.

[30] H.-J. Zang, G.-S. Kim, G.-J. Park, Y.-S. Choi, and H.-Y. Yu, "Asymmetrically contacted germanium photodiode using a metal–interlayer–semiconductor–metal structure for extremely large dark current suppression," *Opt. Lett.*, vol. 41, no. 16, pp. 3686–3689, Aug. 2016.

[31] K.-W. Ang, M.-B. Yu, S.-Y. Zhu, K.-T. Chua, G.-Q. Lo, and D.-L. Kwong, "Novel NiGe MSM photodetector featuring asymmetrical schottky barriers using sulfur co-implantation and segregation," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 708–710, Jul. 2008.

[32] H. Fresser, F. Prins, and D. Kern, "Low-energy electron detection in microcolumns," *J. Vac. Sci. Technol., B: Microelectron. Nanometer Struct.–Process., Meas., Phenom.*, vol. 13, no. 6, pp. 2553–2555, Nov. 1995.

[33] C. O. Chui, A. K. Okyay, and K. C. Saraswat, "Effective dark current suppression with asymmetric MSM photodetectors in group IV semiconductors," *IEEE Photonics Technol. Lett.*, vol. 15, no. 11, pp. 1585–1587, Oct. 2003.

[34] W. Wohlmuth, M. Arafa, A. Mahajan, P. Fay, and I. Adesida, "InGaAs metal-semiconductor-metal photodetectors with engineered Schottky barrier heights," *Appl. Phys. Lett.*, vol. 69, no. 23, pp. 3578–3580, Dec. 1996.

[35] D. Y. Fedyanin, D. I. Yakubovsky, R. V. Kirtaev, and V. S. Volkov, "Ultralow-loss CMOS copper plasmonic waveguides," *Nano Lett.*, vol. 16, no. 1, pp. 362–366, Dec. 2015.

[36] L. Li, J. Liu, and T. Zhu, "Study of plasmon resonance," in *IOP Conf. Series: Materials Science and Engineering*, vol. 381, no. 1. IOP Publishing, 2018, p. 012101.

[37] E. D. Palik, *Handbook of optical constants of solids*. Academic press, 1998, vol. 3.

[38] M. Casalino, M. Iodice, L. Sirleto, I. Rendina, and G. Coppola, "Asymmetric MSM sub-bandgap all-silicon photodetector with low dark current," *Opt. Express*, vol. 21, no. 23, pp. 28 072–28 082, Nov. 2013.

[39] L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "A 3.1 mw 8b 1.2 GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32 nm digital SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3049–3058, Sep. 2013.

[40] E. Testa, S. L. Noor, O. Zografos, M. Soeken, F. Catthoor, A. Naeemi, and G. Demicheli, "Multiplier architectures: challenges and opportunities with plasmonic-based logic," presented at the Design, Automation and Test in Europe (DATE) Conf., Mar. 2020.

[41] J.-M. Liu, *Photonic Devices*. Cambridge Univ. Press, 2005.

[42] L. Tang, S. E. Kocabas, S. Latif, A. K. Okyay, D.-S. Ly-Gagnon, K. C. Saraswat, and D. A. Miller, "Nanometre-scale germanium photodetector enhanced by a near-infrared dipole antenna," *Nature Photonics*, vol. 2, no. 4, pp. 226–229, 2008.