MODELING AND SIMULATION FOR SIGNAL AND POWER INTEGRITY OF ELECTRONIC PACKAGES

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MODELING AND SIMULATION FOR SIGNAL AND POWER INTEGRITY OF ELECTRONIC PACKAGES

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To my family

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格物致知 – study of things and nature to reach for knowledge

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of this dissertation is to develop electrical modeling and co-simulation methodologies for signal and power integrity of package and board applications. The dissertation includes 1) the application of the finite element method to the optimization for decoupling capacitor selection and placement on a power delivery network (PDN), 2) the development of a PDN modeling method effective for multidimensional and multilayer geometries, 3) the analysis and modeling of return path discontinuities (RPDs), and 4) the implementation of the absorbing boundary condition for PDN modeling.

The optimization technique for selection and placement of decoupling capacitors uses a genetic algorithm (GA) and the multilayer finite element method (MFEM), a PDN modeling method using FEM. The GA is customized for the decoupling problem to enhance the convergence speed of the optimization. The mathematical modifications necessary for the incorporation of the capacitor model into MFEM is also presented.

The main contribution of this dissertation is the development of a new modeling method, the multilayer triangular element method (MTEM), for power/ground planes of a PDN. MTEM creates a surface mesh on each plane-pair using dual graphs; a non-uniform triangular mesh (Delaunay triangulation) and its orthogonal counterpart (Voronoi diagram), to which electromagnetic and equivalent circuit concepts are applied. The non-uniform triangulation is especially efficient for discretizing multidimensional and irregular geometries which are common in package and board PDNs. Moreover, MTEM generates a sparse, banded, and symmetric system matrix, which enables efficient

computations. For a given plane-pair, MTEM extracts an equivalent circuit that is consistent with the physics-based planar-circuit model of a plane-pair. Thus, the values of the lumped elements can be simply calculated from the physical parameters, such as material properties and mesh geometries of each unit-cell. Consequently, the modeling of MTEM is flexible and easy to modify for further extensions, such as the incorporation of external circuits, e.g. decoupling capacitors and vertical interconnects.

Power and ground planes provide paths for the return current of signal traces. Typically, planes have discontinuities such as via holes, plane cutouts, and split planes that disturb flow of signal return currents. At the discontinuity, return currents have to detour or switch to different layers, causing signal and power integrity problems. Therefore, a separate analysis of signal interconnects will neglect the significant coupling with a PDN, and the result will not be reliable. In this dissertation, the co-simulation of the signal and power integrity is presented focusing on the modeling of RPDs created by split planes, apertures, and vias.

Plane resonance is one of the main sources of power integrity problems in package and board PDNs. A number of techniques have been developed and published in literature to reduce or prevent the resonance of a plane-pair. One of the techniques is to surround plane-pair edges with absorbing material that effectively damps the outgoing parallel-plate wave and minimizes the reflection. To model this behavior, the boundary condition of MTEM needs to be changed from its original form, the open-circuit boundary condition. In this dissertation, the application of the 1st order absorbing boundary condition to MTEM is presented.

CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

The integration of electronic devices into a single system continues as new concepts of electronic packaging are being introduced. System-in-package (SiP) and system-on-package (SoP) typify the integration of multiple system functions into a single package providing all the needed system-level functions [1]. As a number of dissimilar components are integrated to a single platform requiring diverse power supply strategies, the design of a power delivery network (PDN) becomes more challenging.

1.1.1 Challenges in Electrical Design of Package Systems

The main function of an electronic package is the distribution of signal and power to the ICs. When multiple ICs draw electrical current from power supply, current flowing through a PDN causes voltage drops and fluctuations because of resistances and inductances residing in the power rail. To reduce the path impedance, power and ground nets are designed as conductor planes.

Typical PDNs comprise a stack-up of alternating layers of power and ground planes separated by dielectric substrates. This configuration can reduce the package inductance, and also isolate different levels of supply voltages. However, planes separated by a thin dielectric create a cavity that resonates at resonance frequencies. At anti-resonance frequencies, the cavity created by a plane-pair exhibits maximum impedance. When multiple drivers simultaneously draw power at the rate of the anti-

resonance frequency, the large impedance of the PDN results in large fluctuations in the supply voltage. This unwanted noise is known as simultaneous switching noise (SSN). The large voltage fluctuations impact on the performance of a microprocessor; the insufficient supply voltage slows down, and the excessive supply voltage breaks down the microprocessor [2]. Therefore, the PDN design emphasizes on ensuring that the voltage fluctuations do not exceed the allowed threshold of a system.

Since diverse components assembled in a package demand various supply voltages, power/ground planes are split for DC isolation. Planes also contain apertures and holes for embedded components and signal interconnects. These discontinuities in a PDN provide a path for the coupling of SSN throughout the system. The coupled SSN traverses the cavity created by a plane-pair as a radial wave, and is reflected from the plane edges. The reflected wave creates multiple resonances, which result in the fluctuation of supply voltage on the power/ground planes [3] [4]. The noise in power/ground planes can couple back to signal interconnects through the path created by PDN discontinuities and deteriorate the quality of signal. Since excessive voltage fluctuations cause both signal and power integrity (SI/PI) problems, the generation of SSN needs to be carefully analyzed in the design of a semiconductor system. The SI/PI problems in a package system are conceptually described in Figure 1.1.
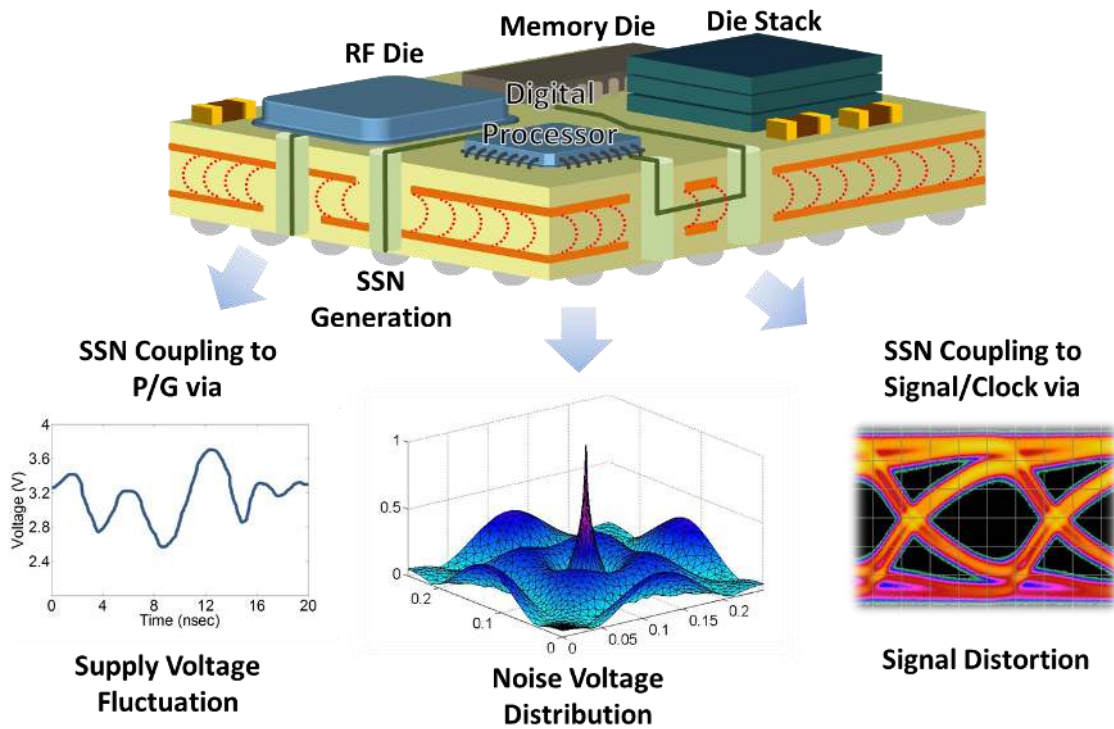
Figure 1.1. SSN generation and influences in a package. (Reproduced from [5].)

To reduce the fluctuation of the supply voltage, the path impedance where the SSN current flows needs to be minimized. Hence, the purpose of the PDN design is to ensure that the impedance seen at the IC terminals meet the target impedance across the operating frequency range. To mitigate excessive fluctuations of the supply voltage, decoupling capacitors can be placed between the power and ground pads of nearby I/O circuits. However, since the decoupling capacitors become inductive at high frequencies, placing a number of capacitors without a well-organized strategy will fail to reduce the PDN impedance. Moreover, manually selecting an appropriate amount and right values of capacitors and placing them on optimal locations are complicated and time consuming processes. This tedious task becomes even more challenging as the level of the target

3

impedance of semiconductor systems is continuously falling, led by the decrease of supply voltage and increase of system current.

1.1.2   Challenges in Electrical Modeling of Package Systems

The impedance profile of a PDN can be obtained by simulations that capture the electromagnetic behaviors of the PDN. PDNs can be simply modeled as a single-node system assuming the voltage variations occur simultaneously across the planes [**6**]. However, the simple model fails to take into account the distributed behavior of the planes at high frequencies. PDN modeling also needs to accurately capture complex geometries, such as a stack-up of multiple planes, gaps and holes in planes, and decoupling capacitors.

The computational efficiency of a PDN modeling and simulation is a critical factor that determines the efficiency of a design process. Figure 1.2 shows a flow chart of the typical design process for packages and PCBs. The process involves SI/PI simulations and analysis to ensure if the design at each step complies with the design rules and specifications. The original design is modified based on the simulation and analysis results, and this process persists until the simulation results satisfy the requirements. Hence, a time-consuming simulation can be a bottleneck that slows down the entire design process, and inevitably results in a long time-to-market cycle.
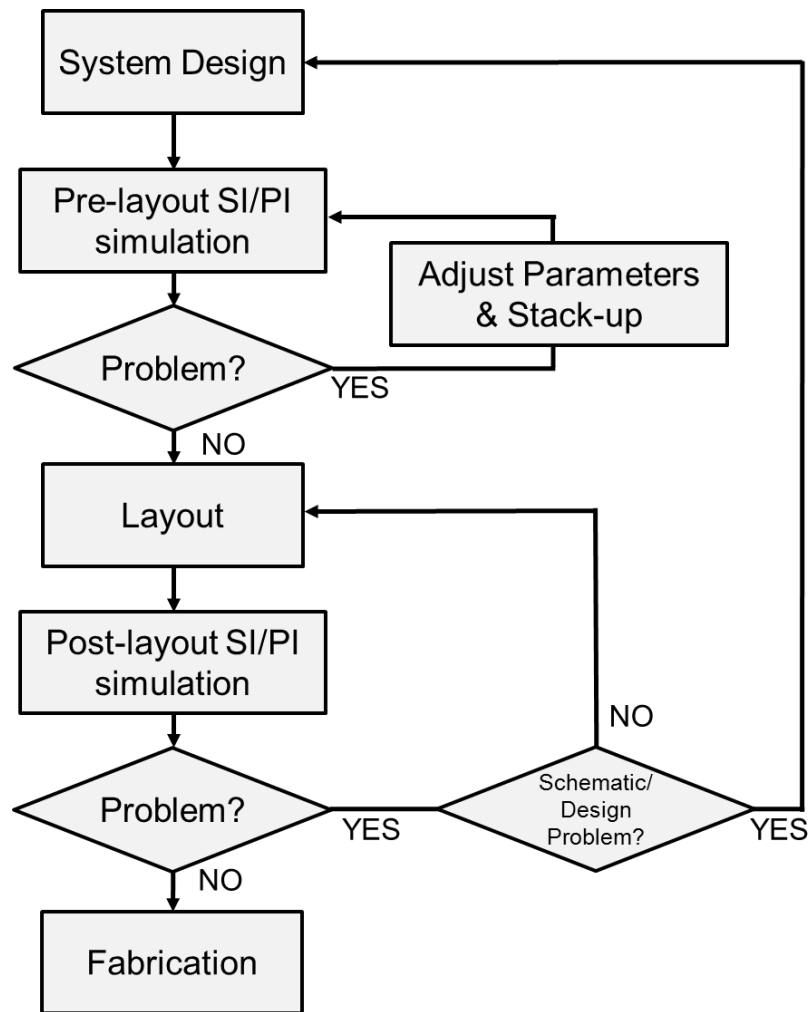
Figure 1.2. A part of the typical design process of electronic packages. (Modified from [7] and [8].)

1.2 Contributions

The major contributions of the dissertation are following:

1) Extension of the multilayer finite element method (MFEM) for the optimization of decoupling capacitor selection and placement using a customized genetic algorithm.

2) Development of a new PDN modeling method, the multilayer triangular element method (MTEM), especially effective for irregular and multidimensional structures, based on the physics-based equivalent circuit.

3) Modeling of the return path discontinuities created by apertures for a signal and power integrity co-simulation.

4) Application of the absorbing boundary condition to MTEM.

1.3 Organization of the Dissertation

The rest of this dissertation is organized as follows: In CHAPTER 2, the problems that will be addressed in this dissertation are defined, and the prior arts in literature are reviewed. In CHAPTER 3, the automation technique of finding optimal solutions of decoupling capacitor values and locations using the multilayer finite element method (MFEM) is presented. The development of a novel modeling method for a power/ground plane structure, the multilayer triangular element method (MTEM) is introduced in CHAPTER 4. In CHAPTER 5, port modeling is presented, and the modeling of return-path discontinuities for the co-simulation of signal and power integrity is provided in CHAPTER 6. In CHAPTER 7, the absorbing boundary condition is presented focusing on its implementation in MTEM. Finally, summary and conclusions of this dissertation is presented in CHAPTER 8.

CHAPTER 2

ORIGIN AND HISTORY OF THE PROBLEM

2.1 PDN Modeling Methods

Typical power delivery networks (PDNs) are composed of metal planes stacked on top of each other separated by low-loss insulators. Since each layer formed by metal planes with the low-loss dielectric can act as a cavity, the PDNs are highly resonant structures. To completely characterize such structures through time-domain analysis, a tremendous amount of time is required for a simulation. Hence, the frequency-domain analysis of package PDNs is more beneficial.

Electromagnetic field solvers that can emulate frequency responses of package PDNs can be classified as two folds: integral equation and differential equation solvers. Integral equation solvers include the method of moments (MoM) and the partial element equivalent circuit (PEEC) method. Since integral equation solvers require a discretization of only the sources of electromagnetic field, the size of the resultant linear system is small. However, the system matrix generated by integral equation solvers is dense, and the density increases according to the square of the problem size, resulting in high computational costs. On the other hand, differential equation solvers, such as the finite element method (FEM) and the finite difference method (FDM), generate a banded and sparse system, because elements are only locally connected. However, differential equation solvers that create volumetric meshes create sparse but impractically large systems for large-sized problems.

A package PDN consisting of planes separated by a dielectric is a planar structure. Since the thickness of a dielectric is electrically small, the field variation along the vertical direction of a power/ground plane-pair can be neglected. Therefore, a pair of power/ground planes can be modeled as a planar circuit [9], and several methods based on the planar circuit concept have been developed.

2.1.1 The Cavity Resonator Model Using Segmentation Method

The cavity resonator model provides an analytic solution in the form of an impedance matrix. If a rectangular plane-pair with metal planes of dimensions $a \times b$, dielectric thickness d, permittivity and permeability of ε and μ, respectively, and ports located at (x_i, y_i) and (x_j, y_j) can be calculated as

$$Z_{ij}(\omega) = j\omega\mu d \sum_{n=0}^{n=\infty} \sum_{m=0}^{m=\infty} \frac{\varepsilon_n^2 \varepsilon_m^2}{(k_{mn}^2 - k^2)ab} f(x_i, y_i, x_j, y_j), \tag{1}$$

where

$$f(x_i, y_i, x_j, y_j)$$
$$= \left(\cos\frac{m\pi x_i}{a} sinc\frac{m\pi t_{xi}}{2a}\right)\left(\cos\frac{m\pi y_i}{b} sinc\frac{m\pi t_{yi}}{2b}\right) \tag{2}$$
$$\times \left(\cos\frac{m\pi x_j}{a} sinc\frac{m\pi t_{xj}}{2a}\right)\left(\cos\frac{m\pi y_j}{b} sinc\frac{m\pi t_{yj}}{2b}\right),$$

t_{xi}, t_{xj}, t_{yi}, and t_{yj} are the size of the port, k is the complex wavenumber, and $k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2$ [10] [11].

Possible geometries that the cavity resonator model can handle are limited to simple structures, such as a square, a rectangle, or an equilateral triangle. To overcome this limit, the structure is segmented into sections that can be separately simulated by the

8

cavity model, and each segment is interconnected at corresponding virtual ports densely created (distance less than $\lambda/10$) at the segment boundaries [12] [13] [14]. However, if a given geometry is extremely irregular, the method creates too many virtual ports, consequently, the model becomes too complicated. Moreover, the double summation in Equation (1) up to a large number of modes can slow down the computation. Although acceleration techniques presented in [13] and [15] can improve the computational efficiency, the approximations associated with the techniques reduce modeling accuracy.

2.1.2 Modeling Methods Based on Discretization

Since the electromagnetic behavior of a plane-pair can be assumed to be two-dimensional (2D), the radial wave propagating in a plane-pair can be expressed with a 2D Helmholtz equation:

$$(\nabla_T^2 + k^2)u = j\omega\mu dJ_z, \tag{3}$$

where ∇_T^2 represents the transverse Laplace operator parallel to the planar structures, k the wavenumber, u the voltage, ω the angular frequency, μ the permeability of the dielectric, d the distance between the planes, and J_z the current density at the excitation port [16]. Plane boundaries are assumed to be a magnetic wall, or an open circuit, which can be described by the Neumann boundary condition.

The governing equation, Equation (3), can be solved by applying the finite difference (FDM) or the finite element methods (FEM), which will be presented in the following sections.

2.1.2.1 Transmission Matrix Method (TMM)

The transmission matrix method (TMM) [17] is a 2D modeling method that solves the equivalent circuit of a plane-pair analyzed as a planar circuit. A plane-pair is segmented into square unit-cells, which are converted to the transmission matrices. By solving the cascaded transmission matrices, TMM can solve the equivalent circuit with less computational effort than that required for a general SPICE solver. However, TMM is not applicable for multiple plane-pairs with a gap or an aperture, since the cascading property prevents the inclusion of coupling elements between neighboring cells [18].

2.1.2.2 The Finite Difference Method (FDM)

By applying the central difference method, the transverse Laplace operator in Equation (3) is approximated as

$$\nabla_T^2 u_{i,j} = \frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{h^2}, \tag{4}$$

where h is the central distance between the neighboring cells, and $u_{i,j}$ is the voltage at node (i,j). Substituting Equation (4) into Equation (3) leads to

$$\frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{-j\omega L} + j\omega C u_{i,j} = I, \tag{5}$$

where $C = \frac{\varepsilon h^2}{d}$, $L = \mu d$, and I is the current source injected into the cell. Since Equation (5) can be represented by the equivalent circuit as shown in Figure 2.1, a standard circuit solver based on the modified nodal analysis approach can be used for the computation. However, a direct solution of a matrix form, $\bar{\bar{Y}}\bar{U} = \bar{I}$, using linear equations is computationally more beneficial, because the resultant system matrix, $\bar{\bar{Y}}$, is sparse and

banded. If a nested dissection method is used, FDM can solve a system with N unknowns in $O(N^{1.5})$ time and $O(N \log_2 \sqrt{N})$ memory [19].
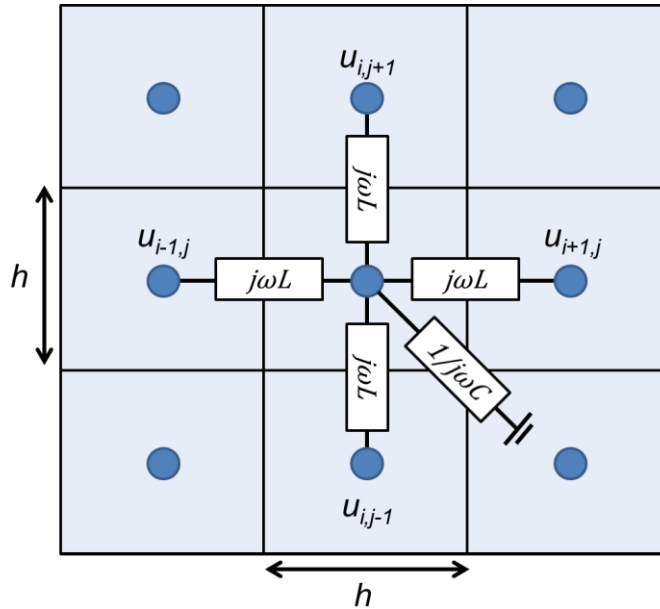
Figure 2.1. Cell-centered discretization of the Laplace operator and the equivalent circuit of FDM.

Including the computational efficiency, FDM has advantages of the ease of implementation, the capability of an equivalent circuit representation, and the application of wide range of shapes. However, this method discretizes surfaces with a square or a rectangular grid, which tend to create too many unit cells for a multidimensional structure that is common in the package PDN. Furthermore, if a structure is geometrically irregular, it is difficult to effectively discretize the structure with a square/rectangular mesh.

2.1.2.3 The Finite Element Method (FEM)

FEM is another approach that applies Equation (3) to each of the discretized segments and solve for the potential, u. For 2D problems, these segments are usually in the form of triangles or rectangles. In [**20**], FEM applied to a power/ground plane structure is presented using a non-uniform triangular mesh. The weak form of Equation (3) is expressed as

$$\sum \iint_{\Omega} \left(\nabla\phi_p \cdot \nabla\phi_q + \omega^2 \mu\varepsilon\phi_p\phi_q + j\omega\mu dJ_z\phi_p \right) dxdy = 0, \tag{6}$$

with linear pyramid basis functions, where Ω is the problem domain, and $\boldsymbol{\phi}_p$ and $\boldsymbol{\phi}_q$ are the basis and test functions, respectively. After some derivations, the solution of Equation (6) can be obtained by solving linear equations,

$$\left(\bar{\bar{K}} + \bar{\bar{M}} \right)\bar{U} = \bar{F}, \tag{7}$$

where the entries of $\bar{\bar{K}}$ and $\bar{\bar{M}}$ are

$$k_{p,q} = \frac{j}{\omega\mu d} \frac{b_p b_q + c_p c_q}{4\Delta}, \tag{8}$$

$$m_{p,q} = \begin{cases} \dfrac{\Delta}{6}\dfrac{j\omega\varepsilon}{d}, p = q \\ \dfrac{\Delta}{12}\dfrac{j\omega\varepsilon}{d}, p \neq q. \end{cases} \tag{9}$$

From the mathematical properties of Equations (8) and (9), Equation (6) can be represented by an equivalent circuit using lumped elements as shown in Figure 2.2.
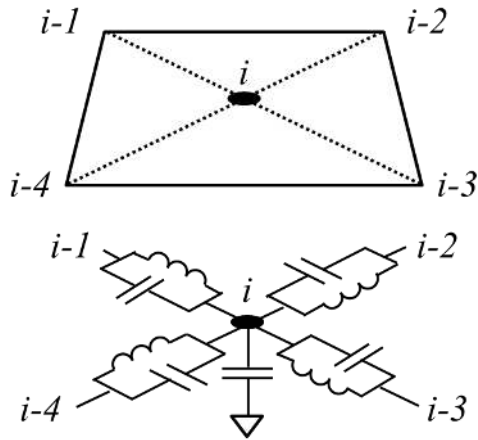
Figure 2.2. Equivalent circuit representation of a plane-pair using FEM (lower plane is not shown).

FEM can utilize a non-uniform triangular mesh scheme, which can effectively discretize multidimensional and extremely irregular geometries. In addition, FEM generates a sparse system, which promises an efficient computation. On the other hand, one of the disadvantages of FEM lies in the difficulty of implementation. Another disadvantage arises from the equivalent circuit representation for a power/ground plane-pair. The values of the lumped elements, Equations (8) and (9), are derived from not only physical properties of a simplex, but also mathematical formulations of FEM. Thus, the further extension of the model, such as the inclusion of external circuit models, is complicated and not physically intuitive.

2.1.3 Overview of Computational Electromagnetic Modeling Methods

Various electromagnetic modeling methods are available as commercial software as well as described in the literature. Each modeling method has its own strengths and weaknesses over another.

Table 1 summarizes and compares mesh and computational efficiency of various computational electromagnetic modeling methods. The selected methods include differential-equations, analytical solutions, and planar circuit methods. The comparison of the computational efficiency is based on the size and density of the system matrix.

Table 1. Comparison of computational electromagnetic modeling methods.

Category	Method	Discretization	Mesh Efficiency	Computational Efficiency
3D Full-Wave	FDM	Tetrahedron or Hexahedron	Inefficient for planar structures	Not good (sparse but large system)
	FEM			
	MoM			Not good (small but dense system)
Planar Circuit Model (Analytical Solution)	Cavity Resonator	-	-	Good for solid rectangle/triangle
	Segmentation Method	Virtual Ports	Not good for irregular geometries (creating too many virtual ports)	Not good for irregular or multi-dimensional structures
Planar Circuit Model (Numerical Solution)	TMM	Rectangle	Inefficient for irregular geometries	Good
	MFDM	Rectangle	Not good for multi-dimensional structures	Good
	MFEM	Triangle	Good	Good

2.2 Extension to Multiple Plane-Pairs

The differential equation methods, FDM and FEM, are expressed as an equivalent circuit using only passive lumped elements and independent current sources. To extend a single plain-pair to multiple plane-pairs, the equivalent circuit of each plane-pair can be stacked on top of each other. However, the simple interconnection of equivalent circuits will fail to take into account different references of each plane-pair, and the resultant model will be completely incorrect. Therefore, the reference of each plane-pair must be shifted to a global reference of multiple plane-pairs, and the shift of a reference can be realized using indefinite admittance matrices [21].

The multilayer finite difference method (MFDM) [22] and the multilayer finite element method (MFEM) [20] utilize the technique of the indefinite admittance matrix to extend a single plane-pair to multiple plane-pairs. This approach, shifting reference nodes, can be applied to any modeling scheme that can be expressed as an equivalent circuit composed of only passive elements and independent sources.

Consider the unit cell model shown in Figure 2.3 (a), which can be decomposed into two plane-pairs as shown in Figure 2.3 (b). The inductance and capacitance models are shown in Figure 2.3 (b) and (c). L_{12} and L_{34} are per unit cell inductances for each plane-pair that can be obtained from Equation (34). Assuming the plane 3 is the system reference, the indefinite admittance matrices for the top and bottom plane-pairs can be derived as follows:

$$
\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_1 & -Y_1 & -Y_1 & Y_1 \\ -Y_1 & Y_1 & Y_1 & -Y_1 \\ -Y_1 & Y_1 & Y_1 & -Y_1 \\ Y_1 & -Y_1 & -Y_1 & Y_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix},
\tag{10}
$$

16

$$\begin{bmatrix} I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_2 & -Y_2 \\ -Y_2 & Y_2 \end{bmatrix} \begin{bmatrix} V_3 \\ V_4 \end{bmatrix},$$ (11)

where $Y_1 = \dfrac{1}{j\omega L_{12}}$ and $Y_2 = \dfrac{1}{j\omega L_{34}}$. Similarly, an admittance matrix for capacitance between planes is obtained as follows:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_{C1} & 0 & -Y_{C1} & 0 \\ 0 & Y_{C1} & 0 & -Y_{C1} \\ -Y_{C1} & 0 & Y_{C1} + Y_{C2} & 0 \\ 0 & -Y_{C1} & 0 & Y_{C1} + Y_{C2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix},$$ (12)

where $Y_{C1} = j\omega C_1$ and $Y_{C2} = j\omega C_2$. Loss terms are omitted in both models for simplification. Finally, superimposing all the indefinite admittance matrices, Equations (10), (11), and (12), completes the total admittance matrix for the given three-layered structure:

$$\begin{bmatrix} Y_{C1} + Y_1 & -Y_1 & -Y_{C1} - Y_1 & Y_1 \\ -Y_1 & Y_{C1} + Y_1 & Y_1 & -Y_{C1} - Y_1 \\ -Y_{C1} - Y_1 & Y_1 & Y_{C1} + Y_{C2} + Y_1 + Y_2 & -Y_1 - Y_2 \\ Y_1 & -Y_{C1} - Y_1 & -Y_1 - Y_2 & Y_{C1} + Y_{C2} + Y_1 + Y_2 \end{bmatrix}.$$ (13)
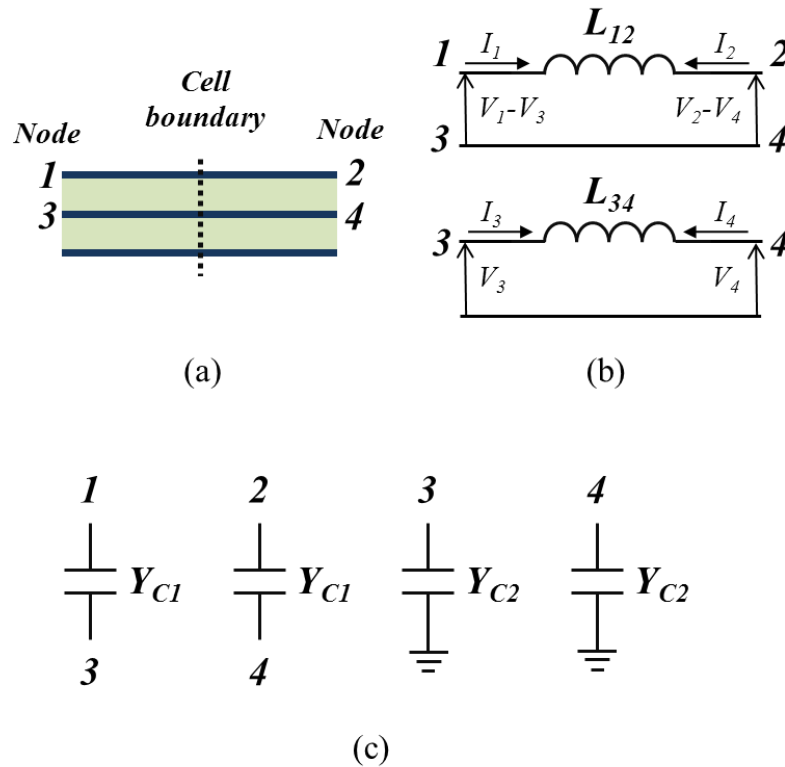
Figure 2.3. (a) Cross-section of a three-layer structure. The equivalent (b) inductance and (c) capacitance model.

2.3 Incorporation of Signal Interconnects into the PDN

In a package and printed circuit board (PCB), the signal interconnects, such as copper traces and vias, link drivers and receiver circuits placed on the PDN. Metal planes in the PDN provide the paths for the return current of the signal interconnects. Power and ground planes typically contain many discontinuities such as plane cut-outs, split planes, and via anti-pads as shown in Figure 2.4 (a). On those metal planes with discontinuities, signal traces are placed as shown in Figure 2.4 (b). If a current-return path of a signal transmission line is discontinuous, the field distribution changes at the discontinuity and mode conversion occurs, which results in the distortion of the signal. Moreover, the mode

conversion can excite the cavity created by the power and ground planes and leads to a

plane resonance, causing fluctuation of supply voltage. A discontinuity of this type along

a signal interconnect is called as return path discontinuity (RPD).

(a)   (b)
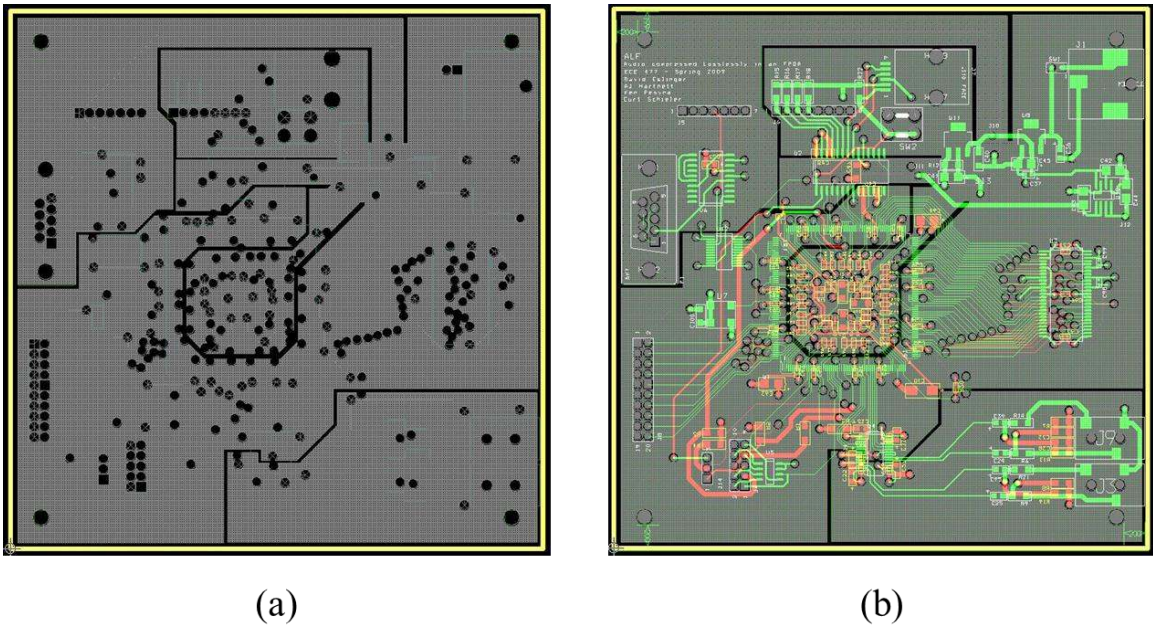
**Figure 2.4. Layout of (a) power and ground planes and (b) signal interconnects. (Courtesy
of class notes for Purdue University ECE477, Spring 2009.)**

The electrical behavior at the RPDs can be explained using an example, a

microstrip line placed above a slotted power plane as shown in Figure 2.5 (a). At the

discontinuity, return current switches layer from power to ground plane and vice versa to

complete the closed current loop. Current jumps from one layer to another as

displacement current that is caused by the stray capacitance between the layers. Hence,

the propagation mode of the microstrip line at the discontinuity changes from its original

form to another, leading to the change of characteristic impedance and effective dielectric

constant. In addition, the displacement current excites the plane-pair created by power

and ground planes, and may result in a plane resonance that causes the fluctuation of supply power. The plane resonance can also deteriorate the signal transmission, since the high impedance of the PDN at anti-resonant frequencies impedes the flow of return current. A similar effect is observed at the RPD created by a via anti-pad (clearance hole) as shown in Figure 2.5 (b). Therefore, in a package or PCB system, the electrical behaviors of the PDN and the signal interconnects are closely coupled, and their interactions must be included in simulations.
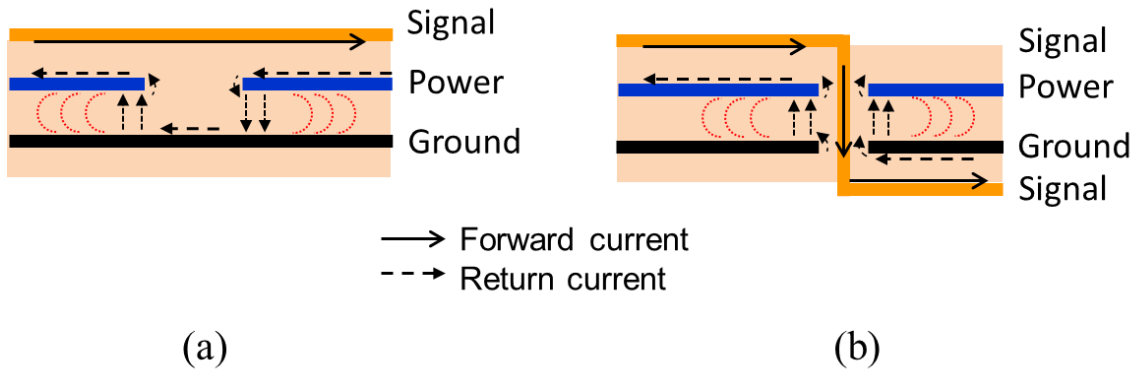
Figure 2.5. Current loops created at the return path discontinuities created by (a) slot and (b) via transition.

One of the methods to co-simulate the PDN and the signal interconnects is to model each domain separately and re-integrate using a modal decomposition technique, which was exploited in many articles or publications [4] [5] [23] [24] [25]. The PDN can be modeled using any analysis method that can provide the impedance profile of a given PDN, and the signal interconnects can be characterized by transmission line parameters, such as characteristic impedance, effective dielectric constant, and the electrical length.

20

The decoupled models are re-integrated by superimposing the admittance matrices of each model.

The co-simulation of a PDN and signal interconnects requires the accurate modeling of an RPD where mode conversions occur. Thus, to model an RPD, the thorough understanding and the analysis of the electromagnetic behaviors at the discontinuities need to precede.

A number of papers that describe and analyze RPDs have been published in recent decades. A microstrip line over a thin slot is analyzed in [26], and the impact of the plane gap RPD is shown in [27]. In [28], the difference between slot-induced and an aperture-induced RPDs is studied, and in [29], the coupling of ground bouncing through an aperture is investigated in time-domain modeling and simulations. The impact of a slot on the differential signaling and the coupling between the signal and the power plane are presented in [30]. Although the previous papers show analysis and modeling of RPDs, thorough analysis on the physics behind the different types and sizes of RPDs in the presence of the PDN is lacking in the literature.

The RPD can also be created by a through-hole via which is widely used for vertical interconnections in package and board systems. The modeling of a via structure and the coupling between a via and a plane has been vigorously investigated and published [31] [32] [33] [34] [35] [36]. Any physical modeling method for a via can be incorporated into the modal decomposition technique for the modeling of the RPD of a via structure in consideration of the via-plate coupling.

2.4 Selection and Placement of Decoupling Capacitors

The main purpose of a PDN is to deliver electric current to the switching circuits from the voltage regulator module. Thus, maintaining low impedance for a PDN is necessary for a stable supply of desired voltage. The required impedance of a PDN is called the target impedance, which is calculated as [6]

$$Z_{tar} = \frac{Supply\ Voltage \times Allowed\ Ripple}{Current}. \tag{14}$$

A practical choice of the allowed ripple is usually 5% of the supply voltage (V_{dd}), and the current (an average current drawn by the switching circuit) is assumed to be the half of the maximum current.

The conventional method to meet the target impedance is to place decoupling capacitors between power and ground nets of a PDN. However, since a decoupling capacitor behaves like an inductor at the frequencies above its self-resonance frequency, the accumulated behavior of decoupling capacitors eventually increases the PDN impedance at high frequencies. Moreover, the decoupling capacitor technique becomes ever challenging as the required target impedance continues to decrease as shown in Table 2. Therefore, selection and placement of hundreds and thousands of decoupling capacitors to meet the challenging target impedance across the wide-range of frequencies is a time consuming and cumbersome task.

Table 2. Target impedance trend [37].

Year	Feature Size (nm)	Power (W)	V_{dd} (V)	Current (A)	Target Impedance (mΩ)
2009	52	143	0.95	151	0.63
2011	36	161	0.72	224	0.32
2013	28	149	0.67	222	0.30
2015	23	143	0.63	227	0.28
2018	16	136	0.57	239	0.24

Searching for the locations and values of decoupling capacitors can be automated by applying an optimization algorithm. The process of finding optimal locations and values for decoupling capacitors that satisfy target impedance is a multi-dimensional combinatorial problem, since the solution is not unique. In addition, since candidate solutions are mutually independent, finding a solution through exhaustive search (generate and test) is infeasible. Therefore, finding optimal solutions for decoupling capacitor locations and values is a combinatorial optimization, which can be solved by metaheuristics such as simulated annealing [**38**], genetic algorithm [**39**], and swarm intelligence [**40**]. Among many metaheuristics, the genetic algorithm (GA) is an effective technique that finds a quality solution from a very large number of possible solutions [**41**]. Unlike other methods, GA can operate in parallel, and can search for an optimal solution using only small number of candidate solutions as explained in Holland's schema theorem [**39**].

A flow chart of the typical GA process is shown in Figure 2.6 [**42**], and MFDM is used to obtain the PDN impedance profile. As explained in Section 2.1.2.1, the FDM is not optimal for complex and multidimensional geometries, which prevail in modern

packages. In [**15**] and [**43**], the authors employ a cavity resonator model in combination of the GA. The cavity resonator model in the paper does not handle multiple plane-pairs, and is limited to simple rectangular planes. In addition, optimization algorithms in [**15**], [**42**], and [**43**] use the general GA that is not customized for the decoupling capacitor problem. Thus, if the GA is combined with the decoupling capacitor placement techniques, which are presented in [**5**] [**44**] [**45**] [**46**] [**47**] and [**48**], further improvement of the convergence speed can be achieved.
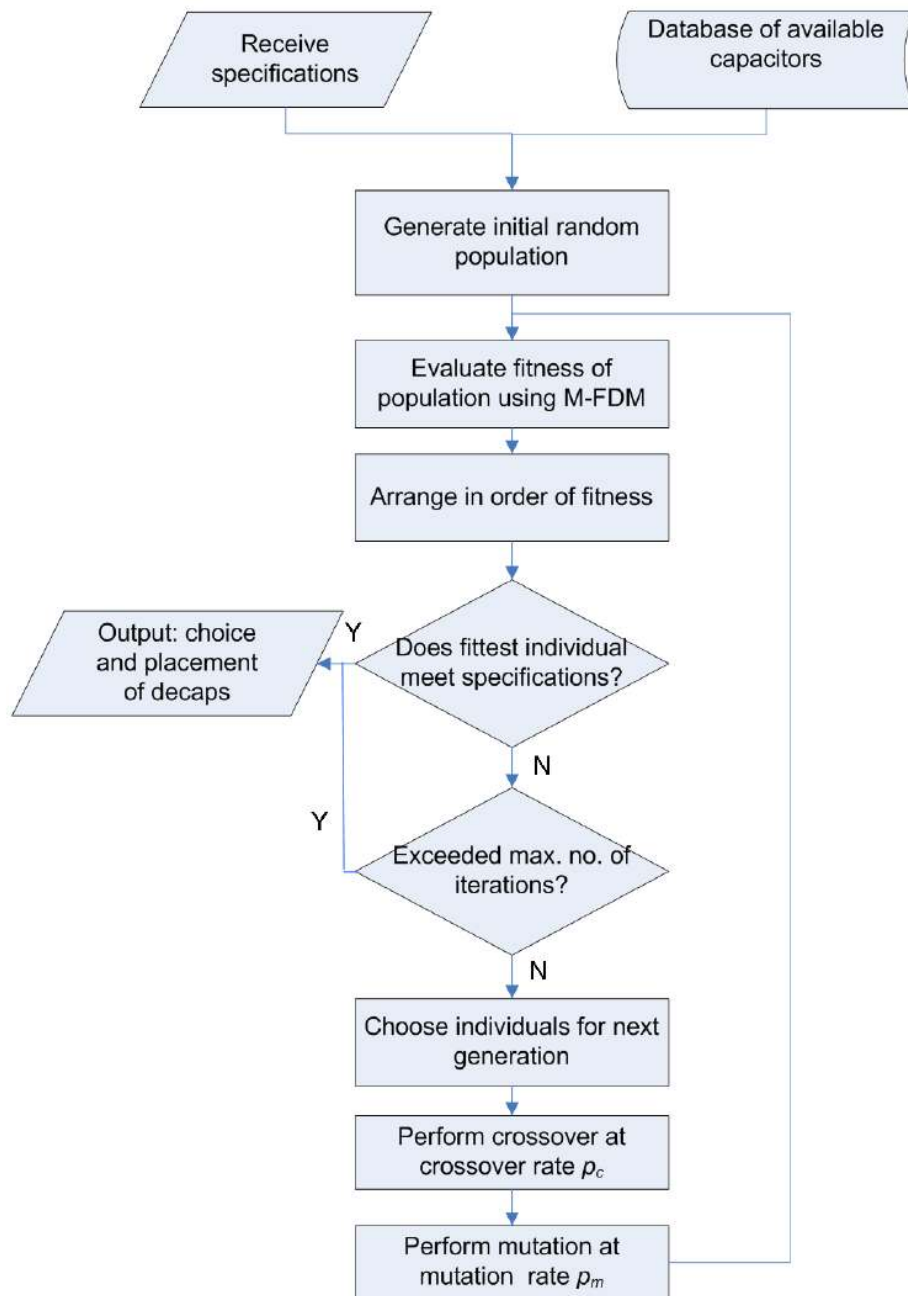
Figure 2.6. A flow chart of the typical optimization procedures of decoupling capacitor selection and placement using the GA [42].

CHAPTER 3

OPTIMIZATION OF DECOUPLING CAPACITOR SELECTION AND PLACEMENT USING MFEM

3.1 Introduction

This chapter presents the extension of the plane-pair modeling method, the multilayer finite element method (MFEM) [20], to include external circuit elements into the plane-pair model. The inclusion of the external circuit element enables MFEM to be applied to the automation of decoupling capacitor selection and placement. The automation employs a selected optimization engine, the genetic algorithm (GA), which is further customized for the decoupling problem to enhance the performance.

3.2 Extension of MFEM

Since the equivalent circuit of MFEM is extracted from mathematical formulations, the circuit model does not directly interpret the physical properties of the PDN. Thus, the incorporation of external circuits into MFEM requires modifications of the external circuit model. This section describes the incorporation method of the decoupling capacitor model into MFEM.

3.2.1 Formulation of Capacitive Elements in MFEM

A standard finite-element approximation with a triangular mesh and linear pyramid basis functions is given in Equation (6), and its matrix form is Equation (7). The admittance matrix, $\bar{\bar{M}}$, represents capacitive components, and its entries are

$$m_{p,q} = \iint_{\Omega} \frac{j\omega\varepsilon}{d} \phi_p \phi_q \, dx \, dy. \tag{15}$$

For simplicity, the Cartesian coordinates are converted to simplex coordinates {*L1, L2, L3*} [49] to obtain

$$L_p = \frac{1}{2\Delta}(a_p + b_p x + c_p y), \tag{16}$$

$$a_p = x_{p+1}y_{p+2} - x_{p+2}y_{p+1}, \tag{17}$$

$$b_p = y_{p+1} - y_{p-1}, \tag{18}$$

$$c_p = x_{p-1} - x_{p+1}, \tag{19}$$

where Δ is the area of the triangle with vertices at *p-1*, *p*, and *p+1*, and the subscripts are evaluated (modulo *3*) + *1*, which circulate at multiples of three. Notice that the integrals in Equation (15) are in the form of

$$I = \iint_{\Omega} L_1^a L_2^b L_3^c \, dL_1 \, dL_2 = \frac{a! \, b! \, c!}{(a + b + c + 2)!}, \tag{20}$$

where *a*, *b*, and *c* are integer powers [49]. Therefore, the substitutions of *a=2*, *b=0*, and *c=0* when *i=j*, and *a=1*, *b=1*, and *c=0* when *i≠j* in Equation (20), and the use of Equations (16) - (19) and the Jacobian,

$$dxdy = dL_1 dL_2 \frac{\partial(x,y)}{\partial(L_1, L_2)} = 2\Delta dL_1 L_2, \tag{21}$$

transform Equation (15) to simplex coordinates as follows:

$$m_{p,q} = \begin{cases} \dfrac{\Delta}{6}\dfrac{j\omega\varepsilon}{d}, p = q \\ \dfrac{\Delta}{12}\dfrac{j\omega\varepsilon}{d}, p \neq q. \end{cases} \tag{22}$$

3.2.2 Inclusion of the Decoupling Capacitor Model to MFEM

To comprehend the way to connect the decoupling capacitor model to the plane-pair model of MFEM, one must understand how vertical components of a plane-pair are represented in the system matrix. As shown in Equation (22), the value of the vertical component is decomposed into two different values for matrix representation: 1/6 and 1/12 of the original value. The reason for decomposition into the particular fractions stems from the nature of simplex coordinates (Equations (16)-(21)). Similarly, if a vertical circuit element is to be added to the system, its admittance must be decomposed into two different values as in Equation (22). Then, each value is added to the appropriate locations in the system matrix. For instance, the admittance of a decoupling capacitor can be represented as

$$Y_{decap} = \cfrac{1}{\left(\cfrac{1}{j\omega C_{decap}} + j\omega ESL + ESR\right)},\tag{23}$$

where C_{decap} is capacitance, *ESL* is equivalent series inductance, and *ESR* is equivalent series resistance of the decoupling capacitor. Next, the admittance is decomposed into 1/6 and 1/12 of the original value:

$$m_{p,q}^{decap} = \begin{cases} \dfrac{1}{6}Y_{decap}, & p = q \\ \dfrac{1}{12}Y_{decap}, & p \neq q \end{cases},\tag{24}$$

where *p* and *q* are the vertices of a selected unit triangle of a mesh. Finally, the 1/6 of the admittance is added to the diagonal locations, and the 1/12 to the off-diagonal locations of the system matrix.

3.3 Test Cases and Results

To verify the incorporation of the decoupling capacitor model into MFEM, a test vehicle, which has two metal plane layers with five ports, is created. The dielectric material is FR-4, with a relative permittivity of 4.5, a loss tangent of 0.025, and a thickness of 355 μm. The actual test vehicle and the top view of the structure with its dimensions are shown in Figure 3.1.
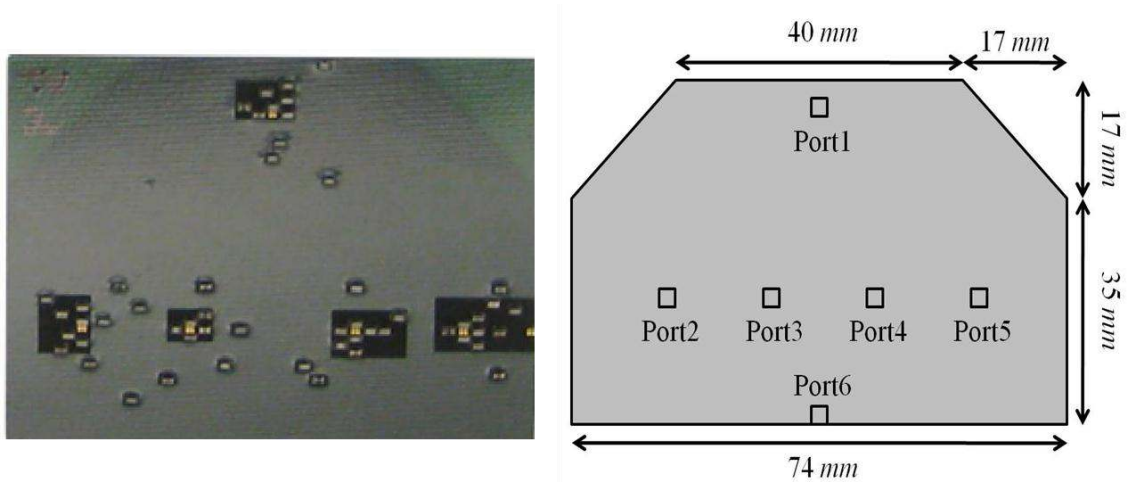
Figure 3.1. Top view of the test vehicle with decoupling capacitors (left) and the dimensions and the port locations (right). (Test vehicle provided by Sony Corp., Tokyo, Japan)

Before examining the results with decoupling capacitors, software simulations were performed for the bare planes without capacitors. Figure 3.2 shows the self-impedance results at port 1 and 2. With MFDM and Sonnet software [50] as references, the results from the three simulations show good correlations.
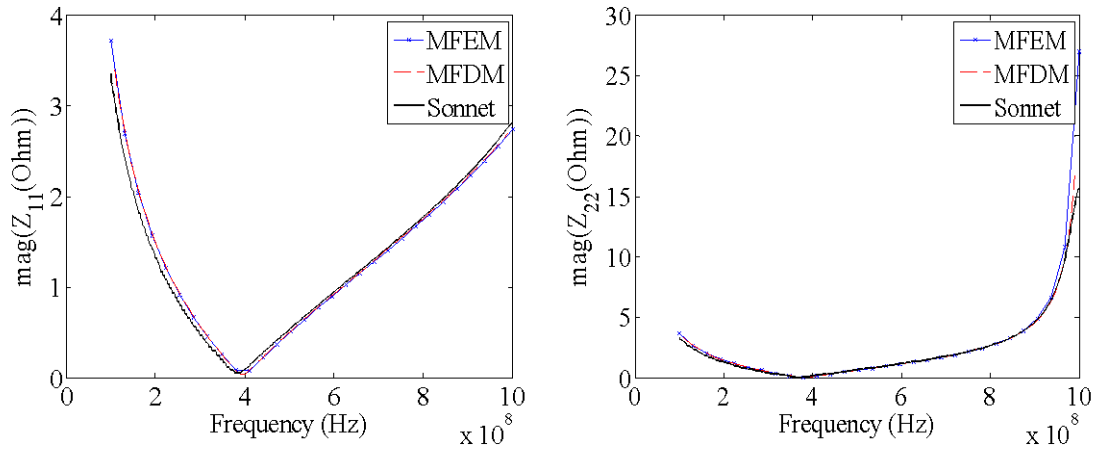
Figure 3.2. Self-impedance responses at port 1 and 2 of the test vehicle without decoupling capacitors.

Next, decoupling capacitors were placed on the bare planes to reduce the self-impedances at the ports, and the target impedance was set at 1.5 Ω at all the ports over the frequency range of 100 MHz to 1 GHz. The GA optimizer randomly selected 55 capacitors from a given library that had twenty different capacitors with their ESL and ESR values, and placed them on the defined regions on the planes. The capacitance values ranged from 680 nF to 33 pF, and ESL and ESR ranged from 0.1 nH to 0.82 nH and from 0.04 Ω to 3 Ω, respectively. The inductance of the vias used for decoupling capacitor connection was 0.3 nH, which was calculated by a 3-D inductance extraction tool [**51**]. Hence, the effective series resonance frequencies of the used capacitors were calculated to be from 20 MHz to 1 GHz.

The measured self-impedance curves at ports 1 and 2 are depicted in Figure 3.3 along with results from MFDM and MFEM simulations. Figure 3.4 compares the generated meshes for MFDM and MFEM for the test vehicle with decoupling capacitors. To capture small dimensions of the decoupling capacitors, MFDM had to create

numerous square unit-cells all over the plane, while MFEM effectively discretized the multi-scale structures using non-uniform triangles. As a result, MFEM resulted in far fewer unknowns (around 3,300) than MFDM (around 8,000). The resonance and anti-resonance frequencies match, and the level of impedances are in good correlation over the frequency range of interest.
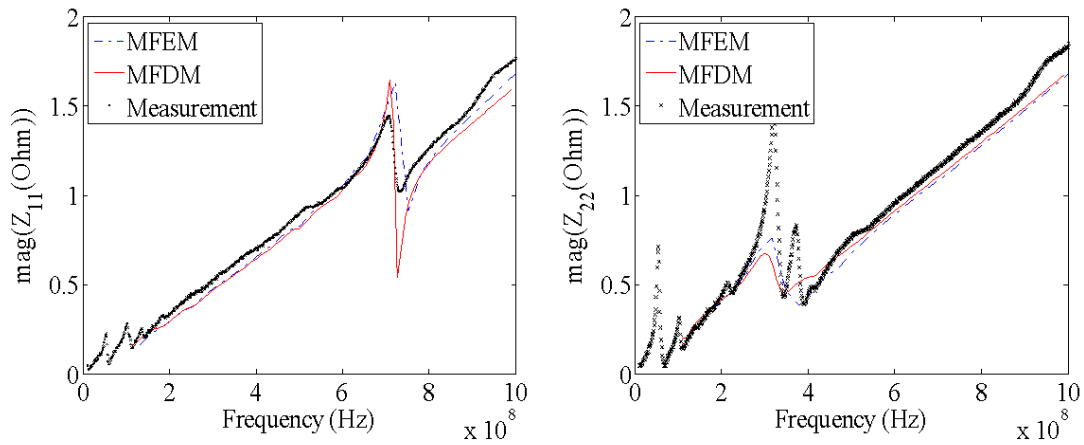
Figure 3.3. Self-impedance responses at port 1 and 2 of the test vehicle with decoupling capacitors.
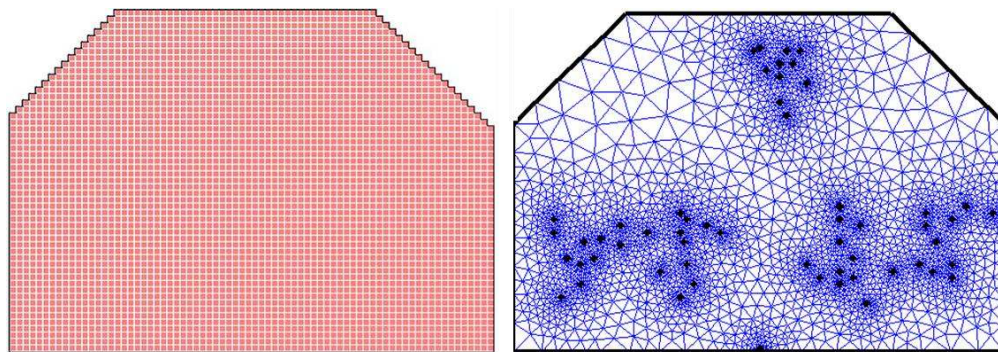
Figure 3.4. Comparison of mesh generations of MFDM (left) and MFEM (right) for the test vehicle with decoupling capacitors.

Some deviation in measurements, especially the anti-resonance peaks at port 2, resulted from the relatively large probe inductance compared to the PDN impedance. Thus, the transfer-impedance can provide a much more accurate result than the self-impedance, especially for a PDN with moderate impedance [5]. However, in this paper only one-port measurements were conducted due to limited probe accessibility. The impedance exceeded the target impedance (at 1.5 Ω) at high frequencies because some decoupling capacitors located too close to the ports were removed for measurement probe access. Since the corresponding capacitors were also removed from MFEM, the model and the hardware are based on the same structure. Therefore, the provided measurement and simulation results validate the accuracy of the model incorporating decoupling capacitors into MFEM.

3.4 The Decoupling Optimization Using Genetic Algorithm (GA)

Manually selecting and placing hundreds to thousands of decoupling capacitors on a PDN to meet the target impedance require a considerable amount of time and effort. Such a complex task can be automated using an algorithm that eventually provides an optimized solution. A GA is suitable for the optimization of the decoupling capacitor selection and placement, since the GA is robust and effective in solving complex, combinational, and related problems [41].

A GA is based on the concepts of natural selection and evolution [39]; it exploits the ideas from evolutionary biology such as population, crossover, selection, mutation, and substitution. Thus, for the decoupling capacitor optimization, the data of the decoupling capacitor locations and their types (e.g., capacitance, ESL, ESR) are

analogous to genes on a chromosome. Each chromosome can contain the following information: capacitor indices, x- and y-locations, layer connectivity, cost, and physical size of the capacitor. These values are randomly generated at the beginning of the optimization for the determined number of chromosomes (population).

Once the chromosomes are initially generated, the core engine is run to produce impedance profiles including the decoupling capacitor data acquired from each chromosome. Once the impedance profiles are obtained, each result is subjected to a quality evaluation using a fitness function that quantifies the optimality of a solution to the target. Thus, it is critical that the fitness function be closely related to the solution and be computed quickly. The goal for the optimization is to minimize the difference between the acquired impedance and the target impedance at a port:

$$F(\bar{x}) = |Z(\bar{x})| - Z_{tar}, \tag{25}$$

where $Z(\bar{x})$ is the obtained impedance with variables $\bar{x}$, which may contain values, locations, and cost for each decoupling capacitor, and Z_{tar} is the target impedance (Equation (14)). Although the lower the PDN impedance the better, overachievement will cost unnecessary decoupling capacitors. Therefore, by accounting for the optimal achievement of the target impedance, the fitness function in Equation (25) can be defined for the number of ports and frequencies as follows:

$$fitness = \sum_{i=1}^{Nport} \left(\sum_{k=1}^{Nfreq} \left(\begin{matrix} \left(Z_{tar,i} - Z_{i,i}(\bar{x},k)\right) \sum \left(Z_{tar,i} > Z_{i,i}(\bar{x},k)\right) - \\ \left(Z_{i,i}(\bar{x},k) - Z_{tar,i}\right) \sum \left(Z_{tar,i} < Z_{i,i}(\bar{x},k)\right) \end{matrix} \right) \right), \tag{26}$$

where $Z_{tar,i}$ represents the target impedance at i^{th} port, and $Z_{i,i}(k)$ is the self-impedance of ith port at frequency k.

At the end of processes for each generation, each chromosome is ranked according to the value of the fitness function. At this stage, if some chromosomes meet all the target impedance criteria at all the frequency points, the optimization process will be terminated and return the qualified chromosomes. Otherwise, the optimization process will proceed to the next step, breeding, which consists of crossover, mutation, and substitution. For the next generation, best chromosomes (chromosomes with best fitness results) are selected as parent chromosomes (elites) for next generation, and are interleaved to create child chromosomes. Child chromosomes are created by the reproduction of parent chromosomes that change random genes each other (crossover) and change the value of some genes to a random value (mutation). This step is equivalent to changing the location and values of decoupling capacitors for selected sets that resulted in the best fitness results in the previous step. The generated parent and child chromosomes substitute the existing chromosomes to proceed to the next generation. Again, they are subject to fitness evaluations, and if some of the chromosomes meet the target impedance requirement, the optimization iteration will be terminated and return the qualified chromosomes; otherwise, another generation will be created and evaluated. The procedure of GA using MFEM is described in Figure 3.5.

```
Input: decoupling capacitor library, PDN geometry, target impedance, initial
population

generation ← initial population

    repeat
        PDN_impedance ← MFEM(generation)
        elites ← FITNESS_FUNCTION(chromosomes, target impedance)
        children ← REPRODUCTION(elites)
        generation ← elites, children
    until PDN_impedance < target impedance

Output: the qualified chromosomes in a generation
```

Figure 3.5. Pseudocode representation of the decoupling capacitor optimization problem using GA and MFEM.

3.5 GA Customized for the Decoupling Capacitor Problem

For more efficient optimization, especially for decoupling capacitor placement, a special strategy can be imposed on the locations of the capacitors. The closer the capacitors are to the noise port, the lower the impedance viewed from the port. The reason is that the decoupling capacitor closely placed to the noise port produces reduced spreading inductance between the port and itself and is adequately explained in [**5**], [**44**], [**45**], [**46**], [**47**], and [**48**]. This strategy, which can maximize the effectiveness of decoupling, can be applied to the GA optimizer to place capacitors only in the close proximity of the ports. In addition, the layer connectivity of the decoupling capacitors follows that of the nearby ports to minimize the loop inductance. These scenarios are described in Figure 3.6. When a regional limit on decoupling capacitor placement is applied, the area of the region has to be carefully determined. Since a certain amount of physical space is

required for the placement of capacitors, even if they are in the forms of a surface mounted device (SMD) or an embedded passive, the area in the model cannot be unrealistically small. On the other hand, if the area is defined as electrically too large, the strategy for applying the regional limit becomes no longer effective. Therefore, choosing the general vicinity of the active device and maintaining a minimal region is essential. The overall flow of customized GA for decoupling capacitor selection and placement is depicted in Figure 3.7.
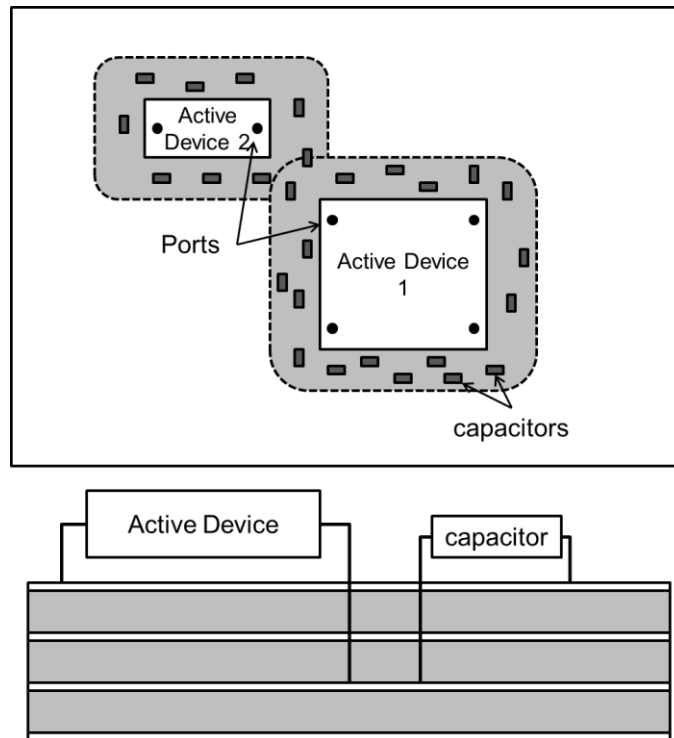
Figure 3.6. Scenarios of decoupling capacitor placement. Capacitors are only placed within the shaded region (top). Connectivity of the capacitors follows that of the nearest active device to reduce the spreading inductance (bottom).
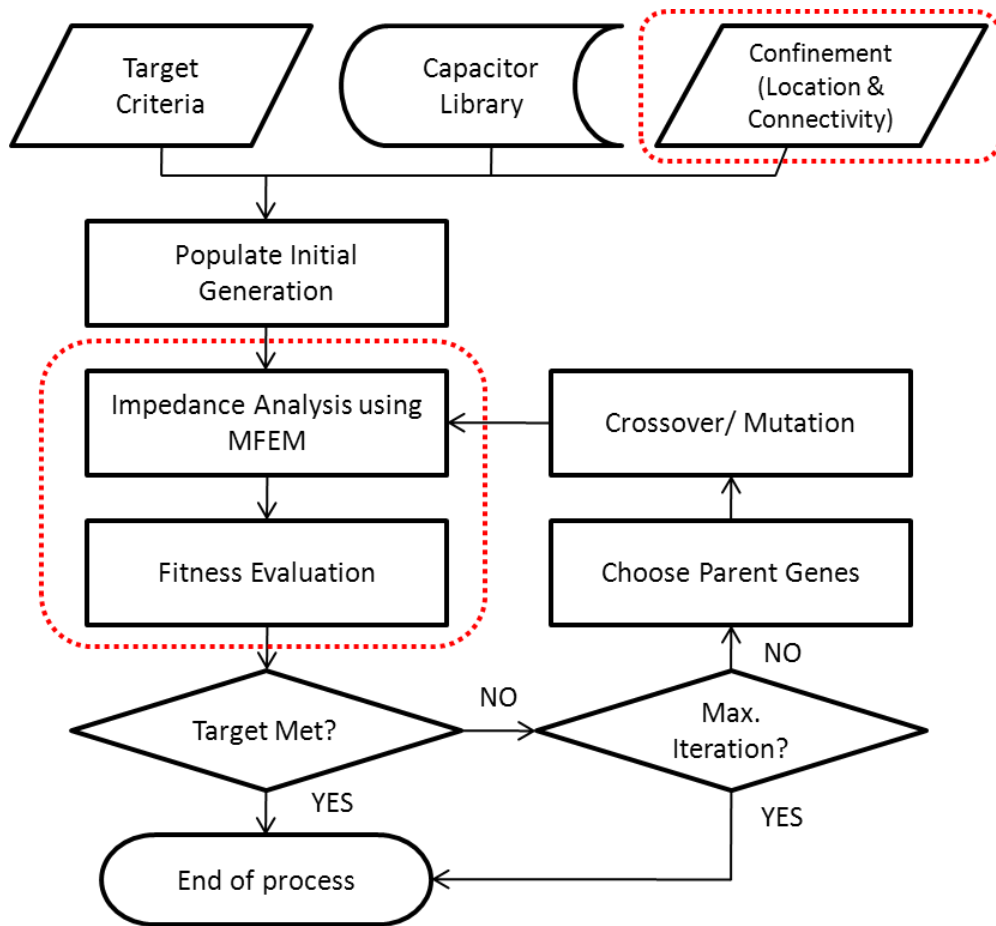
Figure 3.7. A flow chart of the optimization process of selection and placement of decoupling capacitors using the customized GA and MFEM. The components in the dotted-boxes represent the new features added or replaced from the typical GA.

3.6 Test Cases and Results

3.6.1 Test Case 1

An example of a multilayer structure was designed to apply the GA optimizer adapted to decoupling capacitor placement. As shown in Figure 3.8, the structure consists of three layers with slots on the second layer, two ports between the first plane-pair and the second plane-pair. The metal planes are 100-mm long, 75-mm wide, and 30-μm thick. The dielectric is 200-μm thick with a relative permittivity of 4.5 and loss tangent of 0.02.

37
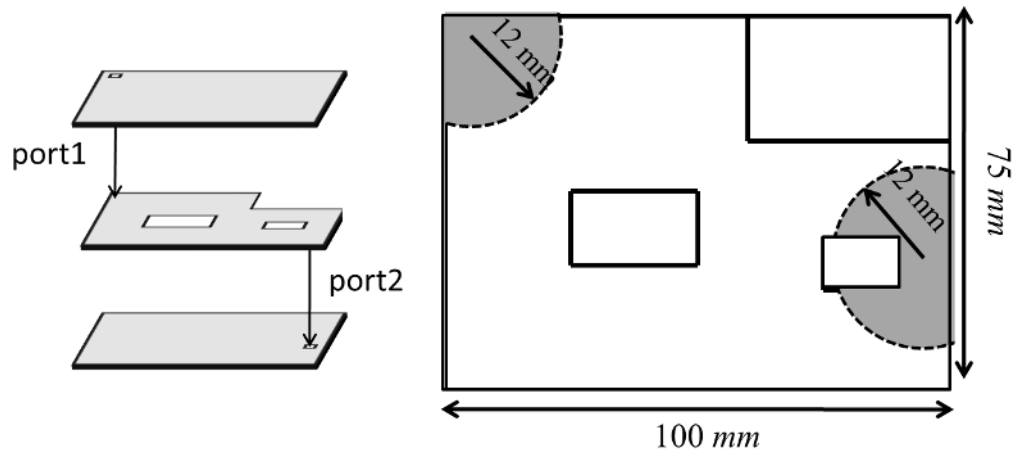
Figure 3.8. Perspective view of an example structure (left). Top view shows the superposition of the feature outlines in each layer and the confined region (gray area) for capacitor placement (right).

The first optimization used an unconstrained GA, and the second used the customized GA optimizer applying the additional regional limit on the locations for capacitors. In the customized optimizer, the regional limit was set at a radial distance of 12.5 mm, which corresponds to 1/12 of the wavelength at 1 GHz, from nearby ports as shown in Figure 3.8. In addition, the connectivity of the capacitors was assigned to follow the connectivity of nearby ports to minimize the loop inductance.

Both optimizers were set to achieve the target impedance of 1 Ω and designed to run until either the target was met or the maximum number of iterations was reached. The number of decoupling capacitors, whose self-resonant frequencies exist between 100 MHz and 1 GHz, was 10. ESL and ESR were equally assigned to all the capacitors with values of 0.4 nH and 0.2 mΩ, respectively. For a fair comparison, both optimizers

applied the equal optimization preferences, such as the number of populations, rates of crossover and mutation, and the fitness function.

The customized GA accomplished the goal in 12 iterations, and the resulting impedance results are shown in Figure 3.9. However, the GA without a regional limit failed to obtain the target impedance within the maximum number of iterations, set at 150. The progress of the fitness evaluations from both optimizations is shown in Figure 3.10, in which the progress of the customized GA shows quick achievement of the optimization target. Notice that although the ordinary GA optimizer went through many iteration steps to reach the same level of fitness as that of the customized GA, its progress shows continuous increments. Furthermore, as the optimization proceeds the decoupling capacitors are being more and more closely placed to the ports, and the pattern of the placement at the later step corresponds to that of the customized GA, as shown in Figure 3.11. As a conclusion, implementing the regional limit technique to the placement of decoupling capacitors can save a large amount of optimization time.
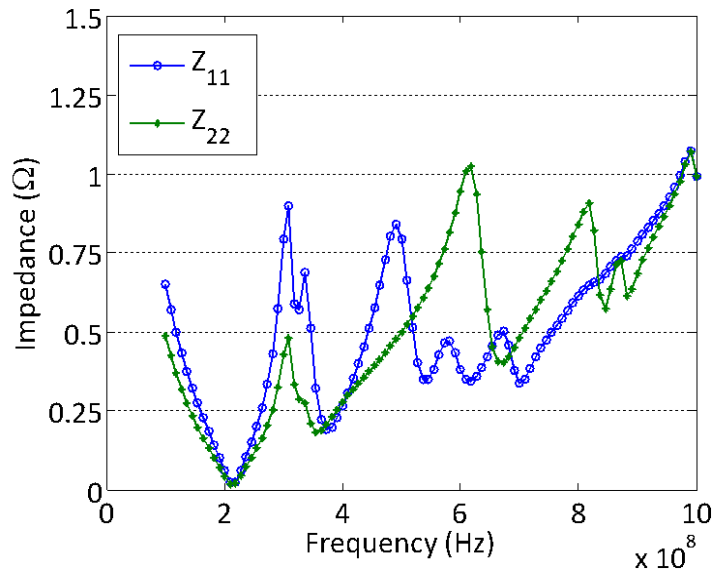
Figure 3.9. Self-impedance responses of port 1 and 2 of the test case 1 after the optimization using the customized GA.
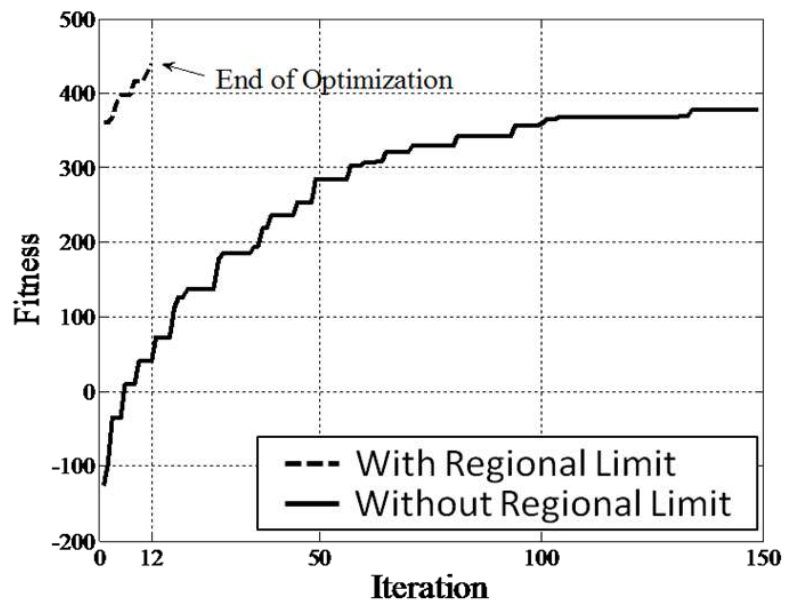
Figure 3.10. Comparison of the convergence between the customized GA and the typical GA using the fitness values.
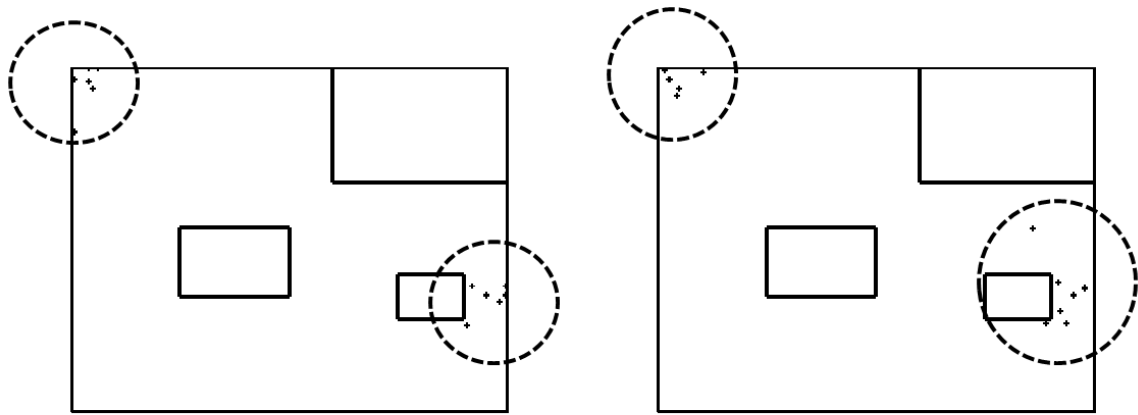
Figure 3.11. Comparison of final placement of capacitors using the customized GA (left) and the typical GA (right).

3.6.2   Test Case 2

The customized GA was applied to the bare board of the test vehicle presented in Section 3.3.   As before, the target self-impedance was set at 1.5 Ω for each port, the same capacitor library was used with a via inductance of 0.3 nH.   The regional limit for capacitor placements was set at a 10-mm radial distance from nearby ports.

The optimizer achieved the goal with only three iterations, and the resulting impedance response is shown in Figure 3.12.   Since randomness could have accounted for the quick results, several additional simulations were performed with the same settings.   However, the optimizer was still able to reach the target at most within five iterations.
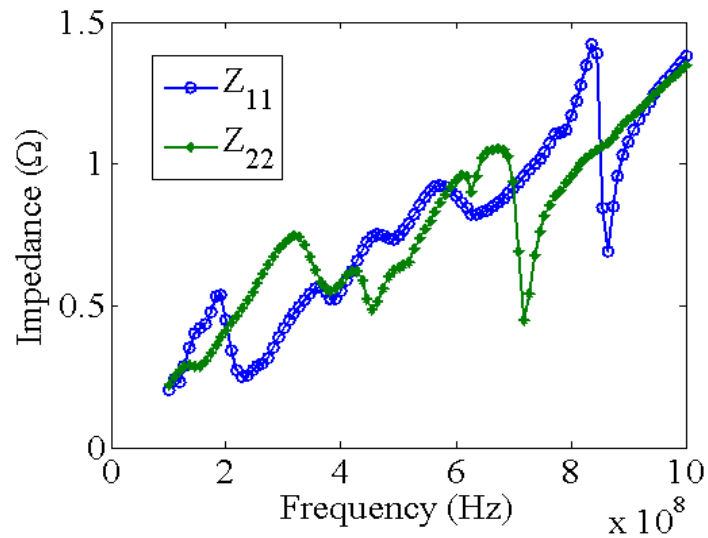
Figure 3.12. Self-impedance responses at port 1 and 2 of the test case 2 after the optimization using the customized GA.

For comparison, the GA optimizer without the regional limit was run under the same conditions. The average number of iterations taken for the GA optimizer to reach the target exceeded 100, which took more than six hours. However, the average optimization time of the customized GA was 10 minutes. Again, the final placement patterns of the ordinary GA optimizer resemble those of the customized GA optimizer as compared in Figure 3.13.
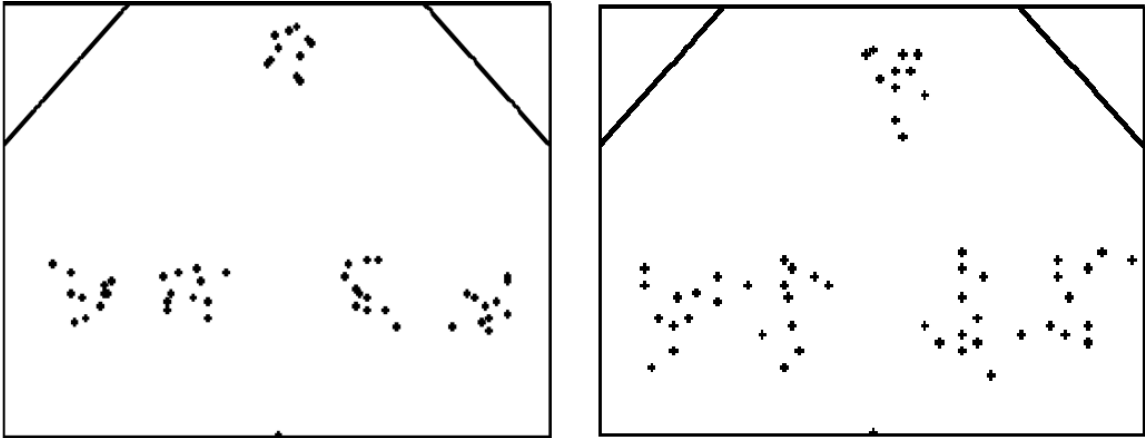
Figure 3.13. Comparison of final placement of capacitors using the customized GA (left) and the typical GA (right).

3.7 Summary

The automation technique for searching optimal solutions of decoupling capacitor values and locations has been presented. For the optimization algorithm, a GA, which simulates the natural evolution process, has been chosen. Each generation consists of a number of genes that contains their unique parameters, such as values and locations of the decoupling capacitors. The capacitor information of each gene is input to the PDN solver, MFEM, to obtain the impedance profile in the presence of decoupling capacitors. The best few genes are selected as parent genes for the next generation, and they pair themselves and mutate to produce children genes. This process continues until solutions from certain genes satisfy the target impedance.

MFEM utilizes 2D FEM that discretizes metal surfaces using non-uniform triangles. Thus, MFEM is a computationally efficient method for the PDN structures with irregular and complicated shape. However, the downside of MFEM is that its equivalent circuit is not a physics-based model. Hence, the simple connection of the decoupling

capacitor model into MFEM results in the incorrect model. Thus, the technique for the incorporation of the external circuit model into MFEM was shown using a decoupling capacitor model with a series connection of a capacitor, inductor, and a resistor.

To improve the convergence speed of the optimization, a decoupling technique that reduces the spread inductance has been applied to the algorithm. Since the spread inductance created between the decoupling capacitor and a noise port reduces the effectiveness of the capacitors by increasing the impedance, the distance between the decoupling capacitors and noise port needs to be minimized. Hence, by limiting the initial locations of the decoupling capacitors to the close proximity of a noise port, the convergence speed was drastically increased. The optimization effectiveness can be further improved by devising a better fitness function, which estimates the performance of each gene.

CHAPTER 4

POWER INTEGRITY MODELING USING THE MULTILAYER TRIANGULAR ELEMENT METHOD (MTEM)

4.1 Introduction

This chapter introduces a new modeling method, the multilayer triangular element method (MTEM), which applies a triangular mesh on the plane surface along with its dual graph, for the analysis of multilayer power/ground planes. The method employs the orthogonal property between Delaunay triangulation and its dual graph, Voronoi diagram.

4.2 Formulation for Single Plane-Pair

4.2.1 Generalization of Planar Circuit Model

As explained in Section 2.1.2, a pair of package power/ground planes can be approximated as a planar circuit. Consider a plane-pair separated by a dielectric, which lies in the x-y plane of a Cartesian coordinate system. Since the x-y dimensions of the structure are comparable to the wavelength while z dimension is much smaller, the electromagnetic fields inside the plane-pair can be assumed to vary only along the x-y directions. Therefore, the electrical model of a plane-pair can be reduced to be two-dimensional (2D) [10] [16], and the plane-pair can be considered as a parallel-plate waveguide. A waveguide is a transmission line, which can be expressed with an equivalent circuit composed of frequency-dependent lumped elements [52]. Although the equivalent circuit shown in [52] is applied to a rectangular geometry, this circuit model

can be extended to arbitrary shape. The equivalent circuit of an arbitrary-shaped unit-cell of a plane-pair is shown in Figure 4.1, and it can be described by Kirchhoff's current law (KCL),

$$(j\omega C_i + G_i)V_i + \sum_{k=1}^{N} \frac{V_i - V_k}{j\omega L_{ik} + R_{ik}} = 0, \tag{27}$$

where V is the unknown voltage at each node. The values of lumped elements can be obtained by applying electromagnetic field theory, the Maxwell-Ampere equation,

$$\oint_C \vec{H} \cdot \overrightarrow{dl} = \iint_S (\vec{J} + j\omega\epsilon\vec{E}) \cdot d\vec{s}, \tag{28}$$

which describes that the change of electric fields (E-fields) of a unit-cell generates magnetic fields (H-fields) along the contour of the unit-cell. Using the 2D approximation, associated field components residing in a plane-pair are H_x, H_y, and E_z. The H-field on the left-hand-side of Equation (28) can be substituted by the E-field using the 2D Maxwell-Faraday equation,

$$\nabla_T \times \vec{E} = -j\omega\mu\vec{H}, \tag{29}$$

where $\nabla_T = \hat{x}\frac{\partial}{\partial x} + \hat{y}\frac{\partial}{\partial y}$, to result in

$$\oint_C \vec{H} \cdot \overrightarrow{dl} = -\frac{1}{j\omega\mu}\oint_C \nabla_T \times \vec{E} \cdot \overrightarrow{dl}$$

$$= -\frac{1}{j\omega\mu}\oint_C \nabla_T \times E_z\hat{z} \cdot \overrightarrow{dl}$$

$$= -\frac{1}{j\omega\mu}\oint_C \nabla_T E_z \cdot \hat{z} \times \overrightarrow{dl}. \tag{30}$$

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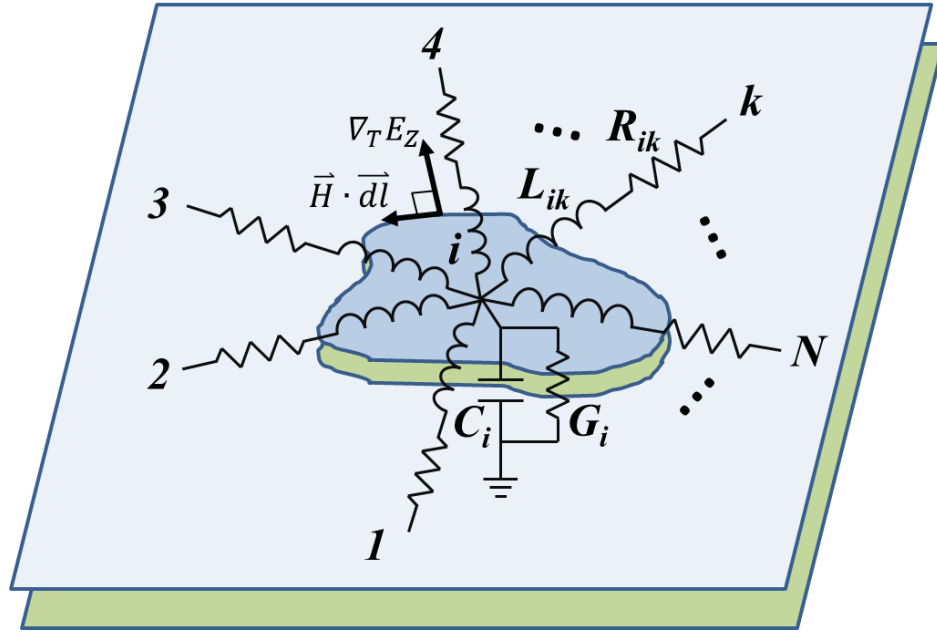
Figure 4.1. The equivalent circuit of a unit-cell in a plane-pair

The gradient, $\nabla_T E_z$, represents the change of E-fields between the unit-cell and the neighboring cells, and the $\vec{dl}$ indicates the contour of the unit-cell where magnetic fields reside. Since the E- and H-fields are mutually orthogonal, the directions of $\nabla_T E_z$ and $\vec{dl}$ must be perpendicular, which necessitates the orthogonal relationship between the unit-cell contour and the equivalent circuit line connecting node i and k, where $k = 1, 2, 3, ...,$ N, as shown in Figure 4.1. This is an essential condition that has to be satisfied before combining the field and circuit theory, and the condition can be realized by creating dual meshes that are mutually orthogonal. The detailed formulation using orthogonal meshes is presented in the following section.

4.2.2 Application of Delaunay and Voronoi Mesh

Considering a number of possible mesh schemes, the modeling method proposed in this thesis employs a non-uniform triangular mesh that has important advantages in terms of

discretization effectiveness. Triangulation requires the least number of polygons for the discretization of multi-dimensional geometries, and can efficiently describe curved surfaces. A triangular mesh can be created by Delaunay triangulation, which avoids the generation of long skinny triangles. Thus, potential numerical precision problems are minimized, and the triangulation is optimal for finite element problems [53]. In addition, the dual graph of Delaunay triangulation corresponds to a Voronoi diagram, which has an orthogonal relationship. Therefore, the dual graphs can provide a mesh for the representation of related fields and the equivalent circuit of a plane-pair.

Figure 4.2 (a) shows Delaunay and Voronoi diagrams created on a plane-pair and depicts the change of E-fields, generated H-fields, and the equivalent circuit. For clarity, loss terms are neglected, and their incorporation is explained in Section 4.2.3. To obtain the values for the lumped elements of the equivalent circuit, the electromagnetic field equation, Equation (28), is applied to the triangle unit-cell using the geometries and node numbers as described in Figure 4.2 (b). By assuming the linear change of E-fields between unit triangles, the left-hand side of Equation (28) can be derived as follows:

$$
\begin{aligned}
\oint_C \vec{H} \cdot \overrightarrow{dl} &= -\frac{1}{j\omega\mu}\oint_c \nabla_T E_z \cdot \hat{z} \times \overrightarrow{dl} \\
&= -\frac{1}{j\omega\mu}\sum_{k=1}^{3}(\hat{u}_{ik})\frac{E_{z,i}-E_{z,k}}{h_{ik}}\cdot(-\hat{u}_{ik})l_k \\
&= \frac{1}{j\omega\mu}\sum_{k=1}^{3}\frac{E_{z,i}-E_{z,k}}{h_{ik}}(l_k) \\
&= \frac{1}{j\omega\mu d}\sum_{k=1}^{3}(V_i-V_k)\left(\frac{l_k}{h_{ik}}\right),
\end{aligned}
\tag{31}
$$

where d is the dielectric thickness. Since the size of a unit-triangle is electrically small, the electric field within a triangle can be assumed to be uniform. Thus, the derivation of the right-hand side of Equation (28) is given by,

$$\iint_S (\vec{J} + j\omega\epsilon\vec{E}) \cdot d\vec{s} = I + j\omega\epsilon \iint_S \frac{V_i}{d} \hat{z} \cdot d\vec{s}$$

$$= I + j\omega\epsilon \frac{V_i}{d} A_i, \tag{32}$$

where I is the total current injected into the unit-triangle, A_i is the area of the unit-triangle. For a source-free ($I=0$) unit-triangle, replacing Equation (28) with Equation (31) and (32), we obtain

$$j\omega\epsilon \frac{V_i}{d} A_i + \frac{1}{j\omega\mu d} \sum_{k=1}^{3} \left\{ (V_i - V_k) \frac{l_k}{h_{ik}} \right\} = 0. \tag{33}$$

Finally, by comparing Equation (27) and (33), the values of the lumped elements in the equivalent circuit can be obtained as

$$L_{ik} = \mu d \frac{h_{ik}}{l_k}, \tag{34}$$

$$C_i = \epsilon \frac{A_i}{d}. \tag{35}$$

49
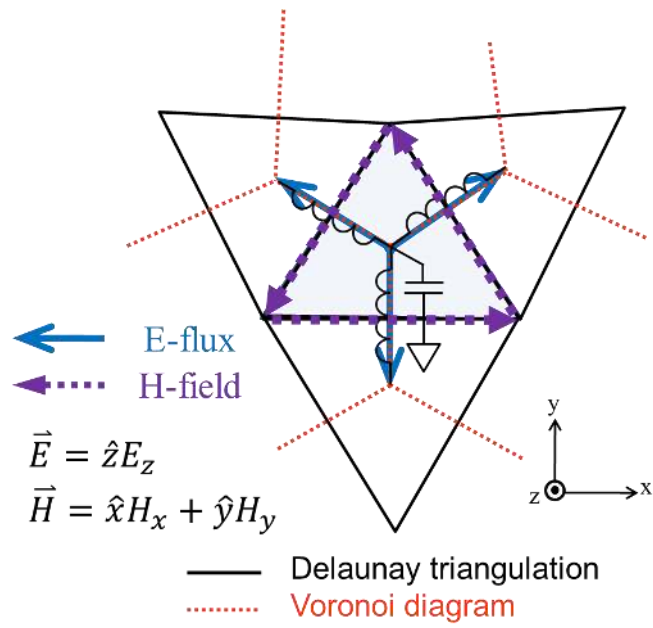
(a) Electromagnetic fields and the equivalent circuit of a triangle.
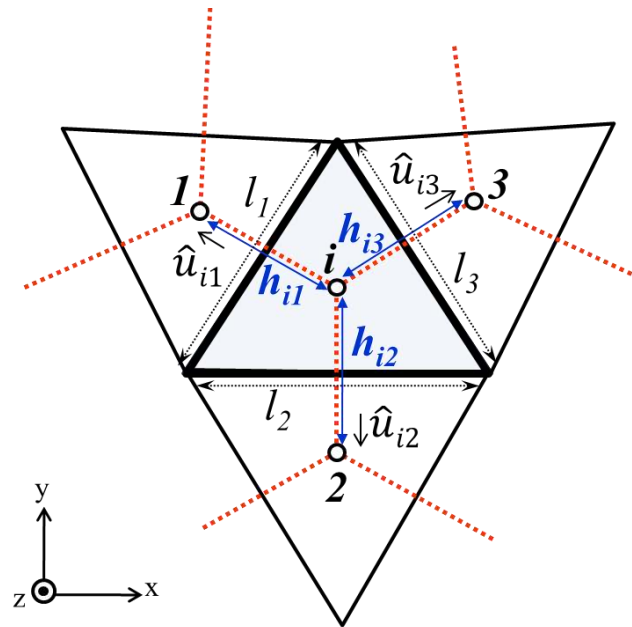
(b) Node numbers and dimensions.

Figure 4.2. Triangle unit-cell and neighboring triangles of a plane-pair.

The authors of [54] present a similar approach for a single plane-pair; however, the unit-cell is not a triangle but a polygon created by the Voronoi diagram. The major difference of using a different unit-cell is the difference in computational efficiency. Due to the nature of Voronoi diagram, each Voronoi-polygon will face six neighboring nodes that require numerical calculations, while a triangle has only three, as shown in Equation (31). As a result, the required computational resource for the triangle-based model is two times lower as compared to the Voronoi-polygon-based model if the same mesh is used. Moreover, the system matrix entries of the Voronoi-polygon-based model have a one-to-one correspondence to those of any FEM-based method, for example MFEM [20]. Therefore, the system matrices generated by the Voronoi-polygon-based and the FEM-based method will be the same size and sparsity, requiring similar computational effort; in particular, the memory requirement will be equivalent. Comparison of the memory consumption and computational complexities is discussed with examples in Section 4.8.

4.2.3 Inclusion of Loss Terms

In the previous section, loss terms are ignored for clarity. However, frequency dependent loss terms need to be included for accurate analysis, especially at high frequencies. The inclusion of frequency dependent loss terms to MTEM can be explained using the equivalent circuit and lumped elements. Consider an equivalent circuit created between two triangle unit-cells as shown in Figure 4.3. The resistance, R, between two triangles represents the conductor loss, which includes DC (R_{dc}) and AC loss (R_{ac}). The conductance, G, connected between each triangle and ground represents the dielectric loss.

51
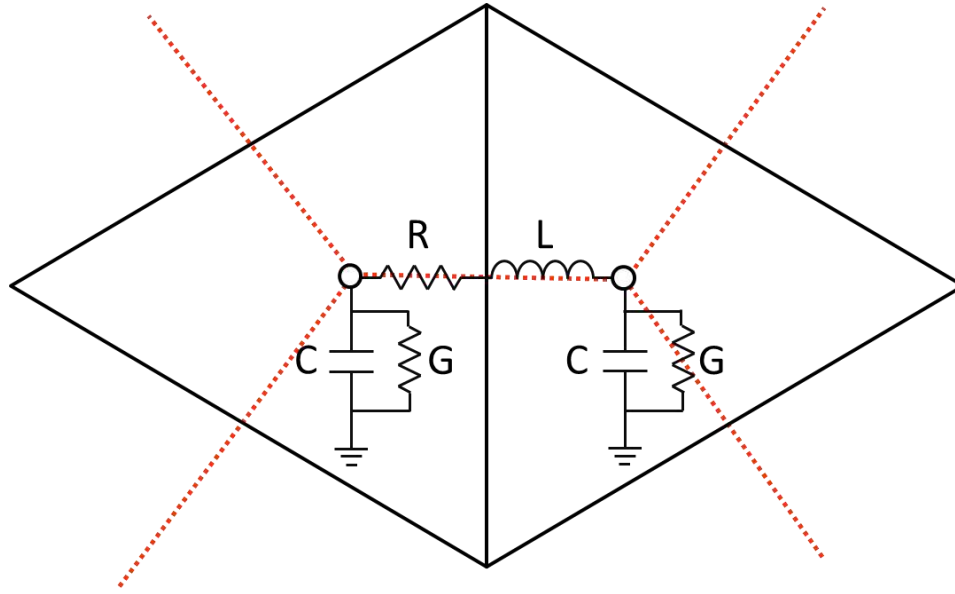
Figure 4.3. Equivalent circuit of MTEM with loss terms.

4.2.3.1 Conductor Loss

The DC conductor loss is mainly caused by the finite conductivity of the metal planes and the area in which the current is flowing. The equation of the DC resistance is

$$R_{dc} = \frac{L}{\sigma A} = \frac{L}{\sigma W t} \ [\Omega], \tag{36}$$

where L is the length, W the width, t the thickness, and σ the conductivity of the metal plate.

The AC conductor loss is dominated by the skin effect, which represents the behavior of electric current flowing at the periphery of the conductor. The skin depth is a parameter for the distance from the surface of a conductor where electric charges are mostly concentrated at a certain frequency. The skin depth is defined as [55]

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \ [m], \tag{37}$$

where f is the frequency. Thus, the AC resistance is

$$R_{ac} = \frac{L}{\sigma \delta W} = \frac{L\sqrt{\pi f \mu \rho}}{W} \ [\Omega], \tag{38}$$

where ρ is the resistivity of the conductor.

Both DC and AC resistances can be combined to represent the total loss resulted from the conductor, and a good approximation is obtained from measurements and given as [56] [57]

$$R_{total} \approx \sqrt{R_{dc}^{\ 2} + R_{ac}^{\ 2}} \ [\Omega]. \tag{39}$$

The equations for the DC and AC conductor loss (Equation (36) and (38)) represent loss terms for rectangular geometry. To apply those equations to MTEM, the resistance equations for rectangles need to be converted to those for triangles. This conversion can be simply realized by replacing W with $0.5W$, which is the average width of the conductor between the two nodes as can be explained with Figure 4.4. In addition, since the loss representations account only for one part of the conductor, the conductor loss of the return current needs to be included as well. Since the upper and lower conductors in a plane-pair are symmetric, the loss terms can be simply doubled to describe the loss terms for both conductors. Consequently, the conductor loss term connecting node i and j of MTEM can be obtained as follows:

$$R_{ij} = 4\sqrt{R_{dc}^2 + R_{ac}^2}\ [\Omega], \tag{40}$$

where R_{dc} and R_{ac} are given in Equation (36) and (38).
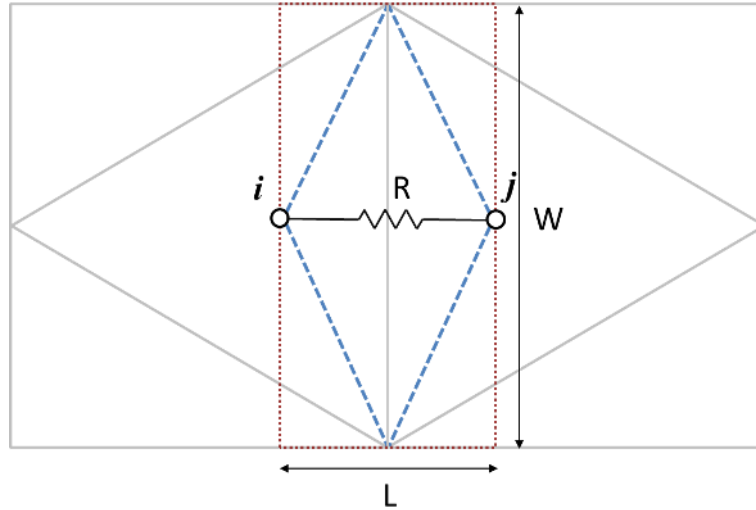
Figure 4.4. Areas for the conductor loss calculation: Area enclosed by blue dashed line is for triangular mesh (MTEM), while red dotted line is for a rectangular mesh.

4.2.3.2 Dielectric Loss

Although the conductor loss is dominant at low frequencies, the dielectric loss becomes significant at high frequencies. The dielectric loss stems from the oscillation of molecular particles of the dielectric material when excited by a time-varying electric field. In the equivalent circuit of MTEM, the dielectric loss is represented by the conductance between the top and bottom conductors of a plane-pair. The dielectric loss can be characterized by the loss tangent, and the relationship between the loss tangent and the conductance is [58]

$$G = \omega C \tan \delta \ [\Omega^{-1}], \tag{41}$$

where ω is the angular frequency, and C is the capacitance per unit length. The application of Equation (41) to node i is straightforward as follows:

$$G_i = \omega \frac{\varepsilon' A_i}{d} \tan \delta \,, \tag{42}$$

where ε' is the real part of the complex dielectric constant, A_i the area of the triangle unit-cell for node i, and d the thickness of the dielectric.

4.3 Extension to Multiple Plane-Pairs

A PDN contains alternating layers of power and ground planes for multi-level voltage supply and/or for miniaturization of the system. Such multilayer structures can be considered as a series stack-up of plane-pairs on top of one another. In a single plane-pair, the noise coupling occurs only along lateral directions. However, the noise coupling in multiple plane-pairs can occur along the vertical direction as well, because of the apertures in the plane. Hence, the mutual coupling between plane-pairs needs to be included in the modeling of multiple plane-pairs.

Consider a three-layer structure with a voltage reference assigned to the bottom-most layer as shown on the left in Figure 4.5. First, the structure can be decomposed into two individual plane-pairs, A and B. Next, each plane-pair can be modeled using the modeling method explained in the previous section, and portions of each equivalent circuit, node i and j, and node $N+i$ and $N+j$, are shown on the right in Figure 4.5. Last, each plane-pair model can be recombined to establish a model for the whole three-layer

55

structure. At this stage, the voltage reference of plane-pair A needs to be shifted from the ideal ground to node $N+i$ and $N+j$, which are on the top layer of plane-pair B. Otherwise, the two plane-pairs are isolated and their interactions are ignored in modeling.
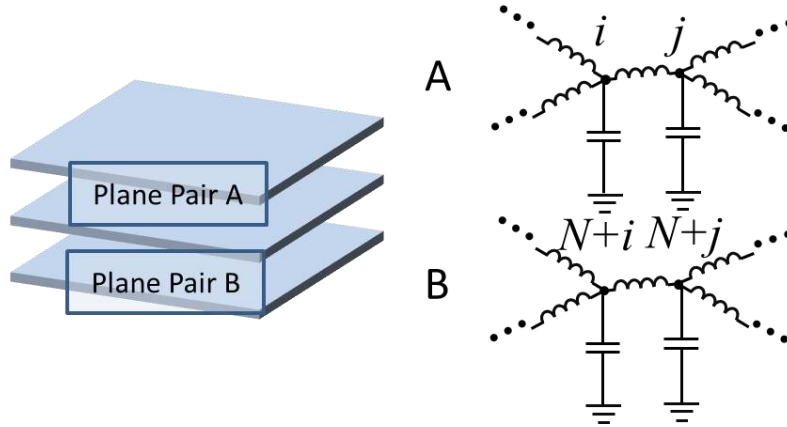
Figure 4.5. Multiple plane-pairs (left) and the equivalent circuit of each plane-pair (right). i and j are node numbers that range between 1 and N, where N is the total number of the nodes on each plane-pair.

The shifting of a voltage reference can be realized by using an indefinite admittance matrix [**21**]. Let $\bar{\bar{Y}}_A$ and $\bar{\bar{Y}}_B$ be the admittance matrices of plane-pair A and B, respectively, and N be the number of nodes on each plane-pair. Hence, the $N \times N$ matrices, $\bar{\bar{Y}}_A$ and $\bar{\bar{Y}}_B$, represent the equations for node 1 through N, and $N+1$ through $2N$, respectively, and they are indefinite admittance matrices, since none of the nodes is considered the reference node. Figure 4.6 shows the block diagrams of each plane-pair model (top) and the combination of the models with a shifted voltage reference (bottom), where i and j are any numbers between 1 and N, and $i \neq j$. To simplify the problem, consider the left-hand-side nodes, node i and $N+i$, and the network equations for plane-pair A and B at those nodes can be obtained as

$$I_i = Y_{A,i}V_i, \tag{43}$$

$$I_{N+i} = Y_{B,i}V_{N+i}, \tag{44}$$

where $Y_{A,i}$ and $Y_{B,i}$ represent $Y_A(i, i)$ and $Y_B(i, i)$, respectively. By stacking plane-pair A on top of plane-pair B, the voltage reference of plane-pair A shifts from the ideal ground to the top layer of plane-pair B. Because of the reference shift, the current at node $N+i$ is changed to $I_{N+i} - I_i$ by accounting for the return current from node i, and the voltage for node i is changed to $V_i - V_{N+i}$. Thus, the network equations for the stacked plane-pairs can be derived from Equation (43) and (44) as follows:

$$I_i = Y_{A,i}V_i - Y_{A,i}V_{N+i}, \tag{45}$$

$$I_{N+i} = -Y_{A,i}V_i + (Y_{A,i} + Y_{B,i})V_{N+i}, \tag{46}$$

which can be expressed in a matrix form:

$$\begin{bmatrix} I_i \\ I_{N+i} \end{bmatrix} = \begin{bmatrix} Y_{A,i} & -Y_{A,i} \\ -Y_{A,i} & Y_{A,i} + Y_{B,i} \end{bmatrix} \begin{bmatrix} V_i \\ V_{N+i} \end{bmatrix}. \tag{47}$$
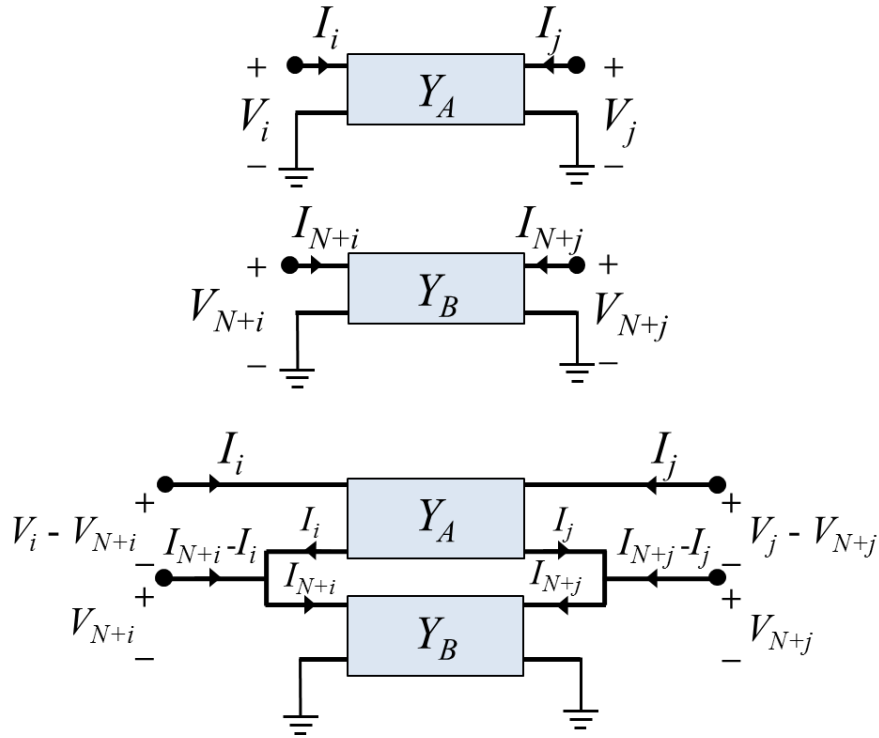
Figure 4.6. Block diagrams of each plane-pair model using indefinite admittance matrices (top), and the combined model with a shift of the ground reference (bottom).

This process can be regarded as stamping admittance $(Y_{A,i})$ to the desired locations that represent the shifted reference (node $N+i$). Using the stamping rule, Equation (47) can be extended to any number of plane-pairs. Assigning the indices as $1, 2, \ldots, k$ to the plane-pairs from the top to bottom, the system matrix for multiple plane-pairs can be obtained as

$$
\begin{bmatrix}
\bar{\bar{Y}}_1 & -\bar{\bar{Y}}_1 & & & & \\
-\bar{\bar{Y}}_1 & \bar{\bar{Y}}_1 + \bar{\bar{Y}}_2 & -\bar{\bar{Y}}_2 & & & \\
& \ddots & \ddots & \ddots & & \\
& & -\bar{\bar{Y}}_{k-1} & \bar{\bar{Y}}_{k-1} + \bar{\bar{Y}}_k & -\bar{\bar{Y}}_k & \\
& & & \ddots & \ddots & \ddots
\end{bmatrix}. \tag{48}
$$

4.4 Mesh Generation

To apply the technique of extending the model for a single plane-pair to multiple plane-pairs, the nodes in each plane-pair must be in the same x-y locations. Hence, each plane-pair shares a unique mesh that is generated on a layer on which all the geometric outlines of each plane-pair are gathered. The geometric outlines can include any physical structures such as apertures and plane boundaries, which need to be meshed. Distinguishable segments, such as conductors and apertures, are assigned to its unique sub-domain, which requires different modeling. Mesh generation for multiple plane-pairs will be discussed with an example in Section 4.8.

4.5 Modeling of Apertures

Apertures in the plane indicate the non-metalized regions in a metal plane, such as via anti-pads and plane splits for power islands. Since conduction current does not flow through such non-metalized areas, the apertures need to be modeled accordingly. Consider unit-cell models that include apertures in either top or bottom layer as shown in Figure 4.7. Since unit-cell A is in a plane-pair without any aperture on either layer, the values of the lumped elements, L_A and C_A, of the equivalent circuit can be obtained from Equation (34) and (35). Unit-cell B, however, misses metallization on the top layer, and unit-cell C the bottom layer. Hence, those unit-cells no longer support the parallel-plate waveguide mode, and do not contribute to the propagation of the wave inside a plane-pair.
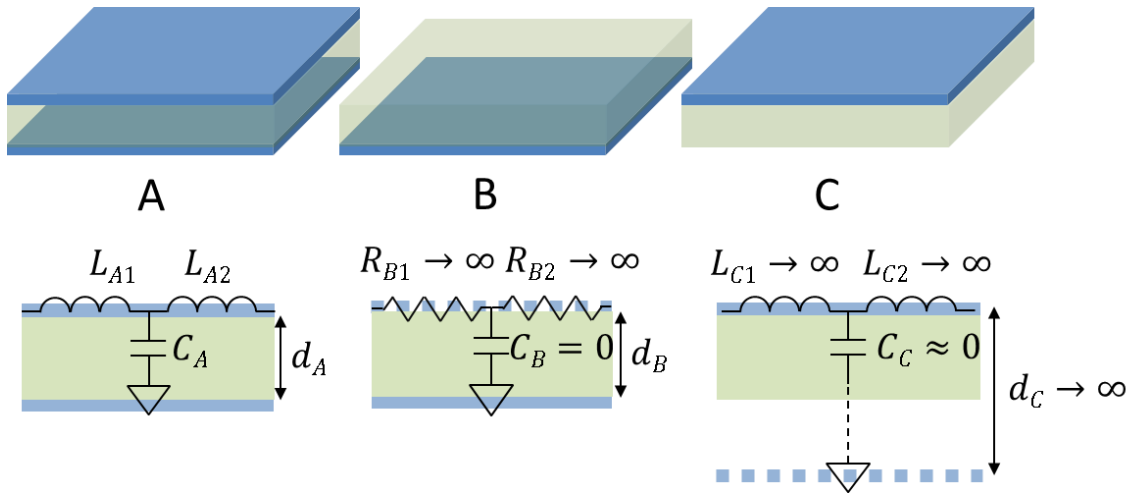
Figure 4.7. Plane-pair sections with and without apertures on the top and the bottom plane (top). One-dimensional equivalent circuits of each section (bottom).

By maintaining a parallel-plate modeling scheme, unit-cell B can be considered as a plane-pair with the top metal plane replaced by a non-conducting material. Therefore, the impedance between the neighboring nodes is infinitely high, and thus L_{B1} and L_{B2} are replaced by infinite values of R_{B1} and R_{B2}. The capacitance, C_B, is zero, because the top plate is not a metal plate.

Unit-cell C can be considered as a plane-pair with the bottom plane located far from the top plane. Since d_c is infinitely large, Equation (34) and (35) result in infinite L_C and zero C_C, respectively. Notice that since both unit-cells B and C represent physically identical structures with only an upside-down relation, the resultant models are equivalent.

These modeling schemes can be consistently applied to the model of an aperture in a multilayer structure as shown in Figure 4.8. Although node i in plane-pair 1 misses the layer right below the top layer, another layer is present at the bottom. Thus, node i corresponds to unit-cell A not unit-cell C shown in Figure 4.7, and the values of L_{i1}, L_{i2},

and C_i can be obtained by replacing d with d_1+d_2 in Equation (34) and (35), respectively. Connecting C_i between node i and $2N+i$ completes the modeling of node i. Notice that node $N+i$ of plane-pair 2 is equivalent to unit-cell B.
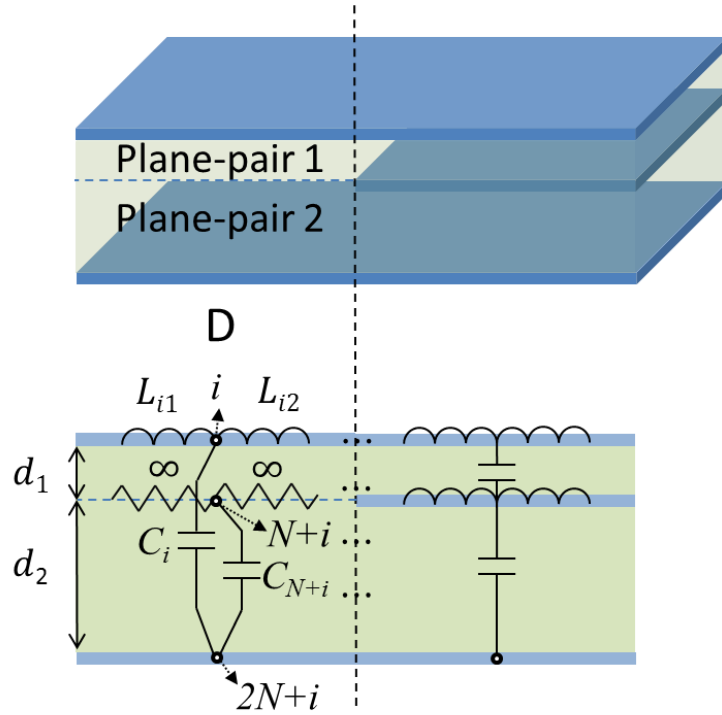
Figure 4.8. Modeling of an aperture in the middle of multiple plane-pairs.

To further explain modeling of unit-cell D, a three-layer structure with an aperture located in the middle layer is shown in Figure 4.9. Since the conductor plane on the second layer is missing, the thickness of the dielectric between node m and node $(2N+m)$ is d_1+d_2 (ignoring the metal thickness). If dielectric material is homogeneous on both layers, modified values of the lumped elements for the node m are

$$C_m = \epsilon \frac{A_m}{d_1 + d_2},\qquad(49)$$

$$L_{mk} = \mu(d_1 + d_2)\frac{h_{mk}}{l_k},$$ (50)

where $k=1$, 2, and 3, representing the indices of neighboring nodes. Since a conductor is missing on node $(m+N)$, which is on the second layer, the reference node of node m has to be shifted to node $(m+2N)$, which is on the third layer, where N is the number of the nodes on each plane-pair. Shifting reference node is done using an indefinite admittance matrix as

$$
\begin{array}{c}
m^{th} \\
\\
(2N+m)^{th}
\end{array}
\begin{bmatrix}
\ddots & & & \\
& Y_{Cm} & \cdots & -Y_{Cm} \\
& \vdots & \ddots & \vdots \\
& -Y_{Cm} & \cdots & Y_{Cm} \\
& & & & \ddots
\end{bmatrix},
$$ (51)

where $Y_{Cm} = j\omega C_m$.
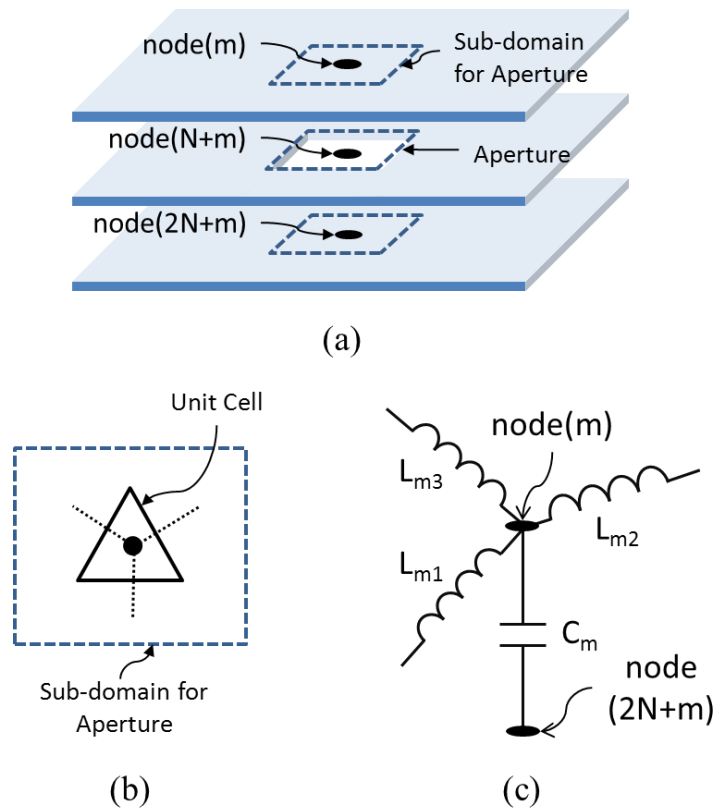
Figure 4.9. (a) A three-layer structure with an aperture in the middle layer. (b) Top view of the sub-domain for the aperture. (c) Equivalent circuit for the node in the aperture.

4.6 Inclusion of External Circuit Elements

The addition of a decoupling capacitor to the power/ground plane model can be conducted in the concept of an equivalent circuit. The equivalent circuit for a typical decoupling-capacitor can be modeled connecting capacitors, equivalent series inductance (ESL), and resistance (ESR) in series as expressed in Equation (23). With the values of the lumped elements, the two-by-two admittance matrix for the decoupling capacitor can be created. Finally, the admittance matrix of the decoupling capacitor is stamped on to the admittance matrix of the power/ground plane in accordance with the node connectivity as similarly done in Equation (51). For example, if a decoupling capacitor is

connected between node n on the upper plane and node ($n+N$) on the lower plane, the admittance matrix of the decoupling capacitor (Y_{decap}) is added to the power/ground system as follows:

$$
\begin{array}{c} n^{th} \\ \\ (n+N)^{th} \end{array}
\begin{bmatrix}
\ddots & & & \\
& Y_{decap} & \cdots & -Y_{decap} \\
& \vdots & \ddots & \vdots \\
& -Y_{decap} & \cdots & Y_{decap} \\
& & & & \ddots
\end{bmatrix}.
\tag{52}
$$

Notice that the addition of the decoupling capacitor model to MTEM is straightforward, whereas mathematical modifications are required for MFEM as explained in Section 3.2.2.

4.7 Test Cases and Results

4.7.1 Multiple Plane-Pairs with Apertures

A multilayer structure consisting of four layers of perforated arbitrary-shape metal planes is designed as shown in Figure 4.10. Metal layers are separated by 200-µm, 500-µm, and 300-µm dielectric layers, whose relative permittivity is 4.5 and loss tangent 0.02. Two ports are assigned between the first and the third plane-pair, respectively. To create a mesh, the outlines of all the objects in each layer were collected onto a single layer, and Delaunay triangulation was created. Subsequently, a Voronoi diagram was drawn on top of the triangulation, thereby completing the creation of the dual mesh. Although the smallest features, namely the apertures in layer 2, are as small as 2×3 mm, they are

electrically large enough to function as gateways for the mutual coupling between plane-

pairs, and need to be discretized for analysis. The final mesh is shown in Figure 4.11.
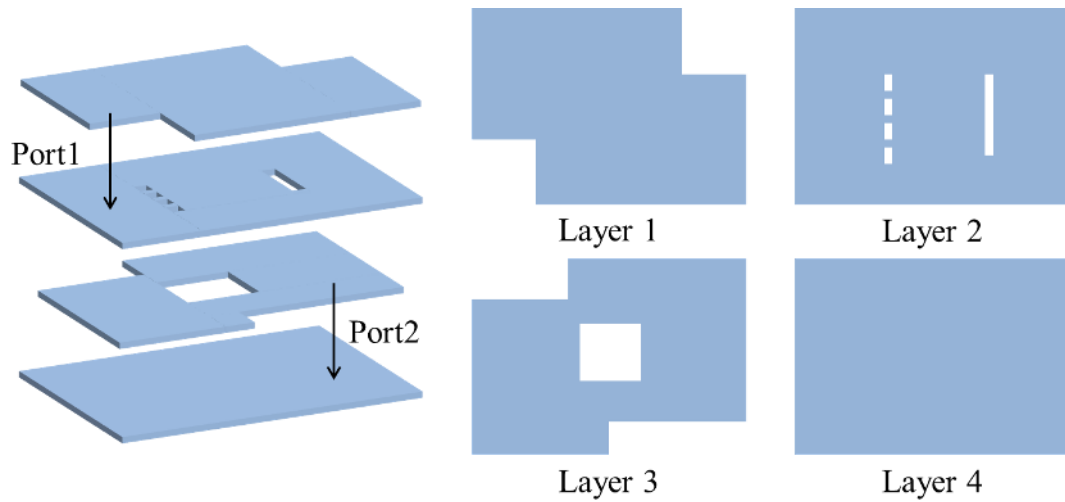
Figure 4.10. Example of a multiple plane-pair structure with apertures on each layer.
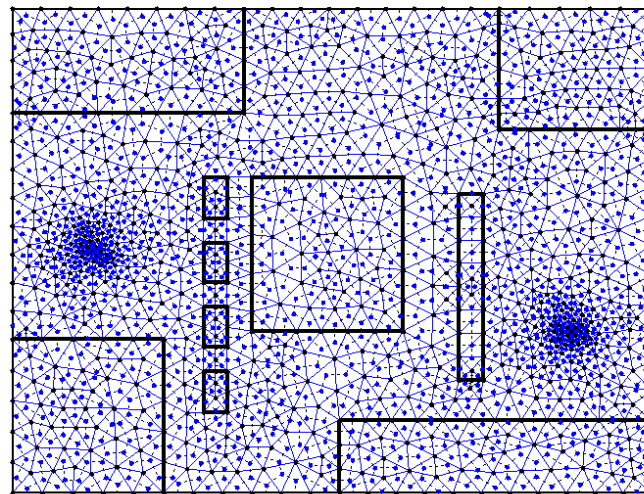
Figure 4.11. Dual mesh created on the layer where all the geometries from each layer are concatenated together.

The structure was simulated using MTEM as well as a commercial 3D full-wave solver, CST Microwave Studio [59]. The self-impedance at port 1 and the transfer-impedance between the ports are shown in Figure 4.12 and Figure 4.13, where a good correlation is observed over the frequency range. In particular, transfer-impedance results indicate that the top and bottom plane-pairs are mutually coupled through the small apertures in layer 2 and 3.
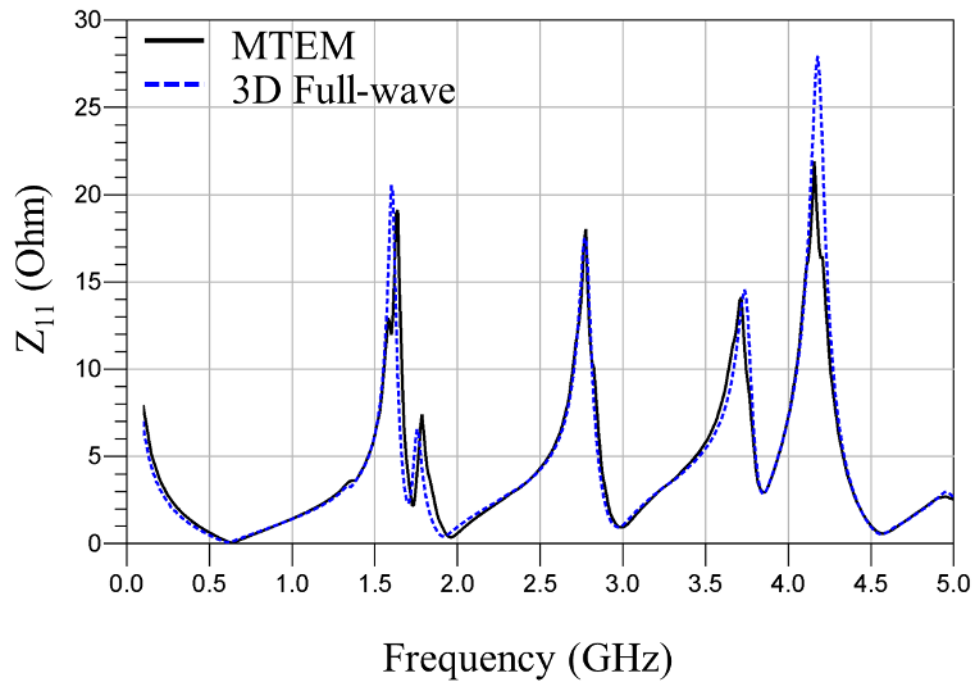
Figure 4.12. Self-impedance at port 1.
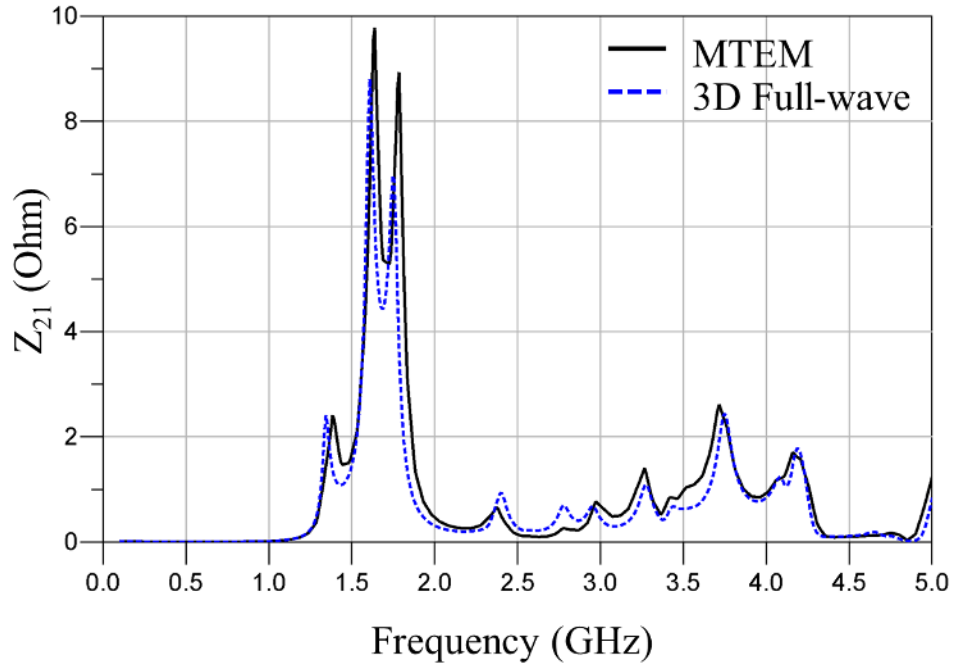
Figure 4.13. Transfer impedance between port 1 and 2.

4.7.2 Decoupling Capacitors

Figure 4.14 (a) shows a plane-pair with a port located at the bottom-left of the structure. Six decoupling capacitors are placed around the source port to minimize the impedance of the plane-pair. Using given values of capacitance as well as ESL and ESR of the capacitors, their equivalent circuits are added to the admittance matrix of the plane-pair as Equation (52). The self-impedance responses of MTEM show good correlation with those of MFDM as shown in Figure 4.14 (b).
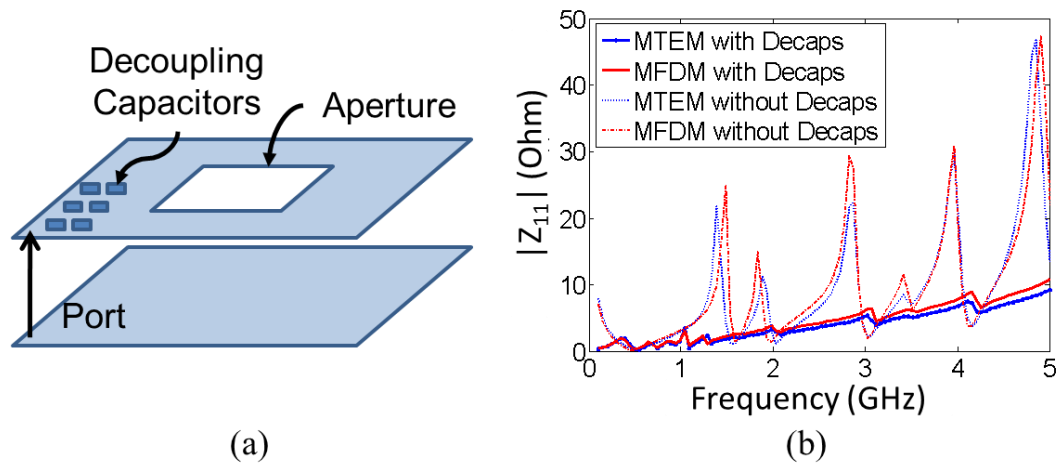
Figure 4.14. (a) Two-layer structure with an aperture and six decoupling capacitors near the port. (b) Self-impedance responses with and without decoupling capacitors.

4.8 Comparison of Computational Complexity

In this section, the computational complexity of MTEM is compared with that of other differential equation methods, MFDM and MFEM.

4.8.1 Multi-Dimensional and Multilayer Structure

One of the advantages of using a non-uniform triangular mesh over using a uniform rectangular or square mesh is the efficiency in discretization, especially for the structures with a broad range of physical dimensions. An example of a three-layer structure with small holes is shown in Figure 4.15 (a) with a non-uniform triangular mesh and its dual mesh. The smallest dimension, 1 mm, is the edge of the holes, and the largest dimension, 40 mm, is the edge of the plane. The transfer impedance results from MFDM, MFEM, and MTEM match well and capture the coupling of electromagnetic energy between plane-pairs as shown in Figure 4.15 (b). For this multidimensional structure, the MTEM and MFEM created about 2,000 and 3,000 unknowns, respectively, while MFDM created

about 8,000 unknowns. Therefore, a uniform square mesh results in a significantly greater number of unknowns than a non-uniform triangular mesh for multidimensional geometries. The created meshes from each method are compared in Figure 4.16.

(a)   (b)
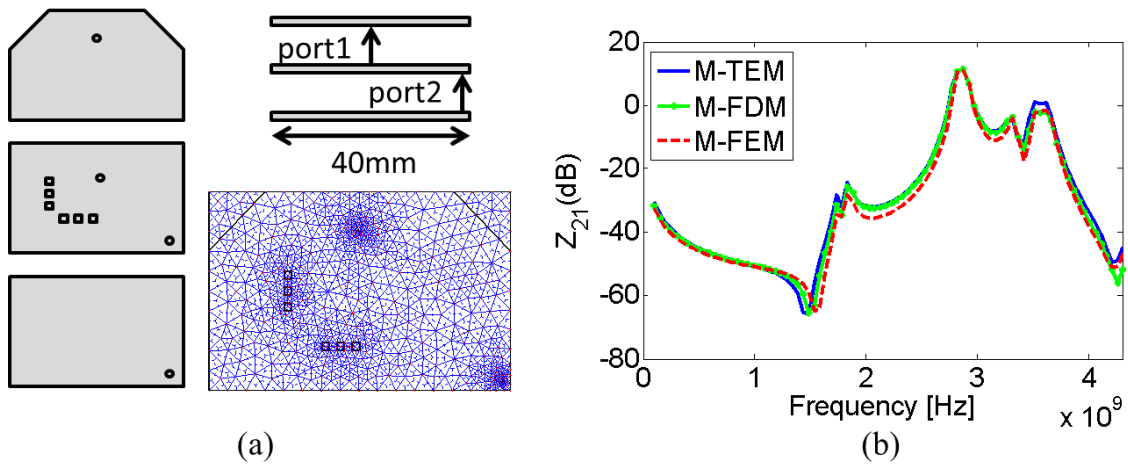
Figure 4.15. (a) Example of a structure with multi-dimensional geometries. (b) Transfer-impedance responses.
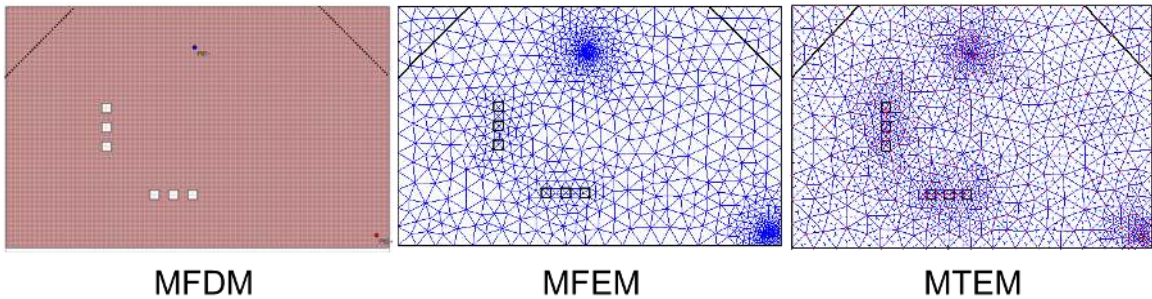
Figure 4.16. Created meshes by MFDM, MFEM, and MTEM for the example structure shown in Figure 4.15.

To simulate the example shown in Figure 4.10, MTEM created 1,446 triangles for each plane-pair and 4,338 unknowns in the system matrix. These numbers are considerably smaller than that for the 3D full-wave solver, which created more than

69

100,000 unknowns for the same structure. To compare the computational efforts of MTEM with other 2D frequency-domain solvers, the structure was simulated using MFDM and MFEM as well. Each method was run until similar accuracy was obtained by creating finer meshes. As a result, MFDM resulted in the largest number of unknowns, which reflects the number of unit-cells in the system, whereas MFEM and MTEM created a much smaller number of unit-cells. The reason for MFDM requiring more unknowns for the same structure is mainly because of the uniformity of the unit-cell size and shape: MFDM uses uniform squares, whereas both MFEM and MTEM use non-uniform triangles. The number of unknowns and non-zero entries in the system matrix of each solver are shown in Table 3.

Table 3. Comparison of system matrices created for the example in Figure 4.10 (K=10^3).

	MFDM	MFEM	MTEM
Unknowns	14,400	5,718	4,338
Non-Zeros	150K	81K	35K

4.8.2 Computational Efficiency under Same Accuracy

The comparison of the computational effort is performed under the assumption that the simulation results of MFDM, MFEM, and MTEM satisfy the allowed level of accuracy. For the accuracy reference, an analytical solution using a cavity resonator model [10] [11] was employed to solve a rectangular plane-pair. The plane-pair was composed of 40 ×30 mm metal planes separated by a lossless 200-µm dielectric with the permittivity of 4.5. Each modeling method continuously refined its mesh until the resultant error falls

below a target percent error. As a result, MTEM created the least number of unknowns as well as non-zero elements for a given accuracy as shown in Table 4. Although MFEM created a similar number of unknowns as MTEM, the number of non-zeros of MFEM outnumbered that of MTEM about a factor of 1.8.

Table 4. Comparison of system matrices under the same accuracy.

Method	Unknowns	Non-Zeros	% Error
MTEM	1,126	4,434	0.027
MFEM	1,153	7,925	0.037
MFDM	4,800	23,720	0.035

4.8.3   Comparison of MTEM and MFEM

Although both MFEM and MTEM apply the same discretization scheme (Delaunay triangulation), the calculation nodes for each method are different: MFEM uses triangle vertices, but MTEM uses triangle circumcenters. Hence, the number of unknowns for MFEM is proportional to the number of triangle vertices, whereas that for MTEM is to the number of triangles. In a large mesh, the number of triangle vertices is typically smaller than that of triangles, since neighboring triangles share some vertices. Therefore, if the same triangular mesh is used, the number of unknowns for MFEM may be smaller than that of MTEM. However, the use of the same mesh does not result in the same modeling accuracy; in fact, that of MTEM is better than that of MFEM. The reason can be best explained by the mesh diagrams shown in Figure 4.17. For the calculation of node *a*, MFEM involves node *a* to *g* in the calculation. Thus, the distance between neighboring nodes are defined by the lengths of triangle edges (solid lines). On the other hand,

71

MTEM calculation for node *1* includes node *2*, *3*, and *4*, and the distance between neighboring nodes are defined by the lengths of the Voronoi-polygon edges (dotted lines). The relationship of Delaunay and Voronoi meshes suggests the lengths of Voronoi-polygon edges are about 60 percent shorter than those of corresponding triangle edges. For example, if the distance between node *b* and *c* is *1*, that between node *1* and *4* is about *0.6*. Since the calculation accuracy of differential-equation techniques depends on the discretization edge lengths, the use of the same mesh will result in a less accurate result for MFEM compared to that for MTEM.
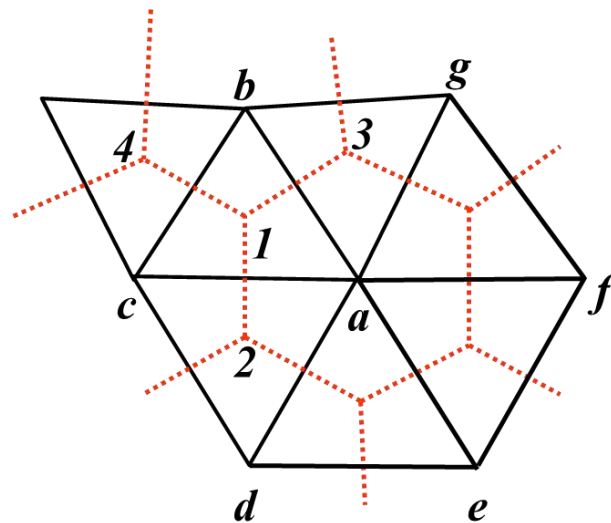
Figure 4.17. Triangular mesh for MFEM and the dual graphs for MTEM.

The computational efficiency of the method in [**54**] can be analyzed using the system matrix of MFEM. Although formulations of the two methods are different, they share the same mesh and use the same neighboring nodes for the calculation of each unit-cell. Consequently, the generated system matrices have the same number of unknowns and non-zero entries, requiring the same or at least similar computational effort.

72

To compare the computational efficiency, MFEM and MTEM were run to solve a 10-layer structure. Both methods continuously refined their meshes until their results satisfy the target accuracy level, which was set by an analytical solution using a cavity resonator model. As a result, similar number of unknowns were created for both methods; 415,000 (MFEM) and 428,000 (MTEM). However, MTEM consumed about 60-percent less memory to store non-zero entries than MFEM as expected from the reason explained above using Figure 4.17. In addition, the reordered system matrices shown in Figure 4.18 show that the bandwidth of MTEM is about 30-percent narrower than that of MFEM. As a result, the computation time for the matrix inversion for MTEM is about 2.4 times faster than that for MFEM. The comparison of the computational effort is summarized in Table 5.
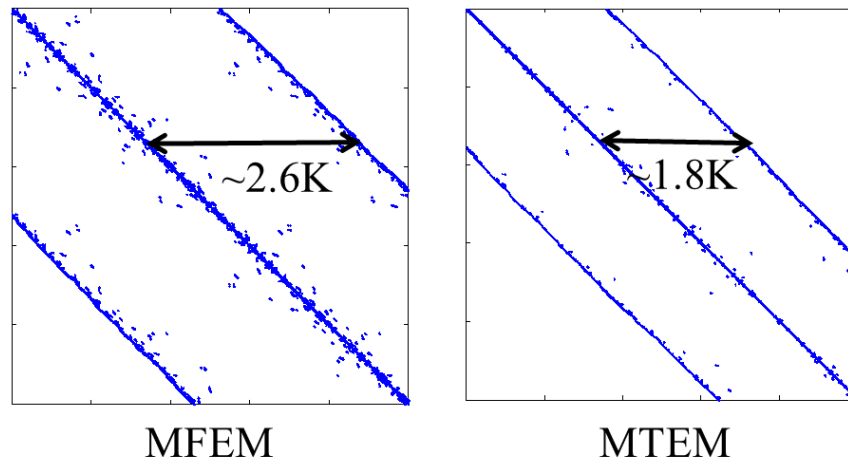
Figure 4.18. Zoomed-in areas of the reordered matrices of MFEM and MTEM (K=10^3).

Table 5. Computational efforts in solving a 10-layer structure ($K=10^3$, $M=10^6$).

Methods	Unknowns	Non-Zeros	CPU Time
MFEM	415K	8.1M	91.3 sec.
MTEM	428K	4.8M	37.5 sec.

4.8.4 Large Sized Problems

Figure 4.19 (a) shows the growth of the simulation speed of each method as the number of unknowns increases. Although the simulation time of all of the methods similarly grows as the number of unknowns increases, MTEM shows a slower increase than MFDM and MFEM by factors of 1.16 and 1.52, respectively.
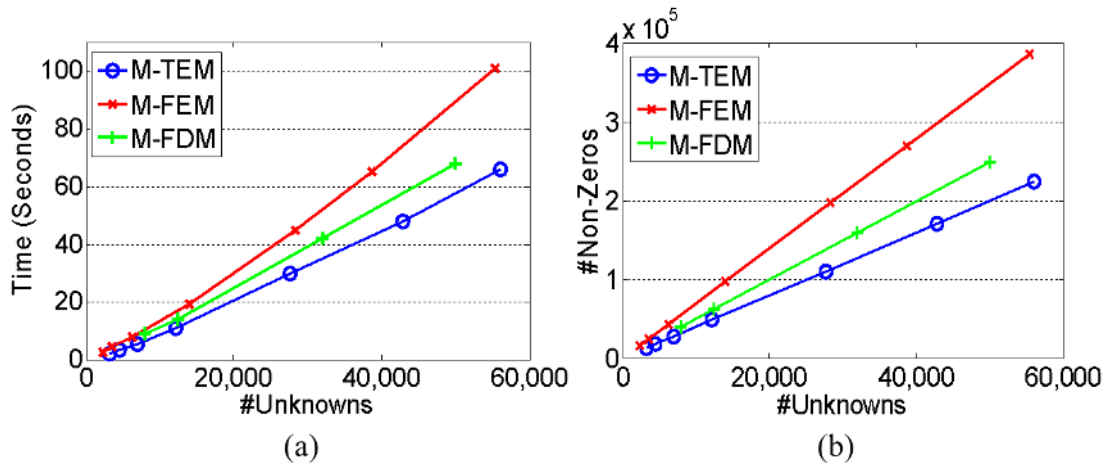
Figure 4.19. (a) Growth of computation time and (b) growth of the number of non-zero entries as the number of unknowns increases.

Memory requirement is proportional to the number of non-zero entries of a system matrix. Figure 4.19 (b) compares the growth of the non-zero entries of each method as the number of unknowns increases. The number of non-zero entries for

MTEM also grows most slowly among the three methods. A similar trend of memory requirement is observed with the increase of the number of layers. Figure 4.20 shows the growth of the number of non-zero entries of each method with respect to the increase of the number of layers. As the number of layers increases, the memory requirement for MTEM grows most slowly, while that of MFEM grows most rapidly.
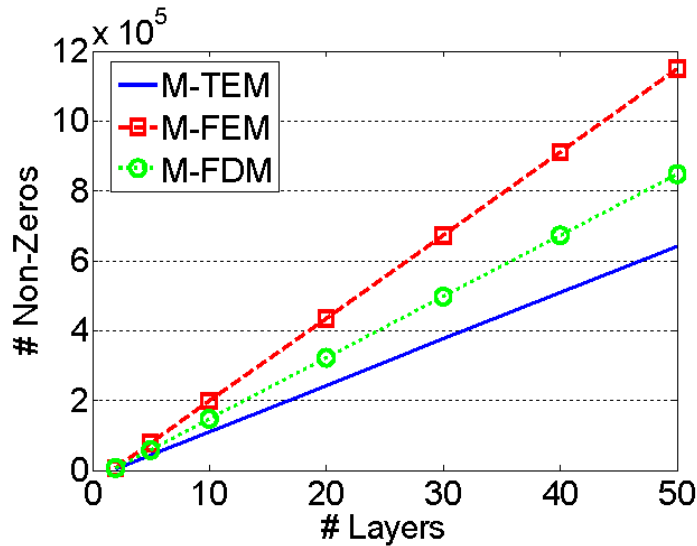
Figure 4.20. Growth of the number of non-zero entries as the number of layers increases.

4.9 Summary

This chapter presented a differential-equation based modeling method that solves for the impedance profile of power and ground planes. The method employs a surface mesh using dual graphs, Delaunay triangulation and a Voronoi diagram, which provide a mutual orthogonality that allows the use of the governing field equations. The use of a non-uniform triangulation enables an efficient discretization of irregular and multi-dimensional geometries, and the resultant system is memory efficient. A single plane-pair model is also extended to multiple plane-pairs by including the mutual coupling between

plane-pairs. The modeling of an aperture is also presented considering all the possible locations in a multiple plane-pairs.

The proposed method was validated by solving a structure consisting of multiple layers of power and ground planes containing apertures, and a good correlation with a 3D full-wave solver was obtained. Computational efficiency was demonstrated by comparing the system matrices of the proposed method and other 2D planar modeling methods.

CHAPTER 5

MODELING OF PORTS

5.1 Port Representations

A port is a point where either the planes are excited or where the response is measured. A *vertical port* is defined as a port with its positive and negative terminals aligned vertically, whereas *non-vertical port* terminals are either horizontally or diagonally aligned. Since the fundamental mode of propagation in a parallel-plate waveguide is a TEM (transverse electromagnetic) mode, a *vertical port* can be used to represent noise source excitation and measurement point for a PDN plane-pair. However, most of the real-world structures can only be measured as a co-planar or *diagonal port*; hence the alignment of port terminals is not necessarily vertical. Consequently, a *vertical port* representation is no longer maintained, if a port is created by following the exact layout of a package or PCB. However, the use of a *non-vertical port* representation in MTEM for multilayer structures creates a modeling artifact due to the plane-pair stacking technique. Hence, this chapter investigates the reason for the artifacts of a *non-vertical port*, and provides an alternative solution that replaces a *non-vertical port* with a *vertical port* by showing that the horizontal excitation of a plane-pair has negligible impact on the plane-pair excitation.

5.1.1 Vertical Port

Figure 5.1 shows a cross-section of a multilayer structure with *L* plane-pairs (*L+1* metal layers). The system equations of the proposed modeling method, MTEM, are,

$$\overline{\overline{Y}}_{NL \times NL} \overline{V}_{NL \times 1} = \overline{I}_{NL \times 1}, \tag{53}$$

where $\overline{\overline{Y}}$ represents the admittance matrix of the total system, $\overline{V}$ the unknown voltages, $\overline{I}$ the current source, L the number of plane-pairs, and N the number of nodes per each plane-pair. To excite a plane-pair created by layer l and $l+1$, a 1A current source can be injected into a port created between node i and $N+i$, which is equivalent to assigning $\overline{I}_i = 1$ and $\overline{I}_{N+i} = -1$. Since the multilayer extension technique presented in Section 4.3 assumes the bottom-most layer to be the voltage reference (zero voltage), exciting a 1A-current at node i represents a port connecting a current source between node i and the bottom-most layer. Similarly, exciting a -1A-current at node $N+i$ creates a current source between node $N+i$ and the bottom-most layer as shown in Figure 5.1 (a). The simultaneous injection of the two currents with opposite phases removes the impact of the two current sources on the layers below layer $l+1$. Therefore, the linear combination of the two current sources can be represented as a single port connecting node i and $N+i$ as shown in Figure 5.1 (b). This equalization remains valid as long as the phase difference is 180° and the port terminals are aligned vertically, and such a port configuration is called a *vertical port* in this paper. The final response of the port can be obtained by subtracting V_{N+i} from V_i.
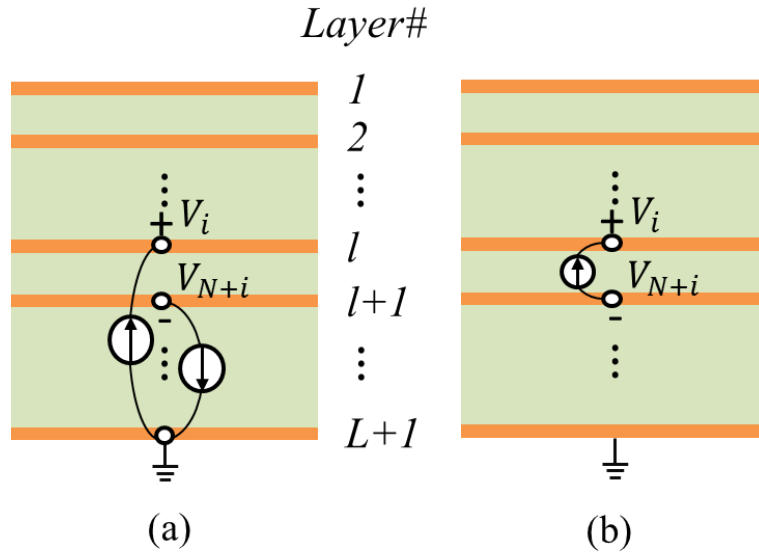
Figure 5.1. Cross-section of a multilayer structure with a vertical port. (a) Excitation of current sources at port terminals and (b) the equivalent source excitation.

5.1.2 Meaning of Horizontal and Diagonal Port

Figure 5.2 shows a driver that draws power from a power and ground plane-pair, which is excited at the discontinuity created by via anti-pads. To model the noise excitation port, a current source can be connected between the nodes on the via pads, node i and $N+k$, where $i{\neq}k$, as shown at the bottom-left in Figure 5.2, and this port configuration is named as a *horizontal port* in this thesis. Assuming via parasitics can be neglected, the via models can be removed and the current source is diagonally connected between the nodes as shown at the bottom-right in the figure, and this port configuration is called a *diagonal port* in this thesis. A *horizontal port* is similar to a *diagonal port* except for the via models, and both can be regarded as *non-vertical port*s as compared to a *vertical port*.

79
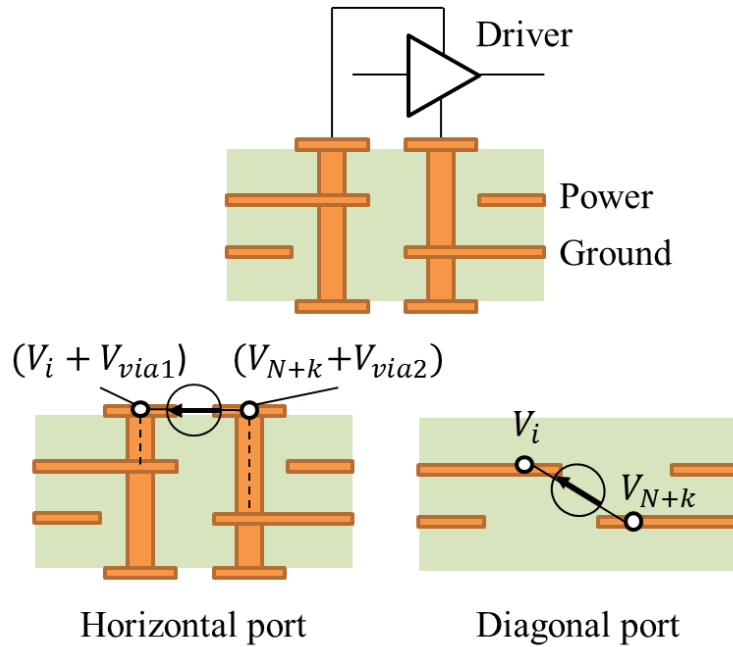
Figure 5.2. Definition of a horizontal and a diagonal port.

Unlike a *vertical port*, the current excitation for a *non-vertical port* requires careful consideration on the voltage reference. Consider the cross-section of a multilayer structure shown in Figure 5.3. Since the driver switching noise excites the plane-pair between layer l and $l+1$, a *diagonal port* can be created between node i and $N+k$, where $i{\neq}k$, as shown in the middle of the figure. To represent a current excitation, 1A and -1A currents are excited at node i and $N+k$, respectively, similar to a *vertical port*, as shown in Figure 6.3 (b). As opposed to the *vertical port* case, the impact of the two out-of-phase current sources on the structure below layer $l+1$ does not disappear for a *non-vertical port*. This modeling artifact arises from the use of the indefinite admittance technique for the multiple plane-pair extension. Consider Equation (45) and (46) for node i and $N+i$. If those nodes are the terminals of a *vertical port*, the excitation current I_i and I_{N+i} are out-of-phase, e.g. 1 and -1. Hence, the equations result in $Y_{B,i}V_{N+i} = 0$ and thus $V_{N+i} = 0$,

which indicates that the voltage below and at layer $l+1$ is zero. However, if node i is the positive terminal of a *non-vertical port*, $I_i=1$ and $I_{N+i}=0$, and the equations result in that $Y_{B,i}V_{N+i}$ is not zero. Although -1-A current is applied to the negative terminal of the *non-vertical port*, node $N+k$, the electric potential at node $N+k$ does not vanish.
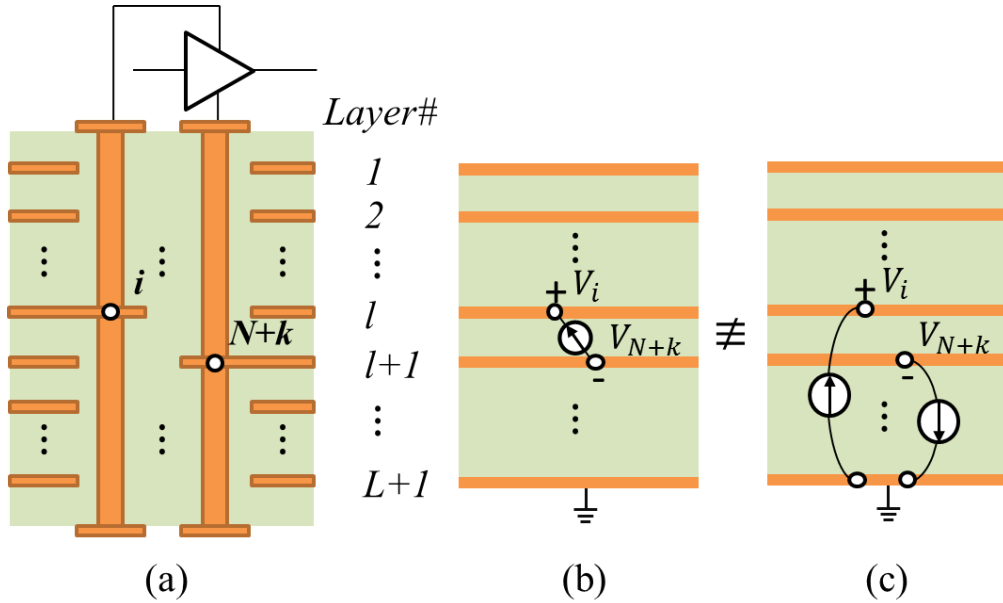
Figure 5.3. (a) Cross-section of a port, and (b) the equivalent port representation. (c) Two current sources vertically connect port terminals and the voltage reference layer.

One possible solution for the *non-vertical port* issue is to replace a *non-vertical port* by creating a *vertical port*. Consider an example of a diagonal port created between a plane-pair as shown in Figure 5.4. The diagonally placed source at (x', z') can be decomposed into its horizontal and vertical components as shown in the figure. The horizontal current source can be expressed as

$$\vec{J}_h(x',z') = \hat{y}J_0\delta(x-x')\delta(z-z'),$$ (54)

whose excitation results in the Helmholtz equation,

$$\left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial z^2} + k^2\right) A_y(x, z; x', z') = -\mu J_0 \delta(\mathrm{x} - \mathrm{x}')\delta(\mathrm{z} - \mathrm{z}'), \qquad (55)$$

where $A_y(x, z; x', z')$ is the vector potential at (x, z) with current excitation at (x', z'), μ the permeability of the insulating material, and δ the Dirac delta function. Since the E-field vanishes at $z = 0$ and d for a perfect electric conductor, the eigenfunctions for the solution of Equation (66) can be chosen as

$$\varphi_m(z) = \sqrt{\frac{2}{d}} \sin\left(\frac{m\pi}{d} z\right). \qquad (56)$$

Finally, Equation (55) can be solved for the vector potential as [60]

$$A_y(x, z; x', z') = \sum_{m=1}^{\infty} \frac{j\mu J_0}{2\zeta_m} \varphi_m(z)\varphi_m(z')\exp(j\zeta_m|x - x'|), \qquad (57)$$

where

$$\zeta_m = \sqrt{k^2 - \left(\frac{m\pi}{d}\right)^2}. \qquad (58)$$
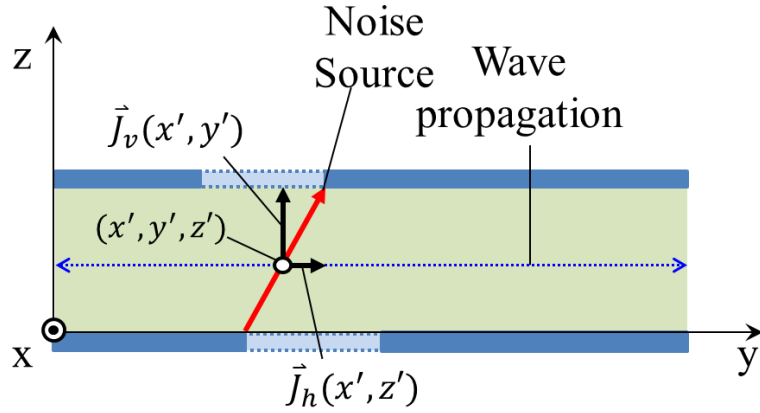
Figure 5.4. Noise source excitation of a diagonal port (red arrow) and generated E-field lines (black arrows).

The vertical component of the current source can be assumed to be sheet current to simplify the problem. The sheet current source at (y', z) can be defined as

$$\vec{J}_v(y', z) = \hat{y} J(z)\delta(y - y'),\tag{59}$$

and the eigenfunctions can be chosen as

$$\varphi_m(z) = \sqrt{\frac{2}{d}} \cos\left(\frac{m\pi}{d}z\right).\tag{60}$$

The resultant vector potential for the vertical current source can be derived as [**60**]

$$A_z(y, z; y') = \sum_{m=0}^{\infty} \frac{j\mu b_m}{2\zeta_m \varepsilon_m} \varphi_m(z) \exp(j\zeta_m |y - y'|),\tag{61}$$

where $b_m = \int_0^d J(z)\,\varphi_m(z)dz$, and $\varepsilon_0 = 2, \varepsilon_1 = \varepsilon_2 = \cdots = 1$.

Notice that for typical PDN geometries and operating frequency used for modern systems, ζ_m in Equation (58) is a very large imaginary value except for when m = 0, which only exists for the vertical component of current source (Equation (61)). For

83

instance, 300-µm FR-4 at the operating frequency of 10 GHz results in the cutoff frequency, f_c=236 GHz, and ζ_1=j1.0463×10⁴. Thus, the propagation constant for the horizontal component of current source in Equation (57) becomes the attenuation constant, leading to a rapidly evanescent wave. On the other hand, the vertical component of current source propagates toward y-direction, since $\zeta_0 = k$. Therefore, the horizontal component of current source does not contribute to the excitation of the plane-pair, and the use of vertical current source suffices for the representation of a diagonal port.

5.1.3   Replacing Non-Vertical Port with Vertical Port

Although the orientation of the source excitation is not critical, the path difference caused by the replacement of a *non-vertical port* with a *vertical port* introduces an approximation error due to path impedance residing between the changed terminals. Consider Figure 5.5 (a) that shows a *diagonal port* and its replacement, a *vertical port*. For the replacement, the negative terminal of the *diagonal port* moves from A to B, and the path impedance associated with the distance between A and B is excluded in the *vertical port* result. Thus, to compensate the impedance difference, the path impedance between A and B can be added to the *vertical port* result. For example, if the obtained voltage result at node i is V_i, the resultant self-impedance at the *vertical port i* can be calculated as

$$Z_{ii} = \frac{V_i}{I_i} + Z_{AB},$$ (62)

where Z_{AB} is the path impedance between A and B. Similarly, Figure 5.5 (b) shows that a *horizontal port* is replaced by a *vertical port*. The excluded path impedance due to the

replacement is equivalent to the series combination of the path impedance between A and B and the impedance of the via parasitic.
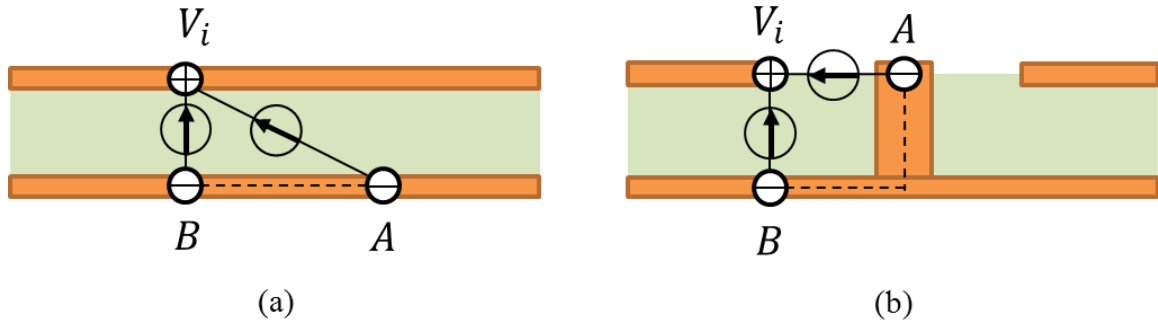
Figure 5.5. Vertical port replaces (a) diagonal and (b) horizontal ports. Dotted lines indicate the path impedance excluded in the vertical port result.

5.1.4 Results

To demonstrate the modeling artifacts created by a *diagonal port*, a multilayer structure is created. Figure 5.6 shows the cross-section of a multilayer structure consisting of four rectangular metal layers with apertures. Power and ground vias are connected to the top and second layer, respectively, exciting the top plane-pair. The structure is simulated with MTEM and CST. For simplicity, the effect of via anti-pads and via-barrels are neglected in both simulations. Thus, the exact port configuration can be represented by a *diagonal port* connecting the positive and negative nodes as shown at the bottom-left of the figure. For comparison, a *vertical port*, shown at the bottom-right of the figure, is also created. The *vertical port* is created at the nearest point from the actual port terminals avoiding via anti-pad regions. In CST, a discrete port component is used to create a *diagonal port* connecting the positive and the negative terminals.
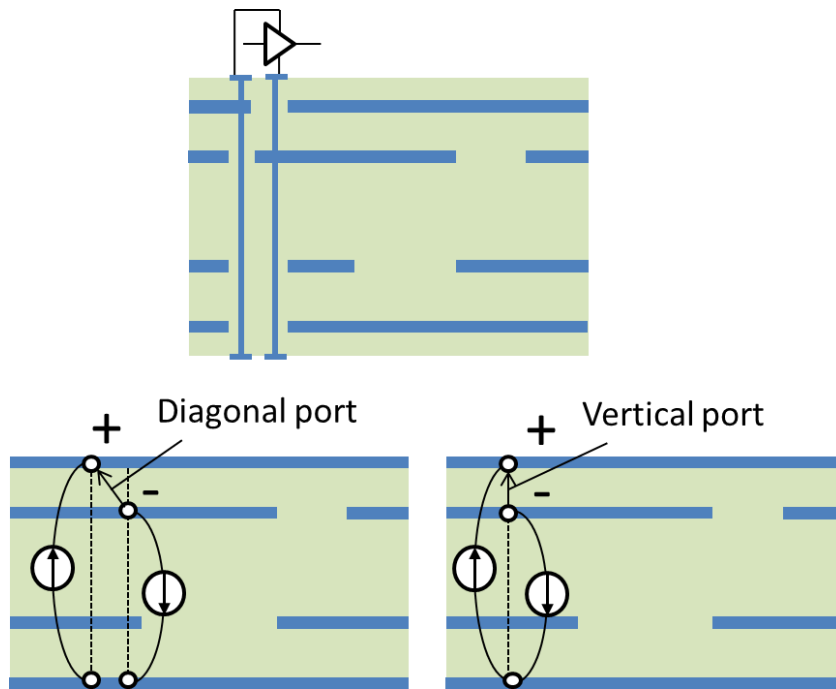
Figure 5.6. Cross-section of four-layer structure (top), and diagonal port (bottom left) and vertical port (bottom right) model.

The distance between the port terminals is 1 mm. The dimensions of the metal layers are 40 mm × 30 mm × 35 µm. The dielectric layers are 300, 700, and 300-µm thick, with the dielectric constant of 4.5 and the loss tangent of 0.02 assumed to be independent of frequency.

The simulated self-impedance curves are shown in Figure 5.7, and the result from MTEM with a *diagonal port* shows much higher impedance along the frequency than that from CST. This excessively high impedance is the artifact of the *diagonal port* model caused by the two independent current sources applied between each port terminal and the bottom-most layer. As a result, the magnitude of the impedance strongly depends on the thickness of the dielectric layers below the port. On the other hand, the *vertical port* result from MTEM shows a good correlation with CST.
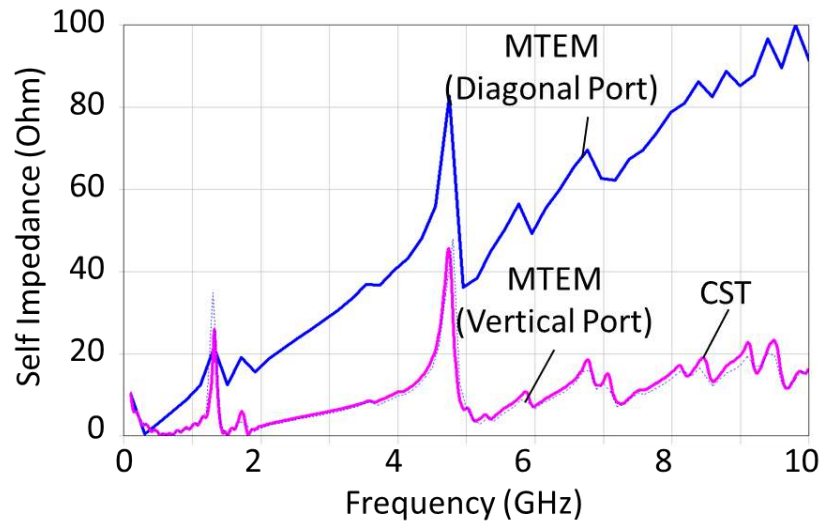
Figure 5.7. Self-impedance results from MTEM and CST with different port configurations.

To observe the effect of the path impedance introduced by the change of port representations, a two-layer structure shown in Figure 5.8 was analyzed using a *horizontal* and a *vertical port*. The structure is composed of 40 × 30 mm planes separated by a 300-µm dielectric, whose relative permittivity is 4.5 with the loss tangent of 0.02. Figure 5.9 compares the self-impedance curves obtained from the 3D full-wave simulations with a *horizontal* and a *vertical port*. The impedance resulted from a *horizontal port* is larger than that from a *vertical port*. Since the conductors are assumed to be lossless, the difference attributes only to the imaginary part of the impedance. Hence, the self-impedance is purely inductive, which can be calculated from the magnitude difference of the impedance curves: The impedance difference at 10 GHz is 4.8 Ω, and the path inductance can be calculated as 77 pH.
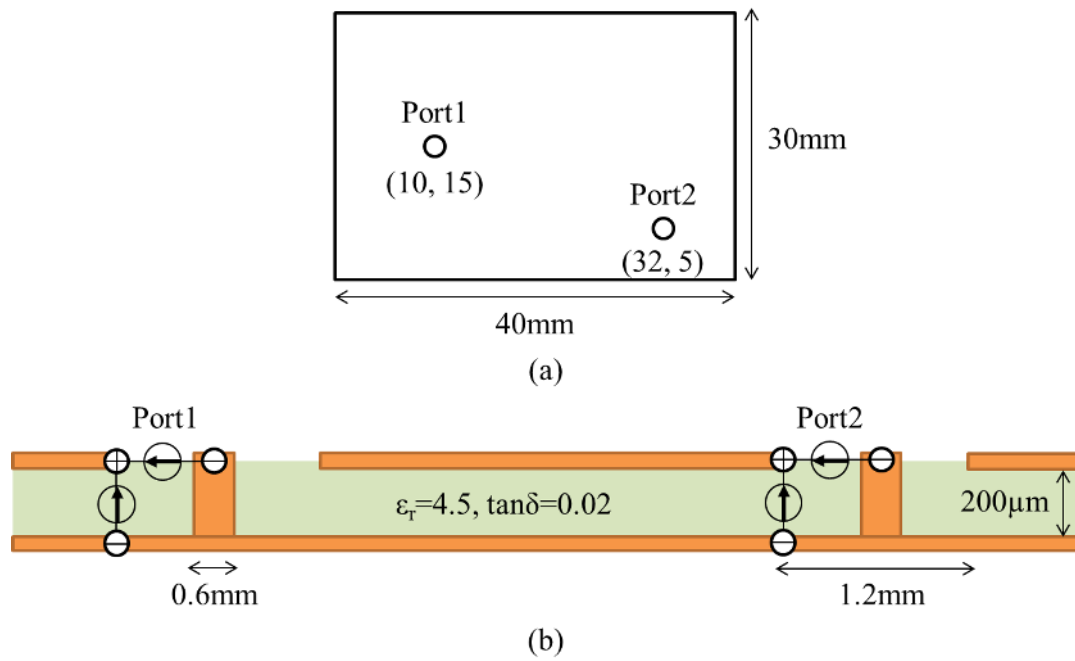
Figure 5.8. (a) Top and (b) cross-sectional view of the structure simulated with a horizontal and a vertical port.
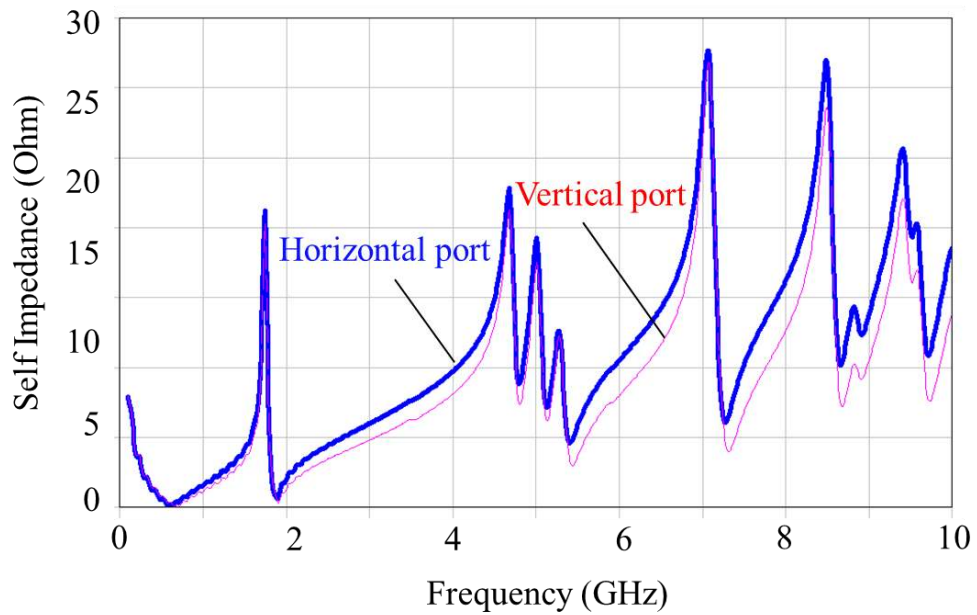
Figure 5.9. Self-impedance results of horizontal and vertical port representations.

Although the use of a *vertical port* results in differences in self-impedance values, such variances do not exist in transfer impedance. Figure 5.10 shows that nearly the same transfer impedances are resulted from both *horizontal* and *vertical port* representations. The sensitivity of self-impedance is addressed in 5.2.
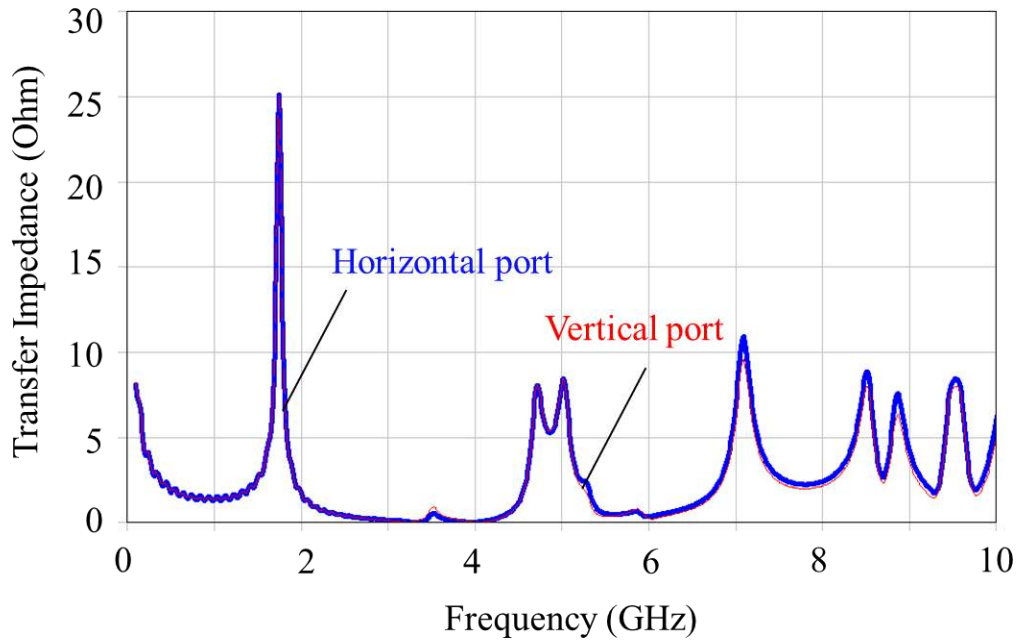
Figure 5.10. Transfer-impedance results of horizontal and vertical port representations.

5.2 Sensitivity of Self-Impedance

Self-impedance is the ratio of the measured voltage to the source current injected into the same port, while transfer impedance is that of the measured voltage at a port to the source current injected into a different port. Differential-equation based methods encounter an issue regarding to the size of the mesh around a port that affects the resultant self-impedance. Consider a plane-pair shown in Figure 5.11. The 300-µm dielectric has the relative permittivity of 4.5, and the loss tangent of 0.02, assumed to be constant along the

frequency. Figure 5.12 shows the self-impedance at port 1 obtained from the simulations

using the multilayer finite difference method (MFDM) [22]. As a mesh size decreases,

resonance frequencies shift to lower frequencies while anti-resonances stay still. The

imaginary part of the self-impedances shown in Figure 5.13 indicates that this mesh size

effect is purely inductive. In addition, creating a finer mesh around the port resulted in

the higher value of the imaginary part of the self-impedance.
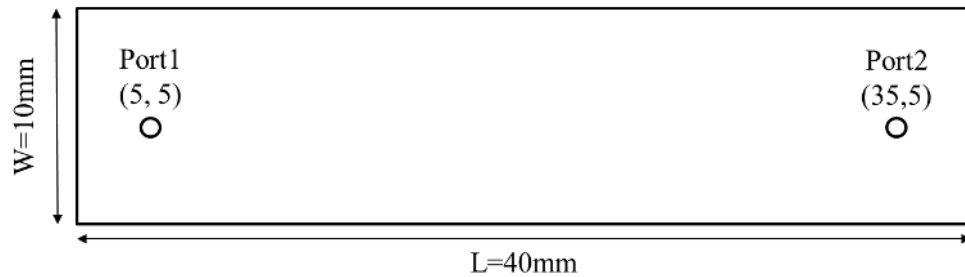
Figure 5.11. Top view of a plane-pair for the sensitivity analysis of the self-impedance.
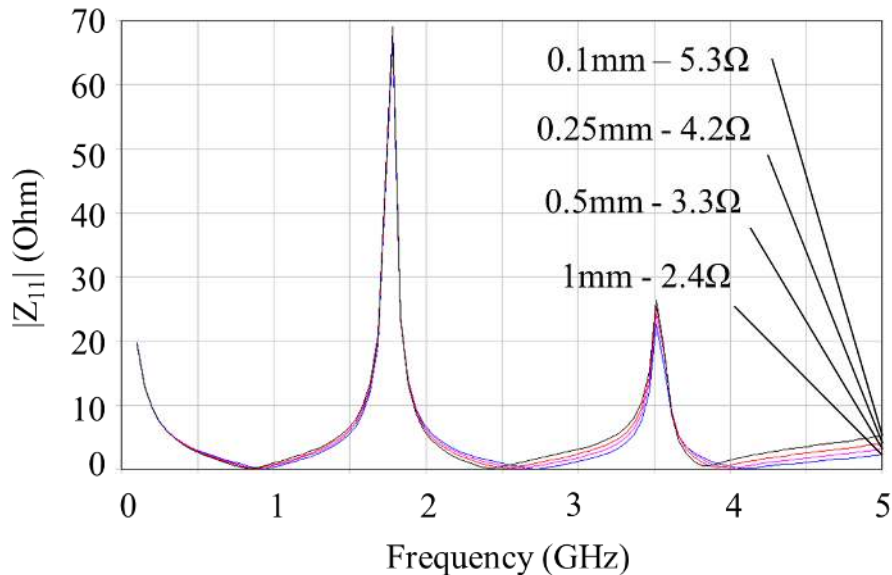
**Figure 5.12. Change of self-impedance along with the different mesh size around a port.
Results are obtained from MFDM simulations.**

90
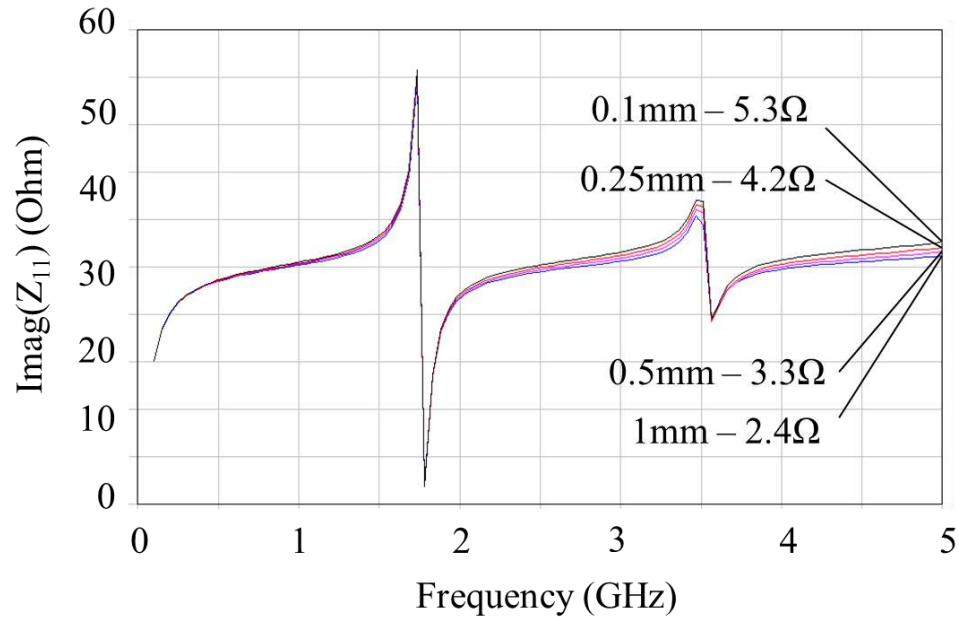
Figure 5.13. Imaginary part of self-impedance.

While self-impedance results show strong dependency on the size of the mesh created around a port, transfer impedance results do not observe the mesh size sensitivity. However, if the distance between two ports approaches to zero, transfer impedance converges to self-impedance, whose value considerably differs along with the mesh size.

In addition to transfer impedance with distant two ports, neither return loss nor insertion loss of S-parameters show strong sensitivity to the mesh size. Of course, these parameters also become sensitive to the mesh size when the operating frequency increases, especially when the mesh size is larger than $\lambda/20$. The change of self- and transfer impedance as well as insertion loss at 5 GHz is summarized in Table 6. For the transfer impedance, port 2 is located at (35, 5) mm.

Table 6. Change of network parameters as mesh size changes.

Mesh Size (mm)	Self-Impedance		Transfer Impedance		Insertion Loss	
	$|Z_{11}|$	% Change	$|Z_{21}|$	% Change	$|S_{11}|$	% Change
1	2.4	-	1.31	-	0.993	-
0.5	3.3	37.5	1.34	2.3	0.992	0.1
0.25	4.2	27.3	1.35	0.75	0.991	0.1
0.1	5.3	26.2	1.36	0.74	0.991	0.0

The impact of the mesh size on the self-impedance is also observed from other simulation tools. CST transient solver [59] is based on the finite difference time domain (FDTD) method, which requires discretization of the calculation field. The different mesh size around a port also results in differences in self-impedance results as shown in Figure 5.14. Similar results can be observed from other discretization-based methods, such as CST frequency domain solver (finite element method) [59], the multilayer finite element method (MFEM) [20] and the multilayer triangular element method (MTEM) (CHAPTER 4).
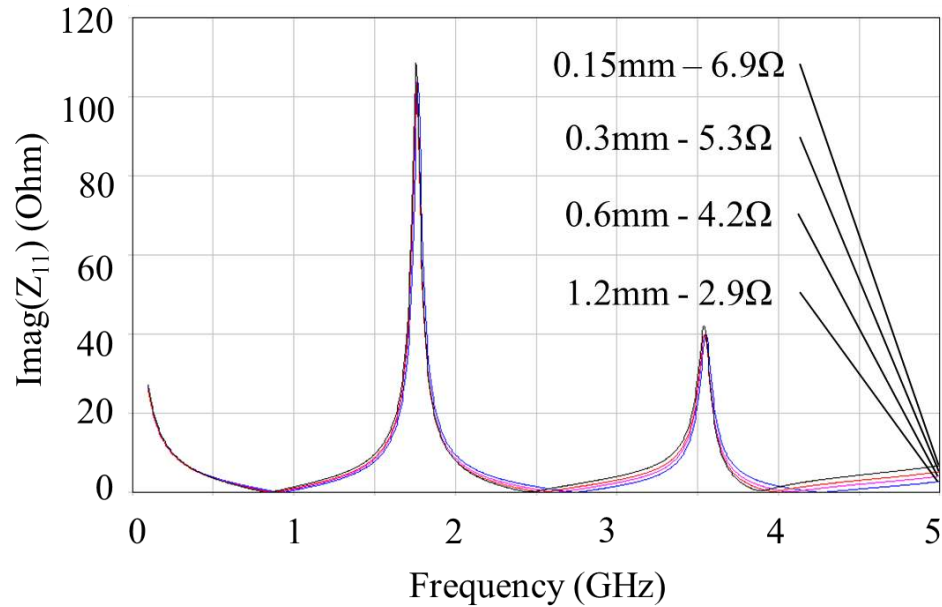
Figure 5.14. Change of self-impedance along with the change of mesh size around a port. Results are obtained from CST transient solver.

The effect of the mesh size around a port indicates that the size of a port is a significant factor that affects the results. The size of a port is an input variable of the cavity resonator model [**10**] [**11**], an analytical modeling method using Green's function. The same structure was simulated using the cavity resonator model by changing port sizes. As shown in Figure 5.15, the resultant self-impedance curves exhibit similar behavior that was observed in the simulations using discretization-based methods. However, self-impedance converges to the result with the port size less than 1 µm. This convergence is valid even at higher frequencies as shown in Figure 5.16.

Although the convergence is observed for this structure, the port size required for the convergence is too small for the efficient mesh creation: 1 µm is only 0.014% of the wavelength at 20 GHz. Thus, a non-uniform mesh scheme is necessary for the discretization-based methods to effectively discretize the area around a port. Otherwise,

93

one of the remedies for the problem of tiny mesh size is to specify a fixed port size, which can be defined as the area within which the current distribution can be assumed to be uniform.
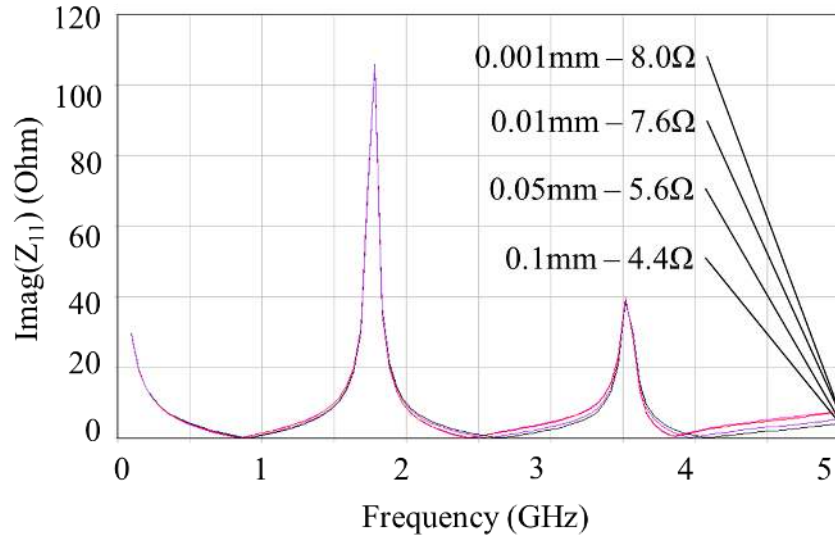
Figure 5.15. Change of self-impedance along with the change of mesh size around a port. Results are obtained from the cavity resonator model.
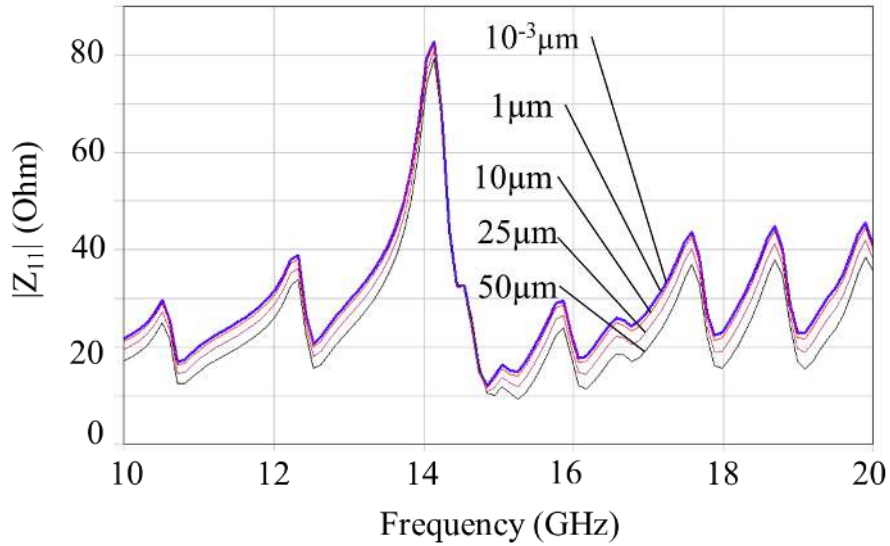
Figure 5.16. Convergence of self-impedance as the port size decreases.

5.3 Summary

Different representations of a port that can be applied to the 2D planar-circuit models were investigated. For the actual representation of the real-world structures, non-vertical alignment of port terminals may be necessary. However, the multilayer extension technique creates modeling artifacts if *non-vertical port*s are used. To mitigate this problem, a *vertical port* can replace a *non-vertical port* without creating discernible modeling errors. The reason was provided by showing the horizontal component of a source current does not propagate inside a parallel-plate waveguide structure up to the cut-off frequency.

Self-impedance results are sensitive to the size of a port. Although the anti-resonance frequencies of self-impedance do not vary with the port size, resonance frequencies and the magnitude of self-impedance shows strong correlation with the port size or the mesh density around the port. Creating a fine mesh around a port can result in more accurate self-impedance results, while sacrificing high computational cost.

CHAPTER 6

MODELING OF RETURN PATH DISCONTINUITIES

6.1 Introduction

When the return path of a signal is not continuous, the return current encounters a large voltage drop, leading to worsening of the signal waveform. In addition, the return current flowing at the discontinuities couples to the power delivery network (PDN) and causes fluctuation of the supply voltage. Since the signal and power integrity is tightly coupled, separated analysis of the signal interconnect and the PDN can result in incorrect results.

In a package and printed circuit board (PCB) PDN environment, return path discontinuities (RPDs) are typically created by split planes, apertures, and vias. For accurate analysis of such various types of RPDs, a thorough understanding of the electromagnetic behavior at the discontinuity is critical. This section presents analysis and quantification of the impact of RPDs on the signal transmission. From the study of the different types of RPDs such as an aperture, split planes, and via transition, the designing and modeling guidelines are provided. The guidelines applied to the signal and power integrity co-simulation can further improve modeling efficiency without loss of accuracy.

6.2 RPD by Split Planes

In the case of a microstrip line crossing a gap created by isolated reference planes, the return current of the microstrip line at the discontinuity switches the layers to complete the closed current loop as illustrated in Figure 6.1. Hence, the reference of the middle

portion of the microstrip line at the gap is the bottom layer (*VDD*) instead of the top layer (*VSS*) of the PDN. Because the characteristic impedance of a microstrip line is proportional to the substrate thickness, the segment of the microstrip line over the gap has higher characteristic impedance than the other segments. The difference between the characteristic impedances results in reflections at the segment boundaries. These reflections are represented as the smooth fluctuation in the insertion loss curve. When the return current of the microstrip line switches layers between the *VSS* and the *VDD* planes, it excites electromagnetic energy into the plane-pair, causing a plane resonance, which is the main cause of power integrity problems. Furthermore, this resonance energy can be coupled back to the microstrip line leading to signal distortion, a signal integrity problem.

To investigate the RPD effects according to the geometric parameters of the gap, the structure in Figure 6.1 was simulated by changing the values of spacing, *L*, and the thickness of the PDN substrate, d_2. The dimensions of the PDN are 40 × 10 mm, d_1 is 0.305 mm, and the width of the microstrip line is 0.51 mm resulting in 50-Ω characteristic impedance. The substrates are homogeneous with a dielectric constant of 4.4 and a loss tangent of 0.02 in the frequency range from 100 MHz to 4 GHz.
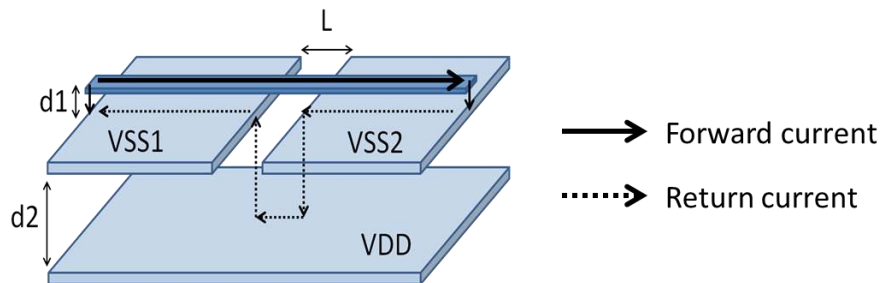
Figure 6.1. Current distribution of a microstrip line crossing split planes.

97

Figure 6.2 (a) shows the insertion loss curves of the microstrip line with the variation of the spacing (*L*). The insertion loss curves show sharp dips at frequencies between 3.5 GHz and 4 GHz, which correspond to the resonant frequencies of the PDN. The slight change in the PDN resonant frequencies is associated with the size change of the *VSS* planes. When the spacing increases from 0.2 mm to 4 mm, the change of the insertion loss is minimal in terms of its shape and the loss level. In contrast, when the substrate thickness (d_2) increases from 0.2 mm to 0.8 mm while the spacing (*L*) is set at 1 mm, the change of the insertion loss is noticeable as shown in Figure 6.2 (b). These results indicate that the amount of the noise coupling from the PDN depends significantly on the impedance of the PDN, which increases as the substrate becomes thicker. However, the opening of the top layer of the PDN only contributes to the small change of the resonance frequency. Therefore, when a microstrip line crosses a gap between the reference planes, maintaining a low noise level of the PDN is most critical.
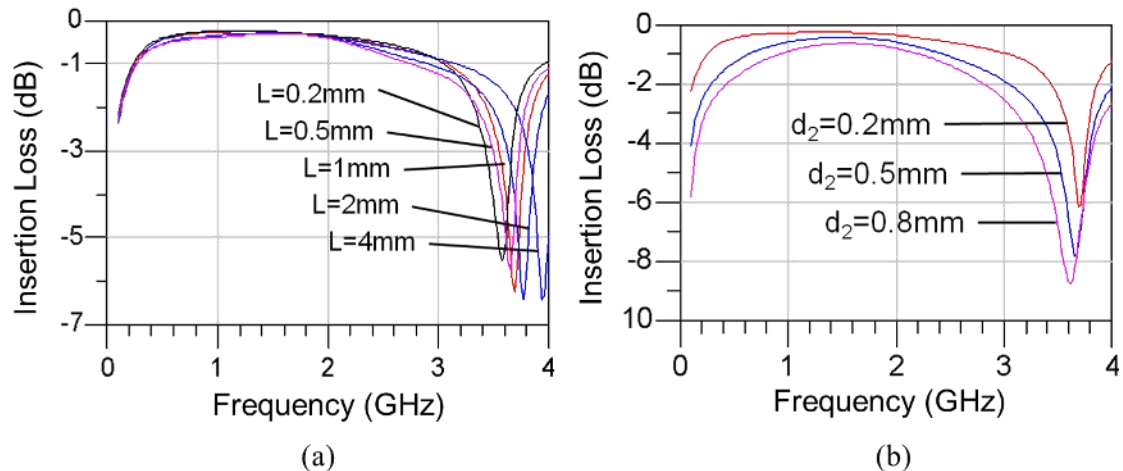
Figure 6.2. Insertion loss curves as (a) the gap spacing and (b) the PDN thickness change.

6.3 RPD by Apertures

The return current behavior of a microstrip line crossing an aperture is more complicated than that of crossing split planes. Consider a microstrip line crossing an aperture created on the top plane as shown in Figure 6.3. The return current of the microstrip line tends to flow along the path of least impedance at the discontinuity. One possible path is to go around the aperture, and the other is to jump down to the *VDD* plane. If the return current flows around the aperture, the signal propagation mode of the microstrip line is similar to a coplanar wave guide with an elevated center conductor; and if the return current flows in the *VDD* plane, the propagation mode of the microstrip line is similar to a microstrip line mode as shown in Figure 6.4. Hence, the mixture of two different modes of propagation forms around the discontinuity.
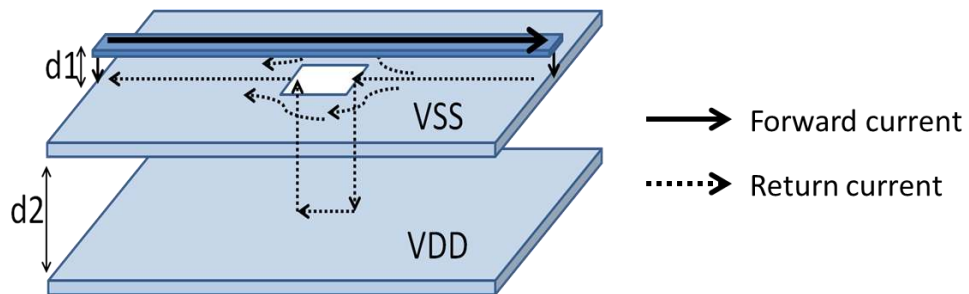
Figure 6.3. Current distribution of a microstrip line crossing an aperture.
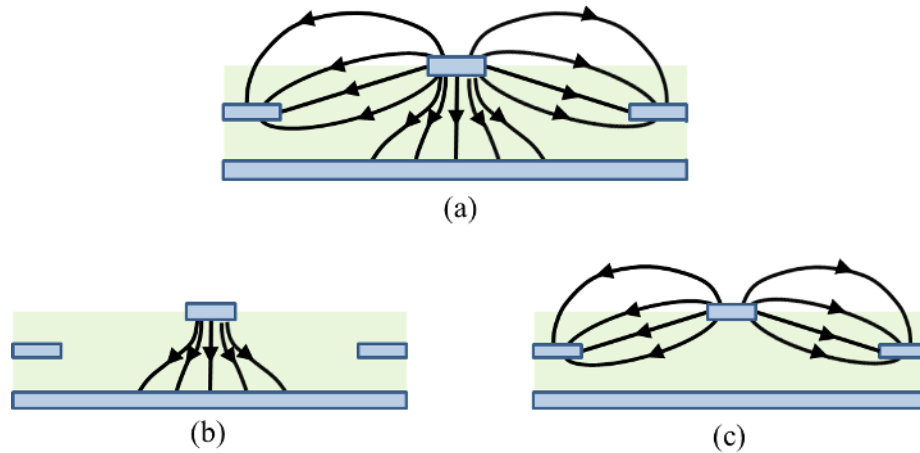
Figure 6.4. (a) E-field distribution at the cross-section of a microstrip line crossing an aperture. The propagation mode can be decomposed into (b) microstrip line and (c) coplanar wave guide mode with an elevated center conductor.

6.3.1 Impact of the Aperture Size on Signal Transmission

The first parametric study is conducted by changing the size of the aperture in Figure 6.3. While maintaining the aperture shape as a square, six steps of simulations change the length of the square edge from 0.5 mm to 6 mm. Figure 6.5 shows the insertion loss curves for each case. As the size of the aperture increases, the insertion loss curve reflects the plane resonances, which appear as sharp dips, at around 1.7 GHz and 3.8 GHz. Additionally, curves gradually show a large but smooth oscillating behavior as the aperture size increases. This large fluctuation is caused by the impedance mismatch at the discontinuity.
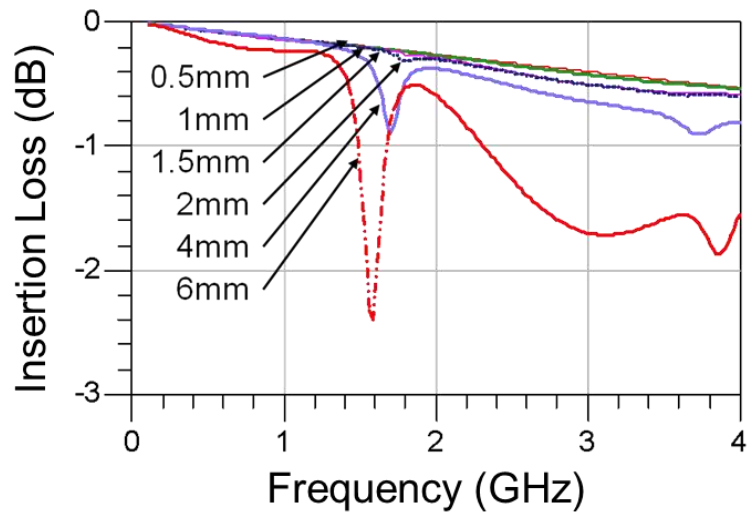
Figure 6.5. Insertion loss changes as the aperture size changes.

While the PDN resonances are coupled to the signal when the aperture is large, very little or no impact of the PDN resonances is observed when the aperture is smaller than 1.5 mm. Because return currents tend to find the path of least impedance, the return currents flow along the edge of the small aperture rather than on the *VDD* layer. For example, when the aperture size is 1 × 1 mm, the distance between the microstrip line and the edges of the aperture is about 0.4 mm, while that between the microstrip line and the *VDD* plane is about 0.54 mm as shown in Figure 6.6. This effect can be seen from the plot of current densities around the aperture shown in Figure 6.7, which shows the top views of the structures with the 1-mm and 6-mm aperture. On the *VDD* layer of the 1-mm aperture (inside the square), the current density is only about 10 A/m, while it is 45 A/m around the aperture (outside the square). On the other hand, the current density on the *VDD* layer of the 6-mm aperture is 42 A/m, while it is only 5 A/m around the aperture.
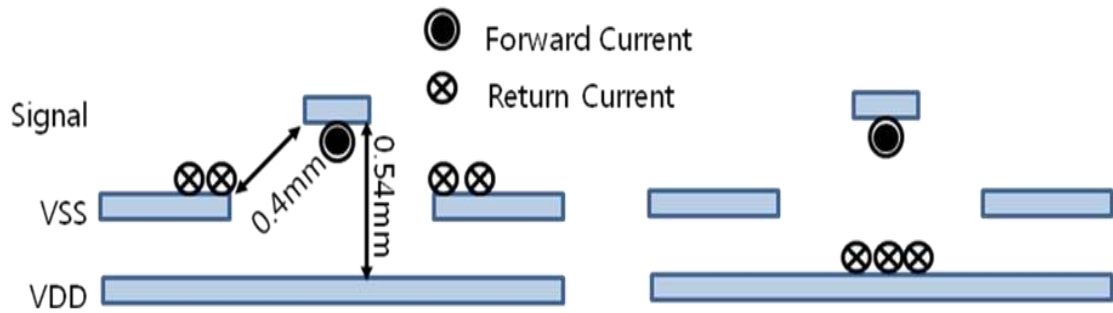
Figure 6.6. Cross-sections of a microstrip line over an aperture. CPW-mode with an elevated center conductor (left) and a parallel-plate mode (right).
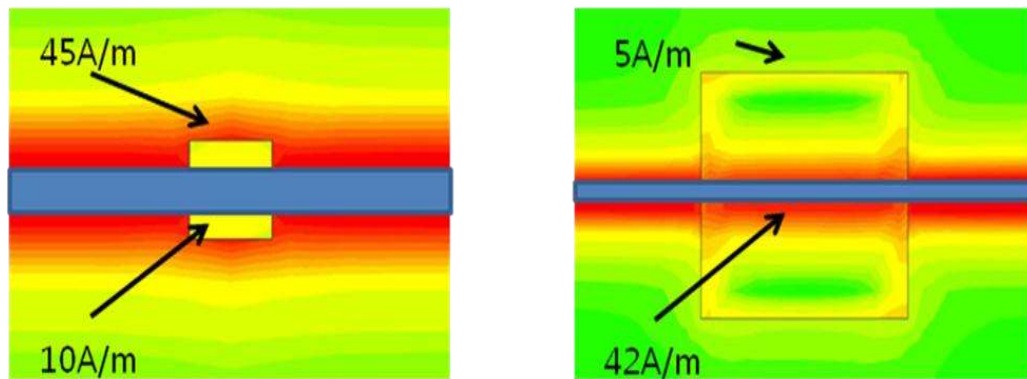
Figure 6.7. Current densities around small and large apertures when a microstrip line transmits a 1-GHz signal.

6.3.2 Impact of PDN Impedance on Signal Transmission

The use of a thicker dielectric in the PDN results in the higher PDN impedance. Since the electric current flows along the path with lower impedance, more return current flows around the aperture instead of the *VDD* layer. Figure 6.8 (b) shows the insertion loss curves of the microstrip line over a 4×4-mm aperture with various thicknesses of the PDN substrate. As the thickness increases and thus the PDN impedance increases, the insertion loss curves exhibit decreasing effect of the PDN resonances. Instead, the microstrip line shows more mismatched behavior by showing larger but smoother

fluctuations along the frequency range. This behavior of the insertion loss curves denotes that the dominant amount of the return path flows around the aperture as the PDN impedance increases.
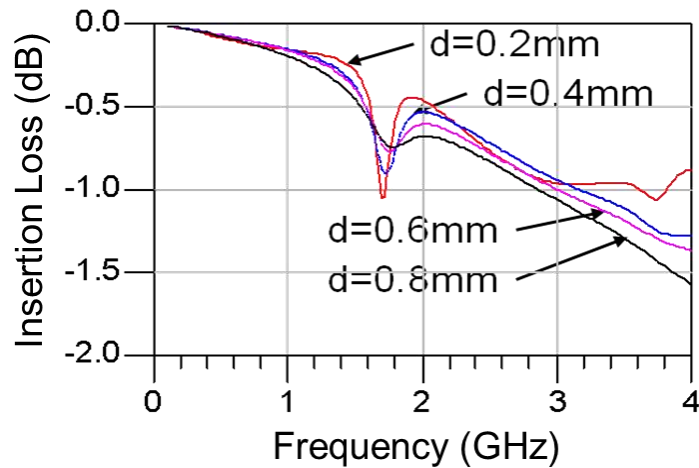
Figure 6.8. Insertion loss changes as the dielectric thickness changes.

6.3.3 Modeling of a Microstrip Line Crossing an Aperture

As discussed in the previous section, the return current of a microstrip line crossing an aperture flows in two different paths: around the aperture and the lower layer of the PDN. The E-field lines formed at the aperture discontinuity are depicted in Figure 6.9 (a). These field lines can be classified as three different propagation modes; a microstrip-line (Figure 6.9 (b)), a parallel-plate (Figure 6.9 (c)), and an elevated-CPW (CPW with an elevated center strip) mode (Figure 6.9 (d)). The parallel-plate mode can be effectively modeled by any PDN modeling method, such as MTEM. The microstrip-line and elevated-CPW modes can be characterized by their characteristic impedance and effective dielectric constants using a 2D-electrostatic solver. The obtained models of the

PDN and the signal interconnects are re-integrated to complete the aperture modeling as depicted in Figure 6.10. Notice that the reference of the mid-segment of the microstrip line and that of the elevated-CPW are not equivalent. The difference of the reference accounts for the divided return path of the microstrip line at the discontinuity which is critical in the modeling of an RPD created by an aperture.
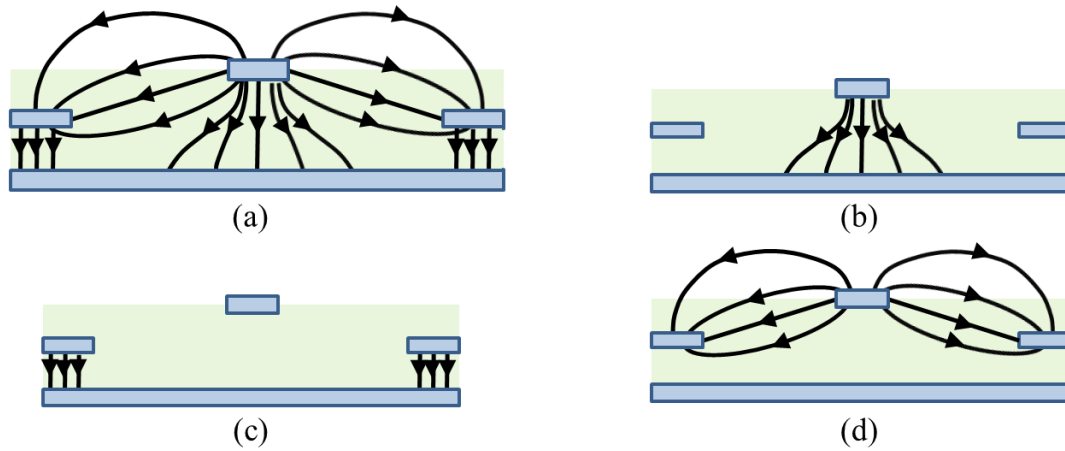
Figure 6.9. (a) E-field lines formed around the RPD created by an aperture. (b)-(d) Decomposed propagation modes.

104
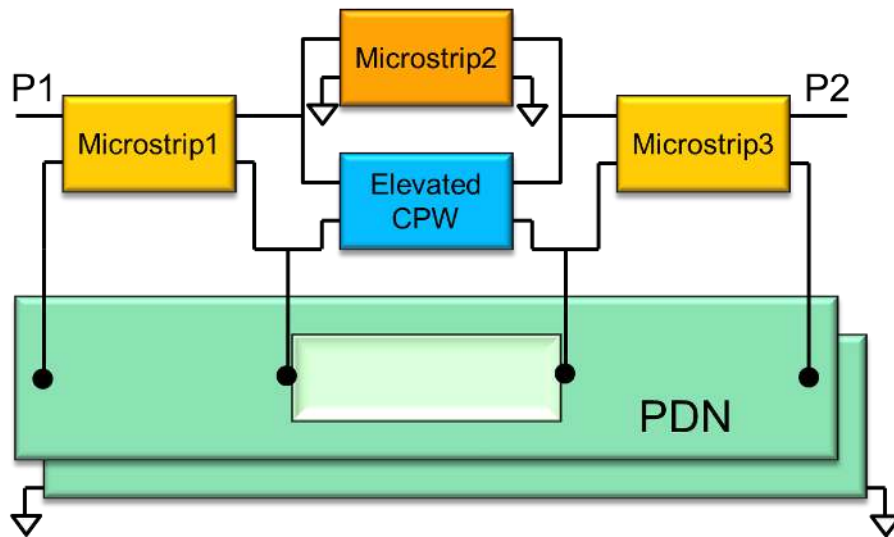
Figure 6.10. Modal decomposition modeling of the microstrip line crossing an aperture.

6.3.4 Small Apertures

A microstrip line crossing a small aperture, for example, via clearance holes, is a common configuration for package and board environment. The level of coupling from PDN resonance to a microstrip line is a function of multiple factors such as size of an aperture, dielectric loss, and a thickness of dielectric layer. As seen from previous sections, the smaller the aperture size and the higher the impedance of a PDN, the lower coupling effect of a PDN is observed in signal propagation.

For typical package and board via environment, the size of via discontinuity is a dominant factor that determines the coupling between PDN resonance and signal propagation. In particular, if the size of an aperture is electrically small, e.g. below an order of wavelength, coupling of the plane resonance through the small aperture can be neglected. The reason can be explained by the return current path of the microstrip line. Consider a microstrip line crossing a small aperture created on the VSS layer shown in Figure 6.11. If s is small or comparable to w, the width of a microstrip line, L_1 is shorter

than L_2. Since current flows through the least impedance path, which is the contour of the small aperture, very little or no current flows on the *VDD* layer as described on the right in Figure 6.11. Thus, the return current of a microstrip line does not excite the plane-pair created by the VSS and VDD planes, and the impact of the small aperture on the microstrip line can be neglected. The relation between the distance L_1 and L_2 can be derived as

$$\sqrt{\left(\frac{d_1}{\lambda}\right)^2 + \frac{1}{4}\left(\frac{s-w}{\lambda}\right)^2} < \frac{d_1 + d_2 + m}{\lambda}, \tag{63}$$

which is normalized by the wavelength. Finally, Equation (63) becomes

$$\sqrt{d_1^2 + \frac{(s-w)^2}{4}} < d_1 + d_2 + m, \tag{64}$$

which is independent of the frequency. The negligible effect of a small aperture is shown with a test vehicle in Section 6.5.2.
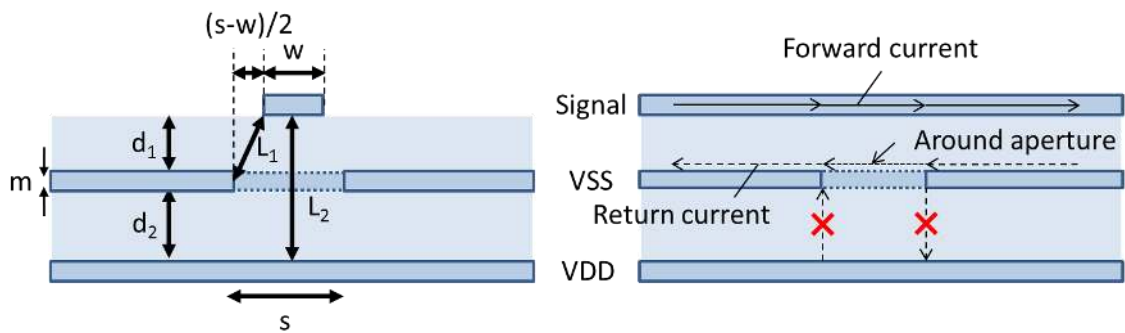
Figure 6.11. Cross-sectional (left) and side view (right) of a microstrip line crossing a small aperture.

6.4 RPD due to Via

In a package or PCB PDN, vias provide a vertical interconnection of signal traces. Consider a via that connects microstrip lines on different layers as shown in Figure 6.12. In order to create a closed current loop between the driver and the load, the return current jumps from the lower plane to the upper plane at the discontinuity. This jump of current, or a displacement current between the plane-pair excites the cavity created by the VDD and VSS planes. Since the impedance of a cavity maximizes at anti-resonance frequencies, the path for the return current becomes highly resistive, resulting in the large insertion loss between the driver and the load. This result also indicates that the vertical transition of signal strongly interacts with the plane-pair, and their interactions must be incorporated in the modeling.
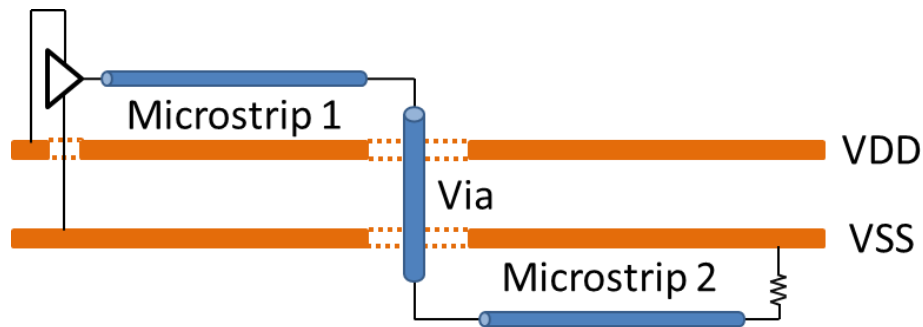
Figure 6.12. Microstrip-via-microstrip transition.

6.4.1   Modeling of a Microstrip-via-microstrip Transition

The modeling of an RPD created at the via can be similarly done using the modal decomposition technique explained in Section 6.3.3. For example, the signal interconnect shown in Figure 6.12 can be decomposed into three segments, one of which is the via and

the others are microstrip lines, as shown in Figure 6.13. The return path of the via is modeled as the plane-pair impedance seen at the via discontinuity; hence, port 2 of the plane-pair and the system reference (VSS) is configured as shown in Figure 6.13. Microstrip line 1 references to VDD plane, and microstrip line 2 to the VSS plane, the system reference.
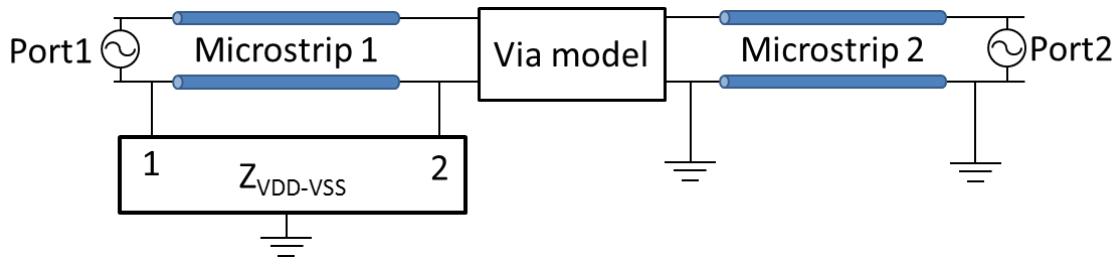
Figure 6.13. Equivalent circuit model for the microstrip-via-microstrip transition.

6.4.2 Coupling Between Via and Power/Ground Plane

A typical model of a via is a PI-model that consists of a series inductance and parallel capacitance as shown in Figure 6.14. Although the value for the inductance, L, can be obtained from [61] [62], the behavior of a via is mainly capacitive and most of the research effort has been devoted to obtain the value of the capacitance [31] [32] [33] [34] [35]. The capacitance represents the amount of coupling between a plane and a via structure, which includes a cylindrical via barrel and a via pad. The authors of [33] presented an analytical solution for the via-plate capacitance that can be incorporated into a physical circuit, such as the model shown in Figure 6.13. Therefore, using the PI-model for the via barrel, and MTEM for the plane-pair, the microstrip-via-microstrip model can be established.
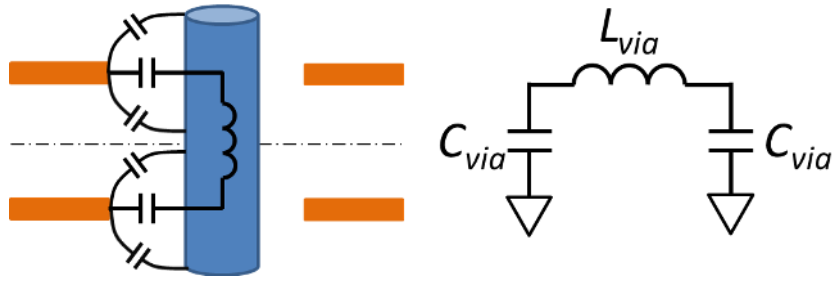
Figure 6.14. Pi-model representation of a plate-through-hole via.

6.5 Test Cases and Results

6.5.1   RPD by Apertures

To validate the modeling for the aperture discontinuity, a test vehicle is designed as shown in Figure 6.15. The dielectric constant of the PDN substrate is 4.7, and the size of the planes is 95 × 10 mm. The size of the rectangular aperture is 30 × 5 mm. The structure can be modeled as shown in Figure 6.10, and the simulation results of the insertion and return loss of the microstrip line show a good correlation with those of measurements as shown in Figure 6.16. Insertion loss curves show large dips at the plane resonance frequencies, which correspond to the peaks in self-impedance of the PDN as shown in Figure 6.16 (c).
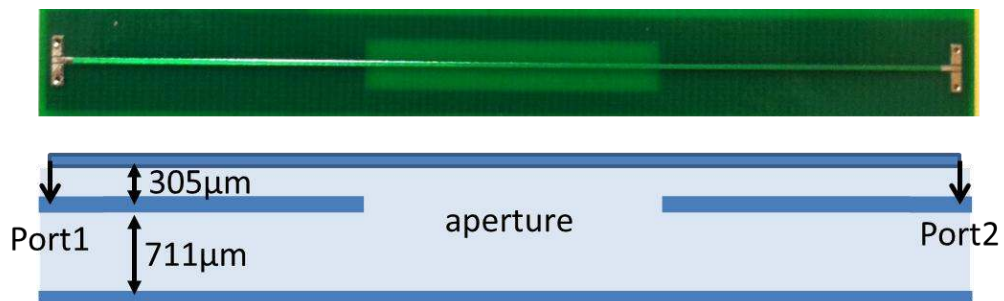
Figure 6.15. A test vehicle of a microstrip line crossing an aperture.
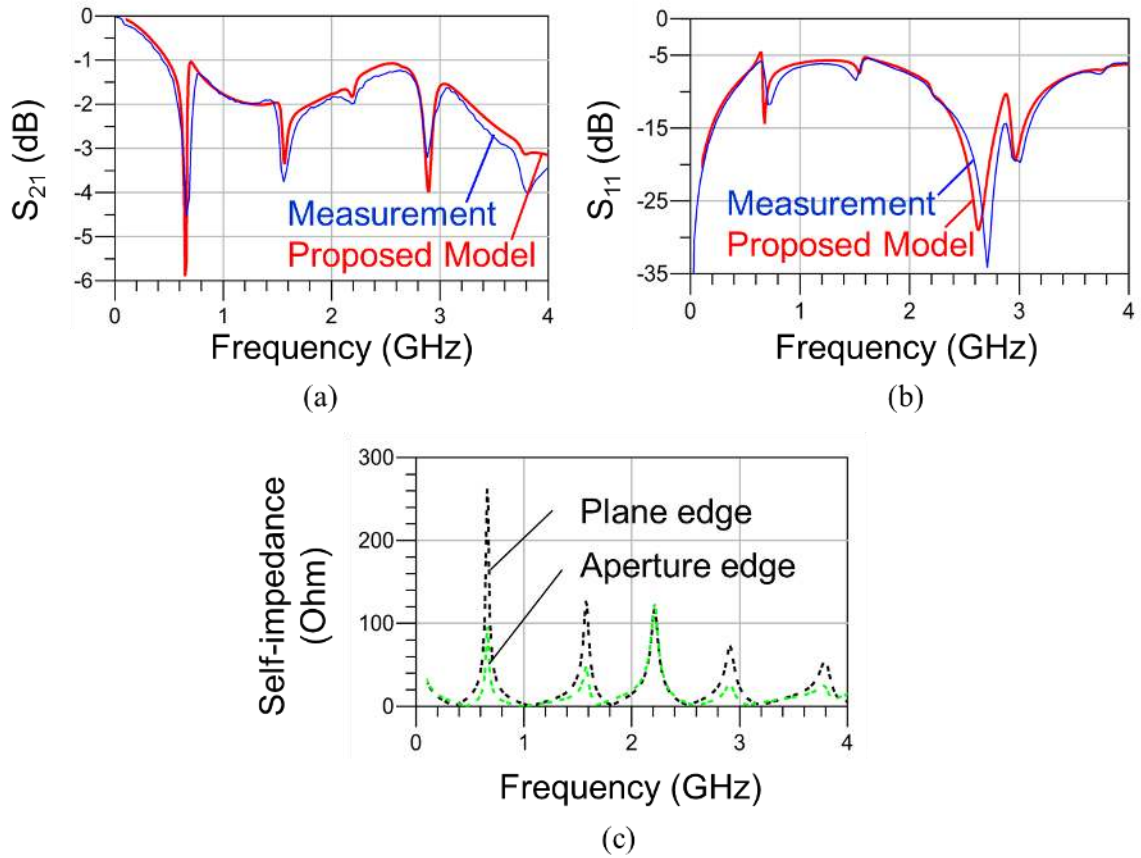
Figure 6.16. (a) Insertion-loss and (b) return-loss responses of the microstrip line. (c) Self-impedance responses at the edge and the middle of the plane.

6.5.2 RPD by Small Apertures

To verify the negligible influence of a small aperture, a test vehicle is designed as shown in Figure 6.17. The dielectric constant of the PDN substrate is 4.7, and the size of the PDN is 95 × 10 mm. A series of ten small apertures of size 0.76 × 0.76 mm are created beneath the microstrip line. Applying the dimensions of the test vehicle to Equation (64), we obtain

$$\sqrt{0.305^2 + \frac{(0.76 - 0.51)^2}{4}} < 0.305 + 0.711 + 0.035, \tag{65}$$

or 0.33<1.05. Hence, the apertures can be classified as *small apertures*, which can be ignored in modeling.
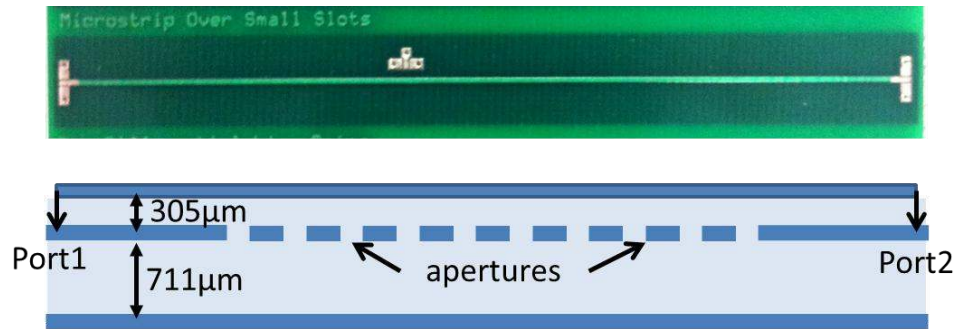
Figure 6.17. Top view of the test vehicle (top) and cross-sectional view (bottom).

The structure is simulated with MTEM and the 3D full-wave solver, and the insertion loss curves show a good correlation with measurement as shown in Figure 6.18. As can be seen from the self-impedance results, PDN resonance is obvious along the frequency range. However, its impact is hardly observed in the insertion loss curve. This result shows that the small apertures do not function as gateways for the coupling of PDN resonance, validating the modeling guidelines for ignoring small apertures.
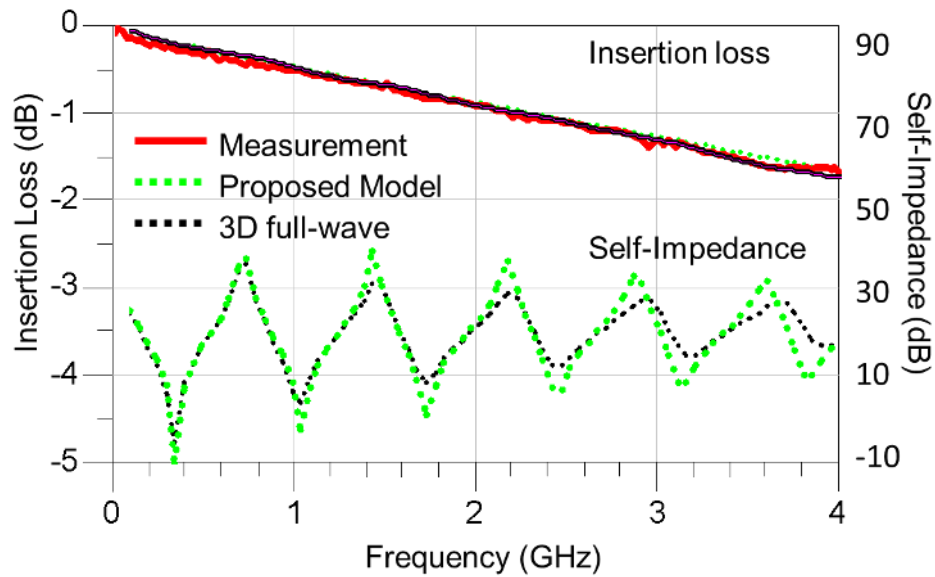
Figure 6.18. Insertion loss and self-impedance curves of the test vehicle with a series of small apertures.

By ignoring the small features in the middle layer, modeling can be significantly simplified, especially because of the decreased number of ports, as compared in Figure 6.19. Moreover, a considerable amount of modeling and simulation efforts can be saved in both the proposed method and the commercial 3D full-wave solver. Each method resulted in an improvement of the simulation time by more than 50%. The modeling using MTEM and the modal decomposition technique resulted in less than 0.1 second of solving time per each frequency point. However, the 3D full-wave solver still spent about 30 seconds per each frequency point even after ignoring the small apertures. One of the reasons is that the 3D full-wave solver yet needs to create a dense mesh for the microstrip line. Table 7 compares the memory consumption of each method. MTEM shows much less memory consumption, while the 3D full-wave solver not only consumed much more memory resources, but also showed less improvement in computational efficiency when the small apertures are removed.
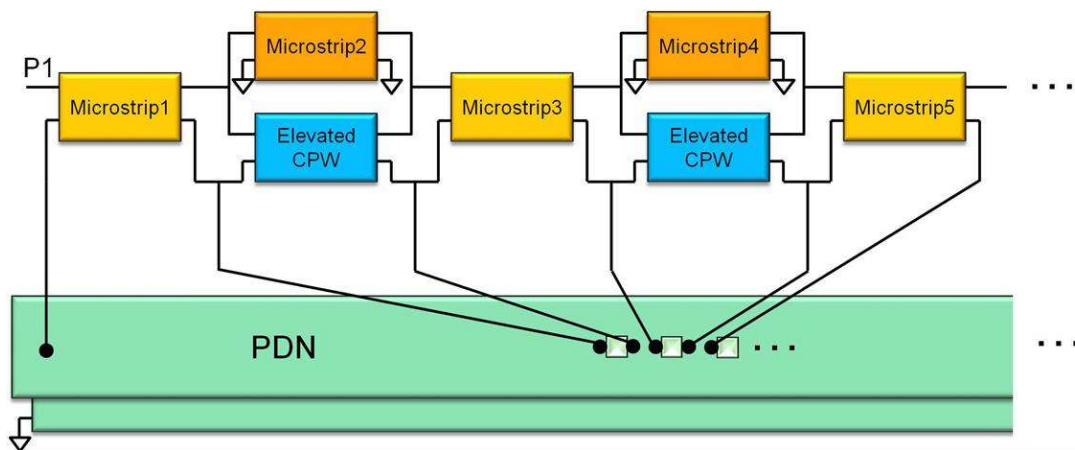
(a)
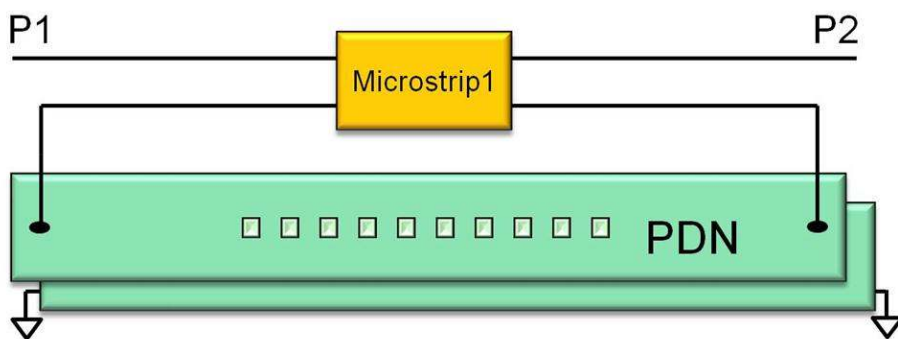
(b)

Figure 6.19. Reduction of modeling complexity by ignoring small apertures. (a) Modeling small apertures. (b) Ignoring small apertures.

Table 7. Comparison of memory consumption (K=10^3).

Methods	# of Unknowns		# of Non-zeros		Improvements
	Before	After	*Before*	*After*	
MTEM	1.3K	0.6K	5K	2.2K	×2.3
3D Full-wave	46K	31K	920K	617K	×1.5

113

6.5.3 RPD due to Via

Figure 6.20 shows an example structure that consists of three metal layers and a microstrip line that transitions from the top layer to the bottom layer through a vertical interconnect. The planes are square with 9.144 edge lengths, and each of the dielectric layers is 305-μm thick. The dielectric constant is 3.5, the loss tangent is 0.02, and both are assumed to be constant along the frequency. Microstrip lines are 1-oz thick and 0.67-mm wide. The radius of the via barrel and the clearance hole are 0.1270 mm and 0.3810 mm, respectively. The via-plate capacitance is obtained using the analytical formula presented in [**33**], and the self-inductance of the via barrel is obtained using a closed form for a cylindrical wire at high frequency given as follows [**63**]:

$$L_{via} = 2l \ln\left(\frac{4l}{d} - 1\right) \ [nH],$$ (66)

where *l* and *d* respectively denote the length and the diameter of the via in centimeter.
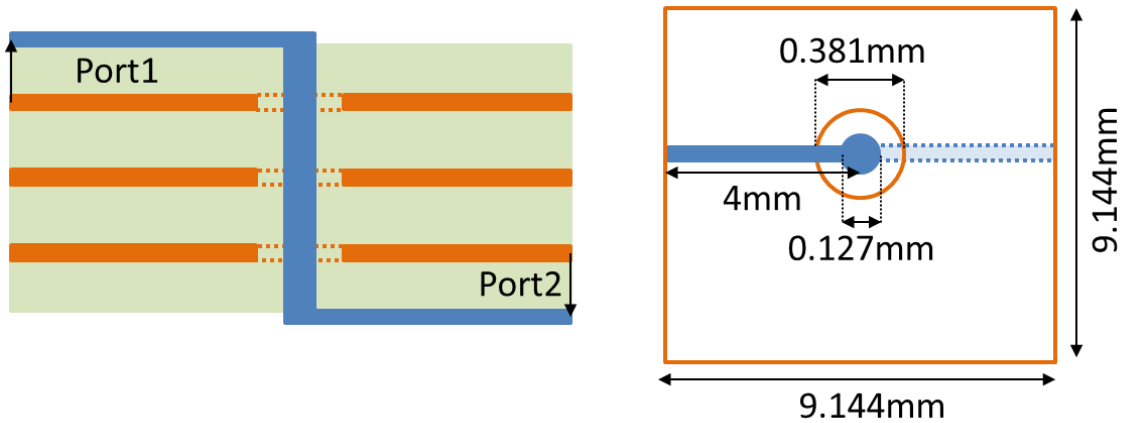
Figure 6.20. Example of a microstrip-via-microstrip transition.

Combining the established via model with the plane-pair impedance profile calculated by MTEM, the insertion loss curve is obtained. For comparison, the result from the same model but without the via model is also plotted. The simulation results of the models with and without the via model are compared with that of the 3D full-wave simulation as shown in Figure 6.21 and Figure 6.22. The insertion loss results show a good correlation, and the removal of the via model does not lose accuracy up to 10 GHz, where the length of the via is one wavelength. Since the calculated value of the via-plate coupling capacitance is only about tens of femto-farads and the combined capacitance is still below hundreds of femto-farads, their impact on the signal transmission is insignificant.
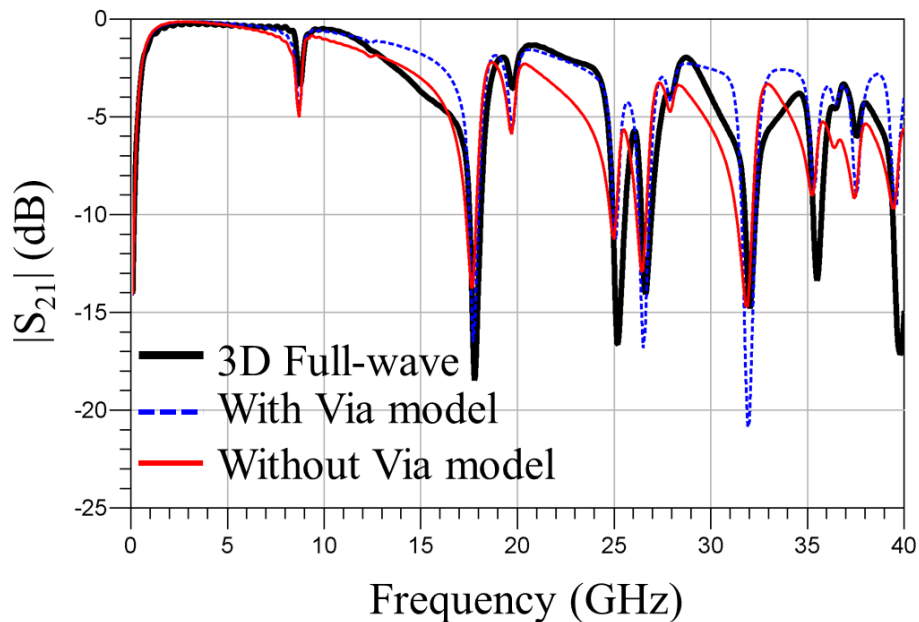
Figure 6.21. Magnitude of the insertion loss of a microstrip-via-microstrip transition.
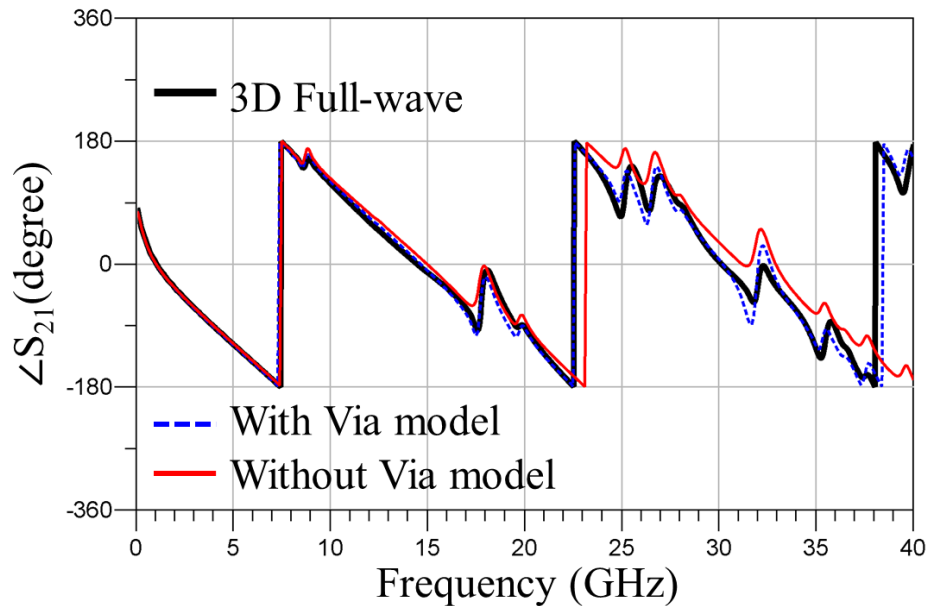
Figure 6.22. Phase of the insertion loss of a microstrip-via-microstrip transition.

The negligible impact of the via-plate capacitance is more obvious in a shorter via structure. Figure 6.23 and Figure 6.24 show the magnitude and phase of insertion loss curves of a microstrip-via-microstrip structure with a short via (length=0.9144 mm) plated through a plane-pair. The difference between the result with and without the via model is indiscernible up to 18 GHz, where the wavelength corresponds to the length of the short via. Therefore, the impact of the coupling between an electrically short via and a plane-pair on the signal transmission is not very critical. By ignoring the unnecessary modeling of the coupling between a short via and a plane, modeling effort for the inductance and capacitance calculations can be saved.
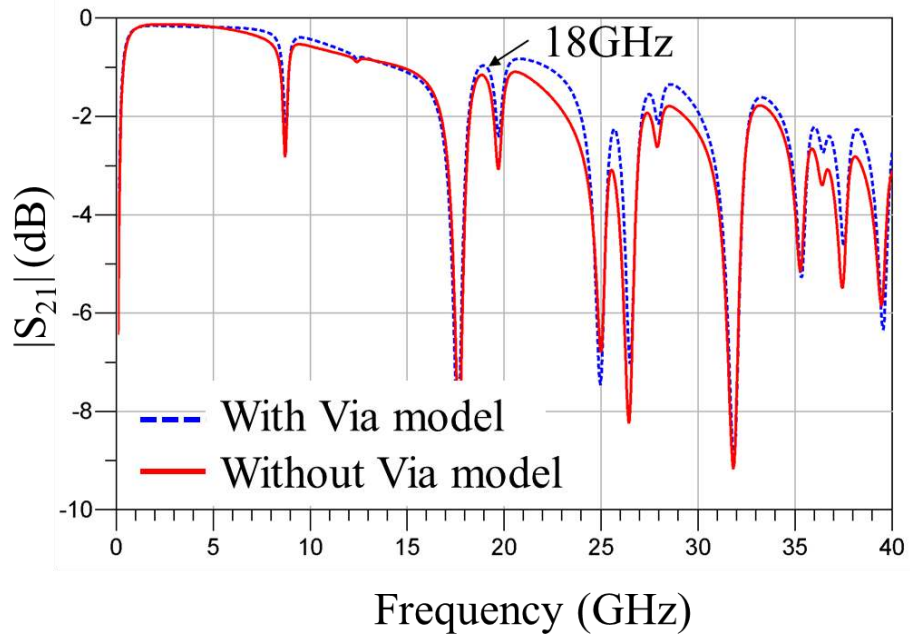
Figure 6.23. Magnitude of the insertion loss of the structure with a short via.
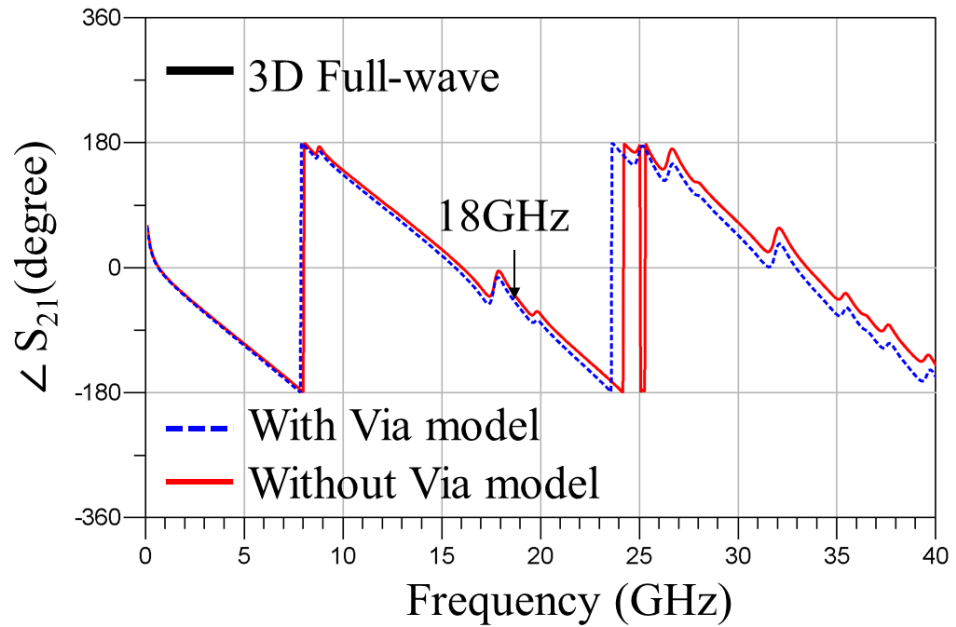
Figure 6.24. Phase of the insertion loss of the structure with a short via.

6.6 Summary

Different types of the RPDs have been presented and categorized along with theoretical and numerical analyses and measurements. RPDs that were shown in this chapter include split planes, apertures, and vias. The various sizes and configurations of RPDs showed different impacts on the signal quality.

The gap distance between separated planes does not significantly affect the amount of the coupling between a PDN and a signal trace that crosses the split. On the other hand, the size of an aperture is a dominant factor that affects the coupling of the signal and power nets. Hence, the difference between the RPDs created by split planes and apertures were differentiated, and the modeling technique for the RPD created by an aperture was explained. In addition, simulation and measurement results showed that small apertures do not function as a gateway of the energy coupling between two domains. Hence, the criteria for a small aperture were obtained, and they can be removed in the RPD model to simplify modeling.

An RPD can be created at the vertical interconnection of signal traces using a via. The discontinuity of the return path is created by the via anti-pad, and the return current jumps from a plane to another, since the via barrel is electrically coupled to the plane-pair at the discontinuity by means of capacitive coupling. The coupling capacitance was obtained from analytical solutions and applied to the co-simulation model using MTEM. The results from the co-simulation model showed good correlation with those from the 3D full-wave solver. To further improve the simulation speed and the modeling complexity, the capacitive coupling between planes and short vias can be neglected.

CHAPTER 7

PLANE-PAIR MODELING WITH ABOSORBING BOUNDARY CONDITION

7.1 Introduction

A plane-pair that supports the propagation of the parallel-plate waveguide mode assumes that fields are zero outside the edges of the metal planes. Thus, the open-circuit boundary condition satisfies the fields at the boundary for planar-circuit modeling methods such as the multilayer finite difference method (MFDM), the multilayer finite element method (MFEM), and the multilayer triangular element method (MTEM). Because of the open-circuit boundary, radial waves propagating between power and ground planes are totally reflected from the edges of the plane-pair. The reflected waves travel back into the plane-pair, and standing waves are formed at the resonance frequencies. Since the resonance of power/ground planes creates many problems such as the increase of power delivery network (PDN) impedance and edge radiation, the reduction or removal of the resonances is a significant practice in signal and power integrity engineering.

Many efforts have been devoted to develop techniques that reduce or remove the plane resonance. Since plane resonance can be damped by reducing the Q-factor of a plane-pair, a conductive layer can be used for the dielectric layer [64], or power and ground planes can be coated with magnetic material [65]. The use of a thin laminated dielectric can also decrease the Q-factor [66].

Decoupling capacitors are the most popular and conventional method of damping plane resonance. In particular, the use of discrete bypass capacitors with high equivalent

119

series resistance (ESR) can effectively reduce resonance peaks as mentioned in many papers [67] [68] [69] [70].

Instead of minimizing the existing plane resonance, the reflection of outward wave can be suppressed at the boundaries of the plane-pair. Novak [71] introduced dissipated edge termination technique by placing series resistors and capacitors along the plane boundaries. Chang [72] proposed a termination technique using external resistance loads. Adsure, Kroger, and Shi [73] presented the edge termination technique placing lossy magnetic material around plane-pair boundaries.

To evaluate the effect of resonance-free plane-pairs, the boundary condition for planar-circuit modeling methods needs to provide the absorbing property. Since the conventional boundary condition for a planar-circuit model is an open-circuit or a short-circuit boundary condition, which exhibits total reflection of the wave, an absorbing boundary condition (ABC) needs to be applied for the representation of resonance-free planar circuits. The application of the 1st order ABC to MTEM is presented in the following section.

7.2 Absorbing Boundary Condition for MTEM

7.2.1 Open-Circuit Boundary Condition

The open-circuit boundary condition can be represented in the form of Neumann boundary condition,

$$\frac{\partial \phi}{\partial n} = 0, \tag{67}$$

where *n* is the direction normal to the plane-pair boundary. The representation of the open-circuit boundary condition (67) for a planar-circuit model can be naturally satisfied by removing nodes outside the calculation domain. For example, consider a unit-cell for MTEM at the plane boundary as shown in Figure 7.1. The MTEM equation for node *i* is

$$j\omega\epsilon\frac{V_i}{d}A_i + \frac{1}{j\omega\mu d}\sum_{k=1}^{2}\left\{(V_i - V_k)\frac{l_k}{h_{ik}}\right\} + \frac{1}{j\omega\mu d}(V_i - V_b)\frac{l_b}{h_{ib}} = 0, \qquad (68)$$

where *d* denotes the dielectric thickness. Since the open-circuit boundary condition (67) suggests the voltage difference between node *i* and *b*, $(V_i - V_b)/h_{ib}$, be zero, node *b* needs to be removed from Equation (68). Hence, the open-circuit boundary condition for a planar-circuit model is equivalent to the omission of the nodes outside the calculation domain, which is a metal plane.
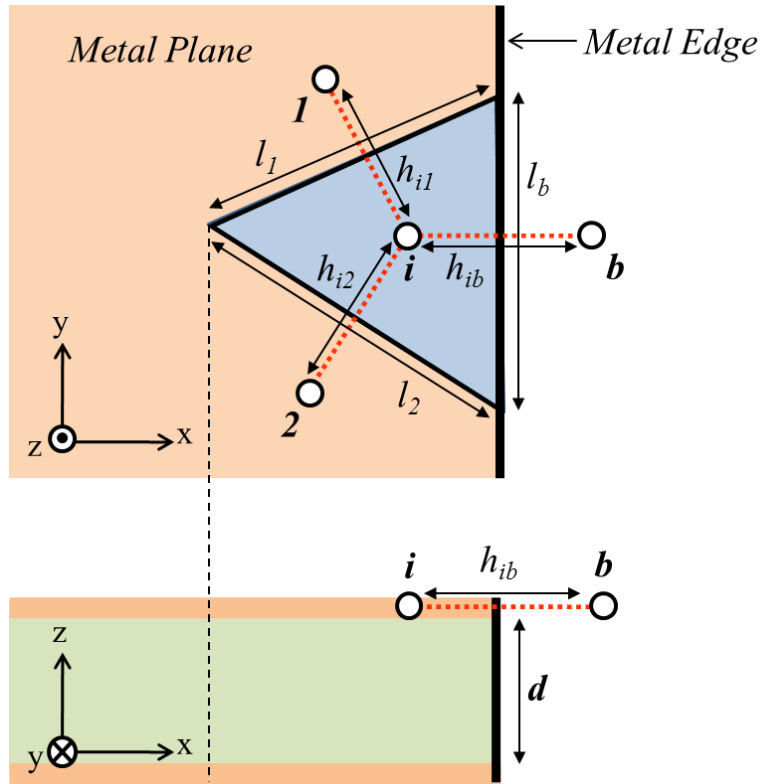
Figure 7.1. Top and cross-sectional view of a unit-triangle located at the boundary of a plane-pair.

7.2.2   1st Order Absorbing Boundary Condition for MTEM

A simple representation of an absorbing boundary is the 1st order ABC, first proposed by Engquist and Majda [**74**],

$$\frac{\partial \phi}{\partial n} = jk\phi, \tag{69}$$

where *n* denote the direction normal to the plane-pair boundary. To apply the 1st order ABC to MTEM, consider Equation (68), which is the MTEM equation for node *i* shown in Figure 7.1. The 1st order ABC at the boundary can be represented as

$$\frac{\partial V_i}{\partial n} - jkV_i = 0, \tag{70}$$

where n is the direction normal to the boundary. Taking forward difference,

$$\frac{\partial V_i}{\partial n} = \frac{V_i - V_b}{h_{ib}}, \tag{71}$$

and the third term in Equation (68) can be represented as

$$\frac{1}{j\omega\mu d}(V_i - V_b)\frac{l_b}{h_{ib}} = \frac{l_b}{j\omega\mu d}(jkV_i). \tag{72}$$

Therefore, the MTEM equation for node i, is

$$\left(j\omega\epsilon\frac{A_i}{d} + \frac{kl_b}{\omega\mu d}\right)V_i + \frac{1}{j\omega\mu d}\sum_{k=1}^{2}\left\{(V_i - V_k)\frac{l_k}{h_{ik}}\right\} = 0, \tag{73}$$

which is in the form of

$$(j\omega C_i + G_i)V_i + \frac{V_i - V_1}{j\omega L_{i1}} + \frac{V_i - V_2}{j\omega L_{i2}} = 0, \tag{74}$$

where

$$G_i = \frac{kl_b}{\omega\mu d} = \frac{l_b}{d}\sqrt{\frac{\epsilon}{\mu}}. \tag{75}$$

Consequently, the application of the 1st order ABC to MTEM is equivalent to the addition of the conductance at the boundary cell.

7.2.3 ABC for One-Dimensional Structure

To validate the 1st order ABC applied to MTEM, a one-dimensional plane-pair is created as shown in Figure 7.2. The lossless dielectric layer is 200-µm thick, and its relative permittivity is 4.5. Since one of the dimensions is much shorter than the other, the first

few resonances are associated with the longer dimension, 'x.' Thus, applying the 1st order ABC only to the left and right edges of the plane-pair can eliminate the first few resonances of the structure.
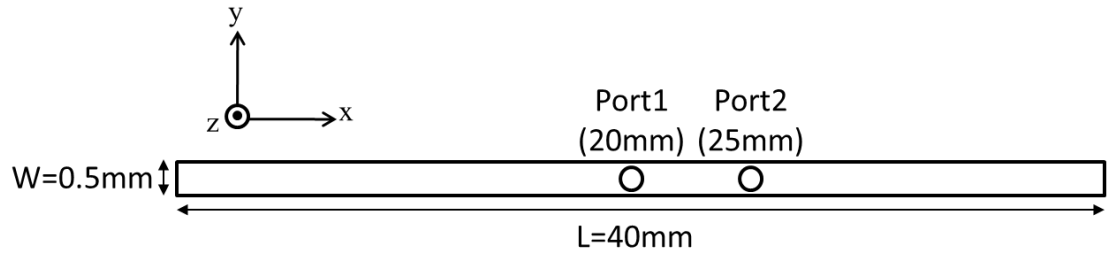
Figure 7.2. Top view of a plane-pair with narrow left and right sides.

Due to the simplicity of the one-dimensional behavior, the impedance between port 1 and 2 can be analytically calculated. The example structure can be modeled as a series connection of three portions of transmission lines with the characteristic impedance, Z_0, as shown in Figure 7.3. The conductance elements, G, at the boundaries represent the 1st order ABC applied to MTEM as explained in the previous section. Notice that the added impedance (1/G) is equivalent to the characteristic impedance (Z_0) of a parallel-plate waveguide, or

$$Z_0 = \frac{1}{G} = \frac{d}{W}\sqrt{\frac{\mu}{\varepsilon}}. \tag{76}$$

Since the transfer impedance between port 1 and 2 is defined as

$$Z_{21} = \frac{V_2}{I_1}, \tag{77}$$

when port 2 is open, V_2 needs to be known. Since half of the source current at port 1 travels to port 2 with only a phase difference of $-jkL_2$, the voltage at port 2 can be defined as

$$V_2 = \left(\frac{1}{2}I_1 e^{-jkL_2}\right) Z_{in}, \tag{78}$$

where

$$Z_{in} = Z_0 = \frac{1}{G}. \tag{79}$$

Consequently,

$$Z_{21} = \frac{\left(\frac{1}{2}I_1 e^{-jkL2}\right) Z_{in}}{I_1} = \frac{Z_0}{2} e^{-jkL_2}. \tag{80}$$
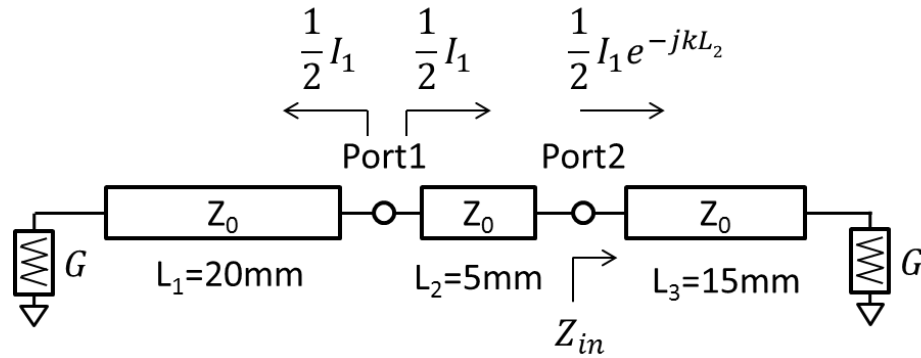
Figure 7.3. Electrical model of the narrow plane-pair shown in Figure 7.2.

Figure 7.4 shows the real and imaginary part of the transfer impedance obtained from MTEM and Equation (80), and a good correlation is observed. Figure 7.5 shows the magnitude of the transfer impedance with a small discrepancy observed. The discrepancy can be reduced by creating a finer mesh at the boundary cells. For this example, creating

125

finer meshes by decreasing triangle edge lengths from 0.25 mm to 0.1 mm reduced the

percentage error from 0.9 to 0.3.

(a) MTEM   (b) Analytical Solution
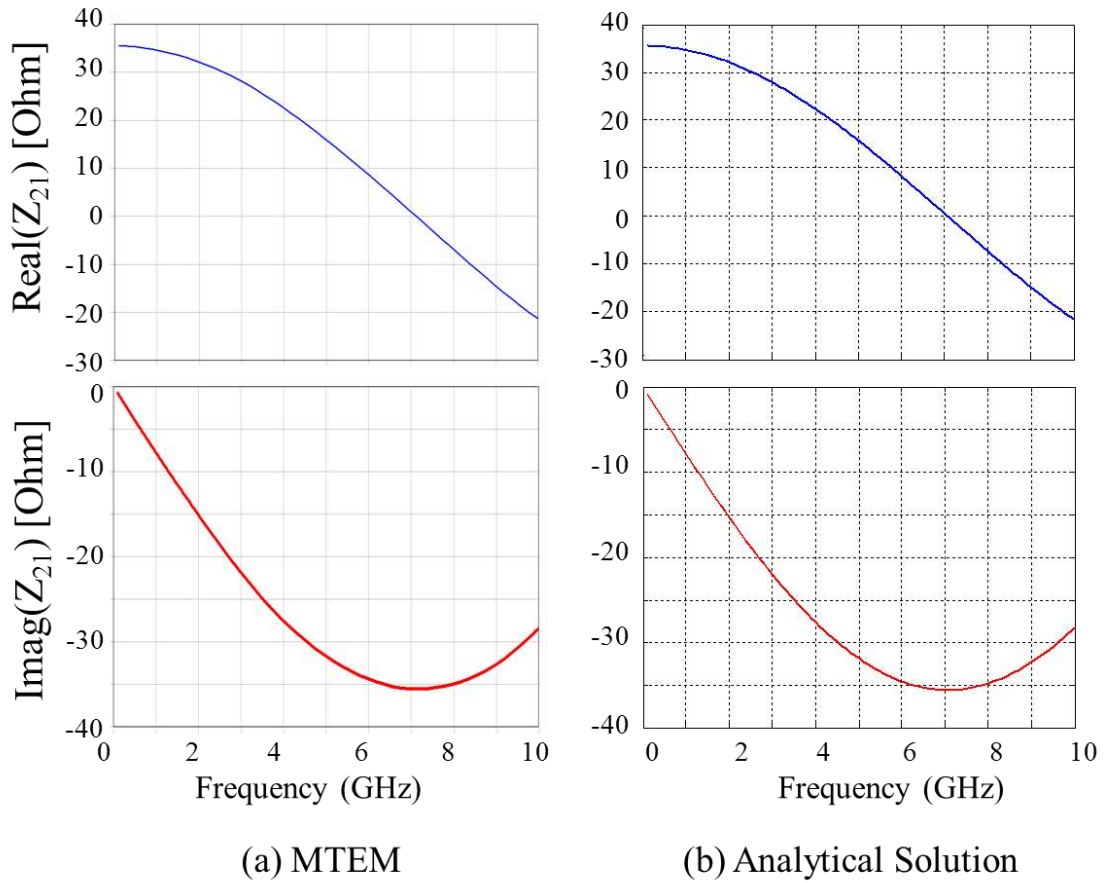
Figure 7.4. Real and imaginary parts of the transfer impedance from (a) MTEM and (b) analytical solution.
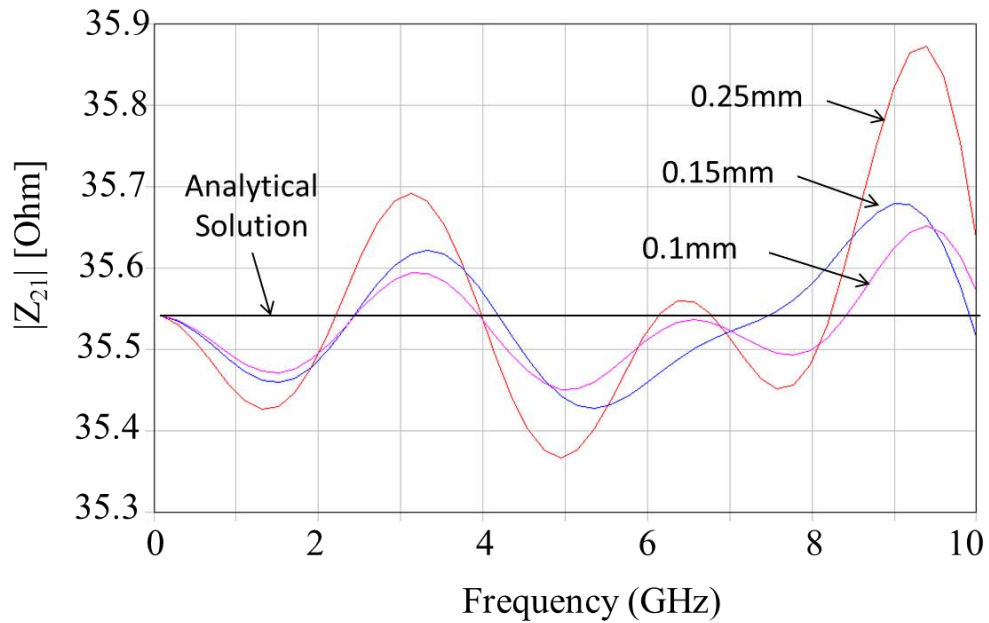
Figure 7.5. Magnitude of the transfer impedance. Discrepancy reduces as mesh size decreases.

7.2.4 ABC for Two-Dimensional Structure

Figure 7.6 shows a plane-pair with both x- and y-dimensions electrically long enough to contribute to the plane resonance. Figure 7.7 shows the transfer impedance between two ports showing multiple resonances associated with both the x- and y-dimensions of the plane-pair. For instance, first resonance occurs at 1.7 GHz ((1, 0) mode) where the half wavelength corresponds to the x-dimension, while second resonance occurs at 4.7 GHz ((0, 2) mode) where the wavelength corresponds to the y-dimension. The dielectric layer is a lossless 200-µm-thick medium with the relative permittivity of 4.5.
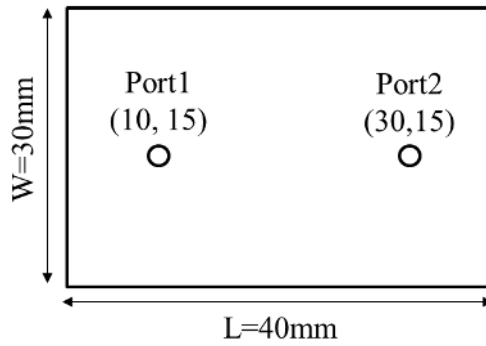
Figure 7.6. Top view of a plane-pair with two ports.
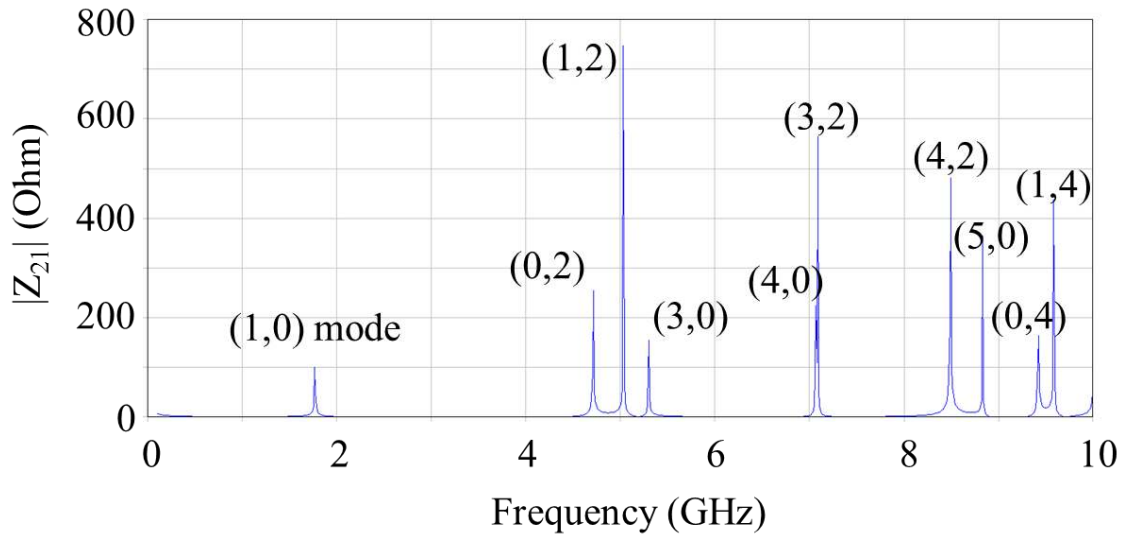
Figure 7.7. Transfer impedance and resonance modes.

As part of the validation of the 1st order ABC applied to MTEM, the boundary condition is applied to the boundary cells located only on the left and right sides, while the top and bottom sides are remain open-circuited. Hence, only y-dimensional resonances are expected to appear in the response. Similar as the one-dimensional analysis, the planar structure can be electrically modeled as shown in Figure 7.8. The

plane-pair is segmented into three sections at port locations, and each segment is modeled as a parallel-plate waveguide whose characteristic impedance (Z_0) can be calculated using Equation (76). Hence, plugging Z_0 in Equation (80) results in the transfer impedance between two ports as

$$Z_{21} = 0.59e^{-jkL_2}. \tag{81}$$
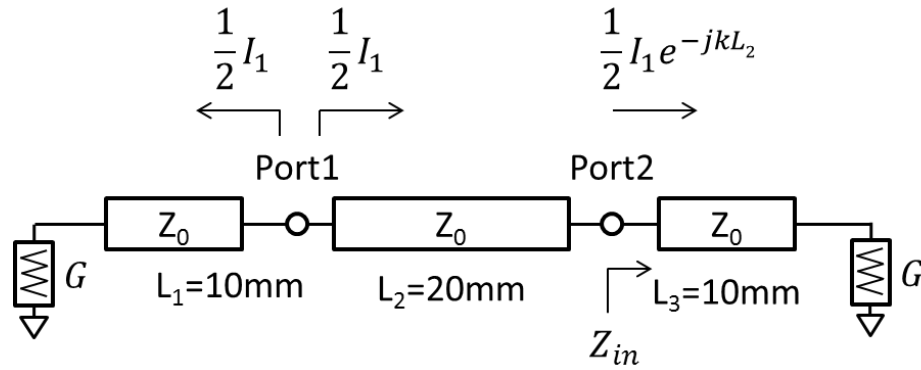
Figure 7.8. Electrical model of the plane-pair shown in Figure 7.6.

The two-dimensional structure was simulated using MTEM with the 1st order ABC as well as a full-wave solver, CST. For CST, a perfectly matched layer (PML) was used to represent the absorbing boundary. The magnitude of the transfer impedance obtained from each simulation shows a good correlation as depicted in Figure 7.9. At frequencies lower than the first resonance, the magnitude of transfer impedance corresponds to the analytical solution obtained from Equation (81). The first resonance appears at 5 GHz that represents the combination of first few modes of y-directional resonances. The second resonance is at 9.6 GHz that corresponds to the next few modes of y-directional resonances. Although the curve shows resonance-like behaviors at these frequencies, the

peak value of transfer impedance is much smaller than that for the structure without ABC. A possible reason can be that the added conductance at the absorbing boundaries dissipate the current flowing between top (y=30 mm) and bottom edges (y=0 mm) of the plane-pair. Thus, some of the y-directional resonances are critically damped and not shown in the transfer impedance curve.
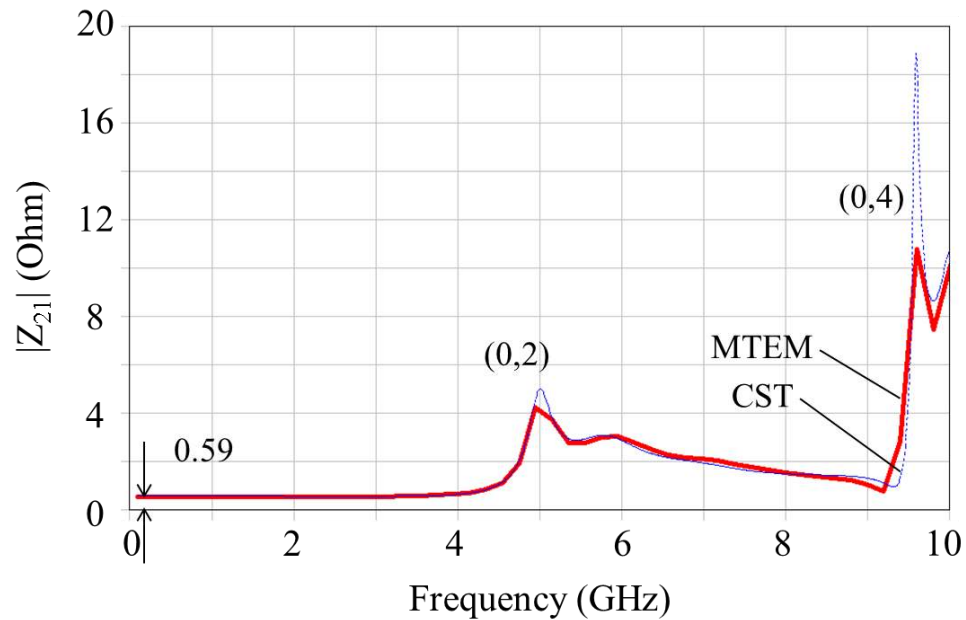
Figure 7.9. Magnitude of the transfer impedance of the plane-pair with ABC applied on left and right edges.

Similarly, the 1st order ABC is applied to the top and bottom edges of the structure. Figure 7.10 shows the simulation results from MTEM and CST, and as expected only x-directional resonances are observed. The calculated impedance at low frequency is 0.44. This value is lower than 0.59 obtained from the previous case for y-directional resonances, because more conductance elements are added to the boundaries at y=0 and y=30 mm than those were added to the boundaries at x=0 and x=40 mm.
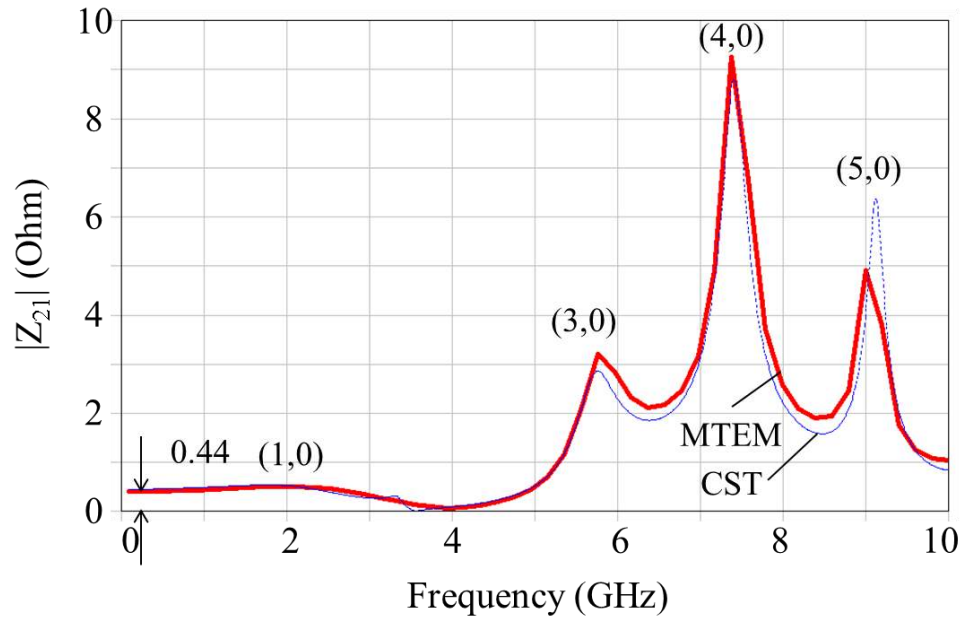
Figure 7.10. Magnitude of the transfer impedance of the plane-pair with ABC applied on top and bottom edges.

7.2.5   Test Cases

7.2.5.1 Test Case 1: Rectangular Plane-Pair

The 1st order ABC was applied to all of the boundaries of the structure shown in Figure 7.6. The magnitude of the transfer impedance obtained from MTEM and CST is plotted in Figure 7.11. At low frequencies and DC, the conductance elements added to the boundary cells result in the transfer impedance of 0.25 Ω. However, the transfer impedance slightly grows as the frequency increases as opposed to that of the one-dimensional structure, which only fluctuates as plotted in Figure 7.5.

131
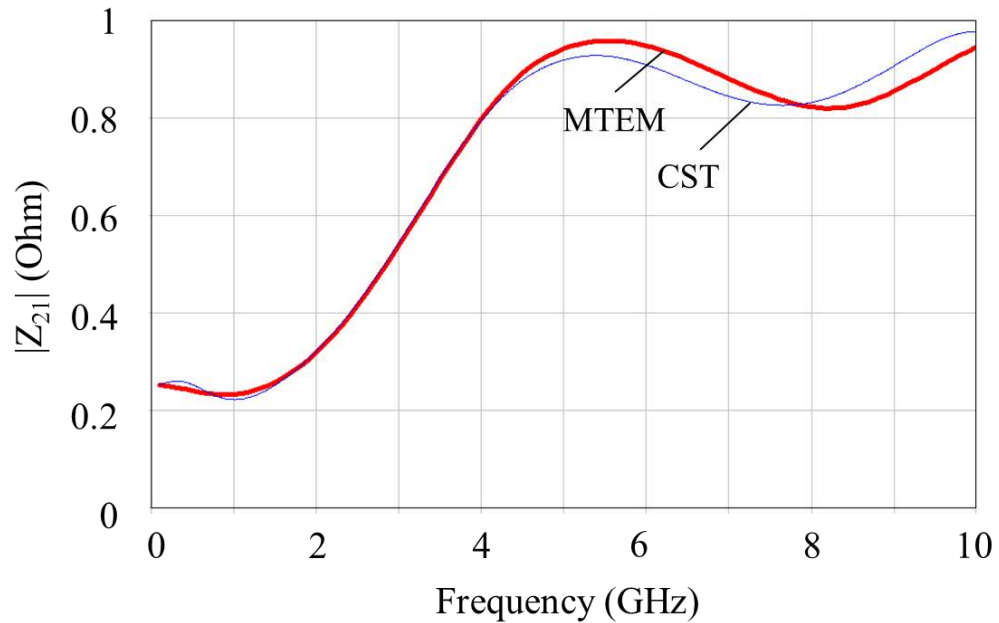
Figure 7.11. Transfer impedance of a plane-pair with ABC applied to the surrounding edges.

7.2.5.2 Test Case 2: Plane-Pair with Aperture

The second test case is a plane-pair with an aperture located in the middle of the top

plane as shown in Figure 7.12. Figure 7.13 shows transfer impedance curves obtained

from MTEM simulations with the 1st order ABC. The presence of the aperture creates a

small but discernible difference in the transfer impedance between the two ports.

Furthermore, applying ABC not only to the outer plane boundaries but also to the inner

boundaries created by the aperture renders transfer impedance even lower.
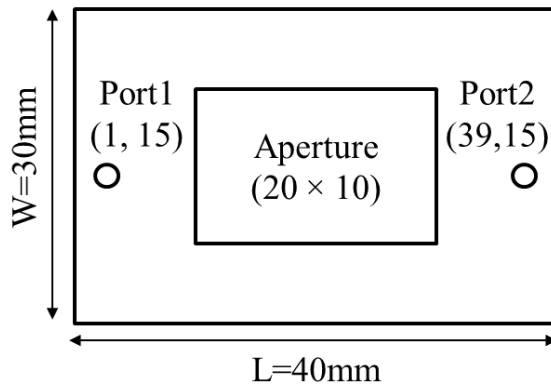
Figure 7.12. Top view of test case 2 with an aperture in the middle of the top plane.
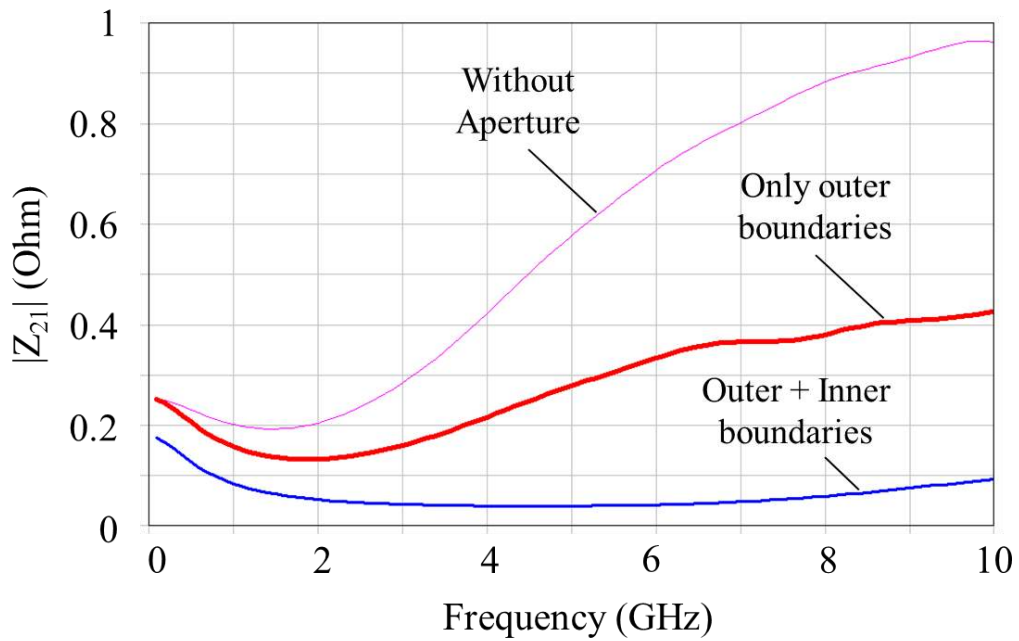
Figure 7.13. Transfer impedance of test case 2.

7.2.5.3 Test Case 3: Plane-Pair with Irregular Shape

Test case 3 is a plane-pair with irregular shape boundaries, and a mesh is created as shown in Figure 7.14. The crosses indicate the boundary cells to which the conductance elements (Equation (75)) are added. The dimensions of the planes are 40×30 mm, and

the dielectric layer is 200-µm thick with the relative permittivity of 4.5 and the loss tangent of 0.02. As the result shows in Figure 7.15, the plane resonance is perfectly removed from the self-impedance curve by applying the 1st order ABC.
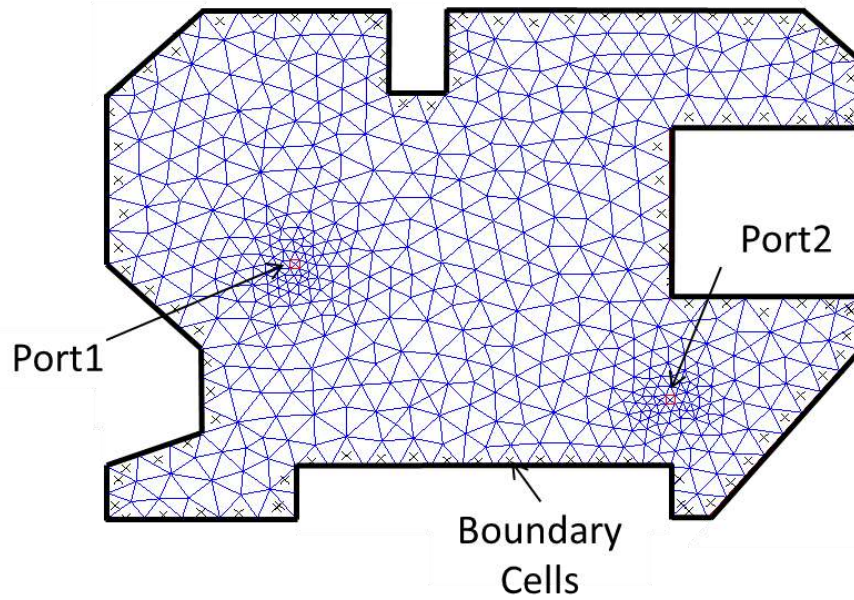
Figure 7.14. Created mesh for an example structure. Crosses represent the boundary cells where 1st order ABC is applied.
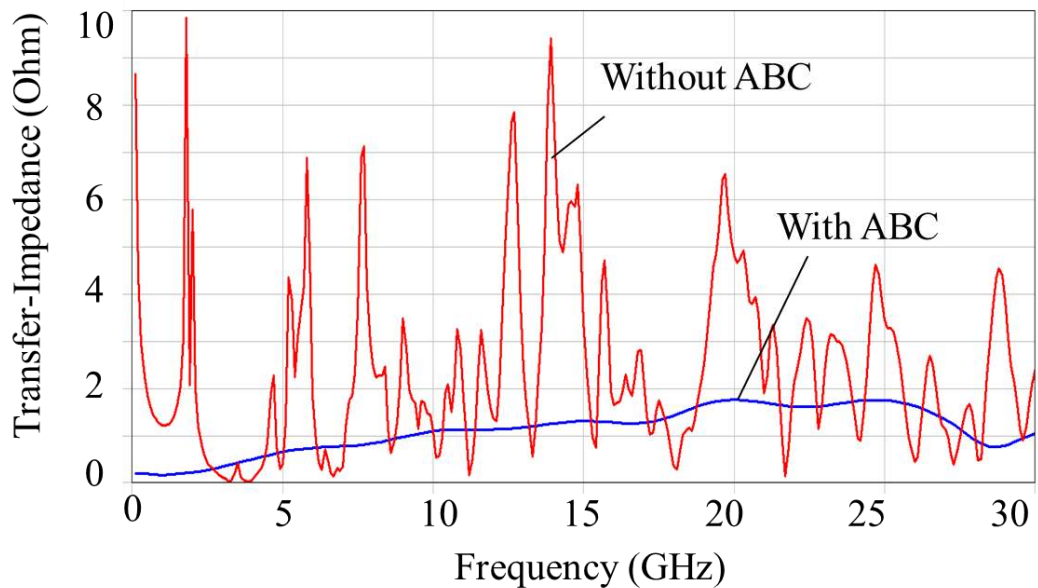
Figure 7.15. Self-impedance results with and without the 1st order ABC implemented in MTEM.

7.2.5.4 Test Case 4: Multiple Plane-Pairs

Test case 4 is a multilayer structure consisting of four layers of metal conductors as shown in Figure 7.16. Two ports are placed between the top and the bottom plane-pair, respectively. Transfer impedance shown in Figure 7.17 indicates that the two ports are heavily coupled because of the slots in the inner layers. Moreover, multiple plane resonances created by open-circuited edges of plane-pairs are captured. To remove the plane resonances, the 1st order ABC is applied to the outer boundaries of the planes, while those of the slots remain open-circuited. Figure 7.18 shows that the plane resonance is removed and a good correlation is observed between the results from MTEM and the 3D full-wave simulation.
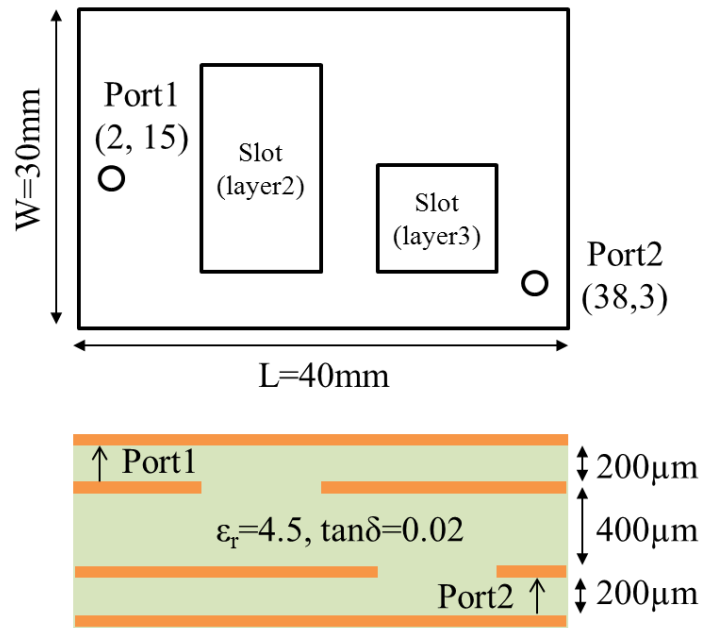
Figure 7.16. Top (top) and cross-sectional view (bottom) of test case 4. Inner layers have slots.
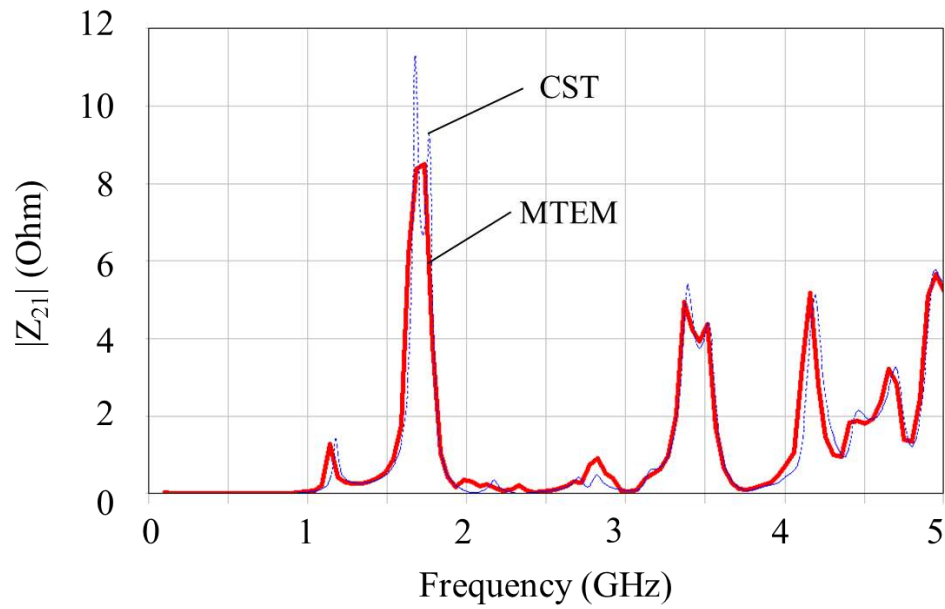
Figure 7.17. Transfer impedance of test case 4 without ABC.
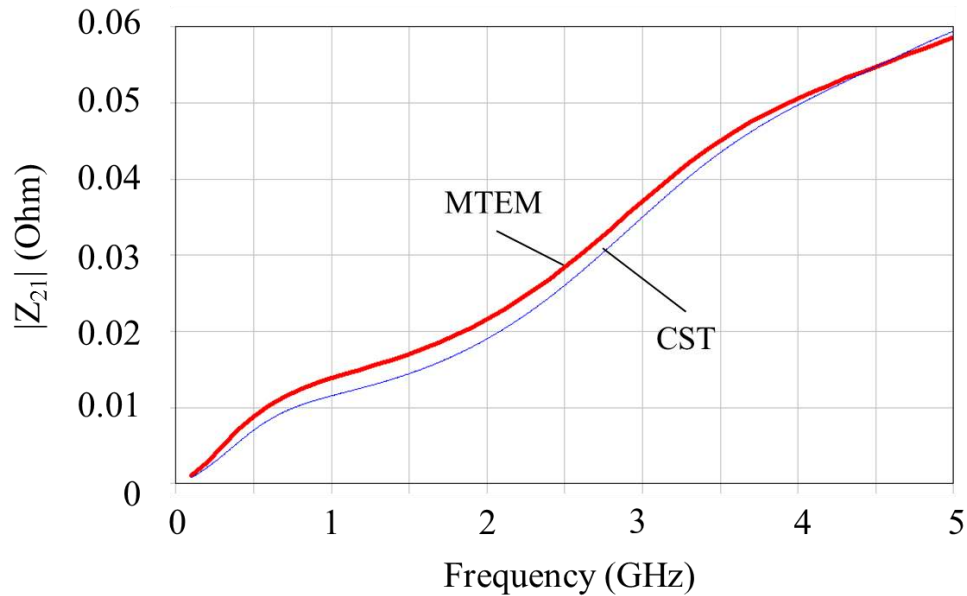
Figure 7.18. Transfer impedance of test case 4 with ABC.

7.2.5.5 Test Case 5: Via Transition

Test case 5 is a microstrip-via-microstrip structure as shown in Figure 7.19. The microstrip line transitions from the top-most to the bottom-most layer through the vertical interconnection. Because of the layer transition of the vertical interconnect, the return current jumps between metal planes by means of displacement current. This layer transition of the return current creates signal and power integrity problems as explained in Section 6.4. Since the effect of the return path discontinuity (RPD) maximizes at the resonance frequencies of the cavity created by the plane-pair, applying ABC to the plane boundary can remove the RPD problem created by the via transition.

The dimensions of the plane-pair are 40×30 mm, and the via is located at (10, 15) mm. The diameter of the via clearance hole and the via barrel are 0.5 mm and 0.3 mm, respectively. The relative permittivity of the dielectric layer is 4.5, and the loss tangent is

137

0.02, assumed to be constant along the frequency. Figure 7.20 shows the simulation results obtained from MTEM and CST with and without ABC at the plane boundary. Without ABC, the insertion loss curve exhibits large dips at plane resonance frequencies, e.g. 1.76 GHz and 4.7 GHz; while with ABC, the large dips are removed from the insertion loss curve.
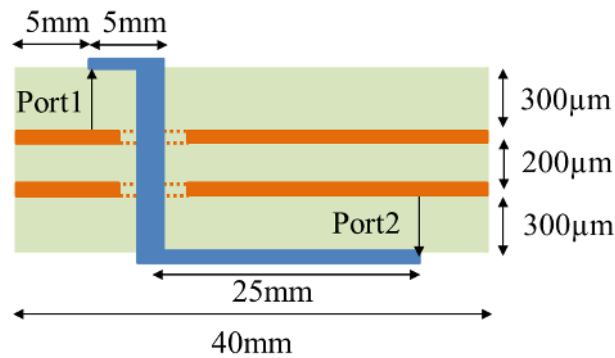
Figure 7.19. Cross-sectional view of test case 5.
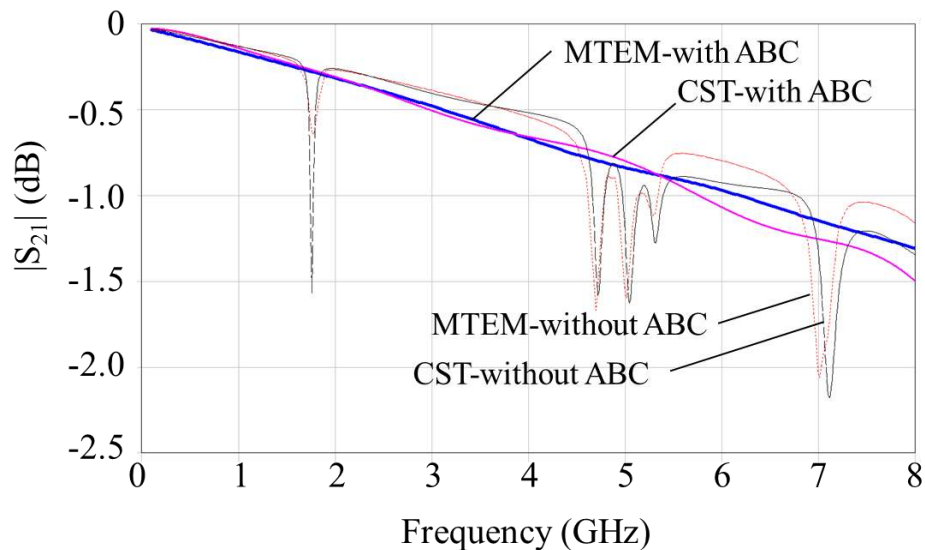
Figure 7.20. Insertion loss of test case 5 simulated with both MTEM and CST with and without ABC at the plane boundary.

7.3 Summary

To remove the resonance of a plane-pair, plane boundaries can be terminated by matched components or absorbing materials. To obtain the numerical solution of a non-resonating plane-pair, the open-circuited boundaries of the plane-pair can be replaced using an ABC. In this chapter, the application of the 1st order ABC to MTEM has been presented. The analytical solution and MTEM result showed a good correlation for a one-dimensional analysis. Simulation results from MTEM and a 3D full-wave solver showed a good correlation for the analysis of two-dimensional structures, including multilayer and irregular shape plane-pairs.

The 1st order ABC applied to MTEM is equivalent to the addition of extra conductance elements at the boundary cells. Hence, this property can be used for estimating an appropriate physical material that effectively absorbs the outgoing wave within a plane-pair or within multiple plane-pairs.

CHAPTER 8

CONCLUSIONS

In an electrical package or printed circuit board (PCB), a power delivery network (PDN) refers to any electrical structure that supplies and distributes power from a voltage regulator module to integrated circuits (ICs). The goal of the PDN design is to ensure the delivery of a constant level of supply voltages to the power and ground pads of the devices. Hence, maintaining the impedance of a PDN below a certain level across the system frequency band is a key design factor.

The impedance of a PDN can be reduced by placing decoupling capacitors between power and ground nets. Since the effectiveness of decoupling is a function of a number of parameters, such as the number and value of capacitors and their locations, manually finding an optimal solution is a time consuming and highly complicated task. Thus, the task can be automated using an algorithm that finds a best solution by simulating a number of different combinations of decoupling capacitors placed on a PDN. Hence, the efficiency of the optimization strongly depends on the performance of the search algorithm and PDN simulations. This dissertation presented an optimization technique that employs a genetic algorithm (GA) which can find a quality solution from a very large number of possible solutions. For the PDN simulation, the multilayer finite element method (MFEM), which can effectively solve plane-pair structures using FEM, was used. A GA was customized to the decoupling problem to further enhance the optimization performance. The difficulty of incorporating decoupling capacitor model into MFEM has been addressed.

This dissertation mainly focuses on the development of a computationally efficient modeling method, the multilayer triangle element method (MTEM) that solves for the impedance profile of PDNs. A dual mesh scheme is used to discretize surfaces of a plane-pair, and an equivalent circuit is extracted. The circuit model is extended to multiple stack-ups of plane-pairs, accounting for the coupling between plane-pairs. The comparison of computational efficiency shows that MTEM outperforms other planar circuit models using finite difference and finite element methods, especially for large-sized and multi-dimensional problems.

A new port representation, a *non-vertical port* whose terminals are with horizontal or diagonal alignment, has been introduced. The *non-vertical port* representation is necessary for the exact realization of the realistic port configurations. However, it was analytically shown that the horizontal component of current excitation is evanescent in a parallel-plate waveguide. Consequently, the use of *vertical port* representation is sufficient. In addition, the sensitivity of self-impedance parameters to the port size was addressed.

The electrical behavior of signal interconnects and a PDN are closely related. Since the return current of signal flows on the planes of a PDN, the integrity of the return path affects the quality of the signal. However, typical PDNs are highly perforated and even split for various reasons, such as vertical interconnection of signal traces, multilevel power supply, and embedded devices. At these discontinuities, signal return current inevitably encounters an impedance change, which deteriorates signal integrity. Furthermore, the coupling of signal to the PDN can also affects the quality of power. Therefore, the effect of the mutual coupling between a PDN and signal interconnects

must be included in the simulation. This dissertation presented the investigation of various types of return path discontinuities (RPDs), such as split planes, apertures, and vias, and the computationally efficient technique for modeling RPDs using MTEM. In addition, modeling and design guidelines suggested further improvement of the RPD modeling efficiency.

Plane resonance is a major reason for the power integrity issue of a PDN. To mitigate or remove the plane resonance, various techniques have been developed in the literature. One of the techniques is to place absorbing material around the plane edges for the damping of the edge reflections. This dissertation presented modeling of such an absorbing boundary by applying the 1st order absorbing boundary condition (ABC) to MTEM.

8.1 Contributions

The contributions of this dissertation can be summarized as follows:

1) **Optimization of decoupling capacitor selection and placement using MFEM**.

   An efficient automation tool to obtain optimal selection and placement of decoupling capacitors on a PDN has been developed. The optimization engine employs MFEM for the PDN analysis and the genetic algorithm (GA) customized for the decoupling capacitor selection and placement. The use of MFEM for a PDN analysis has an important advantage, since each step of the optimization requires a full analysis of a PDN with a set of decoupling capacitors. A modeling technique for the incorporation of the decoupling capacitor circuit model into

MFEM has been explained. A test vehicle with many decoupling capacitors was created to validate the model.

2) **Development of a computationally efficient PDN modeling method**.

A new modeling method, the multilayer triangular element method (MTEM), has been developed. MTEM extracts a physics-based equivalent circuit and effectively discretizes multi-dimensional geometries using a dual mesh, Delaunay triangulation and a Voronoi diagram. An equivalent circuit model can be extracted along the Voronoi diagram of the dual mesh. The values of the lumped circuit elements are calculated from Maxwell's equations applied to each of triangle unit-cells. To extend the model to multiple plane-pairs, indefinite admittance matrices are used to shift the reference of each plane-pair to a system ground. MTEM maintains the advantages of the prior arts based on the planar circuit model, such as MFDM and MFEM, while overcoming their limitations. The non-uniform triangular mesh used by MTEM is especially effective for the discretization of multidimensional and irregular geometries, which are common in modern PDNs. The physically intuitive equivalent circuit model overcomes the demerit of MFEM.

3) **Comparison of the computational efficiency of MTEM with prior arts**.

The computational complexity of MTEM is compared with that of MFDM and MFEM. Because of mesh efficiency of non-uniform triangulation, MTEM and MFEM create far fewer unknowns than MFDM, especially for multidimensional geometries. For the same number of unknowns, the system matrix of MTEM

contains the least number of non-zero entries, while MFEM the most. Overall, the comparisons show that the computational complexity and memory requirement of MTEM grows the slowest as the system size increases.

4) **Modeling of an RPD of a microstrip line created by an aperture**.

If a microstrip line crosses an aperture, the reference of the microstrip line is divided into two: The conductor region around the aperture and the lower conductor plane directly beneath the microstrip line. Therefore, modeling of such configurations must include the discrepancy of references. Transmission lines are segmented at the discontinuities, and the segmented models are combined with a PDN modeled using MTEM by means of a modal decomposition technique. A test vehicle has been created and measured to show the model-to-hardware correlation.

5) **Modeling of an RPD of vertical interconnects**.

The RPD created by a via structure has been modeled. When signal traces transition layers through vias, the reference of the signal also switches layers in the form of a displacement current. The displacement current excites the cavity created by the metal layers, and the plane resonance can affect the signal propagation of the via. Furthermore, capacitive coupling exists between a via barrel and the circumference of the via anti-pad. The modal decomposition technique is used to model the RPD, and the coupling capacitance is obtained from analytical solutions. Thus, the modeling includes both the change of reference and the coupling between a via and plates.

6) **Design and modeling guidelines for RPDs**.

By synthesizing the full-wave simulations of different types of RPDs (split planes and apertures), their different behaviors are quantified and analyzed. In particular, a modeling criterion for a small aperture is empirically set, and the apertures that comply with the criterion can be ignored to simplify modeling without loss of accuracy. A test vehicle has been created and measured to verify the criterion. In addition, the insignificance of the modeling of the capacitive coupling between a short via and a plane-pair was addressed.

7) **Non-vertical Port Representation for Planar-Circuit Model**.

The conventional representation of a port for a planar-circuit model constitutes a vertical alignment of port terminals. However, the port terminals of most of real-world structures are not in a vertical relation, and they can only be measured as a coplanar or *diagonal port*. Although a *non-vertical port* representation may be necessary, its impact on the plane-pair excitation is not distinguishable compared to a *vertical port*. Furthermore, a non-vertical excitation can generate an artificial response if applied to multiple plane-pairs. These issues were addressed, and the negligible impact of horizontal component of a current excitation on a plane-pair was explained.

8) **Absorbing boundary condition for MTEM**.

The resonance of a plane-pair is one of the main contributors of power integrity issues in a package and PCB PDN. If the edges of a plane-pair are well-terminated with the impedance equivalent to the characteristic impedance of a plane-pair, the traveling wave between the planes does not reflect back into the plane-pair, and resonance disappears. This effect can be computationally

represented by an absorbing boundary condition (ABC) applied to the boundaries of the plane-pair. The 1st order ABC was applied to MTEM, and an equivalent circuit was obtained.

8.2 Publications

- J. Y. Choi and M. Swaminathan, "Modeling of power/ground planes using triangular elements," *will be submitted to IEEE Trans. on Electromagnetic Compatibility*.

- S. J. Park, J. Y. Choi, and M. Swaminathan, "Simultaneous switching noise analysis of reference voltage rails for pseudo differential interfaces," *IEEE Proc. on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, Chandler, AZ, Oct. 2012.

- J. Y. Choi and M. Swaminathan, "Decoupling capacitor placement in power delivery networks using MFEM," *IEEE Trans. on Components, Packaging, and Manufacturing Technology*, vol. 1, no. 10, pp. 1651-1661, 2011.

- J. Y. Choi and M. Swaminathan, "Practical aspects of modeling apertures for signal and power integrity co-simulation," *IEEE Proc. on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, San Jose, CA, Oct. 2011.

- J. Y. Choi and M. Swaminathan, "Modeling methods for power/ground plane structures in electronic packages," *IEEE Proc. on International Conference on Electromagnetics in Advanced Applications (ICEAA)*, Torino, Italy, Sep. 2011.

- J. Y. Choi and M. Swaminathan, "An effective modeling method for multi-scale and multilayered power/ground plane structures," *IEEE Proc. on Electronic*

Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 2011.

- K. Bharath, J. Y. Choi, and M. Swaminathan, "Use of finite element method for the modeling of multi-layered power/ground planes with small features," *IEEE Proc. on Electronic Components and Technology Conference (ECTC)*, San Diego, CA, May 2009.

8.3 Patent Application

- J. Y. Choi and M. Swaminathan, "Modeling of Multi-Layered Power/Ground Planes Using Triangle Elements," United States Patent Application: 12/710991, filed on 2/23/2012.

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