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Modeling and Simulation of LDO Voltage Regulator Susceptibility to Conducted EMI

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Abstract—**This paper presents a methodology dedicated to modeling and simulation of low-dropout voltage (LDO) regulator susceptibility to conducted electromagnetic interference (EMI). A test chip with a simple LDO structure was designed for EMC test and analysis. A transistor-level model, validated by functional tests, Z-parameter characterization and direct power injection (DPI) measurements, is used to predict the immunity of the LDO regulator. Different levels of model extraction reveal the weight contributions of sub-circuits and parasitic elements on immunity issues. The DPI measurement results show a good fit with model prediction up to 1 GHz.**

Index Terms—**Low-dropout voltage regulator (LDO), susceptibility, electromagnetic interference (EMI), interference propagation, Z-parameter, direct power injection (DPI), parasitic elements.**

I. INTRODUCTION

Owing to the increasing pollution of the electromagnetic environment and the widespread use of more complex and miniaturized devices, the susceptibility of analog integrated circuits (ICs) has become a major issue as they are very susceptible to EMI [1]-[2]. LDOs have been widely used to provide a regulated and clean voltage source for analog and digital subsystems, as they are easier to use, cost less, are more accurate and subject to less noise [3]. However, there is increasing concern about the susceptibility of LDO regulators, especially in critical, embedded, electronic systems for automobile or aerospace applications for which performance is directly related to power integrity. This is because the sensitive LDOs conduct external interference to very large power supply networks. Under EMI, the induced DC shift is very detrimental to the behavior of LDO circuits since it alters the correct DC biasing and may disrupt the entire circuit [4].

Designers have used various modeling methodologies [5]-[6] to predict electromagnetic emission and susceptibility prior to manufacturing, as redesign is both very costly and time-consuming. The methodologies are based on the IBIS model [7], the Linear Equivalent Circuit and Current Source (LECCS) model [8], the Integrated Circuit Emission Model (ICEM) [9] and the Integrated Circuit Immunity Model (ICIM) [10]. Several examples of digital and analog ICs susceptibility modeling and simulation have already been cited in publications, e.g. [11] which focuses on the immunity modeling of a microcontroller with an assembly of functional blocks, and [12] which presents the susceptibility modeling of a phase-locked loop based on basic circuit information and S-parameter measurements. However, few papers have yet been published on LDO susceptibility modeling and simulation.

Most publications on LDO EMC concentrate on analysis of failure mechanisms of building blocks under EMI: i.e. operational amplifiers (op-amp) [1] [13] and bandgap reference circuits [1] [14]. For op-amps, slew rate symmetry and the finite impedance of the bias source are the main reasons for the DC offset. Parasitic capacitances of input differential pair become predominant at high frequencies and propagate interference [1]. Such publications also highlight the rectification phenomenon of bipolar transistors, as used in the bandgap cell, which degrades performance [14]. In [15], the propagation of EMI through LDO power distribution networks was examined and confirmed by comparison with model predictions. However these articles have not addressed immunity modeling of the complete regulator.

The objective of this paper is to demonstrate how both simple models and physics-based advanced models can accurately predict the susceptibility level for LDO regulator conducted immunity. The link between the proposed models and the global flow for the IEC IC immunity modeling standard ("ICIM") [10] is also clarified here. The detailed modeling process is described, including the Passive Distribution Network (PDN) model and the Immunity Behavior (IB) model. The parasitic components in the LDO model provide possible propagation paths for EMI which are crucial for IC immunity. Different versions of the models are presented and compared to determine the quantitative contributions of each block and parasitic element in the frequency domain.

The paper is structured as follows: the next section II describes immunity measurement under conducted EMI, with information on the test chip, test bench setup and Z-parameter tests. Section III covers the detailed modeling process of the LDO immunity model. The main sub-circuits in the PDN and IB models are presented followed by a full electrical circuit model used for model validation and simulation. Section IV describes

functional and impedance simulations that were carried out for comparison with measurement results in order to validate the model. Section V contains an analysis of the methodology and results. Four types of model from simple to complex levels are discussed step by step to distinguish between the contributions of sub-circuits and parasitic elements. Finally, section VI contains the conclusion and a description of future work.

II. IMMUNITY MEASUREMENT UNDER CONDUCTED EMI

A. Test Chip Description

The LDO regulator being tested has been incorporated in a test chip designed using the Freescale CMOS 90 nm process. The aim is to facilitate the measurement of various EMC effects. The LDO regulator should provide a regulated power supply voltage to a small digital core.
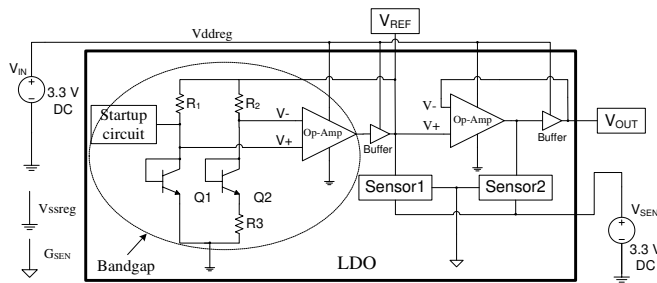

Figure 1.   Test chip LDO module circuit structure

Fig. 1 illustrates the internal structure of the LDO voltage regulator, which contains a Kuijk bandgap reference circuit [16] and an output follower op-amp designed to work with a +3.3V supply. The nominal voltage of the bandgap reference and regulator is 1.25V. The bandgap circuit consists of two bipolar NPN transistors of different sizes (ratio = 8.0) thus creating a common centroid structure, with three resistors (R1=R2=250 kΩ, R3=25 kΩ) and a feedback circuit maintaining the same emitter current in both transistors. An auxiliary circuit helps the bandgap circuit to start. The bandgap reference circuit and regulator outputs are monitored through the terminals V_{REF} and V_{OUT}.

B. Test Bench Setup

DPI measurements were implemented in accordance with the IEC standard 62132-4 [17]. The test bench for DPI measurements as shown in Fig. 2 includes the DUT board, EMI signal generation, test control and monitoring. The instruments include the signal generator, amplifier, coupler, power sensor and National Instrument (NI) data acquisition card, a DC voltage source, bias tees and PC.

As illustrated in Fig. 3, two special boards were designed for Z-parameter and immunity tests. The Z-parameter test board only houses the test chip with minimum PCB tracks for PDN model extraction. The test chip and all of the external components for the regulator were mounted on the immunity test board.
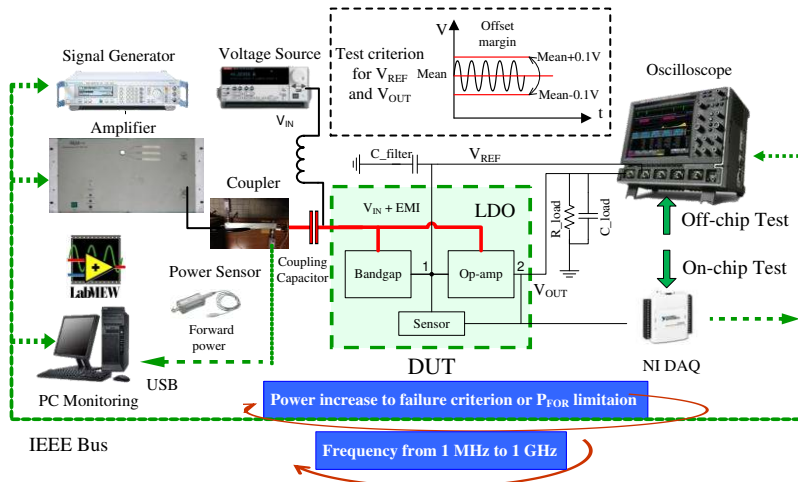

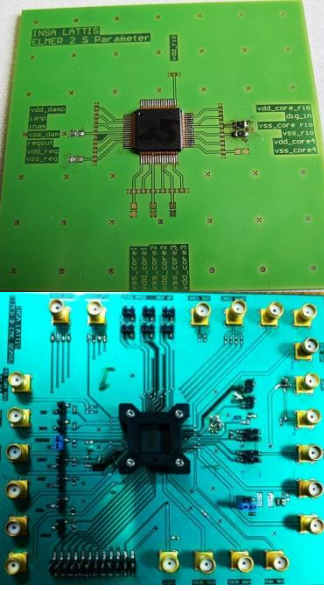Figure 2.   Test chip LDO module structure and general test setup

Figure 3.   LDO regulator test board: Z-parameter (left) and immunity (right)

C. Z-parameter Measurement

Two-port S-parameter measurements were taken on the LDO regulator Vddreg and Vssreg pins (Vdd and ground pins) using a Vector Network Analyzer (VNA) and microscope test bench. The test bench included the VNA, microscope and coplanar GS probes as shown in Fig. 4. The VNA was calibrated in order to remove cable, Z probe and connector effects. The frequency ranged from 1 MHz to 2 GHz.
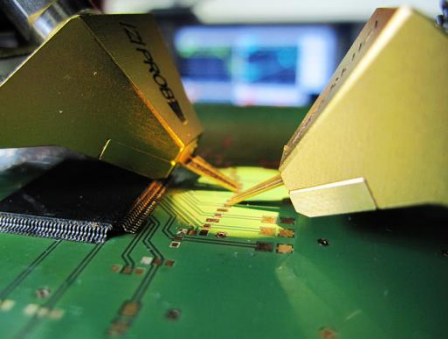

Figure 4.   LDO regulator Z-parameter test bench by VNA and microscope

D. Conducted EMI Measurement

The conducted EMI tests were performed using the standard DPI measurement procedure. Harmonic disturbances from 1 MHz to 1 GHz were added to the V_{IN} power line. An external oscilloscope was used to monitor the outputs of the bandgap circuit and regulator. The voltage at the power supply input was measured by an oscilloscope with an active probe. The probe is fixed to the input port of the test PCB board including a PCB track to the LDO regulator power pin. The test process, as illustrated in Fig. 5, was controlled by NI Labview software.
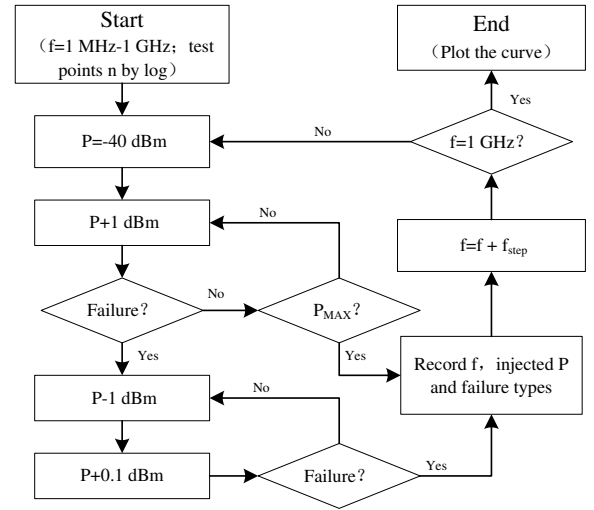

Figure 5.   DPI measurement software control flow

The frequency "f" ranged from 1 MHz to 1 GHz and EMI power "P" ranged from -40 dBm to 30 dBm (P_{MAX}). After a failure occurrence at one frequency, the power is decreased by 1 dB, and then increased by 0.1 dB step until the failure arises once again in order to improve accuracy. By judging the V_{REF} and V_{OUT} output failure criterion as shown in the dashed frame of Fig. 2, the susceptibility level was plotted in terms of forward power or EMI voltage amplitude (Vemi_amp) of the EMI transferred by the power amplifier to induce an +/- 0.1 V offset.

The plot of DPI measurement results is shown in Fig. 6. When the EMI is below the op-amp unity gain frequency (about 2 MHz), the regulator works in the normal mode and V_{OUT} is controlled by a negative feedback circuit. Above this frequency, the op-amp no longer works in the negative feedback regime, which explains the decrease in susceptibility level. The parasitic elements include the package, bonding, on-chip interconnection, functional blocks and substrate circuits like parasitic capacitors, inductors and resistors. With the parasitic effects of the test chip, more EMI noise is transferred to the output and induces more distortion and offset. But at frequencies above 700 MHz, the parasitic effects of bonding, packaging and the PCB will work as filters that improve the immunity level.
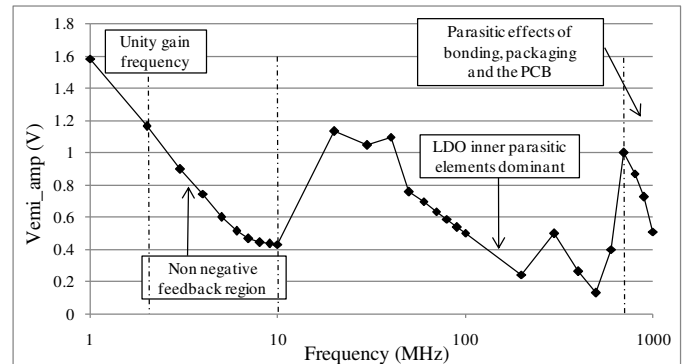

Figure 6.   Sensitivity of the LDO voltage regulator to RF voltage fluctuations applied to its power supply pin

III.   LDO IMMUNITY MODELING PROCESS

The modeling process includes functional, impedance and immunity (DPI) modeling of the LDO regulator. The simulation environment is based on Agilent's Advanced Design System

(ADS) [18]. With ADS, a transistor-level model is built to perform the simulations. The simulation results are compared with measurements to validate the model in section IV.

A. A General Overview of ICIM Methodology

Immunity modeling and simulation flows have become one of the major EMC concerns of the IC community over the last few years. The documentation on the Integrated Circuit Immunity Model (ICIM) is currently being written and the model is due to be submitted for standardization as IEC62433-4 [10]. The basic ICIM model structure, mainly with passive and active elements, is illustrated in Fig. 8.
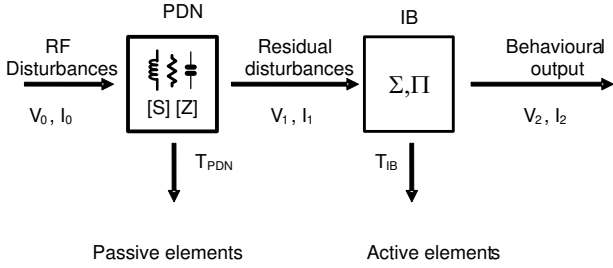

Figure 7. ICIM model structure [10]

The PDN includes all the passive devices, S or Z parameters of a circuit, and the Immunity Behavior (IB) block describes how the IC reacts to applied disturbances. IB covers both in-band and out-of-band IC frequency response. T_{PDN} and T_{IB} are the transmission of PDN and IB respectively. The residual disturbances applied to the IB input are converted to a behavioral output which can be a spectrum or time domain, on which a pass/fail criteria may be applied externally.

B. LDO PDN Models

Between the Vddreg pin and the SMA connector, there is an injection path (about 5 cm) for EMI propagation. As the characteristic of the injection path is very important for DPI simulation, the characteristic of the path is extracted from the PCB board design information. Linear electrical parameters as shown in Fig. 8 are extracted from analytical formulations. The parameters are used for PCB track model building in ADS.
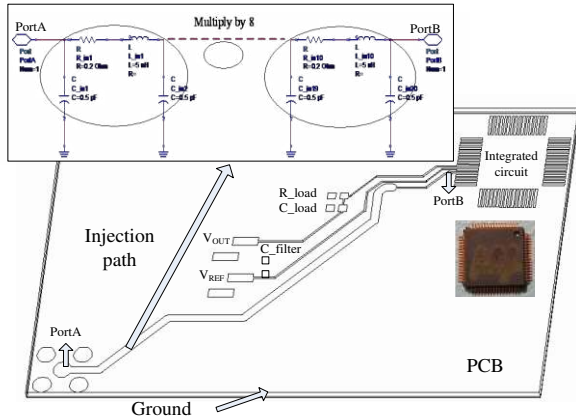

Figure 8. The PCB track model

Fig. 9 illustrates the PDN model of the LDO regulator which includes the Vddreg/Vssreg package, the bonding and coupling capacitor, the power and ground plane coupling capacitor Cx, the decoupling capacitor and resistor and the substrate resistor

and capacitor. This model predicts the amount of noise which is coupled into the LDO because the PDN acts as a filtering element in this test chip. ADS is used to simulate the model and compare the results with S-parameter measurements.
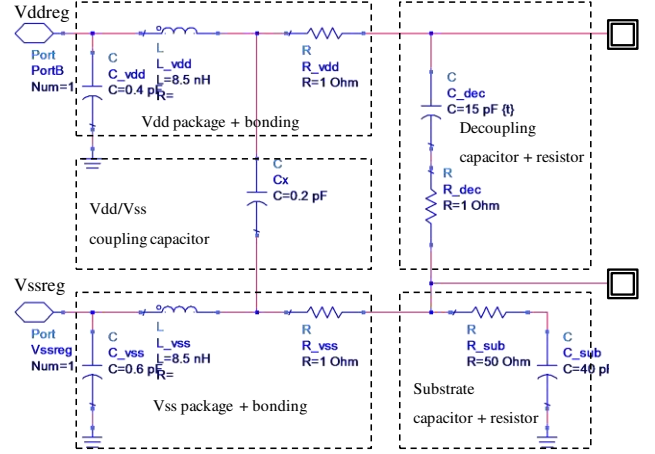

Figure 9. The PDN model of Vddreg and Vssreg for LDO regulator

Decoupling capacitors were removed from the power supply V_{IN} to increase coupling of EMI disturbance to the LDO input. In the test chip design, the filtering capacitor is crucial for op-amp output stability. As the integration of a large capacitor on-chip takes up a very large area, an off-chip 47 nF capacitor (C_filter) was included to improve the output stability of the bandgap reference V_{REF}. By Z parameter test, the actual value of the off-chip capacitor is 44 nF with an equivalent series inductance (ESL) and an equivalent series resistance (ESR).

The regulated output V_{OUT} is loaded by a 330 Ω resistor (R_load) and a parallel 100 pF capacitor (C_load). However, due to the physical presence of the leads, the load capacitor also has an ESL and ESR as shown in Fig. 10. These parasitic elements are important for high frequency immunity simulation.
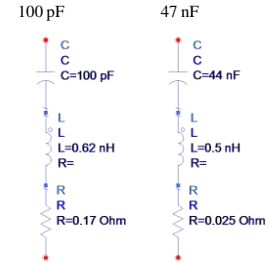
Figure 10. The equivalent load capacitors models with ESL and ESR

C. LDO Regulator: Basic Building Block Models

1) Cascode op-amp model

In ADS, a Level 3 model [19] is used for NMOS and PMOS transistor simulation. This model has been validated from measurements and comparison with results from the original design library, BSIM4 model. Two cascode op-amps were built with a Level 3 model as shown in Fig. 11, offering high gain and good common mode rejection. For individual signals, two robust clamping diodes, one connected to ground, the other connected to the I/O bank power supply, are used for ESD protection (D1 and D2 are for signal "VPOL", D3 and D4 are for signal "EP" and D5 and D6 are for signal "EM"). The two op-amps are implemented in the regulator: one in the bandgap

reference circuit and the other working as a feedback circuit between the bandgap circuit and the regulator output.
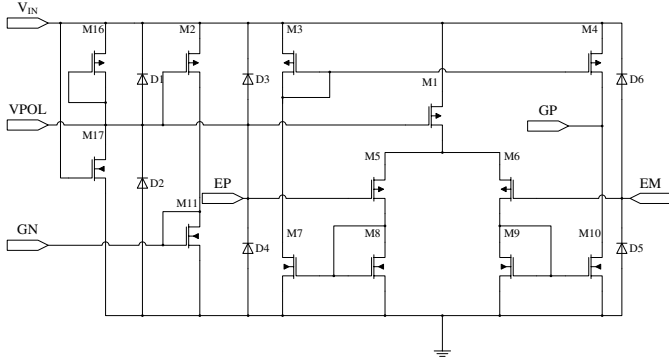
Figure 11. Model schematic of cascode op-amp structure

2) Kuijk bandgap reference circuit model

The bandgap reference circuit is a Kuijk bandgap reference circuit [14] which uses the difference in bias currents through two p-n junctions in combination with the cascode op-amp to generate the necessary reference voltage.

3) Output buffer model

The output buffer cell is created by taking a digital I/O cell from the library and carefully stripping out all the digital circuitry (level translators and slew-rate control), keeping only 10 large output transistors (N-channel and P-channel) and the ESD protection hardware as depicted in Fig. 12.

Figure 12. Model schematic of output buffer P_totem

D. Full Electrical Circuit Model

All the PDN and IB models described above are then assembled. A full electrical circuit model of the LDO regulator according to the DPI setup can be drawn as shown in Fig. 13. The signal generator supplies +3.3 V DC and sinusoidal EMI to the regulator for transient simulations.

Figure 13. Model schematic of full electrical circuit

IV. VALIDATION THE LDO MODELING PROCESS

A. Functional Model Validation

DC simulation validation includes basic MOSFET models, LDO regulator nominal output voltage, the input I/V curve and V_{IN}/V_{OUT} characteristics. The basic MOSFET equivalent model in ADS is validated by comparison with the device simulation (NMOS, PMOS) from the Cadence® design library. The ot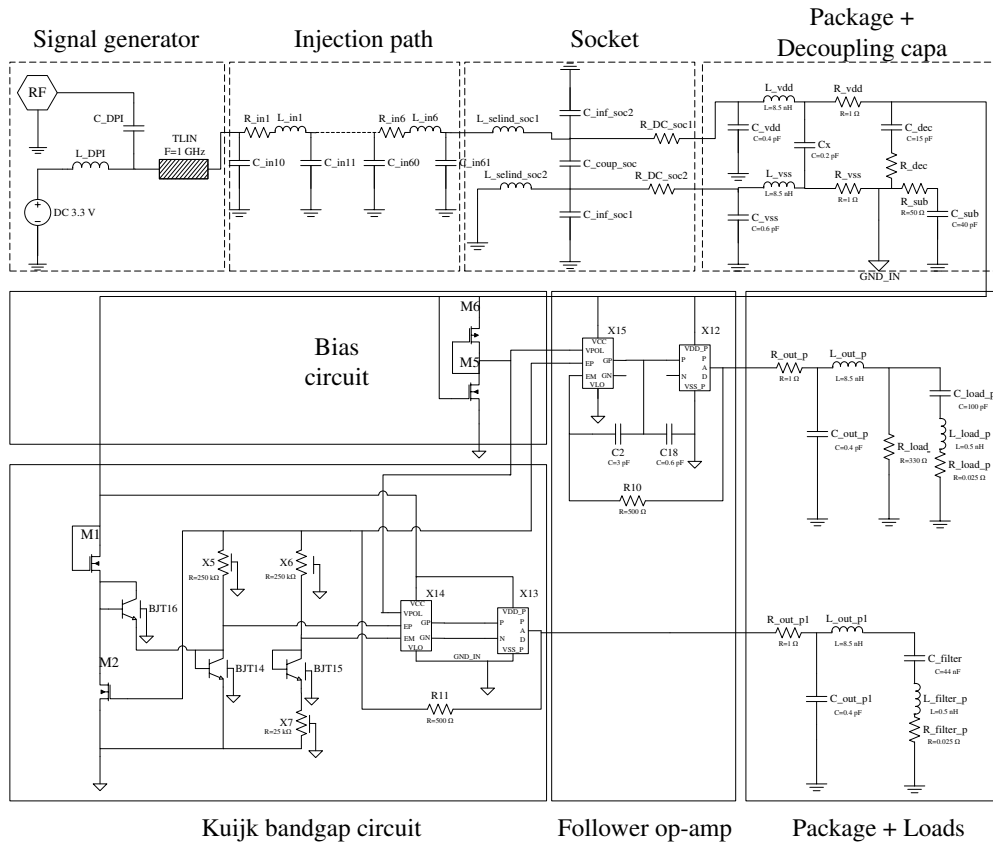hers are validated by comparison between measurements, ADS and Cadence® Virtuoso® Spectre® Circuit (CVSC) [20] simulations.

As the process varies for the samples, we characterized the DC output voltage variation on 22 samples for a nominal input voltage V_{IN} at +3.3 V. All the test samples based on experimental data were used for statistical analysis. The maximum and minimum test values were omitted, and the other results were averaged. The averaged measurement value was close to the transistor-level simulation as shown in Table. I.

TABLE I DC NOMINAL OUTPUT VOLTAGE

	V_{REF}	V_{OUT}
Transistor-level model	1.20 V	1.20 V
Measurement (averaged)	1.27 V	1.26 V
Ideal output value	1.25 V	1.25 V

Fig. 15 gives the measured and simulated results of the input I/V curve and a comparison of the V_{IN}/V_{OUT} characteristics. The fit was excellent, thus validating use of the model in ADS software environments.
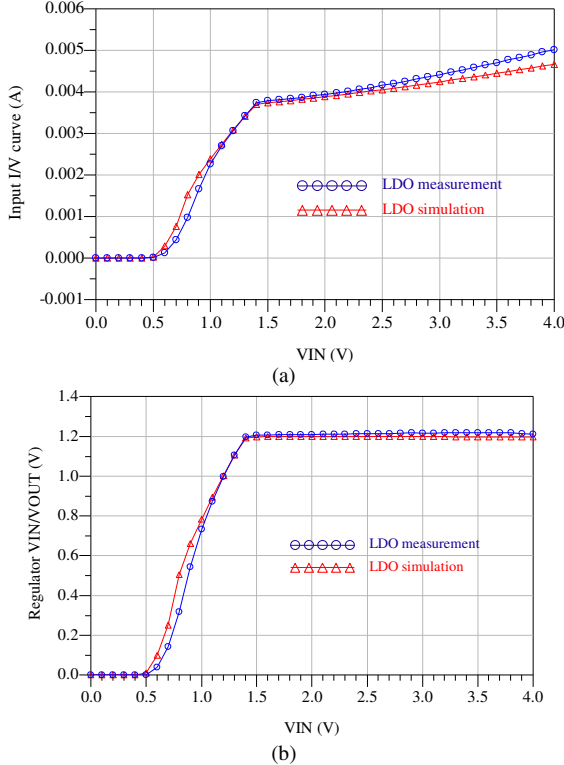

Figure 14. Comparison between measurement and simulation by LDO transistor-level model. (a) input I/V curve. (b) regulator V_{IN}/V_{OUT} characteristic.

B. Impedance Model Validation

On the basis of Z-parameter board measurement results, the regulator simulation results were merged as shown in Fig. 15. According to literature [21], we can extract the models from the measurement results of one port and two-port Z parameters. The one-port Z parameter is Vddreg with Vssreg shorted to ground and the two-port Z parameters are measurements between Vddreg and Vssreg.

From the comparison of the PDN two-port Z parameter results as shown in Fig. 15, a good match was found between measurement and simulation of Vddreg and Vssreg for the frequency range from 1 MHz to 1 GHz. The PDN model can be used for further DPI simulation.
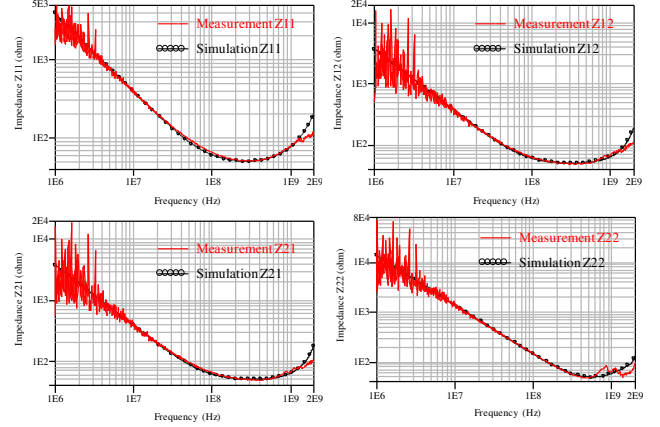
Figure 15. Two ports Z parameter comparison between measurement and simulation of Vddreg and Vssreg [22]

V. IMMUNITY SIMULATIONS RESULTS ANALYSIS

This section first describes the immunity simulation methodology, including a comparison of the results for the simulation algorithm used for the LDO DPI transistor-level model and the measurements. DPI simulations follow the same sequence of experimental tests. Moreover, four types of immunity model from simplified to gradually more complicated levels were simulated. The differences between the four simulations were compared to highlight the contribution and importance of each version.

A. Immunity Simulation Methodology

The DC offsets on both bandgap reference circuit and regulator outputs were monitored. A deviation of +/- 0.1 V from the nominal output voltage V_{OUT} is tolerated. The simulation algorithm flow is chosen in accordance with the DPI standard [17] shown in Fig. 18. The EMI amplitude ranges from 0 to 3 V and the precision is 0.01 V. In ADS, transient simulation is carried out at 31 frequency points from 1 MHz to 1 GHz in logarithm. The total computation time for the simulation is about 450 min.

Figure 16. DPI algorithm comparison of simulation and measurement

B. Susceptibility Mechanism Analysis

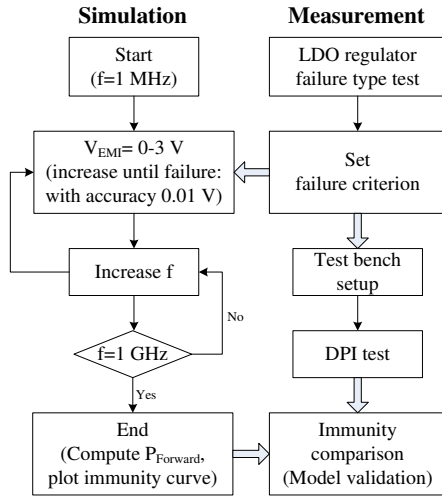There are two cascode op-amps in the regulator circuit, as shown in Fig. 1. For the op-amp in the bandgap reference, there are three paths for disturbance coupling as illustrated in Fig. 19: Ⅰ from V_{IN} to the common node "X" of the PMOS differential pair via the parasitic capacitors C_S (C_S represents the parasitic capacitance between V_{IN} and X) and C_{GS} (gate-to-source capacitance of M1 and M2); Ⅱ from the output to the inverting and non-inverting inputs via the feedback circuit and the Ⅲ one, C_N (C_N represents the parasitic capacitance between "X" and the substrate) which offers a possible path for disturbance to be coupled from the substrate. For the op-amp in the regulator output, the Ⅰ path is also from V_{IN}. The non-inverting input includes the disturbance from the bandgap output; inverting input carries the noise from op-amp output by the follower structure.
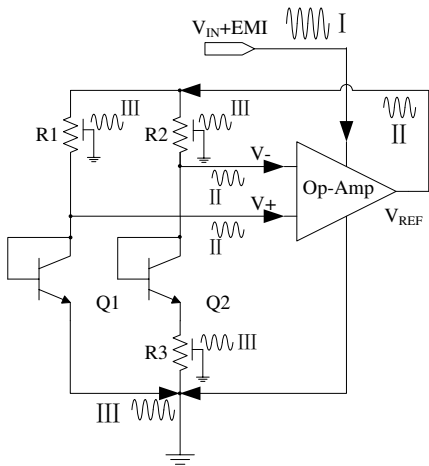

Figure 17. Three disturbance coupling paths in the bandgap reference circuit

This part reuses known works about immunity of bandgap and op-amp to propose a hypothesis about the origin of the susceptibility level. Numerous publications such as [13]-[14] have highlighted the fundamental role of op-amp differential input in the mechanism of generation the DC offset in presence of EMI.
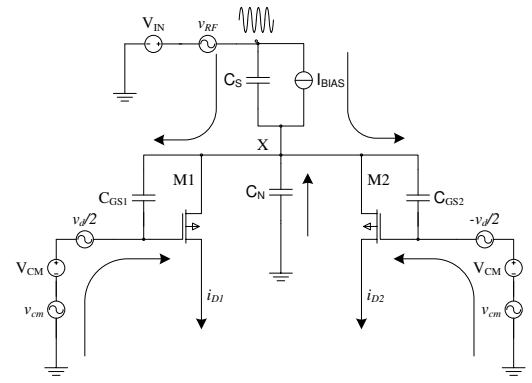

Figure 18. Input PMOS differential pair under interference from power pin and differential pair inputs

C. DPI Simulation Results based on transistor-level model

Building an accurate LDO model under EMI constraints is a difficult task due to the complexity of the interference propagation. Several types of model (Version 1-4: V1-V4) from simplified to complicated levels with improved loads, were evaluated, as well as a PCB model at the PDN level with more parasitic elements in the building blocks of the regulator. The matching between DPI simulations and measurements was then analyzed to evaluate the model relevance.

Table. II shows the comparison between four models over three frequency ranges F1-F3, which cover three successive decades (F1: 1-10 MHz; F2: 10-100 MHz; F3: 100-1000 MHz). A qualitative criterion was assigned as 'good', 'not bad' or 'poor' (good = an average difference of +/- 0.1 V between measurement and simulation over a frequency interval, not bad = an average difference between +/- (0.1 to 0.3) and poor = an average difference of more than +/- 0.3 V) to define the correlation between simulations and measurement results.

TABLE II Model descriptions and evaluations in frequency domains

	Description	F1	F2	F3
V1	Basic circuit from chip design No parasitic elements in IB No PDN	Good	Poor	Poor
V2	Add package and decoupling model Add parasitic elements of loads Add PCB track model	Good	Poor	Poor
V3	Add parasitic capacitors for MOSFETs Add equivalent model of 250 kΩ poly resistor in bandgap circuit Add parasitic capacitors of input differential pair of op-amp	Good	Good	Not bad
V4	Improve PCB track model Improve output buffer model Update parasitic capacitors of input differential pair of op-amp	Good	Good	Good

Model V1 comprises the basic LDO schematic with output loads and without any PDN and parasitic elements in the regulator building blocks. The mean values of the bandgap reference circuit output and regulator output were monitored to determine the failure criterion. Then we compared the simulation result with the measurement result. The result is illustrated in Fig. 19. Over the frequency range F1, the basic model V1 can predict the immunity of the LDO regulator. However, the prediction accuracy is poor over the frequency intervals F2 and F3.
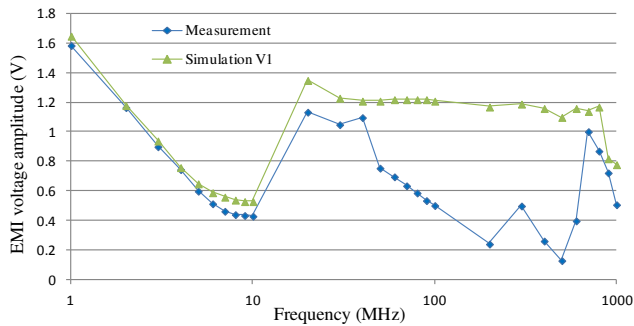
Figure 19. Comparison between DPI measurement and simulation (V1)

Model V2 comprises a PDN model, including package, decoupling capacitor, parasitic load elements and the PCB track. According to Fig. 20, there is no significant improvement over the F2 and F3 intervals, except for the interval from 700 MHz to 1 GHz. Below 700 MHz, the accuracy of the immunity prediction depends mainly on the models of the regulator building blocks. Above 700 MHz, the parasitic effects of bonding, packaging and the PCB are dominant for immunity prediction.
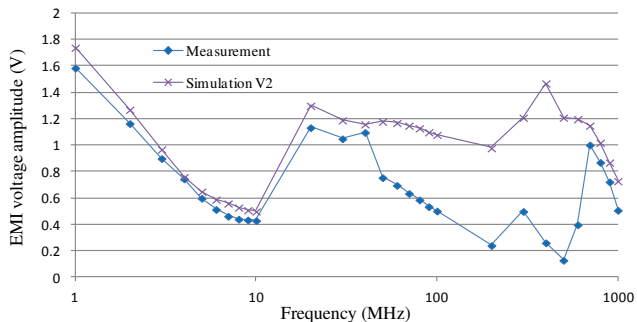

Figure 20. Comparison between DPI measurement and simulation (V2)

In model V3, most of the modifications focus on IB model improvements. The key improvement consisted of the parasitic capacitors C_S and C_N. We then updated the parasitic capacitance C_{GS} of the op-amp input PMOS differential pair. An equivalent model of the 250 kΩ poly resistor in the bandgap reference circuit was built, since it functions as a capacitance (polysilicon-well-substrate capacitances) above 100 MHz [14]. In [23], the author describes a detailed poly resistor model for the bandgap, with the N-well being connected to the power supply where EMI is added. In our case, however, the N-well is connected to the circuit ground which can improve the immunity when noise comes from the power pin. As depicted in Fig. 21, a perfect matching in ranges F1 and F2 is achieved thanks to the parasitic elements working as EMI propagation paths, but in range F3 the model still needs to be improved between 300 and 700 MHz.
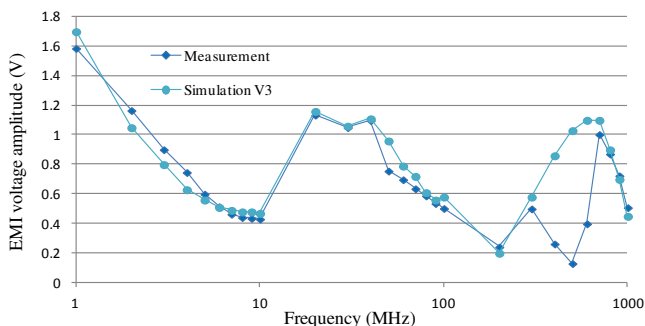

Figure 21. Comparison between DPI measurement and simulation (V3)

Model V4 is an improved version based on V3. An equivalent model of the output buffer was validated to improve simulation efficiency. A more accurate PCB track model was updated for better resonance matching in range F3. The values of C_S (100 fF) and C_N (50 fF) are fixed. Considering the effects of the substrate, C_N is connected to a simplified substrate instead of an ideal circuit ground which is more realistic. In general, the simulation result illustrated in Fig. 22 shows good matching over the frequency intervals F1 to F3. In Fig. 21, the measurement and simulation difference is relatively high from 300 MHz to 700 MHz. At 500 MHz, the difference even reaches 0.9 V. Around 500 MHz, as the LDO regulator has the highest susceptibility level, underestimation of the susceptibility level is the most critical. Compared with model V3, V4 has an improvement between 200 and 600 MHz, but the accuracy is degraded between 20 and 200 MHz. The limitation exists in full consideration of every parasitic and substrate element in the LDO model for interference propagation.
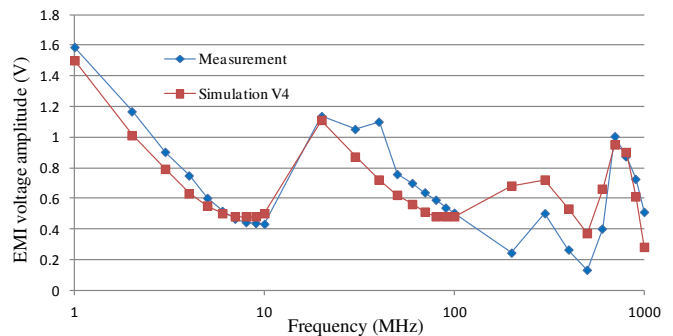

Figure 22. Comparison between DPI measurement and simulation (V4)

VI. CONCLUSION AND FURTHER WORK

This paper presents LDO regulator functional, impedance and immunity modeling and simulations. Several types of models are described from simplified ones to physics-based ones with improved loads and a PCB model at the PDN level, and more parasitic elements at the IB level. The contributions of every change in the LDO immunity models are obvious once compared with DPI measurement results. The PDN model mainly affects the immunity at high frequencies of about several hundred MHz. The precision of the PCB track model determines the right resonance of the immunity level. For conducted interference, the most important elements are the parasitic capacitance and resistance. C_S/C_N and C_{GS} provide direct paths for noise propagation from power/ground to the input differential pair which is crucial for generating a DC offset. A precise model of the substrate is also very important. These conclusions could be useful for IC designers wanting to simulate immunity of ICs including LDO regulator circuits.

Future work will focus on increasing understanding of more accurate parasitic and substrate elements in order to improve transistor-level models. The models described above will also be used for simulating LDO regulator ageing. More attention will be paid to improving op-amp and bandgap reference circuits in order to make useful suggestions to IC design groups for better LDO regulator immunity. Furthermore, design guidelines can be summarized for IC designers to reduce the redesign cost for IC vendors.

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