Modeling and Simulation of Parasitic NPN ESD

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Abstract. Electro-Static Discharge (ESD) is critical for the reliability of integrated circuits. Applying ESD model in circuit simulation could help to predict and avoid potential failure caused by ESD. This paper proposes a SPICE macro model for parasitic NPN ESD and related methods for extracting SPICE model parameters. The macro model utilizes the Taylor series to express collector current of NPN transistor under avalanche breakdown, and thus solves the problem of lack of convergence in prior models. The macro model's parameters are obtained by device measurement together with curve fitting. A device with parasitic NPN was fabricated in SMIC with 0.18um BCD process to verify the macro model. Chip tests indicate that the simulation results of the device's macro model exactly match with the real ESD characteristics of the device, which demonstrate the validity of the macro model for parasitic NPN ESD behavior in circuit simulations.

Introduction

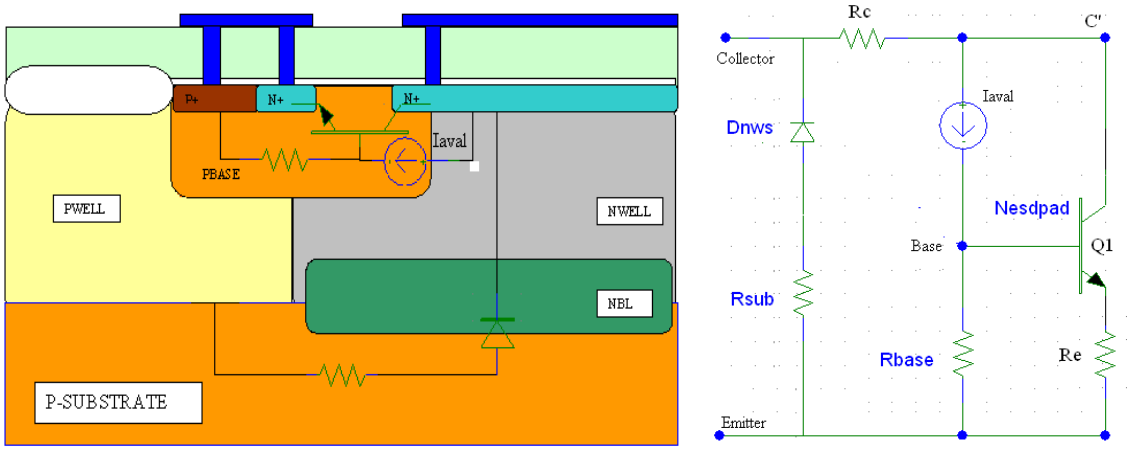
ESD (Electro-Static Discharge) is a serious threat to the reliability and yield of integrated circuits. ESD stress currents flowing into internal circuits may cause unrecoverable damage, so it is necessary to provide ESD protection to integrated circuits [1-6]. At present, ESD stress tests are performed during trial manufacture. If these tests are failed, a conventional approach to response is investigating the cause of the ESD damage and reexamining the design rule and process conditions. Such approach leads to high expense and time waste. Therefore, it is important to predict ESD behavior, potential failure and test damage resistance before trail manufacture. Performing ESD simulation to protection circuits during circuit design and layout is an effective approach for solving the foregoing problem [7, 8]. This paper presents a SPICE macro model for NPN ESD. The SPICE model parameters are extracted based on ESD device measurement. The macro model is verified by experimental data which demonstrates the validity of the macro model for NPN devices in ESD circuit simulations.

An Equivalent Circuit for a Parasitic NPN ESD

Fig. 1(a) shows a cross-sectional diagram of a typical parasitic NPN ESD in a BCD process, Fig. 1(b) shows an equivalent circuit of the parasitic NPN ESD, comprising an NPN transistor Q1 and some parasitic elements.

D_{nws} refers to the parasitic diode between the N-well and P-substrate. R_{sub} refers to the parasitic resistor in the P-substrate. R_{base} refers to a total base resistance, equaling to a sum of resistances of the Pbase resistor and contact resistor. R_c and R_e respectively refer to the parasitic resistor of collector and the parasitic resistor of emitter. The on-resistance R_{on} in the high current linear region after device snapback is approximately complied to the following equation, $R_{on}=R_c+R_e$. I_{aval} refers to a controlled current source to represent the hole injection current when the C-B junction is under avalanche breakdown region.

$$I_{aval} = (M-1)I_c \tag{1}$$



(a) Cross section (b) its equivalent circuit

Fig. 1. A typical Parasitic NPN ESD

Where M is the avalanche multiplication factor [9]

$$M = \frac{1}{1-(V_{cb}/BV_{cb})^n} \tag{2}$$

V_{cb} refers to a biased voltage on the C-B junction and BV_{cb} represents a breakdown voltage of C-B junction.

Avalanche Multiplication

Directly applying formula (1) or (2) into prior SPICE simulators returns an incorrect result indicating that a snapback phenomenon emerges. The reason is that when $V_{cb} \rightarrow BV_{cb,}$ and $M \rightarrow \infty$, the simulating result is lack of convergence. Thus an adjustment to formula (1) is necessary for obtaining a convergent result of SPICE simulation.

$$M = \exp(m) \tag{3}$$

Wherein

$$m = \ln\left(\frac{1}{1-(V_{cb}/BV_{cb})^n}\right) = -\ln(1-(V_{cb}/BV_{cb})^n) \tag{4}$$

According to the Taylor series

$$\ln(1-x) = -x - \frac{x^2}{2} - \frac{x^3}{3} - \ldots \quad \text{for} \quad |x| < 1 \tag{5}$$

The m could be expressed as

$$m = \left(\frac{V_{cb}}{BV_{cb}}\right)^n + \frac{1}{2}\left(\frac{V_{cb}}{BV_{cb}}\right)^{2n} + \frac{1}{3}\left(\frac{V_{cb}}{BV_{cb}}\right)^{3n} + \ldots \frac{1}{x}\left(\frac{V_{cb}}{BV_{cb}}\right)^{xn} \tag{6}$$

To reduce the calculation work, only the first three series are retained, and the others are approximated as R.

$$m = \left(\frac{V_{cb}}{BV_{cb}}\right)^n + \frac{1}{2}\left(\frac{V_{cb}}{BV_{cb}}\right)^{2n} + \frac{1}{3}\left(\frac{V_{cb}}{BV_{cb}}\right)^{3n} + R \tag{7}$$

Wherein R is expressed as

$$R = \frac{1}{4}k_1\left(\frac{V_{cb}}{BV_{cb}}\right)^{k_2 \cdot n} \tag{8}$$

Then, the avalanche multiplication factor M could be expressed as

$$M = \exp\left(\left(\frac{V_{cb}}{BV_{cb}}\right)^n + \frac{1}{2}\left(\frac{V_{cb}}{BV_{cb}}\right)^{2n} + \frac{1}{3}\left(\frac{V_{cb}}{BV_{cb}}\right)^{3n} + \frac{1}{4}k_1\left(\frac{V_{cb}}{BV_{cb}}\right)^{k_2 n}\right) \tag{9}$$

Wherein, k_1 and k_2 are parameters which are extracted by fitting M-V_{cb} curve. The I_{aval} in

formula (1) could be expressed as

$$I_{aval} = (\exp(\left(\frac{V_{cb}}{BV_{cb}}\right)^{n} + \frac{1}{2}\left(\frac{V_{cb}}{BV_{cb}}\right)^{2n} + \frac{1}{3}\left(\frac{V_{cb}}{BV_{cb}}\right)^{3n} + \frac{1}{4}k_1\left(\frac{V_{cb}}{BV_{cb}}\right)^{k_2 n}) - 1)I_c \tag{10}$$

The multiplication factor M may be measured by determining the charge current flowing across the collector barrier as a function of the collector-base reverse bias voltage V_{cb} under a constant emitter current. According to [10],

$$I_c = M\alpha I_e \tag{11}$$

Wherein α is the forward current gain of common-base BJT before avalanche breakdown. It could be easily obtained by measuring I_c and I_e before avalanche breakdown.

The multiplication factor M could be expressed as

$$M = \frac{I_c}{\alpha I_e} \tag{12}$$

And the multiplication factor M could be obtained by measuring I_c and I_e after avalanche breakdown.

Formula (2) could be expressed as,

$$\ln(1 - \frac{1}{M}) = n\ln(V_{cb}) - n\ln(BV_{cb}) \tag{13}$$

$\ln(1 - M^{-1})$ Vs. $\ln(V_{cb})$ is a simple linear relationship. A linear line is obtained as shown in Fig. 2 by measuring M at different V_{cb}, The n and BV_{cb} could be extracted from this linear line shown in Fig. 2. It could be easily obtained that $n=4$ and $BV_{cb}=15$.

The line 1 in Fig. 3 shows an I-V curve depicted according to formula (2) with BV_{cb}=15 and n=4. The value of k_1 and k_2 in formula (9) could be obtained by fitting the I-V curve depicted according to formula (2). The line 2 in Fig. 3 shows an I-V curve depicted according to formula (9) with BV_{cb}=15, n =4, k_1 =44.01 and k_2=136.9.

A Macro Model for the Parasitic NPN ESD

The total base resistance could be simply obtained from Ohm's law

$$R_{base} = \frac{V_{BE,on}}{I_{t1}} \tag{14}$$

Where I_{t1} is the triggering current at the onset of snapback, and $V_{BE,on}$ is the base-emitter diffusion voltage. The voltage is approximately equal to the turn-on voltage and typically $V_{BE,on}$ =0.7~0.8V.

R_c is equal to the slope of I_C Vs. V_{ce} curve when the NPN parasitic transistor is working in saturated region and R_e can be obtained by determining the base current I_b as a function of voltage V_{ce} when the collector is open. R_{on} is obtained by extracting the slope of the linear high current I-V characteristics after snapback. The value of R_c and R_e are complied with the following formula

$$R_{on} = R_c + R_e \tag{15}$$

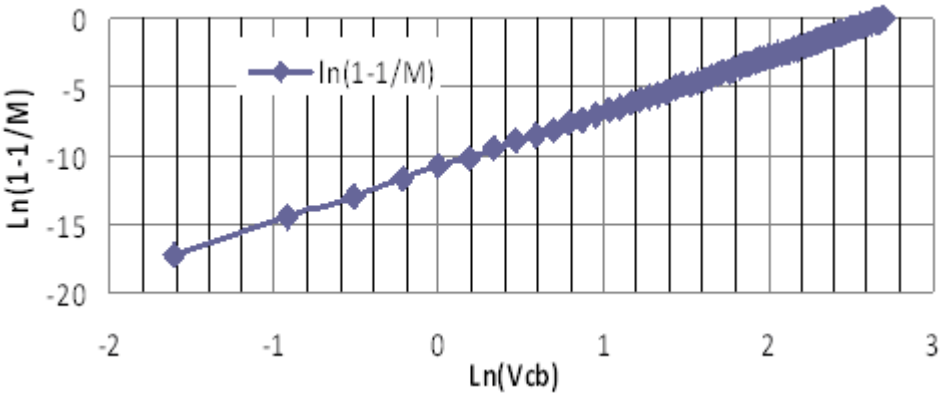


Fig. 2. ln(1-1/M) Vs. Ln(Vcb)

The diode D_{nws} is configured to provide ESD protection at PS mode. The parameter of diode D_{nws} is extracted on the basis of SPICE diode model. R_{sub} is the sum of the ohmic resistance and the substrate resistance.

Fig. 4 shows a schematic sub-circuit diagram based on PSPICE [11]. Compared with the equivalent circuit in Fig. 1(b), an voltage controlled current source (VCCS) Gaval is utilized to replace the current source Iaval, and a 0V voltage source V1 is utilized to test the collector current of Q1. Table 1 describes a PSPICE syntax macro model. The macro model utilizes the Taylor series shown in formula (10) to express the collector current after avalanche breakdown, and thus solves the problem of lack of convergence in prior models. The measured resistances of R_{base}, R_c , R_e and R_{sub} are directly incorporated into the model for easier expression.

Simulation Results and Chip Tests

The proposed parasitic NPN ESD was fabricated in SMIC with 0.18um BCD process to verify the macro model. Fig. 5(a) and Fig. 5(b) show comparisons of DC characteristic between results of PSPICE simulation and chip test. Fig. 5(a) shows a linear I-V curve comparison before and after device snapback, while Fig. 5(b) shows a log I-V curve comparison. The two figures demonstrate that the simulation result perfectly matches with practical snapback characteristics, and thus the model could accurately present device snapback. The error between the results of simulation and chip test may attribute to the high order terms of Taylor series omitted in formula (7).

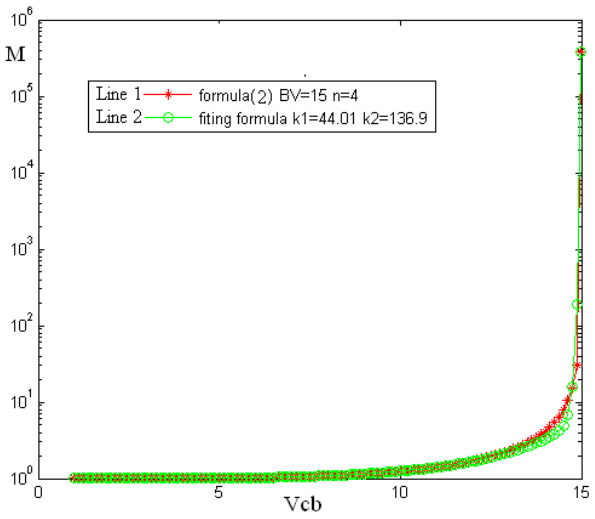


Fig. 3. Multiplication factor fitting

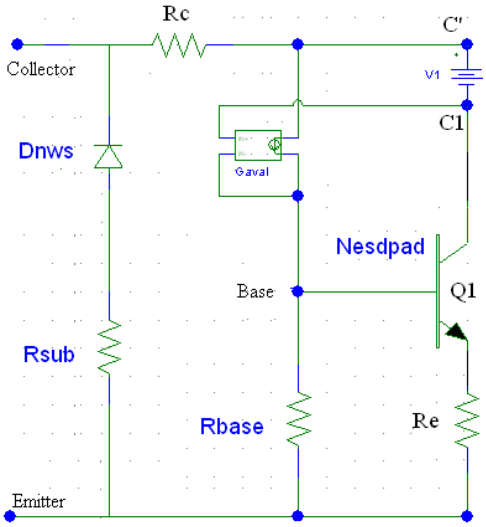


Fig. 4. ESD sub-circuit

Table 1 A PSPICE syntax macro model

```
.SUBCKT    ESD7    pad    VSS
V_V1                c c1 0V
Gaval c b VALUE { (EXP(PWRS(V(c1,b)/BV, +n)+PWRS(0.5*V(c1,b)/
BV,2n)+PWRS(0.333*V(c1,b)/BV,+3n)+0.25k2*PWRS(V(c1,b)/BV,
k2))-1)*I(V_V1) }
Re                VSS e    0.8748
Rb                VSS b    21
Rsub              VSS psub    1.214
Rc                pad c    4.35
Dnws               psub pad Dnws    1
QNesd             c1 b e NQesd    1
.ENDS    ESD7
.model NQesd    npn
.MODEL Dnws    D
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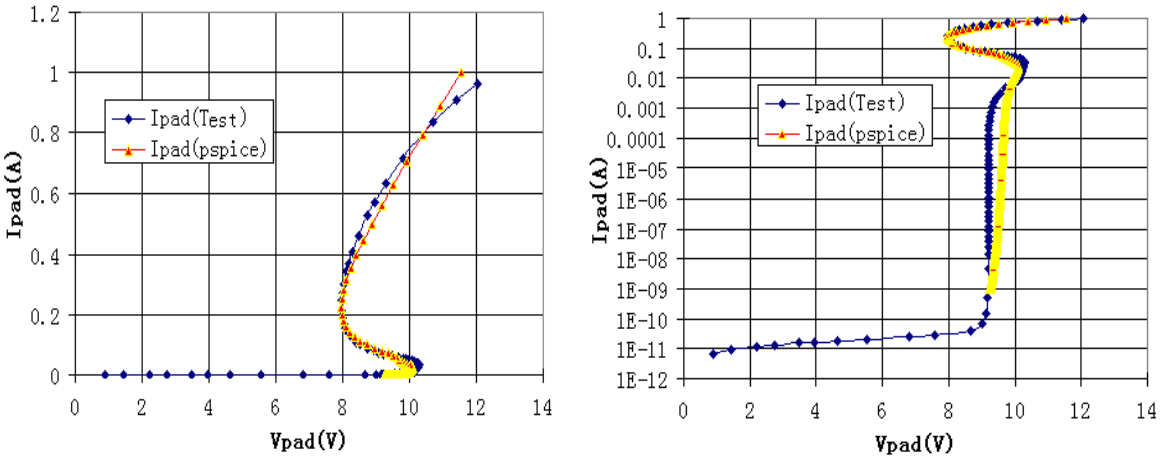
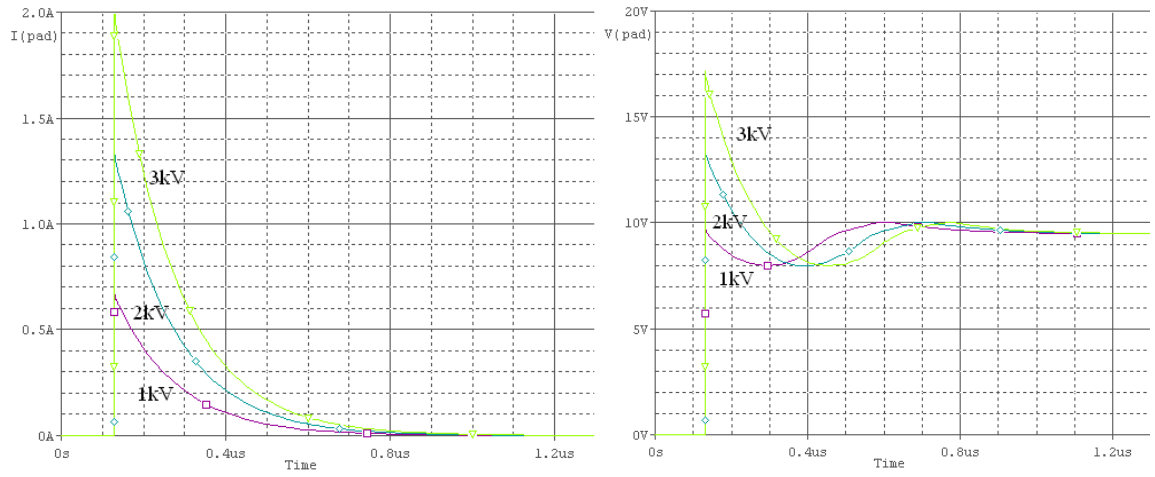


(a) Linear axis (b) Log axis

Fig. 5. Snapback characteristics of NPN ESD, simulation results are compared with test results

Fig. 6(a) and Fig. 6(b) show PSPICE simulation results of ESD human body mode discharge. Fig. 6(a) shows current transient responses of human body mode discharge under different discharge voltages. Fig. 6(b) shows voltage transient responses of human body mode discharge under different discharge voltages.



(a) Current (b) Voltage

Fig. 6. Human body model discharge PSPICE simulation results

Conclusion

A SPICE macro model for NPN protection devices is proposed in this paper. The macro model utilizes the Taylor series to express the collector current under avalanche breakdown, and thus solves the problem of lack of convergence in prior models. The model parameters are extracted based on device measurement, and the model accurately matches device's snapback characteristics. The paper also performed an ESD circuit simulation based on the proposed macro model. The simulation results of the macro model exactly match with the results of chip test, and the macro model could be widely used in various parasitic NPN ESD, and it helps to avoid device failures caused by ESD.

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References

[1] LI Z, MAHESHWARI P, POMMERENKE D J. Measurement methodology for field-coupled soft errors induced by electrostatic discharge[J]. IEEE Transactions on Electromagnetic Compatibility, 2016, 58(3): 701–708.

[2] SITHANANDAM R, KUMAR M J. A novel cascade-free 5-V ESD clamp using I-MOS: proposal and analysis[J]. IEEE Transactions on Device and Materials Reliability, 2016, 16(2):200-207.

[3] MA R, CHEN Q, ZHANG W, et al. A dual-polarity graphene NEMS switch ESD protection structure[J]. IEEE Electron Device Letters, 2016, 37(5): 674–676.

[4] CHEN Q, MA R, ZHANG W, et al. Systematic characterization of graphene ESD interconnects for on-chip ESD protection[J]. IEEE Transactions on Electron Devices, 2016, 63(8): 3205–3212.

[5] ZHANG T, GUI P, CJAKRABORTY S, et al. 10-Gb/s distributed amplifier-based VCSEL driver IC with ESD protection in 130-nm CMOS[J]. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24(7): 2502-2510.

[6] VOLDMAN S H. The state of the art of electrostatic discharge protection: physics, technology, circuits, design simulation, and scaling[J]. IEEE Journal of Solid-State, 1999, 34(9):1272-1282.

[7] MENG K H, SHUKLA V, ROSENBAUM E. Full-component modeling and simulation of charged device model ESD[J]. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35(7): 1105–1113.

[8] MERGENS M P J, WILKENING W, KIESEWETTER G, et al. ESD-level circuit simulation-impact of gate rc-delay on HBM and CDM behavior[M]. Proc. EOS/ESD Symp., 2000:446-455.

[9] SZE S M, Physics of semiconductor devices[M]. Second Edition, Wiley, New York, 1981:451-452.

[10] GRAY P R, HURST P J. Analysis and design of analogue integrated circuits[M], Fourth Education, Higher Education Press, 2003,10:20-22.

[11] Cadence Design Systems, Inc. PSPICE user's guide[M].