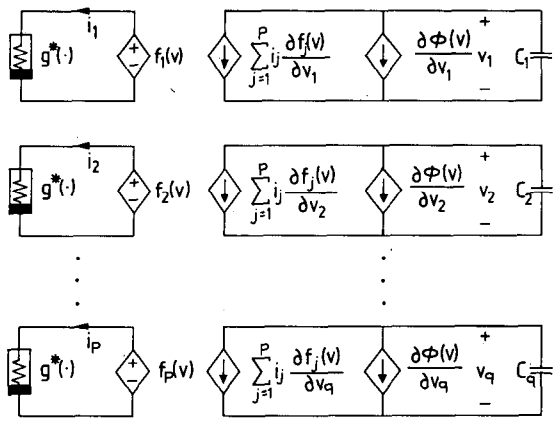

Fig. 6. Canonical nonlinear programming circuit: dynamic model.

The nonlinear programming circuit of Chua and Lin [3] is *canonical* in the sense that it provides the simplest circuit capable of solving the nonlinear programming problem. Infinitely many circuits, not necessarily reciprocal but each obeying the same unifying stationary principle [2] and having the same dc solution, can be derived from this network by bijective mappings. The linear programming problem represents the *simplest special case* of the canonical circuit, since it is reciprocal, and one can therefore apply the stationary cocontent theorem [2] directly.

To demonstrate that the *modified* Hopfield linear programming network described above does indeed optimize the solution to the problem as proposed, a network to implement the example of Tank and Hopfield [1] was built, and the solution recorded. Four linear cost functions were considered, corresponding to different orientations of the cost plane, and in each case the experimental and theoretical results are in close agreement and correspond to stable fixed points of the system.

VI. Concluding Remarks

The reciprocal linear programming circuit of Tank and Hopfield [1], when modified to operate as intended, reduces to the canonical nonlinear programming circuit of Chua and Lin [3] (of which it represents the simplest special case), and has been shown to obey the same unifying stationary principle for nonlinear circuits [2].

The "energy" function $E(v)$ of Tank and Hopfield [1] is simply the total cocontent function of their network. The circuit dynamics cause the solution to seek a minimum of $E(v)$ which, for the canonical circuit, corresponds to the desired minimum of the cost function $\phi(v)$. Allowing for nonideal behavior in the real implementations of this scheme, such as that proposed by Tank and Hopfield, we find that the solution still seeks out a *minimum of the total cocontent function*. This may not correspond to the desired solution of the linear programming model considered if the parasitic conductances are not sufficiently small, and the nonlinearity not appropriately shaped.

Acknowledgment

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Modeling Charge Injection in MOS Analog Switches

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***Abstract*—Charge injection in MOS switches has been analyzed. The analysis has been extended to the general case of including source resistance and source capacitance. Universal plots of percentage channel charge injected are presented. Normalized variables are used to facilitate usage of the plots. A small-geometry switch, slow switching rate, and small source resistance can help reduce the charge injection effect.**

I. Introduction

One major limitation to the accuracy of a sample-and-hold circuit is the disturbance of the sampled voltage when the MOS switch turns off. The majority of sample-and-hold circuits are implemented using MOS technologies because the high input impedance of MOS devices performs excellent holding functions. When the switch connecting the signal-source node and the data-holding node is turned on, the sampling function is performed. After the switch is turned off, the data appearing in the holding node will be held until the next operation step occurs. In general, an MOS switch is not an ideal switch. A finite amount of mobile charge is stored in the channel when an MOS transistor is on. When the transistor turns off, the channel charge disappears through either the source/drain electrodes or the substrate electrode. The channel charge being transferred to the data node superposes an error component to the sampled voltage. In addition to the channel charge, the charge associated with the feedthrough effect of the gate-to-diffusion overlap capacitance enlarges the error voltage [1]. This charge injection phenomenon was identified in the early stages of switched-capacitor circuit development. Various compensation schemes [2], [3] have been used to cancel the switch charge injection to the first order. Comprehensive understanding and detailed analysis of the switch charge injection is needed to improve the accuracy of the MOS circuits. There have been some attempts in the literature to model the switch charge injection. MacQuigg [4] made a qualitative observation and did some SPICE simulation on a simplified case. Sheu *et al.* [1] developed an analytical model corresponding to infinite source capacitance. Experiments were carried out using

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single transistors to verify their model. Wilson *et al.* [5] inserted a two-transistor source follower stage between the interested node and the external prober which shields the loading effect imposed by the external prober. In this letter, analysis of the general case of switch charge injection is described. Universal plots of switch charge injection with normalized variables are included. Experimental results are presented.

II. Analysis

We assume that the charge pumping phenomenon due to the capture of channel charge by the interface traps is insignificant in this analysis. All the channel charge exits through the source and drain electrodes when the transistor turns off. The circuit schematic corresponding to the general case of switch charge injection is shown in Fig. 1. Capacitance C_L is the lumped capacitance existing at the data-holding node. Resistance R_S could be the output resistance of an operational amplifier, while capacitance C_S could be the lumped capacitance associated with the amplifier output node.

Let C_G represent the total gate capacitance, including both the channel capacitance and gate-to-source, gate-to-drain overlap capacitances

$$C_G = WLC_0 + 2C_{0v}. \tag{1}$$

By following the derivation presented in [1], the KCL law at node A and node B requires

$$C_L\frac{dv_L}{dt} = -i'_d + \frac{C_G}{2}\frac{d(V_G - v_L)}{dt} \tag{2}$$

$$\frac{v_S}{R_S} + C_S\frac{dv_S}{dt} = i'_d + \frac{C_G}{2}\frac{d(V_G - v_S)}{dt}. \tag{3}$$

Gate voltage is assumed to decrease linearly with time from the on-value V_H

$$V_G = V_H - Ut \tag{4}$$

where U is the falling rate. When the transistor is operated in the strong inversion region,

$$i'_d = \beta(V_{HT} - Ut)(v_L - v_S) \tag{5}$$

where

$$\beta = \mu C_0\frac{W}{L} \quad \text{and} \quad V_{HT} = V_H - V_S - V_{TE}. \tag{6}$$

Here, V_{TE} is the transistor effective threshold voltage including the body effect. Under the condition $|dV_G/dt| \gg |dv_L/dt|$ and $|dv_S/dt|$, eqs. (2) and (3) simplify to

$$C_L\frac{dv_L}{dt} = -\beta(V_{HT} - Ut)(v_L - v_S) - \frac{C_G}{2}U \tag{7}$$

$$\frac{v_S}{R_S} + C_S\frac{dv_S}{dt} = \beta(V_{HT} - Ut)(v_L - v_S) + \frac{C_G}{2}U. \tag{8}$$

No closed-form solution to this set of equations can be found. Numerical integration can be employed to find the results. Fig. 2 shows the calculated percentage of the channel charge injected to the data-holding node when the source resistance is infinitely large. A dimensionless quantity B, which is equal to $V_{HT}\sqrt{\beta/UC_L}$, has been identified as the driving force of the switch charge injection effect. A family of curves corresponding to various C_S/C_L ratios have been plotted. When the switch turns off, the channel charge exits to the signal-source side and the data-holding side under capacitive coupling and resistive conduction. In the fast switching-off conditions, the transistor conduction chan-

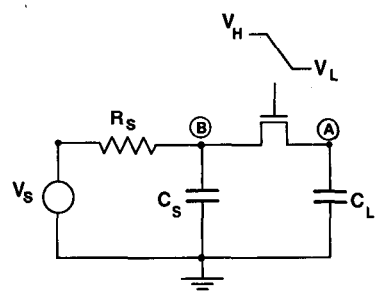


Fig. 1. Circuit for analysis of switch charge injection.

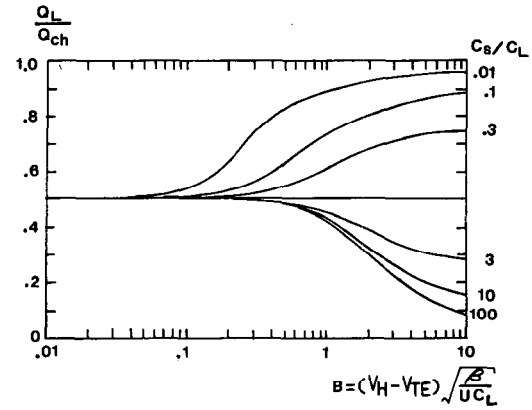
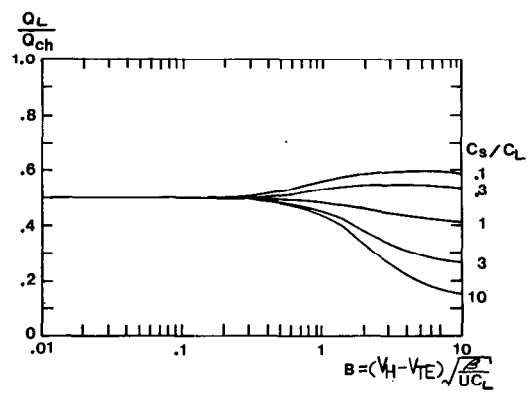
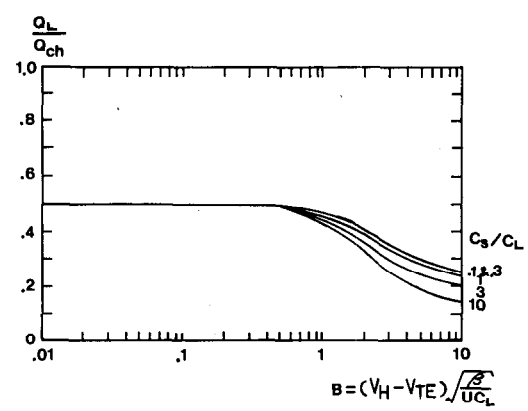


Fig. 2. Percentage of channel charge injected to the data holding node. Source resistance is assumed to be infinitely large in the plots.



(a)



(b)

Fig. 3. Percentage of channel charge injected to the data holding node. (a) Normalized conductance $g = 1$ in the plots. (b) Normalized conductance $g = 5$ in the plots.

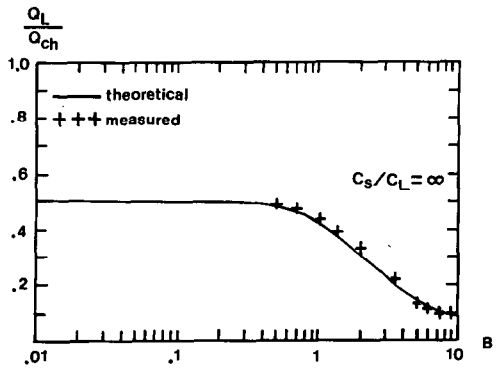


Fig. 4. Measured and theoretical charge injection results.

nel disappears very quickly. There is not enough time for the signal-source side charge and data-holding side charge to communicate. Hence, the percentage of charge injection at the data-holding side approaches 50-percent independence of the C_S/C_L ratio. In the slow switching-off conditions, the communication between the charge at the signal-source side and at the data-holding side is so strong that it tends to make the final voltages at both sides equal. This allows the majority of channel charge to go to the larger capacitance side.

Another important factor in characterizing the switch charge injection is the relative magnitude of the falling rate compared with the signal-source time constant $R_S C_S$. Normalized conductance g, which is equal to $V_{HT}/UR_S C_S$, can be used to monitor this effect. The curves corresponding to two finite g values are shown in Fig. 3(a) and (b). Source resistance effectively offers a leakage path for the channel charge during the switch turning-off period. Hence, a small source resistance will greatly reduce the amount of charge injected into the data-holding node.

III. Experimental Results

The transistors used in the experiments were fabricated using a 3-μm CMOS process. The transistor gate-oxide thickness is 50.0 nm, substrate doping is 10^{16} cm^{-3}, and zero-bias threshold voltage is 0.9 V. The percentage charge injection was measured against the gate voltage falling rate ranging from 1.25×10^6 V/s to 5×10^8 V/s. Fig. 4 shows the measured data and theoretical results. Good agreement is found.

IV. Conclusions

Charge injection is one of the major limitations to the accuracy of sample-and-hold circuits. Charge injection in MOS switches has been analyzed. The analysis has been extended to the general case, which also includes source resistance and source capacitance. This extension makes the results useful for the various conditions encountered in integrated circuit applications. Plots of the percentage charge injection corresponding to various normalized parameters are presented. The source resistance effectively offers a leakage path for the channel charge during the switch turning-off period.

Acknowledgment

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Network Realizability Theory Approach to Stability of Complex Polynomials

N. K. BOSE AND Y. Q. SHI

Abstract—**In this letter, we briefly point out that concepts in network realizability theory provide the basis for a unified approach to stability (or, in general, root distribution) of a polynomial with complex coefficients. Very recent results in the area, then, become easily interpretable. The same approach can be exploited to prove stability results for interval complex polynomials. The counterpart of the basic continuous system result is stated for discrete systems, where a complex polynomial is to be checked for absence of roots on or outside the unit circle. The suggested procedure has capabilities for generalization to the multivariate case. Among other advantages, savings in the computational complexity in the implementation of stability tests on multidimensional filters emerge.**

I. Introduction

Several papers of recent vintage have originated on the root clustering and distribution of univariate polynomials with complex coefficients. The results in [1] are concerned with the location of roots of such polynomials with respect to the principal coordinate axis. There, the central part of the argument dwells on the use of a homotopy approach and Rouche's theorem on analytic functions. In [2], the complex counterpart of the Routh table for real polynomials is developed based on the argument principle in complex variable theory. In both [1] and [2], the nucleus of the development depends on the decomposition of the given polynomial into the sum of two "axially complementary polynomials" [1] (referred to as quasi-real and quasi-imaginary polynomials in [2]). In [2], the table might contain imaginary elements. In [3], a table to test for the zeros of a complex polynomial in the strict left-half plane is given, but the proof has not been completed. In [3], in contrast to [2], the elements in the table are real. A table of real elements similar but not identical to the table in [3] is also given in [10, p. 179].

Complex polynomials are encountered in several applications [4], [5], [10, p. 193]. Bivariate complex polynomials are also now

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