Modeling Differential Through-Silicon-Vias (TSVs) with Voltage Dependent and Nonlinear Capacitance

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***Abstract* — This paper proposes an equivalent lumped element model for the differential Through Silicon Vias (TSVs) with considering the effect of voltage dependent and nonlinear capacitance. The modeling and analysis of the differential signaling with TSVs play a critical role in designing the high performance TSV channel in the three dimensional integrated circuit (3D IC). TSVs have been mostly modeled assuming that the TSV metal insulator semiconductor (MIS) interface is not biased and the silicon substrate is a lossy, low conductive medium. Ignoring the semiconductor properties of the substrate and the resulting MOS capacitance introduce significant inaccuracies in the TSV modeling. In this paper, we investigate the complementary nature of differential signals which introduces a virtual ground and automatically biases the TSV MIS interface, causing carrier accumulation and depletion. Furthermore, the large digital signal swing makes the depletion region change the depletion width dynamically, which introduces a nonlinear and large signal TSV capacitance. The capacitance is modeled analytically and a new equivalent circuit model for the differential TSVs is proposed accordingly. The impact of the voltage dependent and nonlinear capacitance on the performance of high speed differential signals is analyzed through channel simulations with eye diagram approach.**

***Index Terms* — Three Dimensional Integrated Circuit (3D IC), Through Silicon Vias (TSVs), Capacitance, Modeling.**

I. INTRODUCTION

While chip design and fabrication technology have undergone a tremendous evolution, and on-chip clock frequency reaches multi-GHz range, package design has lagged considerably and becomes the bottleneck of high speed system design. With current technology, power and signal integrity are the most important factors to be considered when developing the packaging structures for reliable high speed data transmission and processing. When signal integrity problems happen and the system noise margin requirements are not satisfied, the logic error, data drop, false switching, or even system failure will occur. The noise faults in package are extremely difficult to diagnose and solve after the system is built or prototyped. Three-dimensional integrated circuit (3D IC) is emerging as a natural way to overcome the above power and signal integrity issues [1] [2].

3D IC benefits from smaller footprint area than 2D IC and from vertical interconnections between different dies [3] [4]. Small footprint area of 3D IC allows gates to be placed closer, thereby leading to shorter wire length than 2D IC. 3D chips with Through Silicon Vias (TSVs) going through active chips and can potentially be stacked several dies high. Vertical interconnections by TSV help shorten wire length because gates can be placed on top of each other in different dies, eliminating the need of long cross-chip interconnects existing in 2D IC. This shorter wire length helps alleviate routing congestion, power consumption as well as crosstalk and noise problems. Although TSVs are well known as the most promising 3D stacked chip package technology, the TSVs occupy non negligible silicon area because of their sheer size. Well managed TSVs alleviate congestion, reduce wire length, and improve performance, whereas excessive TSVs not only increase the die area, but also have negative impact on many design objectives. Therefore, an accurate model for TSVs is essential for 3D IC and system design.

There are two conventional signaling methods for TSVs; one is a single-ended and the other one is a differential signaling. Between both signaling methods, many advantages of the differential signaling for the high speed system design were studied such as doubled voltage margin and virtual ground effect [5-7]. The modeling and analysis of single-ended and differential signaling in TSV are quite different. Therefore, the modeling and analysis of the differential signaling with TSVs is significantly important for designing high performance TSV channel in 3D IC.

Recently, many electrical modeling methodologies have been proposed to address the impact of TSVs on high speed signals [8-10], study the TSVs resistance, inductance and capacitance characterization [11-14], as well as analyze the TSVs application on power delivery improvement [15-18] and electromagnetic interference (EMI) reduction [18]. These methodologies can be categorized into three classes based on the types of electromagnetic techniques used: full-wave modeling, quasi-static modeling, and analytical modeling. All these modeling techniques assume that TSV MIS interface is not biased and has no carrier accumulation or depletion due to static biasing or large signals. Silicon substrate is modeled as a dielectric material with a low conductivity. Under these assumptions, TSV MIS structure supports three modes: 1) slow wave mode at low frequencies where the electrical field is

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screened by the silicon substrate and the magnetic field penetrates much further into the substrate; 2) quasi-transverse electromagnetic (TEM) mode when both electrical and magnetic fields penetrate deep into silicon substrate; and 3) skin effect mode at very high frequency when the skin depth in silicon is smaller than TSV spacing. However, when virtual ground associated with differential TSVs biases the TSV MIS interface or the electrical signals carried by TSVs cannot be treated as small signals, the electromagnetic effects at the TSV MIS interface are quite different from what are modeled in the existing methodologies [8-18].

Ref. [19-22] studied the impact of a bias voltage on TSV characteristics (mostly capacitance) theoretically and experimentally. However, these analyses only consider the static biasing and apply for the small signal application. Ref. [23] rigorously modeled the full-wave, both small and large signal wave propagation in a MIS micro strip structure. It requires solving both the full Maxwell equations and Boltzmann transport equation at the same time. The Maxwell equations consider electromagnetic effects and the Boltzmann equation considers carrier transport in semiconductors. Even though the TSVs are small in size and there is no need to consider wave propagation, the Boltzmann equation still needs to be solved simultaneously to consider the carrier accumulation and depletion. It is computationally very intensive. Furthermore, it is very difficult to apply the proposed TSV models to the channel simulations. Therefore, a new circuit model addressing all these issues needs to be discovered.

In this paper, we propose a novel circuit model of the differential TSVs for 3D IC design and analysis. Since the frequent switching of high speed differential signals can dynamically bias the TSV MIS interface and allocate the TSV MIS into the accumulation or depletion regions, the TSV capacitance is expected to be nonlinear and dependent on the biasing of the TSVs with respect to the substrate. Accordingly, an analytical formula is introduced for the large signal and nonlinear capacitance. We verified the proposed analytical formula by comparing it with the *C-V* curve obtained from static simulation and measurement with a static bias. As shown in our test examples, the capacitance obtained from the new model could be up to 97% higher than that obtained from conventional models. Based on this novel capacitance formula, a new circuit model for differential TSVs is proposed. The compact lumped circuit model accounts for wide frequency range, high frequency skin effect, eddy currents in substrate, and MOS effect. We evaluate the circuit model through channel simulations with eye diagram approach. The model's compactness and compatibility with SPICE simulators allows the electrical modeling of various TSV arrangements without the need for computationally expensive field solvers, which significantly reduces the simulation running time. The proposed circuit model could be a promising solution to both academic and industrial need for broadband electrical modeling of TSVs in 3D IC.

II. Nonlinear, Large Signal Capacitance of Differential TSVs

A. *Self-Biased Differential TSVs*

The basic structure of a TSV is shown in Fig. 1. In a silicon substrate, a hole is etched out, a thin silicon dioxide layer, called TSV liner, is formed, and a conductive via is plated. A TSV is essentially a MIS device.

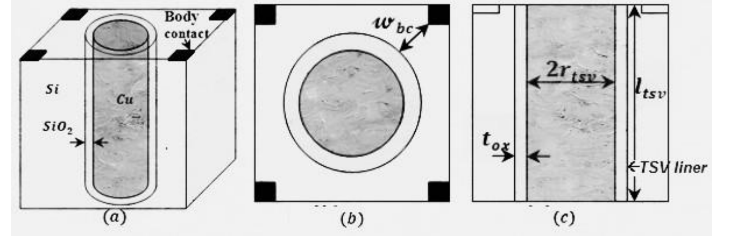

Figure 1: TSV Structure (a) 3D View, (b) Top View, and (c) Side View

Figure 2 shows the self-biasing of differential TSVs is a pair of TSVs carrying a differential signal. The differential mode has a positive voltage on one TSV and a negative one on the other. There is a virtual electrical ground in the silicon substrate in order satisfy the voltage boundary conditions at the TSVs as shown in Fig. 3.

The maximum voltage difference between the differential signal TSVs and the virtual ground is:

$$V_{diff} = +/- \frac{V_{pp}}{2}, \tag{1}$$

where V_{pp} is the peak-to-peak differential signal swing. This voltage difference with respect to the silicon substrate biases the TSV MIS interface. Since differential signals change versus time rapidly, the biasing will be dynamic.

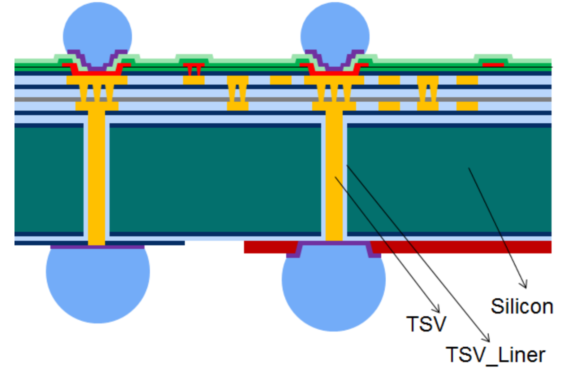

Figure 2: Self-biasing of Differential TSVs Structure

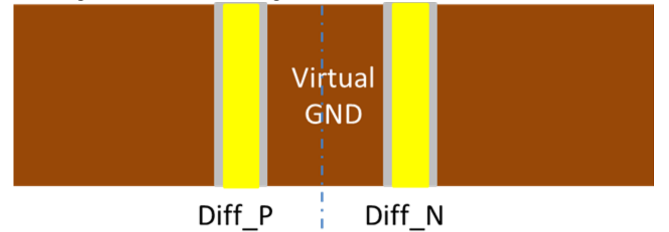

Figure 3: Differential TSVs and Virtual Ground

B. TSV MIS in Accumulation and Depletion Regions

When a TSV MIS interface is biased statically, the TSV MIS will be in the accumulation or depletion regions. Since most of silicon interposers are made from p-type silicon substrate, we will derive based on p-type substrate. Similar results are expected to apply to n-type substrate cases.

In a p-type substrate, the majority carriers are positively charged holes. A flat band voltage (V_{FB}) can be defined for MIS interface and it corresponds to the voltage that induces zero net charge in silicon. If there is no charge present in the oxide or at the oxide-semiconductor interface, the flat band voltage (V_{FB}) simply equals the work function difference between the gate metal and the semiconductor. The work function is the voltage required to extract an electron from the Fermi energy to the vacuum level. The flat band voltage (V_{FB}) is defined as:

$$V_{FB} = \varphi_m - \varphi_{si} - \frac{Q_S}{C_{ox}}, \tag{2}$$

where φ_m and φ_{si} are the work functions of TSV metal and silicon, respectively, Q_s is the space charge, and C_{ox} is the silicon liner capacitance.

When a voltage V is applied to a TSV, if $V < V_{FB}$, the positively charged holes in silicon are dragged to Si-SiO2 interface, and an accumulation layer is formed, as shown in Fig. 4; if $V > V_{FB}$, holes are pushed away and a depletion region is formed, as shown in Fig. 5. V_{FB} depends on material properties as well as fabrication processes (doping, etc.). V_{FB} can vary in a wide range. Note that the non-biasing assumption, or the flat band condition ($V = V_{FB}$) is usually not valid.

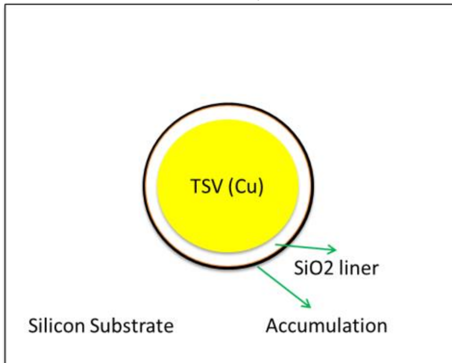

Figure 4: TSV MIS in Accumulation Region

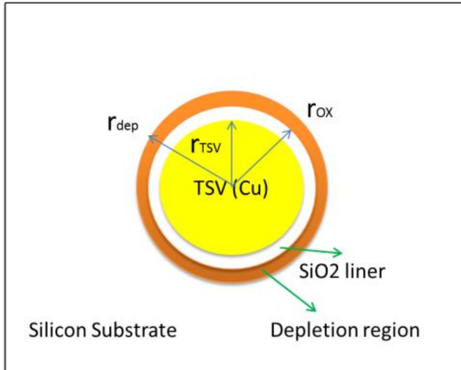

Figure 5: TSV MIS in Depletion Region

C. TSV Capacitance Equations

Planar MOS Capacitor structures are well known and have been studied extensively in literature [23-26]. The capacitance of a MOS capacitor varies with change in the gate voltage as shown in Fig. 6.

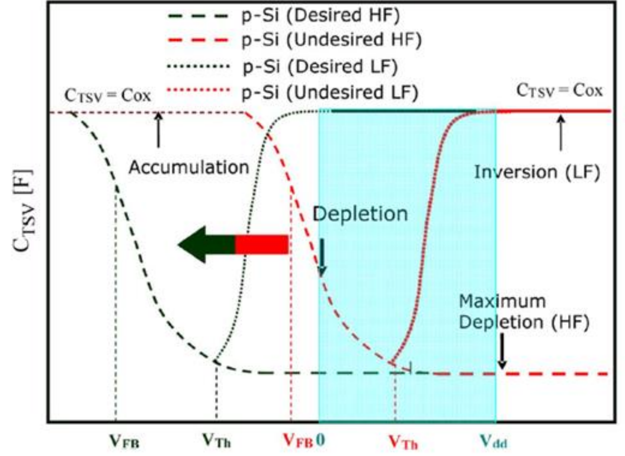

Figure 6: Typical Capacitance vs. Gate Voltage Plot for Planar MOS Capacitance [23].

When the TSV MIS is in the accumulation region, the electrical field is confined in the SiO_2 liner. As shown in Fig. 6, the TSV capacitance is equal to C_{ox}, which is the capacitance of the SiO_2 liner. C_{ox} can be calculated through equation (3):

$$C_{ox} = 2\pi\varepsilon_{ox}\frac{h}{\ln(\frac{r_{ox}}{r_{TSV}})}, \tag{3}$$

where h is the TSV height, ε_{ox} is the dielectric constant of the SiO_2 liner , r_{TSV} is the radius of the TSV, and r_{ox} is the radius of a TSV with SiO2 liner in the accumulation region.

When TSV MIS is in the depletion region, the electrical field can penetrate into the substrate, and the TSV capacitance is equal to C_{ox} in series with C_{dep}, which is defined as the capacitance of the depletion region. To calculate the depletion capacitance C_{dep}, we first need to figure out how to calculate depletion width (as shown in Fig. 5) since the large digital signal swing makes the depletion region to change its depletion width dynamically. The depletion width w_{dep} is defined as:

$$w_{dep} = r_{dep} - r_{ox}. \tag{4}$$

The depletion width w_{dep} can be calculated by solving a Poisson's equations of scalar potential in the depletion region and a Laplace's equation in the SiO_2 liner.

Space oxide charges and interface trapped charges are assumed to be zero. Therefore, when the distance (r) between the target point (in SiO2 liner) and the center point of the TSC is larger than r_{dep}, the charge density of the target point is nearly zero [11] and expressed as:

$$\rho(r) \approx 0. \tag{5}$$

When the distance (r) between the target point and the center

point of the TSC is larger than r_{ox} and smaller than r_{dep} ($r_{ox} < r < r_{dep}$), the charge density of the target point could be defined as [11]:

$$\rho(r) \approx qN_a, \tag{6}$$

where N_a is the silicon doping concentration, q is the electronic charge ($1.6022*10^{-19}$ coulombs). Therefore, the potential and electrical field in the depletion region should satisfy the equation (7):

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \phi}{\partial r}\right) = \frac{\rho}{\varepsilon_{si}} = -\frac{q}{\varepsilon_{si}}(-N_a + p - n), \tag{7}$$

where ϕ is the potential, ε_{si} is the dielectric constant of Si. Equation (7) is derived from the Poisson's equation in cylindrical co-ordinates. The equation (7) could be simplified as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \phi}{\partial r}\right) = \frac{q}{\varepsilon_{si}}N_a. \tag{8}$$

The potential and electrical field in the SiO2 liner should satisfy the equation (9):

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \phi}{\partial r}\right) = 0. \tag{9}$$

The electrical field at the edge of the depletion region ($r = r_{dep}$) is zero:

$$E = -\frac{\partial \varphi}{\partial r} = 0, \tag{10}$$

and φ and $\varepsilon_r \partial\varphi / \partial r$ are continuous at $r = r_{ox}$.

When a voltage V is applied to a TSV, we have

$$V - V_{FB} = \varphi \quad (r = r_{TSV}),$$

when φ is set to zero in the silicon substrate. Solutions to above differential equations yield the following equation to solve for r_{dep}:

$$V - V_{FB} = \frac{qN_a r_{ox}^2}{2\varepsilon_{ox}}\left(1 - \frac{r_{dep}^2}{r_{ox}^2}\right)\ln\left(\frac{r_{TSV}}{r_{ox}}\right) - \frac{qN_a}{2\varepsilon_S}\left(\frac{r_{dep}^2 - r_{ox}^2}{2} + r_{dep}^2 \ln\left(\frac{r_{ox}}{r_{dep}}\right)\right) \tag{11}$$

Depletion width w_{dep} is usually sub-micron in silicon substrates [11-13]. The SiO_2 liner thickness (t_{ox}) which is denoted as:

$$t_{ox} = r_{ox} - r_{TSV}, \tag{12}$$

is also submicron [8] [9]. Therefore, we have the following equations for the relationship between w_{dep}, t_{ox} and r_{ox}:

$$\frac{w_{dep}}{r_{ox}} << 1, \tag{13}$$

$$\frac{t_{ox}}{r_{ox}} << 1. \tag{14}$$

Based on equation (13-14), the equation (11) can be simplified accordingly with the following steps.

$$\left(1 - \frac{r_{dep}^2}{r_{ox}^2}\right) = 1 - \left(\frac{r_{ox} + w_{dep}}{r_{ox}}\right)^2 = 1 - \left(1 + \frac{w_{dep}}{r_{ox}}\right)^2$$
$$\approx 1 - \left(1 + \frac{2w_{dep}}{r_{ox}}\right)$$
$$= -\frac{2w_{dep}}{r_{ox}}$$

$$\ln\frac{r_{TSV}}{r_{ox}} = \ln\left(\frac{r_{ox} - t_{ox}}{r_{ox}}\right) = \ln\left(1 - \frac{t_{ox}}{r_{ox}}\right)$$
$$= -\frac{t_{ox}}{r_{ox}}$$

$$\frac{r_{dep}^2 - r_{ox}^2}{2} = \frac{(r_{ox} + w_{dep})^2 - r_{ox}^2}{2} = \frac{2w_{dep}r_{ox} + w_{dep}^2}{2}$$

$$r_{dep}^2 \ln\frac{r_{ox}}{r_{dep}} = (r_{ox} + w_{dep})^2 \ln\left(\frac{r_{ox}}{r_{ox} + w_{dep}}\right)$$
$$= (r_{ox} + w_{dep})^2 \ln\left(\frac{1}{1 + \frac{w_{dep}}{r_{ox}}}\right)$$
$$\approx (r_{ox} + w_{dep})^2 \ln\left(1 - \frac{w_{dep}}{r_{ox}}\right)$$
$$\approx (r_{ox} + w_{dep})^2 \left(-\frac{w_{dep}}{r_{ox}}\right)$$

Therefore, equation (11) could be transformed to:

$$V - V_{FB} = qN_a\left(\frac{w_{dep}t_{ox}}{\varepsilon_{ox}} + \frac{3w_{dep}^2}{4\varepsilon_s}\right) \tag{15}$$

Based on equation (15), we can have the following equation to calculate the depletion width w_{dep}:

$$\frac{3}{4\varepsilon_s}w_{dep}^2 + \frac{t_{ox}}{\varepsilon_{ox}}w_{dep} + \frac{(-V + V_{FB})}{qN_a} = 0 \tag{16}$$

The depletion width w_{dep} can be solved when the TSV is in depletion region and expressed in equation (17):

$$w_{dep} = \frac{2\varepsilon_s}{3\varepsilon_{ox}}\left(-t_{ox} + \sqrt{t_{ox}^2 + \frac{3\varepsilon_{ox}^2}{\varepsilon_S}\frac{V - V_{FB}}{qN_a}}\right). \tag{17}$$

As shown in equation (17), the large digital signal swing makes the depletion region to change its depletion width dynamically. Figure 7 shows one example of w_{dep} changes with the supply voltage.

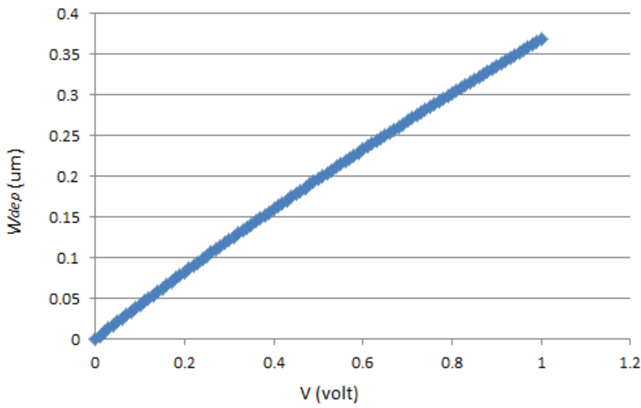

Figure 7 Dynamic change of w_{dep} with the supply voltage

Therefore, the equation for calculating the total TSV capacitance in depletion and accumulation regions is summarized in table 1.

Region	Depletion	Accumulation
V	$V - V_{FB} > 0$	$V - V_{FB} < 0$
Cap	$C_{TSV}(V) = \dfrac{1}{1/C_{ox} + 1/C_{dep}}$ $C_{dep} = \dfrac{2\pi\varepsilon_S h}{\ln\left(\dfrac{r_{ox} + w_{dep}}{r_{ox}}\right)}$	$C_{TSV} = C_{ox}$

Table 1: Total TSV Capacitance

D. *TSV Dimension*

The dimensions of TSVs used for 3D IC are determined by the stacking/bonding method. There are currently three different bonding approaches namely, chip-to-chip, chip-to-wafer, and wafer-to-wafer [27] [28]. For chip-level bonding (i.e., chip-to-chip or chip-to-wafer), low density TSVs having diameters approximately between 5 and 30 *um* are mostly used. High density TSVs for 3D IC applications typically have diameters less than 5 *um* and are used for wafer bonding (i.e., wafer-to-wafer) processes [27-29]. TSVs in Si interposers usually have diameters larger than 50 *um* [29]. In this paper, TSVs for wafer-bonding, chip-bonding and Si interposers are simply called wafer-level TSVs, chip-level TSVs, and interposer TSVs, respectively. Their dimensions are presented in Table 2.

	3D IC		Interposer TSV
	Wafer Level TSV	Chip Level TSV	
Diameter (*um*)	4	10	75
Pitch (*um*)	9.2	20	150
Height (*um*)	24	60	300

Table 2: Typical TSV Dimensions Used for 3D IC and Interposers.

E. *Voltage Dependent TSV Capacitance*

In this section, we will examine what happens when a differential signal $V(t)$ biases the TSV MIS interface. One important point to note is that, when a TSV MIS interface is in the accumulation or depletion regions, it is essentially a majority carrier device because majority carriers are responding to changing the electrical fields. Majority carriers can respond to very high frequency electromagnetic fields. The highest frequency that majority carriers can respond to is determined by the relaxation time of the carriers in silicon, and the typical relaxation time is $T_{relax} < 1$ picosecond. Both the metal semi-conductor field effect transistors (MESFET) and Schottky diodes have the same dynamic change of depletion width and find extensive applications in the microwave engineering. For the high speed differential signals (for example, 25Gbps), the majority carriers can instantly respond to the changing electromagnetic fields. When high speed differential signals propagate though the TSVs, the depletion width $w_{dep}(t)$ is modulated by the momentary signal voltage $V(t)$ on the TSVs. The TSV capacitance C_{TSV} is dependent on the differential signals voltage $V(t)$ and can be expressed as $C_{TSV}(V(t))$. The $C_{TSV}(V(t))$ is nonlinear and changes dynamically with the TSV signals. Therefore, we can find that the capacitance calculation with considering the physics nature of the dynamic depletion region movement and the one that used for non-biasing, small signal analysis [8-18] are quite different.

TSV MIS interface under a static bias could be in the accumulation, depletion, or inversion regions. However, for the TSV MIS interface is biased by the high speed differential signals, we consider that carrier inversion does not occur [11]. Most high speed differential Serializer/Deserializer (SERDES) signals are encoded, which requires the maximum number of consecutive identical digits (CID, usually in the order of tens to hundreds) for a robust clock-data recovery. Consequently, the biasing differential signals will toggle very often (>> 1MHz) and prevent the carrier inversion occurs [11]. Therefore, the biased TSV MIS interface can only be in accumulation and depletion regions and it is always a majority carrier device.

Fig. 8-10 show the TSV capacitance $C_{TSV}(V(t))/Cox$ vs. $(V\text{-}V_{FB})$ of the wafer level TSV, chip level TSV, and interposer TSV, as described in Table 2. As shown in Fig. 8-10, the TSV capacitance $C_{TSV}(V(t))$ depends on the TSV structure as well as the biasing condition $(V\text{-}V_{FB})$. If a TSV is biased in the accumulation region, TSV capacitance is C_{ox}. If a TSV is biased in the depletion region, the smaller the doping N_a and the TSV liner thickness t_{ox} are, the more dominant the depletion capacitance C_{dep} becomes, and the more the nonlinear TSV capacitance $C_{TSV}(V(t))$ is.

The TSV capacitance $C_{TSV}(V(t))$ is much higher than the capacitance obtained assuming small signal analysis and non-biasing condition [8-10]. Table 3 compares the capacitance between previous methods and our method for three cases: the wafer level TSV, the chip level TSV, and the interposer TSV. The sample frequency for the differential signal is 10GHz. As shown in table 3, the non-linear capacitance can be as high as

3280fF in the interposer TSV, but the capacitance from previous methods in [8-10] is much lower. We verified the proposed analytical formula by comparing it with the *C-V* curve obtained from static simulation and measurement with a static bias.

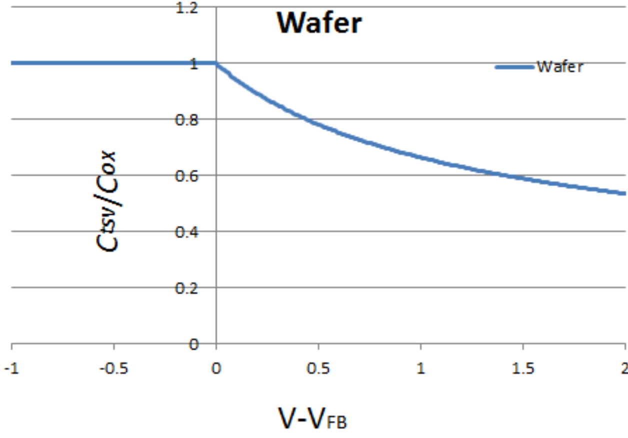

Figure 8: TSV Capacitance vs. Biasing of the Wafer Level TSV in 3D IC

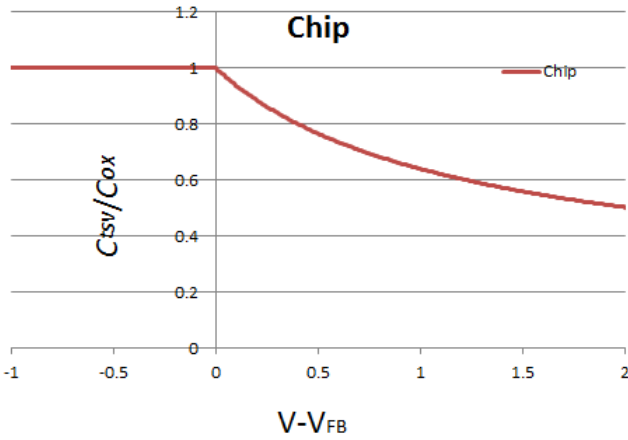

Figure 9: TSV Capacitance vs. Biasing of the Chip Level TSV in 3D IC

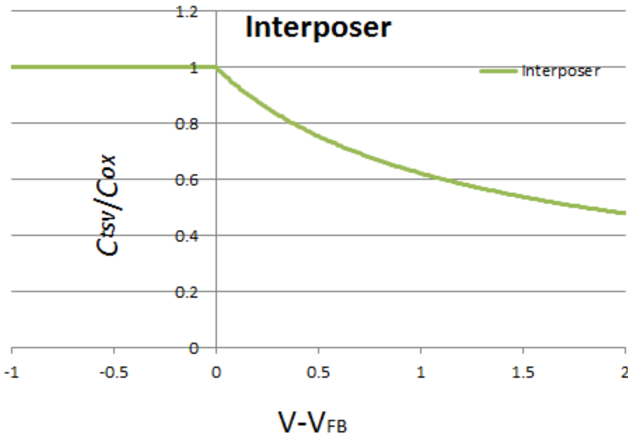

Figure 10: TSV Capacitance vs. Biasing of the Interposer TSV

	3D IC		Interposer TSV
	Wafer Level TSV	Chip Level TSV	
Ref. [8-10] Cap. (fF)	6.5	24.5	98.7
Our method Cap. (fF)	16.4	93.2	3280
Difference (%)	60%	74%	97%

Table 3: Capacitance from [8-10] vs. Accumulation Capacitance

There are two ways to simulate the nonlinear capacitance $C_{TSV}(V(t))$ in HSPICE simulator. The first one is using the HSPICE support for Verilog A, and the second one is using the equation-based capacitance method. Note that the $C_{TSV}(V(t))$ which could be obtained from the static bias measurements [14] or the EM simulations [13] can also be used in HSPICE with the same approach mentioned above. Nonlinear and voltage dependent TSV capacitance $C_{TSV}(V(t))$ follows the same *C-V* curve obtained from simulation or measurement with a static bias as discussed in [11]. The *C-V* curves cam also be applied to characterize the TSV capacitance $C_{TSV}(V(t))$ by measuring the static *C-V* curve. Such measurement techniques are readily available and discussed in [11].

III. Circuit Models of Differential TSVs

The TSVs can be modeled using lumped or distributed circuit model. However, since the TSV size is much less than the wavelength of the considered frequency range, lumped circuit model is adapted [30]. The equivalent circuit for differential signal TSVs is proposed and shown in Fig. 11. The proposed model contains resistance (R), capacitance (C), and inductance (L). The compact lumped circuit model accounts for wide frequency range, high frequency skin effect, eddy currents in substrate, and MOS effect. The capacitance effect is very different from what is described in [8-10]. The capacitive effect of each TSV with the differential signal is modeled as a nonlinear capacitance $C_{TSV}(V(t))$. These two differential TSV capacitances are different since the TSVs have complementary signals. The TSV MIS capacitance is the total capacitance for a TSV, and there is no capacitive coupling between the two TSVs since they're shielded by the virtual ground.

Well established expressions for calculation of the circuit parameters: *R* and *L* [31-33]. For the calculation of frequency dependent *R*, the equation below is used

$$R = \frac{R_s}{2\pi}\left(\frac{1}{r_i} + \frac{1}{r_0}\right), \qquad (18)$$

where r_i and r_0 are the radio of the outer and inner conductors, respectively, R_s is the surface resistance and defined as:

$$R_s = \frac{1}{\sigma\delta} = \sqrt{\frac{\pi\mu_0 f}{\sigma}}, \qquad (19)$$

where σ is the conductivity of the conductor, f is the carrier frequency of the differential signals.

Due to the skin and proximity effect, the inductance (L) of the TSVs is also frequency dependent. To calculate the inductance (L), the conventional inductance expression of a coaxial transmission can be extended to capture the frequency dependent behavior of the TSVs. The equation of L is given below:

$$L = \frac{\mu_0}{2\pi} \ln\left(\frac{r_0}{r_i}\right) + \frac{R}{2\pi f} \tag{20}$$

where μ_0 is the permeability of vacuum, respectively. The inductance equation considering the high frequency effect has been verified by comparing the analyzed extracted value with the inductance extracted from 2D field simulation [8].

Depletion region caused by the TSV biasing does not impact the magnetic field distribution. Magnetic field can easily penetrate into an accumulation layer since 1) the accumulation layer is thin, it's in the order of a Debye length [11], which is 0.01*um*-0.1*um* range when doping is between 10^{15}-$10^{17}/cm^3$, and 2) the conductivity is low (much less than metal copper). Therefore, TSV inductance (L) and resistance (R) applied for the non-biasing, small signal analysis is still valid.

The conductance (G) of a TSV is different from that in [8-10] [34] [35] as well. In non-biasing, small signal analysis, electric field can penetrate into the silicon substrate and it experiences a high loss:

$$\tan\delta_d + \frac{\sigma_s}{\omega\varepsilon_S} \approx \frac{\sigma_s}{\omega\varepsilon_S}, \tag{21}$$

where $\tan\delta_d$ and σ_S are the polarization loss and the conductivity of the silicon, respectively. However, when we consider the differential TSV with static biasing or large signals, the electric field of differential signals exists only in the region depleted with majority carriers and it only has the loss $\tan\delta_d$ which is very small and can be ignored. Therefore, our proposed model for differential TSVs only contains the resistance (R), capacitance (C), and inductance (L).

The model's compactness and compatibility with SPICE simulators allows the electrical modeling of various TSV arrangements without the need for computationally expensive field solvers, which significantly reduces the simulation running time. The proposed circuit model could be a promising solution to both academic and industrial need for broadband electrical modeling of TSVs in 3D IC.

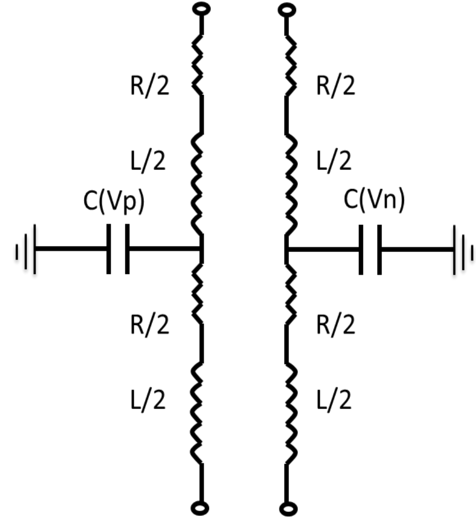

Figure 11: Equivalent circuit model for differential TSVs

IV. TSV Performance Analysis

The effect of TSVs on the signal integrity of high data-rate signals is studied with eye diagram approach. As we discussed in section II, the nonlinear and voltage dependent TSV capacitance $C_{TSV}(V(t))$ can be modeled in HSPICE simulator by using the Verilog A block or using the equation-based capacitance. Differential plus and minus signal voltages are used to control TSV capacitances.

Fig. 12-14 show the simulate eye diagrams of pseudo-random data transmitted over the wafer level TSV, chip level TSV, and interposer TSV. The eye diagram is a general tool which gives insight into the amplitude behavior of the waveform as well as the timing behavior. An eye diagram is created when many short segments of a waveform are superimposed such that the nominal edge locations and voltage levels are aligned. If the waveform is repeatable, a sampling scope may be used to build an eye diagram from individual samples taken at random delays on many waveforms.

As shown in Fig. 12-14, the differential signals are running at 10Gbps through a simple channel consisting of a 5*mm* PCB and a silicon interposer. (V-V_{FB}) is assumed to be around 0.5V. At any instant, the positive and the negative TSVs have different nonlinear capacitances, therefore, different impedances and delays, due to biasing difference.

Table 4 summarizes the vertical and horizontal eye openings, driver power consumption, and signal delays (from driver input to receiver input) for wafer level TSV at 10Gbps, 15Gbps, 25Gbps, and 50Gbps. As shown in table 4, the bit period is a measure of the horizontal opening of an eye diagram at the crossing points of the eye and is usually measured in picoseconds for a high speed digital signal (i.e., 200 ps is used for a 5Gbps signal).

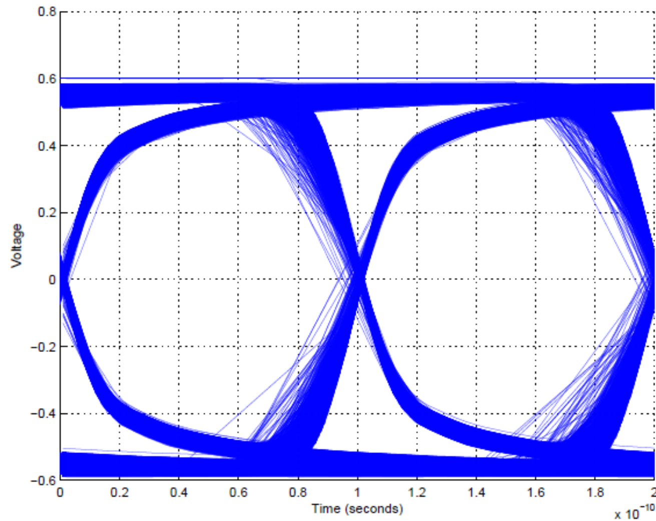

Figure 12: Eye Diagram of the Wafer Level TSV in 3D IC.

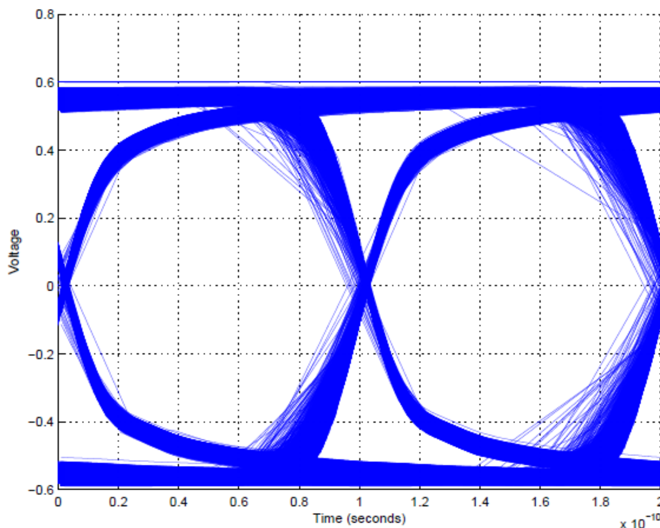

Figure 13: Eye Diagram of the Chip Level TSV in 3D IC.

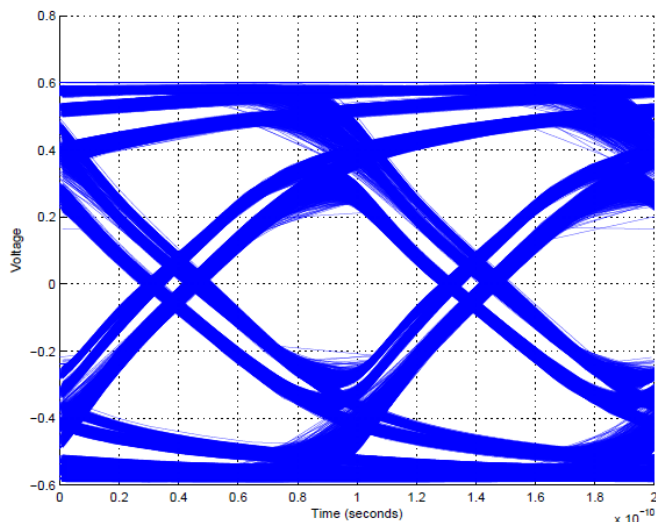

Figure 14: Eye Diagram of the Interposer TSV.

Data Rate (Gbps)	Horizontal Eye Opening (UI)	Vertical Eye Opening (mv)	Jitter (ps)
10	0.98	96	0.9
15	0.95	88	2
25	0.90	70	3
50	0.75	40	5

Table 4: Performance prediction for pseudo random data transmitted over the Wafer Level TSV in 3D IC

The data rate is the inverse of bit period (1/bit period). The bit period is commonly called the Unit Interval (UI) when describing an eye diagram. The advantage of using UI instead of actual time on the horizontal axis is that it is normalized and eye diagrams with different data rates can be easily compared. Vertical eye opening is a measure of the vertical opening of an eye diagram. Jitter is the time deviation from the ideal timing of a data−bit event and is perhaps one of the most important characteristics of a high speed digital data signal. To compute jitter, the time deviations of the transitions of the rising and falling edges of an eye diagram at the crossing point are measured.

V. Conclusion

Virtual ground associated with differential TSVs biases TSV MIS interfaces. This biasing introduces voltage dependent nonlinear TSV capacitance. Frequent switching of high speed differential signals put TSV MIS in the accumulation or depletion regions. The TSV capacitance changes dynamically with the TSV differential signals. An analytical formula for TSV capacitance is obtained and a new equivalent circuit model for differential TSVs is proposed. This model is readily usable in the channel simulations. The effect of the differential TSVs on the signal integrity of high data-rate signals is studied with eye diagram approach. As shown in our resulting eye diagrams, the differential TSVs have different capacitance, therefore, different impedances and delays, due to biasing difference.

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