Modeling Independent Multi-Gate MOSFETs

Juan Pablo Duarte, Sourabh Khandelwal, Huan-Lin Chang, Yen-Kai Lin, Pragya Kushwaha*, Yogesh S. Chauhan*, and Chenming Hu

Dept. of Electrical Engineering and Computer Science
University of California, Berkeley, USA, jpduarte@eecs.berkeley.edu
*Nanolab, Dept. of Electrical Engineering
Indian Institute of Technology Kanpur, India

ABSTRACT

This work presents the industry standard compact BSIM-IMG, a fully-featured turn-key compact model for independent multi-gate MOSFETs. The two independent (front- and back-gate) control of the channel charge in these devices enables novel applications wherein back-gate can be in depletion or inversion, and BSIM-IMG accurately models these scenarios. Modeling of the channel-charge in this device requires a consistent solution of coupled Poisson's equations at the front- and the back-gate. This papers presents an analytical solution which is numerically robust and passes important quality tests for an industry grade compact model. To represent real device effects, several extra models are incorporated such as drain-induced barrier lowering, velocity saturation, short-channel effects, self-heating effect, mobility-field dependence, substrate-depletion effect, etc.

Keywords: BSIM, multi-gate MOSFETs, compact model

1 INTRODUCTION

Ultrathin Body silicon-on-insulator (UTBSOI) technology has been developed with excellent low power, scaling and, variability characteristics [1]. UTBSOI has been recently adopted in sub-20nm IC technologies [2–4] as an alternative to FinFET technology [5–8], as both technologies are replacements of the conventional bulk planar technology. For UTBSOI transistor technology, the Compact Model Coalition (CMC) has chosen BSIM-IMG [9–12] as one of the first industry-standard compact model for advanced circuit design.

Developing a compact model for independent multi-gate MOSFETs is challenging due to the nature of the Poisson's solution with front- and back-gate boundaries conditions [9]. It is well known that the Poisson's solution for these devices [9] lies in trigonometric and hyperbolic domains, making the desired numerical robustness extremely difficult; however, fast speed, numerical robust, and accuracy are fundamental characteristics of compact models for circuit design and technology development. An industry compact model must be able to calculate terminal (drain, source, front/back-gate) currents and charges, which are then utilized by circuit simulator engines to solve a complete circuit under various analyses such as dc, ac, transient, etc. This work is presenting the fundamentals of the BSIM-IMG compact model for UTBSOI technologies, and discuss all the important features of this model, which demonstrates the readiness of BSIM-IMG model for developing process-design-kits (PDKs).

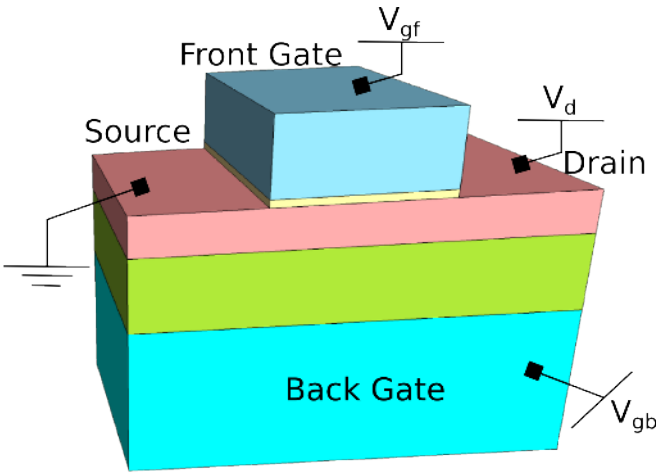

Figure 1: 3-dimensional schematic of a ultra-thin-body silicon-on-insulator device.

2 INDEPENDENT MULTI-GATE MOSFETS

Figure 1 shows a 3-dimensional schematic of UTBSOI, similar to that demonstrated in [1]. It has a traditional planar structure similar to conventional bulk MOSFETs, with source, drain, and gate contacts in the top; however, the silicon channel layer is thin (Fin), and placed between front/back insulators, where the additional back gate serves as a potential modulator of the silicon fin. This additional tuning feature can be use in several contexts, for example, as a threshold voltage modulation or device variability control [1] [13].

Figures 2 and 3 show structural and energy band cross-sectional view of a UTBSOI, respectively, where it is easy to appreciate front and back gates, silicon insula-

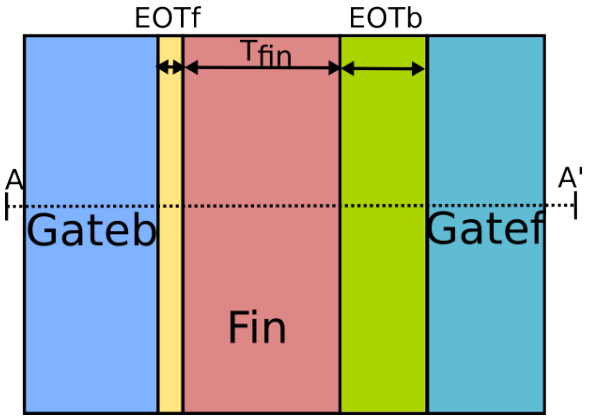

Figure 2: 1-dimensional cross-sectional view of a UTB-SOI with independent potential control of the channel from front and back gates.

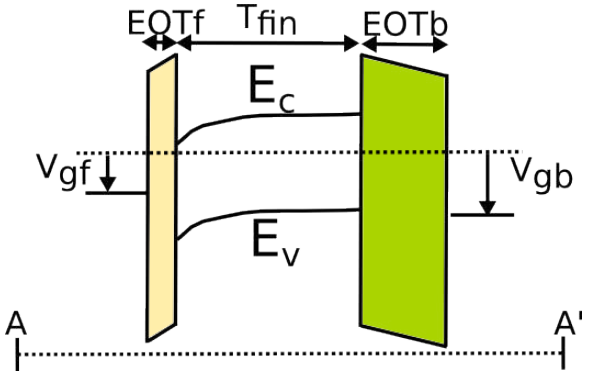

Figure 3: 1-dimensional cross-sectional view of the energy diagram of a UTBSOI. Two different boundary conditions defines the energy shape in the semiconductor channel.

tor layer (or Fin), and back and front insulators (EOT_f and EOT_b).

Figure 3 represent the ideal structure taken as a reference for the derivation of the core model, this model must be able to capture potential in the front and back silicon-insulator interfaces; thus, making possible the calculation of back/front charges and mobile charge in the channel. In a different manner compared to conventional FinFETs, front- and back-gate potentials can produce different set of bias conditions as shown in figures 4 to 7. Figure 4, shows the first case, where channel is in the substhreshold condition and it is fully depleted, this is accomplished when back and fornt channels are turned off due the low potential at both gates. The second bias case is when the front potential is large enough for inversion but back is not, figure 5 shows that there is inversion in the front gate, but back gate is still off and in the subthreshold condition. The third case, figure 6, show the case where front potential is not large enough to produce front charge inversion but back gate can induce inversion in the back channel. Finally, figure

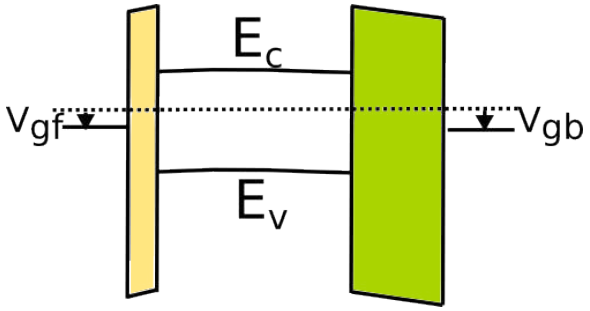

Figure 4: 1-dimensional cross-sectional view of a UTB-SOI where channel is in the substhreshold condition.

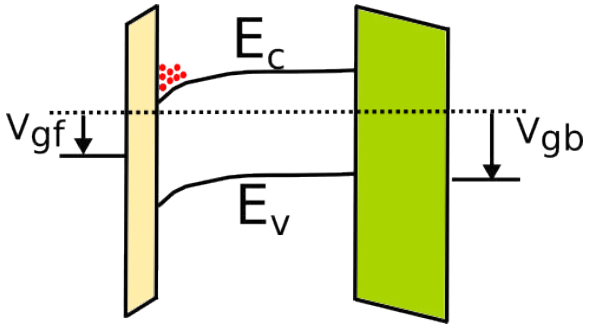

Figure 5: 1-dimensional cross-sectional view of a UTB-SOI where only front surface is in strong inversion condition.

7 shows the last case where both, front and back, channels are in inversion condition due the large potential at both gates. All four configurations must be capture in an accurate and robust manner by a core compact model so it can be used for circuit simulation and design. In the following sections, the core compact model used in BSIM-IMG is described in detailed.

3 CORE MODEL

There is an extensive amount of work related to the development of core compact model for UTBSOI de-

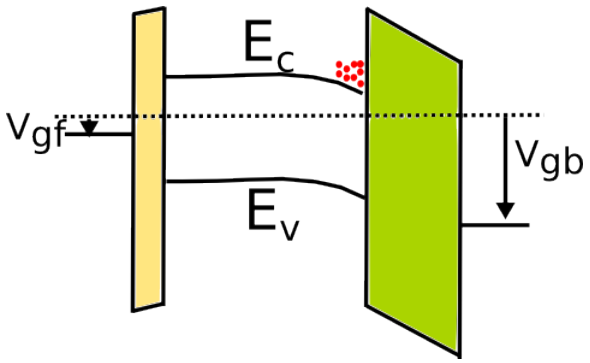

Figure 6: 1-dimensional cross-sectional view of a UTB-SOI where only back surface is in strong inversion condition.

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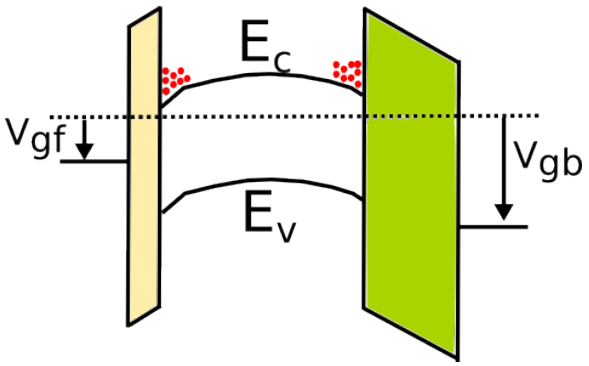


Figure 7: 1-dimensional cross-sectional view of a UTB-SOI where back and front surfaces are in strong inversion condition.

vices. For example, the work presented in [9] represent a robust solution that simplifies the Poisson's equation, with a single variable equation that can be solved for devices where front inversion is the dominant component for the current. In [14], a compact model with three different solution regions was presented, it take into account hyperbolic and trigonometric domains, having a difficult numerical challenge related to the mathematical implementation of the model to keep accuracy and track of the analytic solution. The work presented in [15] proposed a set of three equations that can be solved simultaneously to obtain the solution for back and front potentials. Based on the work of [15], [16] removed the extra unknown of [15], leading to a single variable compact model which can be used to obtain the potentials in UTBSOI devices. This paper proposes a robust core compact model based on the work of [16], which is used to obtain the mathematical equations to be solved, then using the results of [9] and [17], a robust algorithm is developed to be used in the core model of BSIM-IMG.

The 1-dimensional Poisson's equation (neglecting channel doping) for the cross-sectional section of a UTBSOI device (figure 3) can be written in the following form:

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{\rho(\psi)}{\varepsilon_{\text{ch}}} = \frac{qn_i}{\varepsilon_{\text{ch}}} e^{\frac{\psi - V_{ch}}{v_T}} \tag{1}$$

where ψ is the electrostatic potential in the fin, q is the magnitude of the electronic charge, n_i is the intrinsic carrier concentration, ε_{ch} is the dielectric constant of the channel (fin), v_T is the thermal voltage given by k_BT/q, where k_B and T are the Boltzmann constant and the temperature, respectively; V_{ch} is the quasi-Fermi potential of the channel ($V_{ch}(0) = V_{\text{s}}$ and $V_{ch}(\text{L}) = V_d$). The next step is to apply boundary conditions at each semiconductor-insulator interfaces. This is done using Gauss's law boundary condition which gives two boundary conditions:

$$\varepsilon_{EOTf}\frac{V_{gf} - V_{fbf} - \psi_{sf}}{EOTf} = -\varepsilon_{ch}\frac{\partial\psi_{sf}}{\partial x} \tag{2}$$

$$\varepsilon_{EOTb}\frac{V_{gb} - V_{fbb} - \psi_{sb}}{EOTb} = \varepsilon_{ch}\frac{\partial\psi_{sb}}{\partial x} \tag{3}$$

Note that the total charge in the channel can be expressed by the following formula:

$$Q_m = -\varepsilon_{ch}\frac{\partial\psi_{sf}}{\partial x} + \varepsilon_{ch}\frac{\partial\psi_{sb}}{\partial x} \tag{4}$$

Integrating once the Poisson's equation with respect to potential and after variable normalization it is possible to obtain the following two expressions:

$$\alpha^2 = k_f(x_f - \varphi_f)^2 - A_0 e^{\varphi_f} \tag{5}$$

$$\alpha^2 = k_b(x_b - \varphi_b)^2 - A_0 e^{\varphi_b} \tag{6}$$

The next step is to integrate the electric field using α and then, using algebraic manipulations as in [16], obtain the following equation:

$$\begin{aligned}\alpha\coth(\alpha/2)(k_f(x_f - \varphi_f) + k_b(x_b - \varphi_b)) + \\ k_fk_b(x_b - \varphi_b)(x_f - \varphi_f) + \alpha^2 = 0\end{aligned} \tag{7}$$

The previous three equations form a system of three variables and three equations which can be solved to obtain back and front potentials. Note that if $\alpha^2 < 0$: $\coth, \sinh \to \cot, \sin$. However, these equations can be combined into a single variable equations as follows [16]:

$$\begin{aligned}f(\varphi_f) = (k_f(x_f - \varphi_f) + \alpha\coth(\alpha/2))(k_f(x_f - \varphi_f) + \\ k_b(x_b - \varphi_b)) - A_0 e^{\varphi_f} = 0\end{aligned} \tag{8}$$

with:

$$\begin{aligned}\varphi_b = \varphi_f - \ln(k_f(x_f - \varphi_f) + \\ \alpha\coth(\alpha/2)) + \ln\left(\tfrac{\alpha}{\sinh(\alpha/2)}\right)^2\end{aligned} \tag{9}$$

Equation (8) represent a single variable equation that must be solved for the condition $f(\varphi_f) = 0$; thus, for different values of φ_f, f must be minimized. The challenge relies in the hyperbolic and trigonometric nature of f for different values of φ_f. For example, figure 8 shows the evaluation of $f(\varphi_f)$ for different values of φ_f. Note that for the hyperbolic region there is a single minimum value (single solution); however, in the trigonometric region, there are several values of φ_f where $f(\varphi_f) \sim 0$. This implies a challenging issue, because traditional iterative methods used in compact models, such as Newton's method, may bring the solution to a false solution as shown in figure 8, producing discontinuities in the final compact model. Therefore, in the following section, a method to limit the solution to valid regions is presented.

4 CORE MODEL ANALYTICAL SOLUTION

An anlytical solution for the derived core model from previous section consist of two main parts. First, an

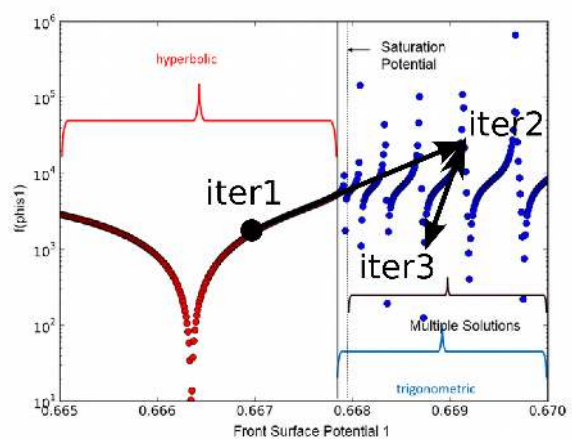
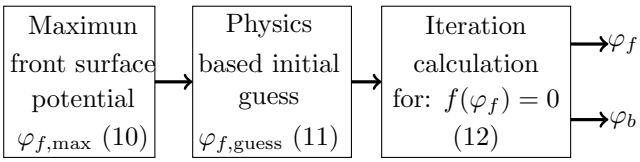


Figure 8: Evaluation of $f(\varphi_f)$ for different values of φ_f where an iteration example fell into a false solution.

initial guess that must be continuous and as close as possible to the final solution. The second part of the analytical solution consists of updates to the initial guess solution so the accuracy is further refined. The following diagram represent a schematic of the analytical solution implemented in BSIM-IMG:



The first step is to solve equation (10). Note that this work call the solution of this equation as saturation potential. As shown in figure 8, it represents the maximum value of the front potential where the trigonometric region has a single solution. Knowing this value, it is possible to limit the analytical algorithm to a values lower than this maximum, so false solutions are avoided. Equation (10) can be simply solved using Newton's method.

$$-4\pi^2 = k_f(x_f - \varphi_{f,\max}) - A_0 e^{\varphi_{f,\max}} \qquad (10)$$

Once $\varphi_{f,\max}$ is obtained, it is possible to obtain a very accurate initial guess by taking the minimum, in a smooth manner, of the $\varphi_{f,\max}$ value and the approximated value of front potential in the subthreshold region, as obtained in [9].

$$\varphi_{f,\text{guess}} = \max_s\left(\frac{rEOT_f(x_f - x_b)}{T_{fin} + r(EOT_f + EOT_b)} + x_b, \varphi_{f,\max}\right) \qquad (11)$$

Since the initial guess is very closed to the final solution, only fist order Newton updates are needed to improve the accuracy of the solution. In addition, in order to keep the final solution in valid regions, the update

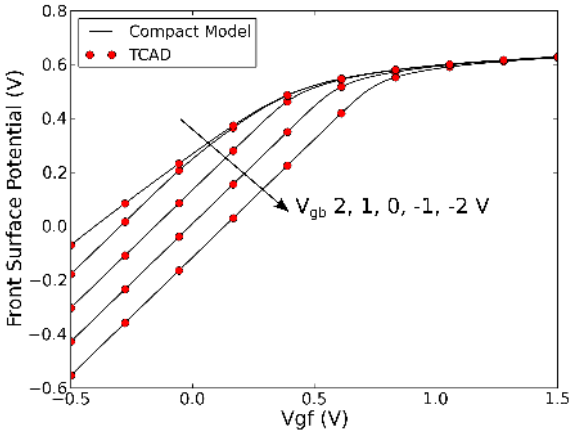


Figure 9: Front potential versus front gate voltages for different back gate biases obtained from compact model and TCAD simulations.

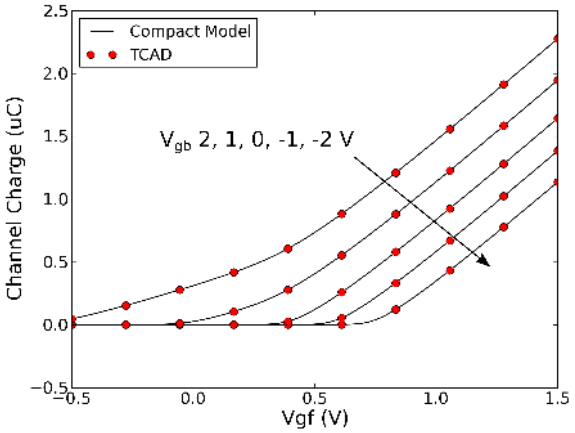


Figure 10: Channel charge versus front gate voltages for different back gate biases obtained from compact model and TCAD simulations.

is smoothly limited to values lower than the saturation maximum potential obtained in (10).

$$\varphi_{f,n} = \varphi_{f,n-1} - \min_s\left(\frac{f}{f'}, \frac{\varphi_{f,\max} - \varphi_{f,n-1}}{2}\right) \qquad (12)$$

with $\varphi_{f,0} = \varphi_{f,guess}$. Note that $\max_s$ and $\min_s$ are smooth versions of max and min functions.

Figures 9 and 10 shows the front potential and the channel charge obtained from the proposed compact model versus TCAD simulations for different front and back gate potentials. The proposed model accurately describes the potential and charge in the channel, in addition, figure 11 shows the C_{FGFG} capacitance versus front gate voltage. These results show that the proposed compact model smoothly capture the back inversion effect for different back bias configurations.

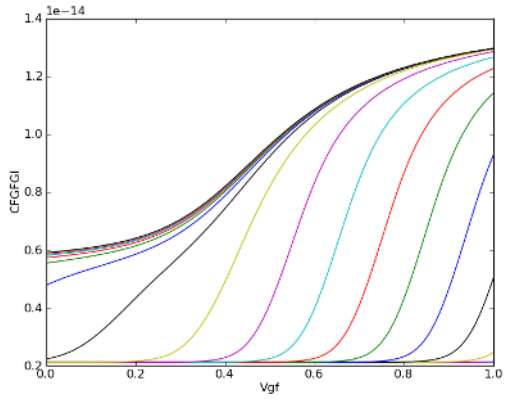


Figure 11: CFGFG capacitance versus front gate voltage for different back gate biases. Note that back inversion effects is accurately obtained by the compact model.

5 DRAIN CURRENT MODEL

The drain current model for independent-gate MOSFETs is well known and reported in [18]. It is based in the 1-dimensional Poisson equation formulation, thus, it is compatible with the core model derived for BSIM-IMG. The normalized current ids_0 is then given by:

$$ids_0 = 2v_T(q_{fronts} - q_{frontd}) - \frac{\frac{q_{frontd}^2}{c_{ox1}} - \frac{q_{fronts}^2}{c_{ox1}}}{2} + 2v_T(q_{backs} - q_{backd}) - \frac{\frac{q_{backd}^2}{c_{ox2}} - \frac{q_{backs}^2}{c_{ox2}}}{2} \quad (13)$$

where q_{fronts}, q_{frontd}, q_{backs}, and q_{backd}, are front charge at source, front charge at drain, back charge at source and back charge at source, respectively. Each quantity is calculate using the core model and the back and front charge definitions.

Since core and drain current models are completed, additional real device effects are incorporated to the final model in BSIM-IMG. As explained in [10], several extra models are added to the core and drain current models such as drain-induced barrier lowering, velocity saturation, short-channel effects, self-heating effect, mobility-field dependence, substrate-depletion effect, etc. Figures 12 and 13 shows simulations of BSIM-IMG model, with all real device models included, versus measured data. The good accuracy demonstrates the capabilities of the model as an industry stand compact model.

6 CONCLUSIONS

The new features of the industry standard compact BSIM-IMG have been presented in this work. It includes a new analytical solution for the core compact model, which is capable of capturing the electrostatics behaivor of UTBSOI MOSFETs with independent front and back gate control. The analytical solution accurately captures front and back surface inversion effects in a robust manner, crucial for circuit simulation. Real device effects, currently used in BSIM-IMG model, have been incorporated to the new frame work, demonstrating the readiness of BSIM-IMG model in the development of PDKs.

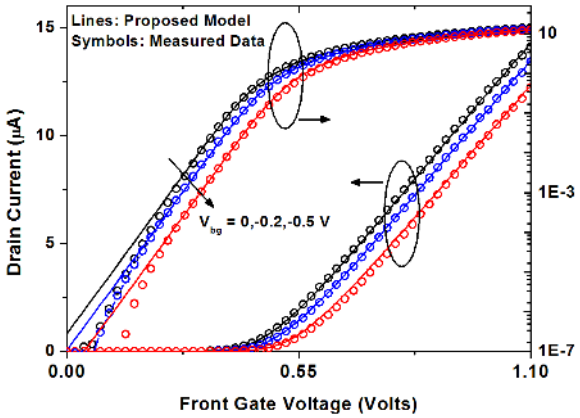


Figure 12: BSIM-IMG model versus measured data for linear $I_{DS} - V_{fg}$ characteristics at different values of V_{bg} for a long-channel device [10].

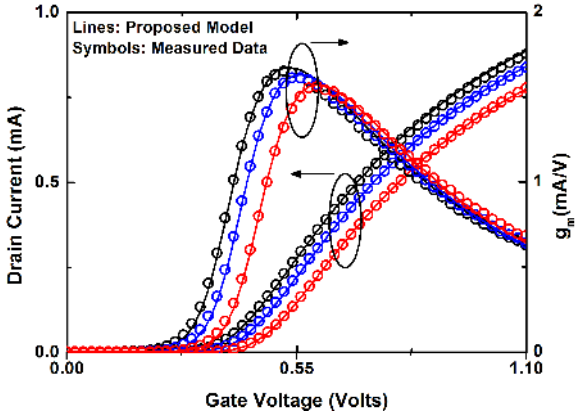


Figure 13: BSIM-IMG model versus measured data for linear $I_{DS} - V_{fg}$ and $g_m - V_{fg}$ characteristics at different values of V_{bg} (0,-0.2,-0.5V) for a long-channel device [10].

REFERENCES

[1] Y. Choi, K. Asano, N. Lindert, V. Subramanian, T. King, J. Bokor, and C. Hu, "Ultra-thin body soi mosfet for deep-sub-tenth micron era," in *Electron Devices Meeting, 1999. IEDM Technical Digest. International.* IEEE, 1999, pp. 919–921.

[2] S. Monfray, M. Samson, D. Dutartre, T. Ernst, E. Rouchouze, D. Renaud, B. Guillaumot, D. Chanemougame, G. Rabille, S. Borel *et al.*, "Localized soi technology: an innovative low cost self-aligned process for ultra thin si-film on thin box integration for low power applications," in *Electron*

Devices Meeting, 2007. IEDM 2007. IEEE International. IEEE, 2007, pp. 693–696.

[3] T. Ohtou, N. Sugii, and T. Hiramoto, "Impact of parameter variations and random dopant fluctuations on short-channel fully depleted soi mosfets with extremely thin box," *IEEE electron device letters*, vol. 28, no. 8, pp. 740–742, 2007.

[4] Y. Morita, R. Tsuchiya, T. Ishigaki, N. Sugii, T. Iwamatsu, T. Ipposhi, H. Oda, Y. Inoue, K. Torii, and S. Kimura, "Smallest v th variability achieved by intrinsic silicon on thin box (sotb) cmos with single metal gate," in *VLSI Technology, 2008 Symposium on*. IEEE, 2008, pp. 166–167.

[5] C. Auth *et al.*, "A 22nm high performance and low-power cmos technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density mim capacitors," in *VLSI Technology (VLSIT), 2012 Symposium on*. IEEE, 2012, pp. 131–132.

[6] S. Natarajan *et al.*, "A 14nm logic technology featuring 2nd-generation finfet, air-gapped interconnects, self-aligned double patterning and a 0.0588 um2 sram cell size," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, Dec 2014, pp. 3.7.1–3.7.3.

[7] S.-Y. Wu *et al.*, "An enhanced 16nm cmos technology featuring 2nd generation finfet transistors and advanced cu/low-k interconnect for low power and high performance applications," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, Dec 2014, pp. 3.1.1–3.1.4.

[8] C.-H. Lin *et al.*, "High performance 14nm soi finfet cmos technology with 0.0174 um2 embedded dram and 15 levels of cu metallization," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, Dec 2014, pp. 3.8.1–3.8.3.

[9] D. Lu, "Compact models for future generation cmos," 2011.

[10] S. Khandelwal, Y. S. Chauhan, D. D. Lu, S. Venugopalan, M. A. U. Karim, A. B. Sachid, B.-Y. Nguyen, O. Rozeau, O. Faynot, A. M. Niknejad *et al.*, "Bsim-img: A compact model for ultrathin-body soi mosfets with back-gate control," *Electron Devices, IEEE Transactions on*, vol. 59, no. 8, pp. 2019–2026, 2012.

[11] P. Kushwaha, C. Yadav, H. Agarwal, Y. S. Chauhan, J. Srivatsava, S. Khandelwal, J. P. Duarte, and C. Hu, "Bsim-img with improved surface potential calculation recipe," in *India Conference (INDICON), 2014 Annual IEEE*. IEEE, 2014, pp. 1–4.

[12] Y. S. Chauhan, S. Venugopalan, M. A. Karim, S. Khandelwal, N. Paydavosi, P. Thakur, A. M. Niknejad, and C. C. Hu, "Bsimindustry standard compact mosfet models," in *ESSCIRC (ESSCIRC), 2012 Proceedings of the*. IEEE, 2012, pp. 30–33.

[13] V. P.-H. Hu, M.-L. Fan, P. Su, and C.-T. Chuang, "Threshold voltage design of utb soi sram with improved stability/variability for ultralow voltage near subthreshold operation," *Nanotechnology, IEEE Transactions on*, vol. 12, no. 4, pp. 524–531, 2013.

[14] G. Dessai and G. Gildenblat, "Solution space for the independent-gate asymmetric dgfet," *Solid-State Electronics*, vol. 54, no. 4, pp. 382–384, 2010.

[15] A. Ortiz-Conde and F. J. García-Sánchez, "Generic complex-variable potential equation for the undoped asymmetric independent double-gate mosfet," *Solid-State Electronics*, vol. 57, no. 1, pp. 43–51, 2011.

[16] T. Poiroux, O. Rozeau, S. Martinie, P. Scheer, S. Puget, M. Jaud, S. El Ghouli, J. Barbé, A. Juge, and O. Faynot, "Utsoi2: A complete physical compact model for utbb and independent double gate mosfets," in *Electron Devices Meeting (IEDM), 2013 IEEE International*. IEEE, 2013, pp. 12–4.

[17] T. Poiroux, O. Rozeau, P. Scheer, S. Martinie, M. Jaud, M. Minondo, A. Juge, J. Barbe, and M. Vinet, "Leti-utsoi2. 1: A compact model for utbb-fdsoi technologiespart i: Interface potentials analytical model," *Electron Devices, IEEE Transactions on*, vol. 62, no. 9, pp. 2751–2759, 2015.

[18] A. Ortiz-Conde and F. J. G. Sánchez, "Unification of asymmetric dg, symmetric dg and bulk undoped-body mosfet drain current," *Solid-state electronics*, vol. 50, no. 11, pp. 1796–1800, 2006.