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Modeling Noise Coupling Between Package and PCB Power/Ground Planes With an Efficient 2-D FDTD/Lumped Element Method

Ting-Kuang Wang, Sin-Ting Chen, Chi-Wei Tsai, Sung-Mao Wu, James L. Drewniak, *Fellow, IEEE*, and Tzong-Lin Wu, *Senior Member, IEEE*

***Abstract*—An efficient numerical approach based on the 2-D finite-difference time-domain (FDTD) method is proposed to model the power/ground plane noise or simultaneously switching noise (SSN), including the interconnect effect between the package and the print circuit board (PCB). The space between the power and ground planes on the package and PCB are meshed with 2-D cells. The equivalent R–L–C circuits of the via and the solder balls connecting the package and PCB can be incorporated into a 2-D Yee cell based on a novel integral formulation in the time domain. An efficient recursive updating algorithm is proposed to fit the lumped networks into the Yee equations. A test sample of a ball grid array (BGA) package mounted on a PCB was fabricated. The power/ground noise coupling behavior was measured and compared with the simulation. The proposed method significantly reduces the computing time compared with other full-wave numerical approaches.**

***Index Terms*—Ball grid array (BGA), print circuit board (PCB), signal integrity (SI), simultaneous switching noise (SSN), two-dimensional (2-D) finite-difference time-domain (FDTD) modeling.**

I. Introduction

SIMULTANEOUS switching noise (SSN) on power and ground planes is a primary concern in the design of advanced high-speed digital systems with fast edge rates, high clock frequencies, and low voltage levels. In traditional lead frame packages, the SSN results from the fast transient switching current passing through the equivalent inductance of the power or ground leads. As electronic packages have progressed from lead frame packages, to packages with power/ground planes in high-speed design, the SSN problem has progressed from inductance effects to the cavity resonance between the power and ground planes on the package and print circuit board (PCB) [1]–[4]. From the chip-level perspective, there are two major cavity resonators in the high-speed circuit package. One is formed by the power/ground planes on the package substrate, and the other is formed by the power/ground planes on the PCB. These two cavities are electrically connected through the vertical interconnects comprised of the via holes on the package or PCB, and the solder balls. On the BGA package, the SSN can be coupled through the interaction of these two cavities and degrades the power integrity of the packaged integrated circuits. Understanding the coupling mechanism between these two cavities and their impact on system power integrity is important for package designers to manage noise coupling and SSN. In addition, developing an efficient numerical approach that includes the mutual coupling between the two power/ground planes cavities is also essential to anticipate and predict the SSN behavior, both in time domains and frequency domains from the chip-level perspective.

Several methodologies have been reported for modeling of power/ground plane noise. Three-dimensional full-wave approaches include the method of moments (MoM) with integral equations [5], [6], the partial element equivalent circuit (PEEC) method with retardation effects [7], [8], and the finite-difference time-domain method (FDTD) with broadband responses in one simulation [9], [10]. These methods can accurately model the power/ground plane structure, but require substantial computing resources. Several efficient approaches based on 2-D approximations have been developed, such as a cavity resonator method [11], [12], a transmission-line grid method [13], and a finite-difference frequency-domain method [14].

In this work, an efficient 2-D FDTD approach is proposed to model the power delivery network (PDN), including the interconnect coupling between the package and PCB. The equivalent R–L–C circuit networks of the via and the solder balls connecting between the package and PCB can be incorporated into 2-D Yee cells based on an integral formulation in the time domain. An efficient recursive updating algorithm is proposed to fit the lumped networks into the Yee equations. Although the well-known lumped-element FDTD (LE-FDTD) has been proposed to include a lumped element into FDTD modeling [15], [16], several cells for the interconnect modeling between the package and PCB with several lumped elements are needed. Because the interconnects between the PCB and the package are vertical to the power/ground planes, 3-D modeling is needed when using the LE-FDTD approach. In addition, the distribution of the lumped networks over the FDTD grids leads to numerical inaccuracy as the number of lumped elements is increased in a two-port connection [17]. The approach proposed includes all

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the lumped elements into one cell in the 2-D FDTD, and provides good accuracy. In addition, the computing time can be significantly reduced based on the 2-D FDTD method compared with other full-wave approaches.

A test sample comprised of a ball grid array (BGA) package mounted on a PCB was fabricated. The power/ground noise coupling behavior was measured and compared with the simulation based on the proposed 2-D FDTD method. In addition, the effect of decoupling capacitors on the PDN response is numerically and experimentally demonstrated. The mechanism of noise coupling between the package and PCB is also shown in this paper. Section II describes the novel recursive algorithm including the interconnect between the package and PCB based on the integral formulations of 2-D FDTD method. Section III demonstrates the proposed modeling approach by comparing with measurement.

II. Two-Dimensional FDTD/Lumped Element Formulation

A two-port lumped network is used to demonstrate the algorithm for incorporating lumped networks into the 2-D FDTD method for simplicity. In a general, two-port network consisting of passive R, L, and C elements, the voltage and current at Port 1 and Port 2 can be related in the frequency domain as

$$\begin{bmatrix} \sum_{r=0}^{R_{11}} a_{11,r}(1/s)^r & \sum_{r=0}^{R_{12}} a_{12,r}(1/s)^r \\ \sum_{r=0}^{R_{21}} a_{21,r}(1/s)^r & \sum_{r=0}^{R_{22}} a_{22,r}(1/s)^r \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} = \begin{bmatrix} \sum_{m=0}^{M_{11}} b_{11,m}(1/s)^m & \sum_{m=0}^{M_{12}} b_{12,m}(1/s)^m \\ \sum_{m=0}^{M_{21}} b_{21,m}(1/s)^m & \sum_{m=0}^{M_{22}} b_{22,m}(1/s)^m \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} \quad (1)$$

where $s = j\omega$, and the coefficients $a_{ij,r}$ and $b_{ij,m}$ ($i, j = 1$ or 2) are obtained by the series or shunt combination of the R, L, C lumped elements with their corresponding impedance R, sL, and $1/(sC)$, respectively. The elements in the admittance and impedance matrices in (1) are arranged as a polynomial of $(1/s)$ in order to relate the voltage and current in the integral form in the time domain. Taking the inverse Fourier transform of (1) and discretizing it in the time domain, the voltage and current at time step $n+1$ can be related as

$$\begin{aligned} &\begin{bmatrix} a_{11,0} & a_{12,0} \\ a_{21,0} & a_{22,0} \end{bmatrix} \begin{bmatrix} I_1^{n+1/2} \\ I_2^{n+1/2} \end{bmatrix} + \begin{bmatrix} \sum_{r=1}^{R_{11}} a_{11,r} I_{1,r}^{n+1/2} + \sum_{r=1}^{R_{12}} a_{12,r} I_{2,r}^{n+1/2} \\ \sum_{r=1}^{R_{21}} a_{21,r} I_{1,r}^{n+1/2} + \sum_{r=1}^{R_{22}} a_{22,r} I_{2,r}^{n+1/2} \end{bmatrix} \\ &= \begin{bmatrix} b_{11,0} & b_{12,0} \\ b_{21,0} & b_{22,0} \end{bmatrix} \begin{bmatrix} V_1^{n+1} \\ V_2^{n+1} \end{bmatrix} + \begin{bmatrix} \sum_{m=1}^{M_{11}} b_{11,r} V_{1,r}^{n+1} + \sum_{m=1}^{M_{12}} b_{12,r} V_{2,r}^{n+1} \\ \sum_{m=1}^{M_{21}} b_{21,r} V_{1,r}^{n+1} + \sum_{m=1}^{M_{22}} b_{22,r} V_{2,r}^{n+1} \end{bmatrix} \end{aligned} \quad (2)$$

where

$$\begin{aligned} I_{i,r}^{n+1/2} &\equiv \sum_{k_r=0}^{n} \cdots \sum_{k_2=0}^{k_3} \sum_{k_1=0}^{k_2} I^{k_1+1/2} (\Delta t)^r \\ &= I_{i,r}^{n-1/2} + \Delta t \cdot I_{i,r-1}^{n+1/2} \quad (3a) \\ V_{i,m}^{n+1} &\equiv \sum_{k_m=0}^{n} \cdots \sum_{k_2=0}^{k_3} \sum_{k_1=0}^{k_2} V^{k_1+1} (\Delta t)^m \\ &= V_{i,m}^{n} + \Delta t \cdot V_{i,m-1}^{n+1} \quad (3b) \end{aligned}$$

with $i = 1$ or 2, and $r = 1$ to R_{11}, R_{12}, R_{21}, or R_{22}, $m = 1$ to M_{11}, M_{12}, M_{21}, or M_{22}. It is noted $I_{i,r}^{n+1/2}$ and $V_{i,m}^{n+1}$ are the rth order and mth order summation at time step $n+1$, respectively. Rearranging (2), the voltage-current relation can be written as

$$\mathbf{A}\mathbf{I}^{\mathbf{n+1/2}} + \mathbf{I_0^{n+1/2}} = \mathbf{B}\mathbf{V}^{\mathbf{n+1}} + \mathbf{V_0^{n+1}} \quad (4)$$

where

$$\mathbf{A} = \begin{bmatrix} \sum_{r=0}^{R_{11}} a_{11,r}(\Delta t)^r & \sum_{r=0}^{R_{12}} a_{12,r}(\Delta t)^r \\ \sum_{r=0}^{R_{21}} a_{21,r}(\Delta t)^r & \sum_{r=0}^{R_{22}} a_{22,r}(\Delta t)^r \end{bmatrix} \quad (5a)$$

$$\mathbf{B} = \begin{bmatrix} \sum_{m=0}^{M_{11}} b_{11,m}(\Delta t)^m & \sum_{m=0}^{M_{12}} b_{12,m}(\Delta t)^m \\ \sum_{m=0}^{M_{21}} b_{21,m}(\Delta t)^m & \sum_{m=0}^{M_{22}} b_{22,m}(\Delta t)^m \end{bmatrix} \quad (5b)$$

$$\mathbf{I_0^{n+1/2}} = \begin{bmatrix} \sum_{r=1}^{R_{11}} a_{11,r} \tilde{I}_{1,r}^{n+1/2} + \sum_{r=1}^{R_{12}} a_{12,r} \tilde{I}_{2,r}^{n+1/2} \\ \sum_{r=1}^{R_{21}} a_{21,r} \tilde{I}_{1,r}^{n+1/2} + \sum_{r=1}^{R_{22}} a_{22,r} \tilde{I}_{2,r}^{n+1/2} \end{bmatrix} \quad (5c)$$

$$\mathbf{V_0^{n+1}} = \begin{bmatrix} \sum_{m=1}^{M_{11}} b_{11,r} \tilde{V}_{1,r}^{n+1} + \sum_{m=1}^{M_{12}} b_{12,r} \tilde{V}_{2,r}^{n+1} \\ \sum_{m=1}^{M_{21}} b_{21,r} \tilde{V}_{1,r}^{n+1} + \sum_{m=1}^{M_{22}} b_{22,r} \tilde{V}_{2,r}^{n+1} \end{bmatrix} \quad (5d)$$

$$\mathbf{I^{n+1/2}} = \begin{bmatrix} I_1^{n+1/2} \\ I_2^{n+1/2} \end{bmatrix} \quad (5e)$$

$$\mathbf{V^{n+1}} = \begin{bmatrix} V_1^{n+1} \\ V_2^{n+1} \end{bmatrix} \quad (5f)$$

and

$$\tilde{I}_{i,r}^{n+1/2} = I_{i,r}^{n+1/2} - (\Delta t)^r \cdot I_i^{n+1/2} \quad (6a)$$

$$\tilde{V}_{i,m}^{n+1} = V_{i,m}^{n+1} - (\Delta t)^m \cdot V_i^{n+1} \quad (6b)$$

with $i = 1$ or 2. Separating $\mathbf{I}^{n+1/2}$ and $\mathbf{V}^{n+1}$ with other terms, (4) can be rearranged as

$$\mathbf{I^{n+1/2}} = \mathbf{A^{-1}}\mathbf{B}\mathbf{V^{n+1}} + \mathbf{A^{-1}}\left(\mathbf{V_0^{n+1}} - \mathbf{I_0^{n+1/2}}\right). \quad (7)$$

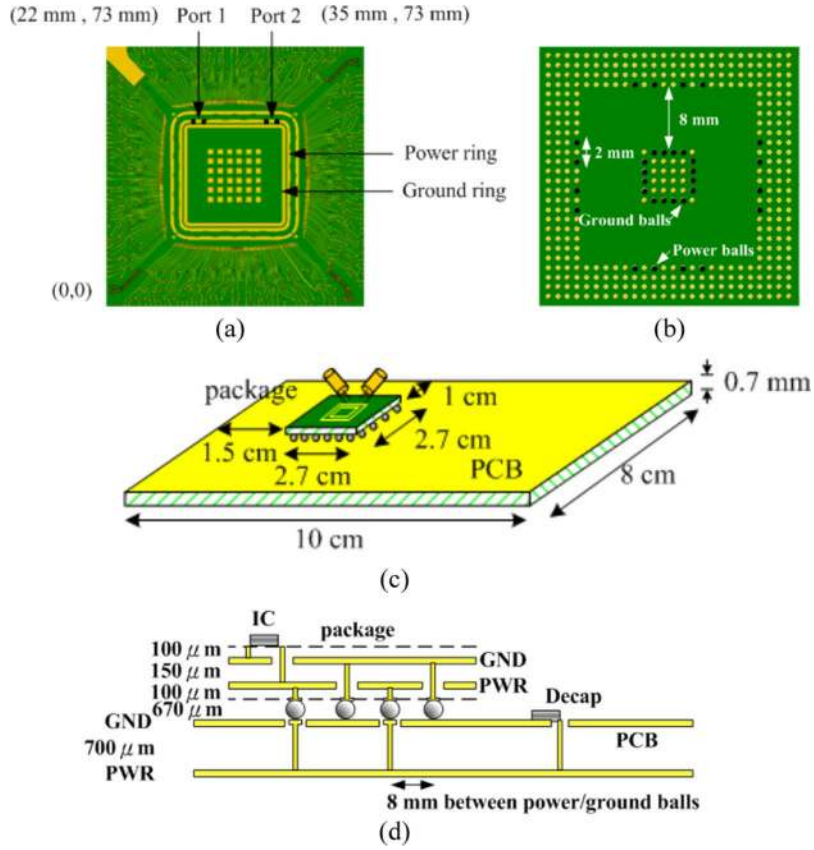

Fig. 1. (a) Top view of the BGA package. (b) Bottom view of the BGA package. (c) Measurement configuration for the BGA package attached on the PCB. (d) Cross section of the test sample.

The two-port update equation for $\mathbf{E}_z^{n+1}$ in FDTD for the cells with the lumped networks is

$$\mathbf{E}_\mathbf{z}^{\mathbf{n+1}} = \mathbf{E}_\mathbf{z}^{\mathbf{n}} + \frac{\Delta t}{\varepsilon}(\nabla \times \dot{\mathbf{H}})_z^{n+1/2} - \frac{\Delta t}{\varepsilon \Delta x \Delta y}\mathbf{I}^{\mathbf{n+\frac{1}{2}}}. \quad (8)$$

Substituting (7) into (8) and using $\mathbf{V}^{n+1} = \mathbf{E}_z^{n+1}\Delta z$, the update equation for $\mathbf{E}_z^{n+1}$ at the cell with the lumped networks is obtained as

$$\mathbf{E}_\mathbf{z}^{\mathbf{n+1}} = \left[\mathbf{E}_\mathbf{z}^{\mathbf{n}} + \frac{\Delta t}{\varepsilon}(\nabla \times \dot{\mathbf{H}})_z^{n+1/2} - \frac{\Delta t}{\varepsilon \Delta x \Delta y}\mathbf{A}^{-1} \times \left(\mathbf{V}_0^{\mathbf{n+1}} - \mathbf{I}_0^{\mathbf{n+1/2}}\right)\right] / \left(1 + \frac{\Delta t \Delta z}{\varepsilon \Delta x \Delta y}\mathbf{A}^{-1}\mathbf{B}\right). \quad (9)$$

Critical to efficiently updating (9) is calculating $\tilde{I}_{i,r}^{n+1/2}$ and $\tilde{V}_{i,m}^{n+1}$ efficiently. The recursive updating form of $\tilde{I}_{i,r}^{n+1/2}$ can be obtained by employing the definition of (3a) into (6a), and is expressed as

$$\begin{aligned}\tilde{I}_{i,r}^{n+1/2} &= I_{i,r}^{n+1/2} - (\Delta t)^r \cdot I_i^{n+1/2} \\ &= I_{i,r}^{n-1/2} + \Delta t \cdot I_{i,r-1}^{n+1/2} - (\Delta t)^r \cdot I_i^{n+1/2} \\ &= \left\{I_{i,r}^{n-1/2} - (\Delta t)^r \cdot I_i^{n-1/2}\right\} + \Delta t \\ &\quad \cdot \left\{I_{i,r-1}^{n+1/2} - (\Delta t)^{r-1} \cdot I_i^{n+1/2}\right\} + (\Delta t)^r \cdot I_i^{n-1/2} \\ &= \tilde{I}_{i,r}^{n-1/2} + \Delta t \cdot \tilde{I}_{i,r-1}^{n+1/2} + (\Delta t)^r \cdot I_i^{n-1/2} \quad (10a)\end{aligned}$$

where $\tilde{I}_{i,r=0}^{n+1/2} \triangleq 0$ and $\tilde{V}_{i,m}^{n+1}$ results from a similar treatment of (3b) and (6b) as

$$\tilde{V}_{i,m}^{n+1} = \tilde{V}_{i,m}^{n-1} + \Delta t \cdot \tilde{V}_{i,m-1}^{n+1} + (\Delta t)^m \cdot V_i^{n-1} \quad (10b)$$

where $\tilde{V}_{i,m=0}^{n+1} \triangleq 0$.

The algorithm can be summarized in the following steps for each time step.

Step 1) Express the two-port lumped networks as the impedance/admittance matrix form of (1) and obtain the coefficients of $a_{ij,r}$ and $b_{ij,m}$ $(i, j = 1$ or 2). Calculate the matrices $\mathbf{A}$ and $\mathbf{B}$ according to (5a) and (5b).

Step 2) Calculate $\tilde{I}_{i,r}^{n+1/2}$ and $\tilde{V}_{i,m}^{n+1}$ with the recursive updating formulations (10a) and (10b).

Step 3) Calculate $\mathbf{I}_0^{n+1/2}$ and $\mathbf{V}_0^{n+1}$ using (5c) and (5d).

Step 4) Obtain the two-port $\mathbf{E}_z^{n+1}$ from (9).

Step 5) Go to Step 2 for the next time update.

III. Power/Ground Plane Noise Coupling

A. Measurement and Modeling Setup

Fig. 1(a) and (b) shows the top and bottom view of a BGA package sample, respectively. In the center of the top layer, there is a square ground plane of side length 10.5 mm and a square power ring of 11.4 mm side length surrounding the ground plane. The line width of the power ring is 0.25 mm and the edge to edge distance between the power ring and the ground plane on the top layer is 0.2 mm. The solder ball array is

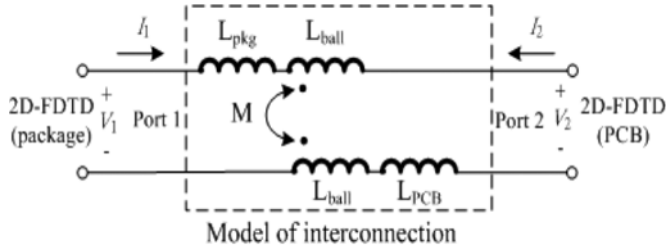

Fig. 2. Relation between the 2-D FDTD and the interconnection matrix.

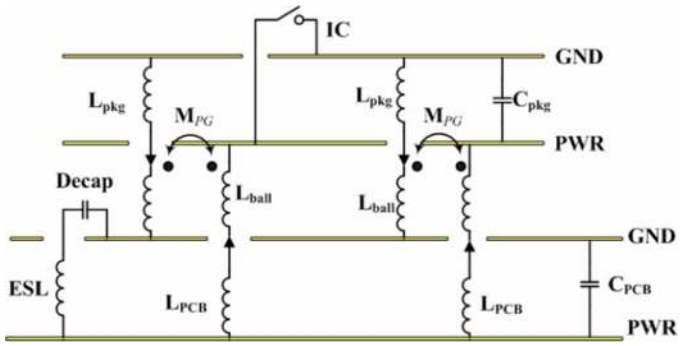

Fig. 3. Equivalent circuit model based on the geometry of the combined structure.

designed on the bottom layer and, as shown in Fig. 1(b), there are 16 ground balls surrounded by another 16 power balls. As shown in Fig. 1(c), the BGA package of 2.7 cm × 2.7 cm is electrically mounted on a test PCB of 10 cm × 8 cm through 32 solder balls of 670 μm diameter. The BGA package is located at 1.5 cm and 1 cm distance from the PCB left and top edge, respectively. Fig. 1(d) shows the cross section of the test sample. The BGA package consists of four copper layers with a total substrate thickness of 350 μm. The inner two layers are ground and power layers with 150 μm spacing. A two layer PCB with substrate thickness 700 μm are the power and ground planes on the PCB. The dielectric constant of the BGA and PCB is 4.3. The PDN of the BGA package is electrically connected with that of the PCB by 16 pairs of power and ground balls. S-parameters of the PDN were measured with a vector network analyzer (HP8510C) from 50 MHz to 2 GHz using a Cascade Microtech probe station with two 450-μm-pitch GS probes.

Fig. 2 shows the modeling concept of the 2-D FDTD, including the equivalent circuit model for the interconnects. The space between the power and ground planes on the package and PCB are meshed with 2-D cells of $\Delta x = \Delta y = 1$ mm. The vias and solder balls that connect between the package and PCB are equivalently modeled by lumped inductors in series. As shown in Fig. 3, $L_{\rm PCB}$ and $L_{\rm pkg}$ are the self-inductance of the vias between power/ground plane of the package and PCB, respectively. $L_{\rm ball}$ is the self-inductance of the solder balls. The $M_{\rm PG}$ is the mutual inductance between the power and ground balls. The self inductance associated with the via or balls can be approximated as [18]–[20]

$$L = \frac{\mu_0 d}{2\pi}\left[\ln\left(\frac{R}{r}\right) - 0.75\right] \tag{11}$$

where $R = (a+b)/4$, a and b are the lengths of the longer and shorter edges of the planes, r is the radius of the via, and d is the thickness of the planes. The self inductance of the solder balls are calculated by assuming it is a metal cylinder with the same length and diameter. The mutual inductance between two balls can be approximated as [18]–[20]

$$M_{\rm PG} = \frac{\mu_0 d}{2\pi}\left[\ln\left(\frac{R}{s+r}\right) - 0.75\right] \tag{12}$$

where s is spacing between two vias. The calculated inductance for $L_{\rm PCB}$, $L_{\rm pkg}$, $L_{\rm ball}$, $M_{\rm PG}$ are 0.71, 0.19, 0.52, and 0.02 nH, respectively. Each power/ground interconnects pair is modeled by a two-port equivalent lumped network, as shown in Fig. 2, and linked with the 2-D FDTD updating algorithm based on the proposed recursive algorithm. The parasitic capacitance of the interconnections is neglected.

B. SSN Coupling Between Package and PCB

Fig. 4 demonstrates the measured and simulated $|S_{21}|$ of the PDN with the excitation and receive ports at (22 mm, 73 mm) and (35 mm, 73 mm), respectively. The left lower corner of the package is defined as (0, 0) here. The agreement between the proposed 2-D FDTD and measurement is good, and the proposed approach predicts the noise coupling behavior for the PDN combining the package and PCB from dc to 2 GHz. Simulated results using FEM are also presented in this figure for comparison. Agreement between these two numerical approaches is good as well. A discrepancy exists at frequencies above 1.4 GHz between numerical results either from FEM or the proposed 2-D FDTD/lumped element approach and the experimental results. It could be caused by the perforated power and ground planes in the BGA package sample. They are, however, modeled as solid perfect conductors in these two numerical simulations. As shown in Fig. 1(b), there are over 400 through via holes on the BGA package, and these holes on the planes will increase the effective inductance of the vertical interconnection between package and PCB, which is not accounted for in the simulation. The computing time to obtain the S-parameter responses as shown in Fig. 4 is over 20 h with the 3-D FEM based method, but less than 3 min by the proposed approach. The computing hardware is a personal computer with a Pentium 4 CPU and 1GB memory. In order to understand the interaction between the planes on the distributed PDN, Fig. 5 shows the measured $|S_{21}|$ for three different PDN combinations. The combinations are the package only, PCB only, and the PCB with package attached. In measuring the $|S_{21}|$ of the PCB only, the two ports are located at the positions just beneath the ports of the package as it is attached on the PCB shown as Fig. 1. The PDN of the package behaves as a pure capacitor for frequencies up to 2 GHz, because the first cavity resonance occurs above 2.8 GHz due to its small size. In this frequency range, the noise coupling on the package significantly decreases as the frequency is increased. For the PCB planes only, there are several noise coupling peaks occurring at 0.76, 0.95, 1.22, 1.52, and 1.79 GHz. These peaks correspond to the resonant cavity modes $\rm TM_{10}$, $\rm TM_{01}$, $\rm TM_{11}$, $\rm TM_{20}$, $\rm TM_{21}$, respectively. Comparing

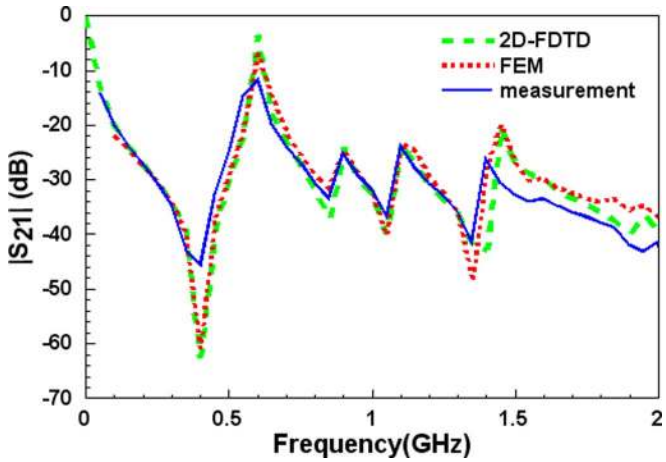

Fig. 4. Measurement and 2-D FDTD/lumped element simulation of the BGA package attached on the PCB.

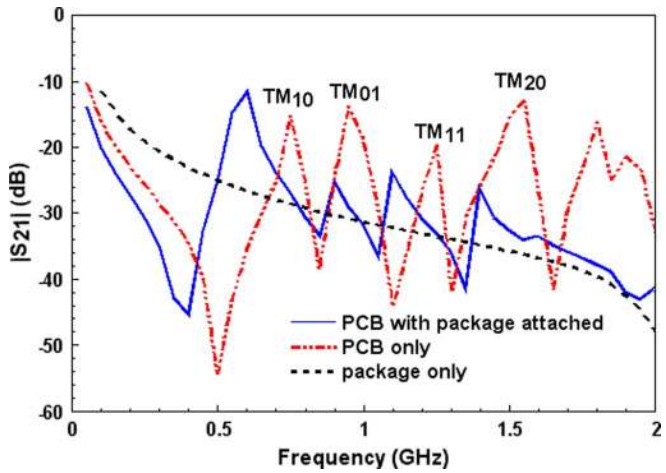

Fig. 5. Measured $|S_{21}|$ of the PDN demonstrating the package/PCB interaction.

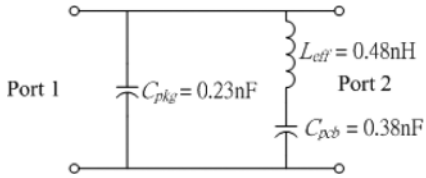

Fig. 6. Equivalent circuit model of the combined PDN for the first peak in Fig. 5

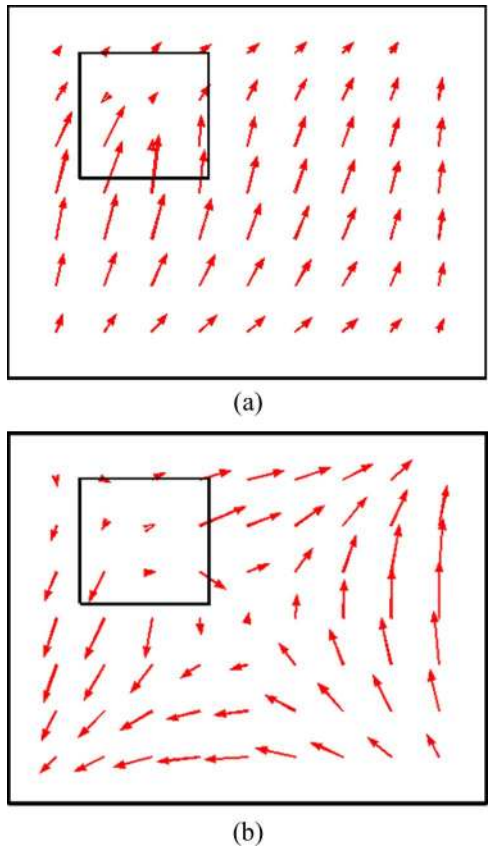

Fig. 7. Current distribution of this multilayer structure at peak frequencies. (a) 900 MHz. (b) 1.1 GHz.

these two cases, the PCB planes provide better noise suppression below approximate 0.7 GHz than the package planes only due to larger parallel-plate capacitance. At higher frequencies, the PCB planes have higher noise coupling than the package planes because of the larger resonant cavity with lower resonance frequencies. With the package mounted on the PCB, the noise coupling seen on the package shows interactions between the package and PCB. As shown in Fig. 5, the PDN behavior is derived by the two shunted capacitors ($C_{\rm pcb} = 0.38$ nF for PCB and $C_{\rm pkg} = 0.23$ nF for package) at frequencies below 0.4 GHz. At frequencies above 0.4 GHz, there are four peaks. The first peak at 0.58 GHz could be explained as the parallel resonance of the capacitance of the package and PCB and the equivalent inductance ($L_{\rm eff} = 0.48$ nH) of the interconnection between the package and PCB, as shown in Fig. 6. The resonant frequency can be calculated as

$$f_r = \frac{1}{2\pi}\sqrt{\frac{C_{\rm pkg}+C_{\rm PCB}}{C_{\rm pkg}C_{\rm PCB}L_{\rm eff}}} \simeq 0.6\ \text{GHz}. \qquad (13)$$

The equivalent inductance is estimated as 0.48 nH, which is larger than the total shunting inductance of the vias and balls calculated by (11). This larger estimation is due to the consideration of the perforated power and ground plane effects near the solder balls. The next three peaks in $|S_{21}|$ are due to the cavity resonance coupling between the PCB and the package.

The calculated vector current distributions on the power plane of the PCB are shown in Fig. 7(a) and (b) at the second and third peak frequencies, 0.9 GHz and 1.1 GHz, respectively. It is clearly seen that the current distributions are similar to those of the cavity $\rm TM_{01}$ and $\rm TM_{11}$ modes on the PCB power/ground planes. Because the power noise fed through the package excites the resonant $\rm TM_{01}$ and $\rm TM_{11}$ modes inside the PCB, the energy of the resonant modes is coupled to the BGA packages through the solder balls. The last peak in $|S_{21}|$ at 1.45 GHz is due to the higher-order $\rm TM_{20}$ mode on the PCB cavity.

C. Decoupling Capacitor Effect on the PDN Response

Fig. 8(a) shows the $|S_{21}|$ for the combined PDN of the package and PCB with eight 100 nF SMT decoupling capacitors on the PCB. As shown in Fig. 8(b), these capacitors are placed around the package with locations indicated in the figure.

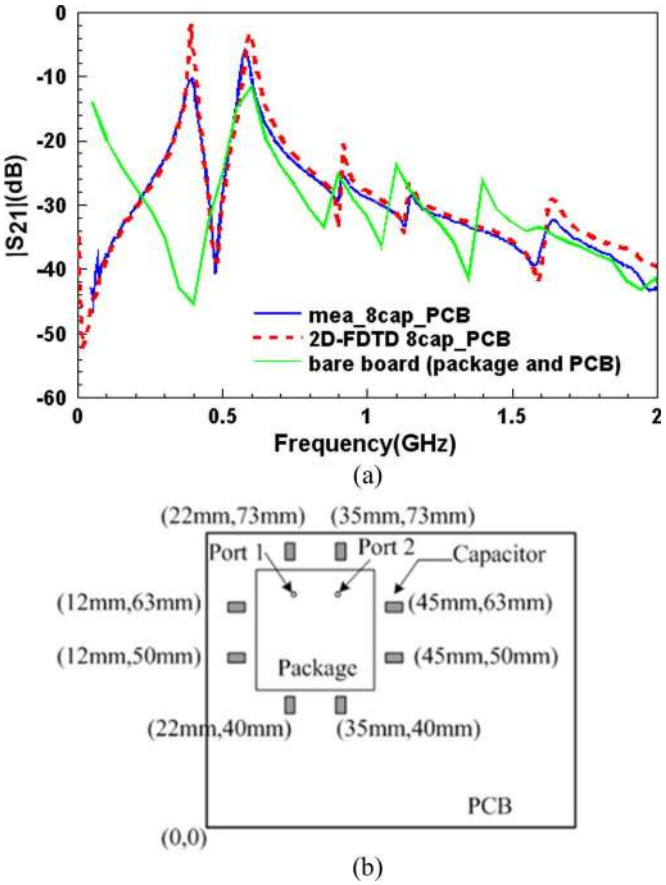

Fig. 8. (a) Comparison of the $|S_{21}|$ between eight capacitors and no capacitors on the PCB. (b) Arrangement of the decoupling capacitors on the PCB.

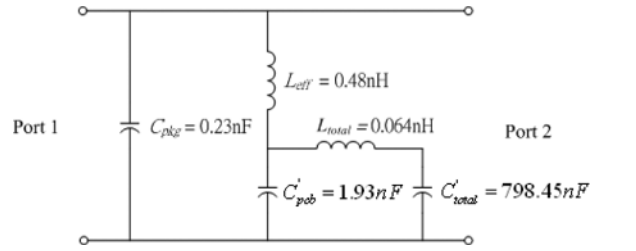

Fig. 9. Equivalent circuit model of the combined PDN with the decoupling capacitors placed on the PCB.

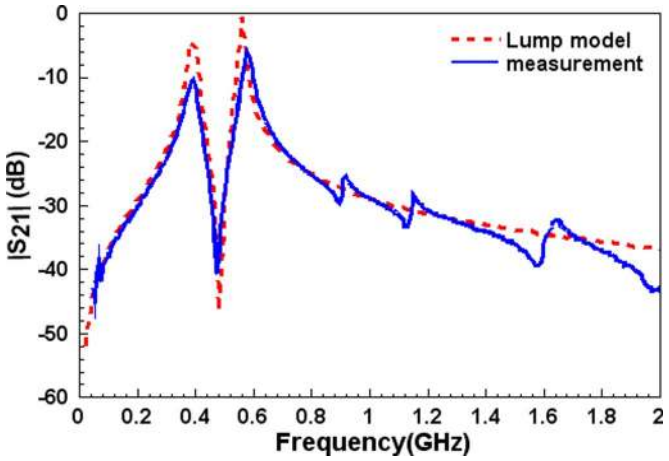

Fig. 10. $|S_{21}|$ of the lumped model for the combined PDN with the decoupling capacitors placed on the PCB.

Comparing the measured and modeled results in Fig. 8(a), the proposed 2-D FDTD modeling algorithm agrees well with the measurement including the decoupling capacitors. Each capacitor is modeled as a lumped one-port network in the 2-D FDTD method with an equivalent series inductance (ESL) of 0.512 nH. The computing time for obtaining the S parameter response is also less than 3 min. The previous measured result for the combined PDN with no decoupling capacitors is also shown for comparison. The $|S_{21}|$ is significantly decreased below approximately 200 MHz, because there is a transfer impedance zero at approximately 23 MHz, which results from the series resonance of the decoupling capacitors and their ESL. However, in the frequency range between 200 and 500 MHz, the PDN with eight capacitors on the PCB has a noise peak at approximately 400 MHz. The reason could be the parallel resonance of the ESL of the decoupling capacitor and the shunting capacitance of the PCB and package. Fig. 9 shows the equivalent lumped model of the combined PDN with eight decoupling capacitors $(C_{\text{total}} = 800\ \text{nF})$ placed on the PCB. The L_{total} in Fig. 9 is obtained by shunting eight ESL of decoupling capacitors. Fig. 10 shows the $|S_{21}|$ of the lumped model and the measurement result. Good agreement is seen. It is noted that this agreement is fitted by simultaneously increasing the parallel-plate capacitance of the PCB and decreasing the total capacitance of the eight decoupling capacitors by a small number $\Delta = 1.45\ \text{nF}$, i.e., $C'_{\text{PCB}} = C_{\text{PCB}} + \Delta = 1.93\ \text{nF}$ and $C'_{\text{total}} = C_{\text{total}} - \Delta = 798.45\ \text{nF}$. The reason for the adjustment could be explained by the variation of the PCB capacitance due to the soldering of these eight decoupling capacitors on PCB. Above 500 MHz, the noise coupling behavior is similar to the case without SMT capacitors on the PCB.

There are many factors that can influence the noise coupling behavior with using SMT decoupling capacitors, such as the capacitor number, capacitor value, capacitor locations (on the package or on the PCB), and so on. The focus of this work is on the time-domain modeling and its validity, and the PDN designs are not discussed here.

IV. Conclusion

An efficient numerical approach based on the 2-D FDTD method is proposed to model the power/ground plane noise coupling on the PDN including the interconnects between the package and PCB. The equivalent R–L–C circuits of the via and the solder balls connecting between the package and PCB can be incorporated into the 2-D Yee cells based on an integral formulation in the time domain. An efficient recursive updating algorithm is proposed to fit these lumped networks into the Yee equations. A test sample with BGA package attached on a PCB was fabricated, and its noise coupling behavior was measured and compared with the numerical results. The effect of decoupling capacitor on the power noise coupling was also modeled numerically and demonstrated experimentally. The proposed approach predicts the results well. In addition, the computing efficiency is significantly improved for the proposed

approach as compared with the other 3-D-based methods. The stability issue is not discussed here, and it will be our further research.

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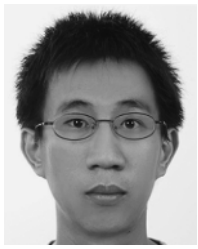

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