Modeling of Crosstalk in Through Silicon Vias

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***Abstract*—This paper presents analytical formulas to extract an equivalent circuit model for coupled through silicon via (TSV) structures in a 3-D integrated circuit. We make use of a multiconductor transmission line approach to model coupled TSV structures. TSVs are embedded in a lossy silicon medium, hence they behave as metal–insulator–semiconductor (MIS) transmission lines. The models we present can accurately capture the transition between slow-wave and dielectric quasi-TEM modes, which are characteristic for MIS transmission lines, as well as the metal–oxide–semiconductor (MOS) varactor capacitance. The results agree well with 2-D quasi-static simulations and 3-D full-wave electromagnetic simulations. The derived equivalent circuit models can easily be applied in circuit simulators to analyze crosstalk behavior of TSVs in a 3-D integrated system.**

***Index Terms*—3D IC, crosstalk, metal–insular–semiconductor (MIS) transmission line, through silicon via (TSV).**

I. Introduction

POWER delivery and dissipation are the primary limiters of performance and integration in CMOS scaling [1]–[3]. Conventional 2-D integration technologies are also limited in terms of bandwidth. As an example, the only way to achieve >1 TB/s memory bandwidth between a CPU and memory module has been identified as memory on logic using 3-D integration in [4]. Hence, 3-D IC integration is a necessary path for further power reduction and improved bandwidth in electronic systems. Even though other approaches have been studied in the past toward a 3-D computer [5], the 3-D IC integration technology and silicon interposers at the present rely on through silicon vias (TSVs) for vertical interconnections. The improvement in power and bandwidth by adapting a 3-D integration methodology, therefore, depends on the electrical properties of TSVs.

At the present, 3-D integration technology is rapidly evolving with different configurations being investigated. One major classification can be made in terms of the choice of bonding sides of the dies consisting of face-to-face, back-to-back, and face-to-back bonding. Another major classification can be made in terms of the TSV process order consisting of via-first, via-middle, and via-last approaches. An example is shown in Fig. 1, which corresponds to a via-last, face-to-back configuration. Various TSV configurations exist as well, such as coaxial [6]–[8], rectangular, circular, and tapered configurations [9]. TSV pitches down to 3 μm have been reported [10] promising a 3-D IC without an interconnect routing bottleneck. In all possible configurations, it is of great interest to understand the electrical properties of TSVs inside the silicon substrate. The purpose of this paper is to develop models to be able to better understand the cross talk mechanisms in commonly used circular TSVs. This paper presents a TSV modeling approach based on a formula previously used for modeling of crosstalk in ribbon cables [11], [12].

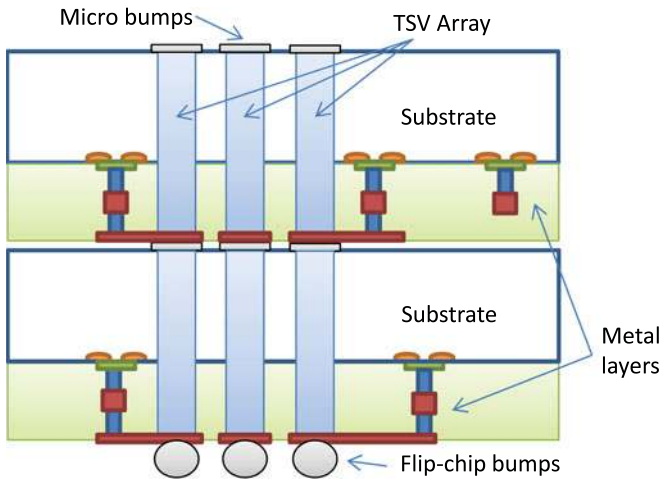

Fig. 1. Simplified cross section of a 3-D IC showing TSVs connecting two tiers in face-to-back configuration.

Inductance and resistance models for TSVs studied in the literature include analytical determination of RL values for tapered TSV configurations [13], lumped skin effect model for the TSV resistance [14], and modeling of the eddy-current losses on silicon for a pair of TSVs in [15] and [16]. RF and millimeter wave measurements of these parameters have been reported in [17]–[19].

Capacitance and conductance models for TSVs in the literature differ significantly in terms of handling the metal–oxide–semiconductor (MOS) capacitance effect. The nonlinear semiconductor effects are typically neglected in TSV analysis, assuming that within the range of biasing conditions the semiconductor can be described as a linear medium with its conductivity and permittivity. To simultaneously account for the wave propagation and nonlinear semiconductor effects, one would need to solve Maxwell's equations along with motion equations for charged particles [20]–[22]. The nonlinear semiconductor effect for TSVs is typically represented in a simpler way with the formation of a depletion capacitance depending on the substrate bias voltage [23]. Closed form expression for TSV RLC parasitic elements are given in [24] including a planar

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depletion capacitance approximation neglecting the curvature of the via. A more accurate depletion width can be calculated by solving the 1-D Poisson's equation in cylindrical coordinates as in [25] and [15]. By tailoring the oxide charges, the depletion width can be kept at a maximum (hence at a constant value) for regular substrate biasing conditions, resulting in minimal TSV capacitance [26]. The variation of TSV capacitance due to the transition from accumulation to depletion mode was also experimentally confirmed in [27]. In this study, we adopt the approach of modeling the depletion region as a lossless dielectric in electromagnetic simulation of TSVs [28]. We also assume that the substrate is not grounded in the vicinity of the TSVs, which would change the electric field distribution and hence the total capacitance of the TSV pair. The depletion capacitance is still included in the model though, as it is formed at high frequency as a result of slow thermal generation of electrons [29], independent of the proximity of substrate contact. If a signal TSV is closer to a substrate contact than a ground TSV, accurate analysis would require 3-D simulation to take into account the presence of the substrate contact (see e.g., [30] and [31]).

In TSVs, the medium carrying high-frequency signals is the lossy silicon, similar to metal-insulator-semiconductor (MIS) planar microstrip lines or coplanar waveguides. Electromagnetic behavior in MIS TSVs and MIS transmission lines are different than in traditional transmission lines, due to the presence of the slow-wave, dielectric quasi-TEM, and skin-effect modes. Existence of these three types of modes has been shown for MIS microstrip lines [32], [33], and MIS coplanar waveguides [34]–[36]. A methodology for obtaining closed-form expressions for the series impedance of planar MIS interconnects based on a complex image method has been presented in [37]. The mentioned three modes have been confirmed recently on TSVs in [38]. The transmission line behavior can be adequately described using a quasi-TEM mode assumption as in traditional transmission lines considering all the three modes [39], hence it is possible to use simple 2-D quasi-static simulations to capture the effects of various modes. In this study, we develop a multiconductor transmission line model that can capture the slow-wave and dielectric quasi-TEM modes. Skin-effect mode occurs at a higher frequency than 100 GHz for the types of parameters we studied.

There are only few works that study or model the MOS capacitance effects in MIS transmission lines. In [40], the dependence of MIS coplanar waveguide properties on the bias voltage has been demonstrated with the conclusion that the attenuation is at a minimum at the depletion region, since interface losses are negligible.

Capacitive crosstalk among TSVs is considered critical in 3-D ICs in [41]. Crosstalk and noise coupling among TSVs studied in the literature include formulas for capacitive coupling effects between TSVs and nearby interconnects [42], and numerical methods for a TSV array embedded in a parallel-plate waveguide structure [43], [44]. Modeling of noise coupling in a TSV array by extending single TSV model to coupled TSVs is presented in [45]. In this study, we adopt an equivalent circuit model for the coupled capacitance and conductance similar to the model in [46]. Unlike other works, we develop an analytical approach for the calculation of the circuit elements.

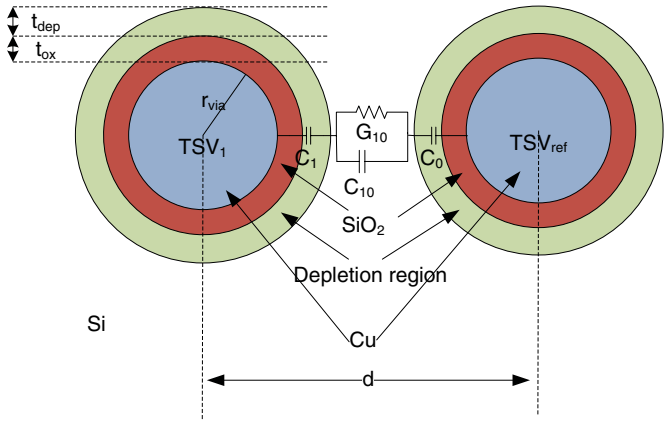

Fig. 2. TSV pair and its equivalent circuit model showing the side wall capacitances C_1 and C_0 and the capacitance and conductance through silicon C_{10} and G_{10}.

The main contribution of this study is the development of an analytical TSV model that captures the MOS capacitance effect, slow-wave and dielectric quasi-TEM modes, and full RLGC coupling terms in an array of TSVs. The presented approach is based on 2-D analysis of TSVs. Since transmission line models are used, any length of TSVs can be accurately modeled. There is also no restriction on the number of TSVs in the array.

II. TSV as an MIS Transmission Line With MOS Capacitance

Consider a TSV pair as shown in Fig. 2. Because of the presence of a low-loss SiO_2 layer in addition to a lossy silicon layer between the two vias, such a TSV pair will support wave propagation in slow-wave, dielectric quasi-TEM, and skin-effect modes similar to an MIS transmission line. At low frequencies, the wave propagation will be in slow-wave mode. At this mode, the magnetic field is not affected by the presence of the lossy silicon, hence the loop inductance is same as if the two vias were in free space. The capacitance of the vias, however, is side wall capacitances defined by the gate-oxide thickness and depletion widths, since silicon behaves more as a lossy conductor than a dielectric (i.e., $\omega C_{10} \ll G_{10}$). Note that the conductance and capacitance of silicon are related by its conductance σ_{Si} and permittivity ε_{Si} as follows:

$$G = C\frac{\sigma_{Si}}{\varepsilon_{Si}}. \tag{1}$$

Hence, as the frequency significantly exceeds

$$f_e = \frac{\sigma_{Si}}{2\pi\varepsilon_{Si}} \tag{2}$$

the relationship turns to $\omega C_{10} \gg G_{10}$, and wave propagation occurs in quasi-TEM dielectric mode. In this mode, wave propagation is similar to a lossy transmission line, since the displacement current through silicon completes electric field lines from the signal TSV to the reference TSV.

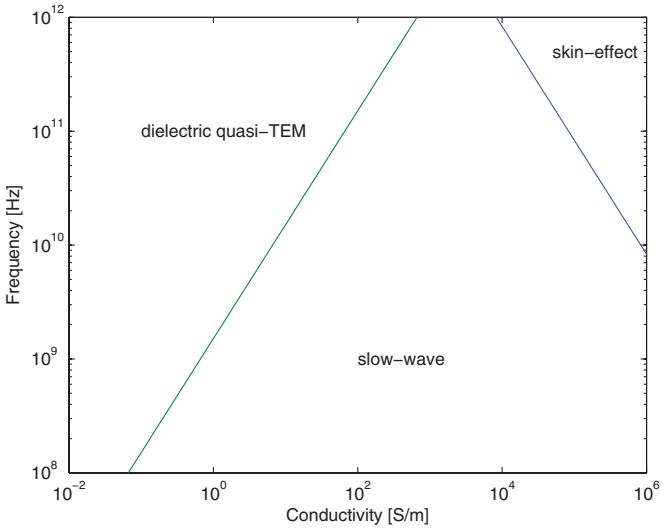

Fig. 3. Conductance-frequency chart showing the possible propagation modes on TSVs assuming a silicon depth of $b = 5.52\,\mu$m between the vias and $\varepsilon_{Si} = 11.9\varepsilon_0$.

In both modes, the loop inductance of the vias remains the same. If conductivity of silicon is high, there may be a transition from the slow-wave mode to a skin-effect mode around the frequency

$$f_\delta = \frac{1}{b^2 \pi \mu \sigma_{Si}} \tag{3}$$

when the skin depth in silicon becomes same as the depth of the silicon layer ($b = d - 2[r_{\rm via} + t_{\rm ox} + t_{\rm dep}]$) between the two vias. In the skin effect mode, the return current of the signal via flows on the silicon substrate, increasing the signal loss.

The location of these boundaries is shown on the conductance-frequency chart on Fig. 3. As the chart demonstrates, a very high conductivity would be required for the skin-effect mode to occur below terahertz frequencies, hence we will not consider the skin-effect mode in the developed models. The modeling of the inductance and resistance can then be done similar to a two-wire system in free space.

The transition from slow-wave to quasi-static TEM mode occurs at a low enough frequency to be of concern for medium-resistivity silicon at about $\sigma_{\rm Si} = 10$ S/m. Hence, it needs to be captured for accurate modeling. As an example, a 10-μm long TSV pair with the parameters $r_{\rm via} = 1\,\mu$m, $t_{\rm ox} = 0.5\,\mu$m, $t_{\rm dep} = 0.74\,\mu$m, $d = 10\,\mu$m, $\varepsilon_{Si} = 11.9\varepsilon_0$, $\varepsilon_{ox} = 3.9\varepsilon_0$, $\sigma_{\rm Si} = 10$ S/m has been simulated using a 3-D full-wave simulator Ansys HFSS [47] as shown in Fig. 4. The capacitance and conductance were extracted from full-wave simulation by calculating the TSV input admittance when the far-end is left unterminated. The figure also shows the transition frequency f_e between slow-wave and dielectric quasi-TEM modes calculated for this example using (2). The frequency-dependent behavior observed in these parameters is due to the transition between the two modes around f_e. It can also be explained based on the equivalent circuit model shown in Fig. 2. At low frequencies (i.e., in the slow-wave mode region), the total capacitance is the series of C_1 and C_0 only, since the susceptance of C_{10} is

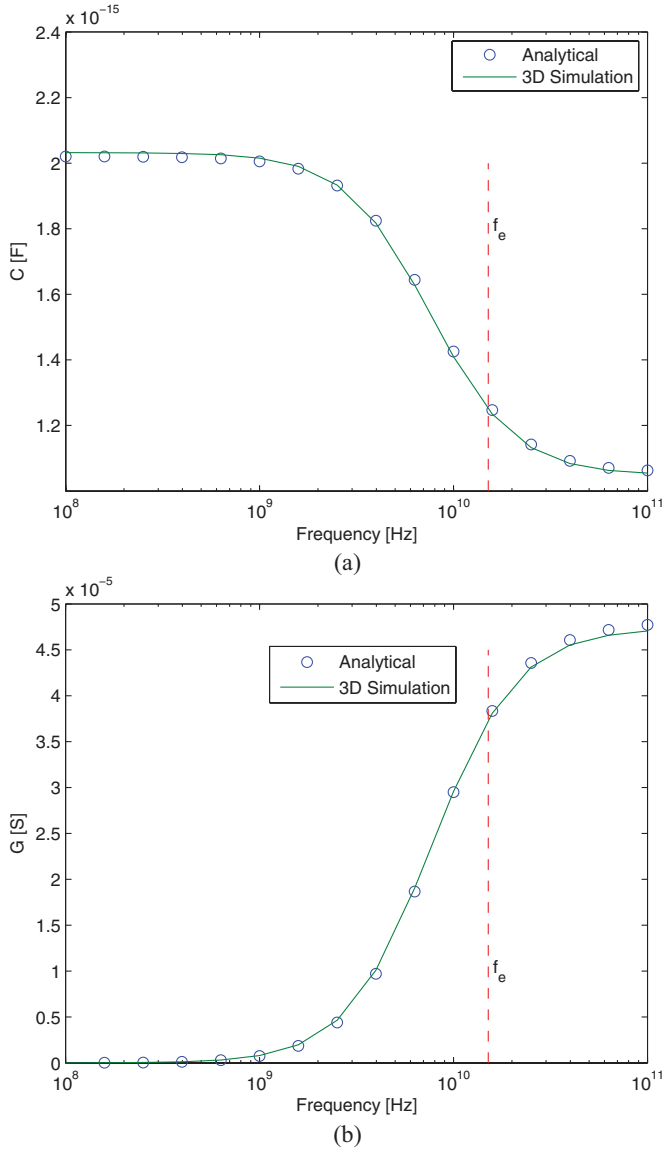

Fig. 4. Analytical results versus HFSS simulation of (a) capacitance and (b) conductance of a TSV pair.

negligible compared to G_{10}. As the frequency increases (i.e., in the dielectric quasi-TEM mode region), the total capacitance ultimately becomes the series of C_1, C_0, and C_{10}.

Fig. 4 also shows good agreement with the analytical method, which will be described next. The capacitance and conductance of a via pair is represented using the equivalent circuit model shown in Fig. 2. In this model, the side-wall capacitance C_1 can be extracted using coaxial line capacitance formula as follows:

$$C_1 = \left(\frac{\ln\left(\frac{r_{\rm via}+t_{\rm ox}}{r_{\rm via}}\right)}{2\pi\varepsilon_{\rm ox}} + \frac{\ln\left(\frac{r_{\rm via}+t_{\rm ox}+t_{\rm dep}}{r_{\rm via}+t_{\rm ox}}\right)}{2\pi\varepsilon_{\rm Si}} \right)^{-1} \tag{4}$$

where $\varepsilon_{\rm ox}$ is the permittivity of the SiO_2 layer [15]. We apply multiconductor transmission line theory to generate an equivalent circuit model, so all the circuit elements we derive in this paper will be per unit length.

The first term in the side-wall capacitance formula in (4) is the oxide capacitance, whereas the second term is the depletion capacitance. Hence, the major effect of the depletion capacitance is decreasing the total TSV capacitance. The depletion capacitance in general depends on the gate bias. For signal TSVs, it is desirable to have small capacitance, hence the depletion width should be kept at a maximum. This can be achieved by tailoring oxide charges during the oxidation such that the TSV is in the maximum depletion region for signals between 0 V and V_{dd} [26]. Under this assumption, the depletion width will be at a maximum for practical gate bias voltages, hence a constant depletion capacitance will be in effect. In this paper, we will assume maximum depletion width.

The TSV side-wall capacitance then behaves similar to an MOS varactor, where the formula for the depletion layer width $t_{\rm dep}$ [15] is repeated here for completeness:

$$\frac{4\varepsilon_{\rm Si}kT}{q^2N_a}\ln\left(\frac{N_a}{n_i}\right) = -0.5t_{\rm dep}^2 - t_{\rm dep}(r_{\rm via}+t_{\rm ox}) + (r_{\rm via}+t_{\rm ox}+t_{\rm dep})^2\ln\left(\frac{r_{\rm via}+t_{\rm ox}+t_{\rm dep}}{r_{\rm via}+t_{\rm ox}}\right). \quad (5)$$

This nonlinear equation needs to be solved to extract the maximum depletion width $t_{\rm dep}$. Assuming that the curvature of the via is negligible compared to the depletion width (i.e., $t_{\rm dep} \ll r_{\rm via}+t_{\rm ox}$), the truncated Taylor series expansion of (5) provides the well-known formula for the maximum depletion width of planar MOS capacitors:

$$t_{\rm dep} = \sqrt{\frac{4\varepsilon_{Si}kT}{q^2N_a}\ln\left(\frac{N_a}{n_i}\right)} \quad (6)$$

where silicon permittivity $\varepsilon_{\rm Si} = 11.9\varepsilon_0$, Boltzmann constant $k = 1.38\times10^{-23}$ J/K, room temperature $T = 300$ K, electron charge $q = 1.602\times10^{-19}$ C, intrinsic semiconductor concentration $n_i = 1.08\times10^{10}$ cm^{-3}, doped acceptor concentration $N_a = 1.25\times10^{15}$ cm^{-3} has been used throughout this study. For a TSV radius of $r_{\rm via} = 1\,\mu$m and oxide thickness of $t_{\rm ox} = 0.5\,\mu$m, (5) results in a maximum depletion width of $t_{\rm dep} = 0.74\,\mu$m.

Fig. 5 shows a comparison of the maximum depletion width obtained through the cylindrical MOS capacitor formula in (5) with the planar approximation in (6). For small vias, the planar approximation can introduce an error approaching 10%; therefore, we will use the cylindrical capacitor formula in this paper.

The capacitance C_{10} can then be calculated using the capacitance formula for a two-wire system, where the wire boundaries are taken from the edge of the depletion layer. Hence, the assumption being made is that the distance between the two vias is much larger than the depletion width and the oxide thickness so that an equipotential surface exists at the edge of the depletion layer. In the next section, we use this approximation to extend this modeling approach to multiple coupled vias.

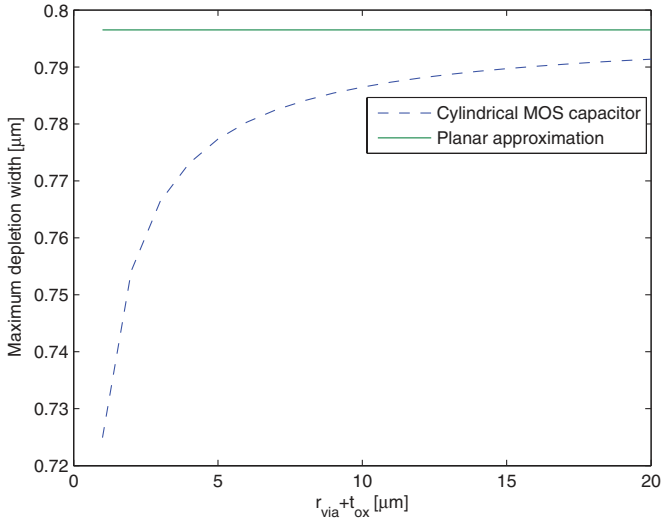

Fig. 5. Maximum depletion width obtained through the cylindrical MOS capacitor formula in (5) compared with the planar approximation in (6).

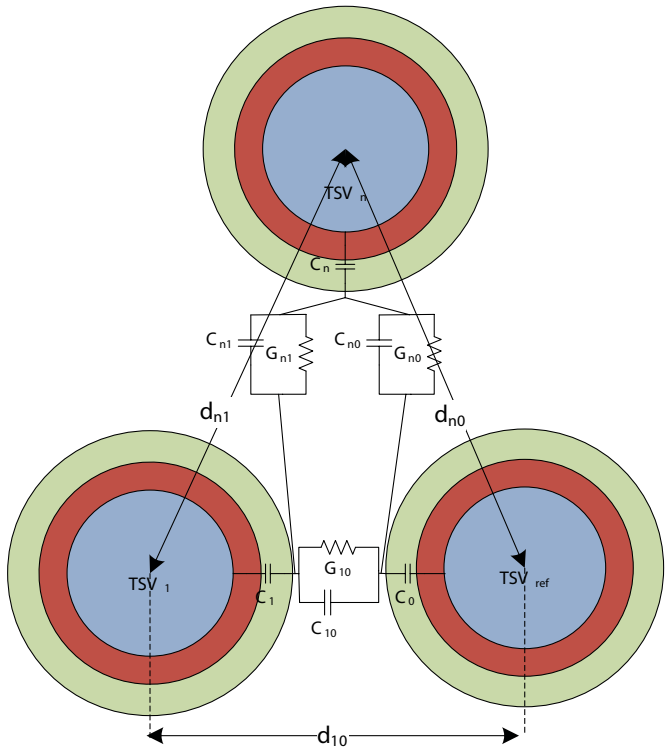

Fig. 6. Capacitance and conductance model for multiple coupled TSVs.

III. Capacitance and Conductance Models for Coupled TSVs

Consider that there are other TSVs in the vicinity of the original TSV pair. A corresponding equivalent circuit model for this configuration is shown in Fig. 6.

The presence of other TSVs do not affect the side-wall capacitances C_i; however, the capacitances through the silicon layer C_{ij} change in the presence of other TSVs. Hence, the formulas for a single TSV pair cannot be applied for this configuration.

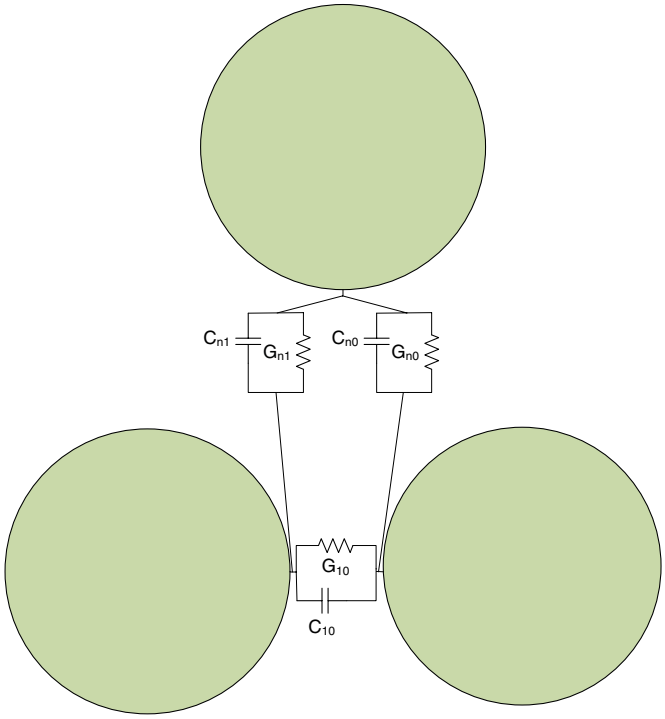

Fig. 7. Equivalent model for Fig. 6 to calculate the silicon capacitance and conductance. The circles represent the outer edges of the depletion region.

The full coupled TSVs need to be simultaneously considered. Since the problem is calculating C_{ij}, we consider an equivalent problem as shown in Fig. 7, where the capacitances that need to be calculated are between the outer edges of the depletion layers. Similar to a single TSV pair case, we regard each circle representing the outer edge of the depletion layer as an equipotential surface. The problem then reduces to calculating the capacitance matrix of round wires in a homogeneous medium as shown in Fig. 7. A similar problem has been considered in the literature to calculate the capacitance matrix of ribbon cables [11], [12]. We follow the same approach, which first starts with calculating the inductance matrix of the structure:

$$L_{ii} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_{i0}^2}{r_i r_0}\right) \tag{7}$$

$$L_{ij} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_{i0} d_{j0}}{r_0 d_{ij}}\right) \tag{8}$$

where μ_0 is the permeability of free space. The radius of the ith circle is given by $r_i = r_{\mathrm{via},i} + t_{\mathrm{ox}} + t_{\mathrm{dep}}$, whereas the radius of the reference wire is r_0. For the examples we consider, all the vias have same radius. The capacitance and conductance matrices can then be obtained as

$$\overline{\overline{C}} = \mu_0 \varepsilon_{Si} \overline{\overline{L}}^{-1} \tag{9}$$

$$\overline{\overline{G}} = \mu_0 \sigma_{Si} \overline{\overline{L}}^{-1}. \tag{10}$$

In (7) and (8), the inductance matrix is not the total inductance between vias, since the radius of the circles is not taken as $r_i = r_{\mathrm{via},i}$. Therefore, even though the silicon capacitance and conductance is obtained using transmission-line matrix relations as in (9) and (10), we emphasize that the total capacitance and inductance matrices are not related by these equations in the slow-wave mode. The total capacitance includes the contribution of the side-wall capacitance, which is not considered in (9) and (10).

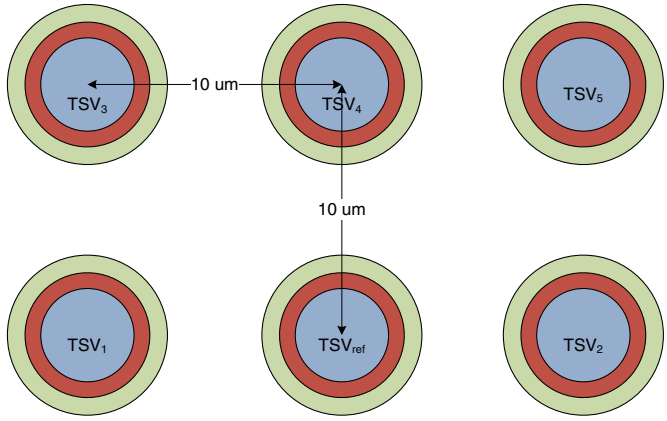

Fig. 8. Six coupled TSVs where the middle TSV in second row is taken as the ground TSV.

This method has been applied on six coupled TSVs as shown in Fig. 8. The pitch between TSVs is $10\,\mu\mathrm{m}$, and the individual TSV dimensions are the same as in previous examples.

Fig. 9 shows all the simulated admittance parameters for the six coupled TSVs as well as the admittance parameters obtained through the analytical model. The simulations were done using a 2-D quasi-static simulator (electric current module in COMSOL [48]). An excellent match can be seen. Because of geometrical symmetry, some of the admittance matrix elements are same and not repeated in the figure.

For a single TSV pair, it is intuitive to convert the real and imaginary parts of the admittance to an equivalent frequency-dependent conductance and capacitance as in Fig. 4. However, if we treat a coupled TSV structure as a conventional transmission line and extract the coupled conductance and capacitances, the resulting element values can be negative and nonintuitive because of the presence side-wall capacitances C_i. Therefore, we chose to compare the admittance matrix elements directly as shown in Fig. 9.

IV. Inductance and Resistance Models for Coupled TSVs

The inductance matrix can similarly be obtained using (7) and (8), where $r = r_{\mathrm{via}}$. This corresponds to the external inductance of the TSVs. Considering the conductance-frequency chart in Fig. 3, we assume that the skin-effect mode is not effective and the medium can be treated as lossless for series inductance calculations. For each TSV, we apply the formula for the internal impedance of a round wire that can be computed analytically as

$$Z = \frac{\sqrt{j\omega\mu/\sigma}}{2\pi r} \frac{I_0(r\sqrt{j\omega\mu\sigma})}{I_1(r\sqrt{j\omega\mu\sigma})}\ \Omega/m \tag{11}$$

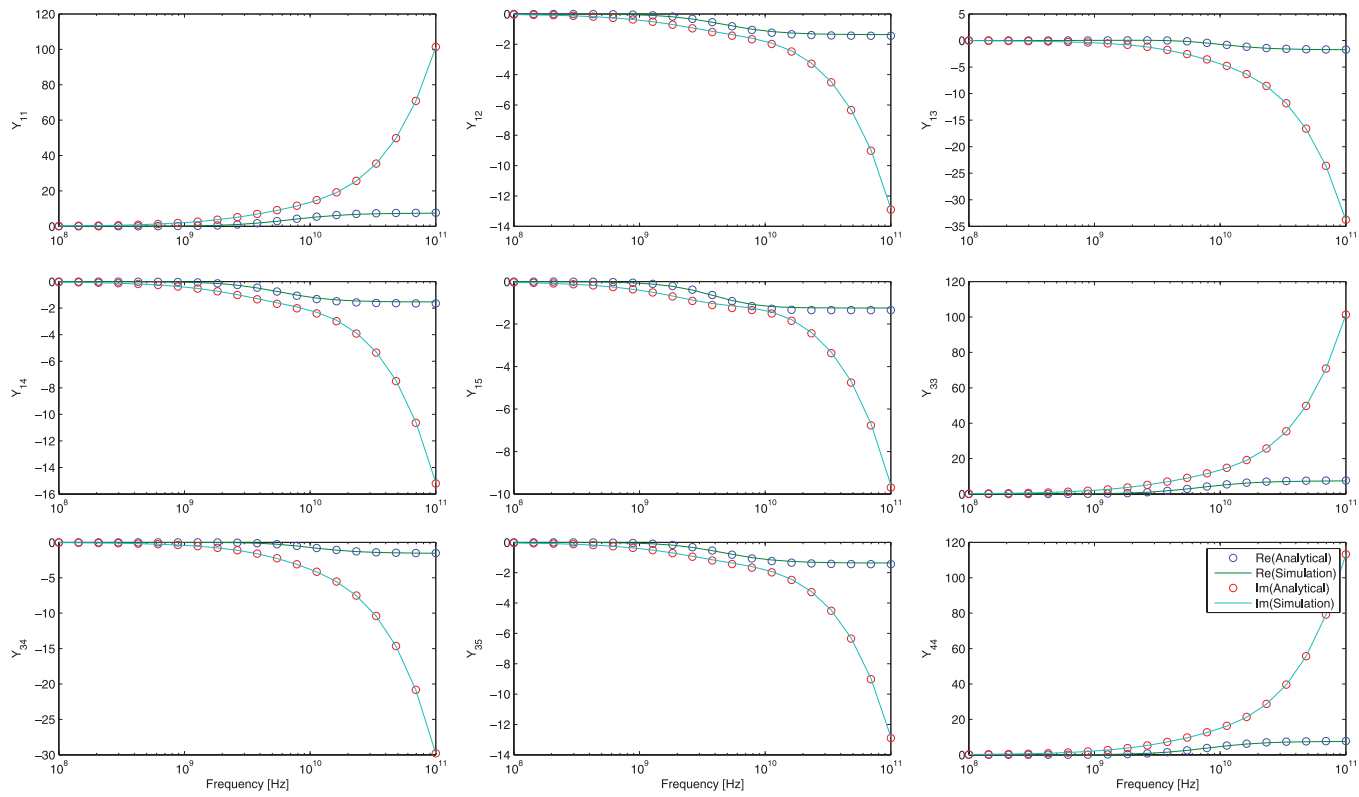

Fig. 9. Per unit length admittance matrix for six coupled TSVs (units in S/m). Proposed analytical approach versus quasi-static 2-D (COMSOL) simulations.

where σ is the conductivity of the via metal, I_0 and I_1 represent the modified Bessel functions of order zero and one, and r is the radius of the via [49]. In Fig. 12, the series internal impedances can then be calculated as $Z_i = Z$. The imaginary part of the internal impedance contributes as internal inductance to the overall inductance matrix.

As an example, elements in the first row of the inductance matrix calculated using 2-D quasi-static simulation (COMSOL) and presented model are shown in Fig. 10. The self, mutual inductances along with the frequency-dependent variation of the inductance matrix due to the internal inductance is very accurately captured.

The resistance matrix elements are shown in Fig. 11. All the off-diagonal terms of the resistance matrix are similar to R_{12} (since they correspond to the resistance of the reference TSV); therefore, they are not shown in the figure. The self-resistance R_{11} is approximately twice as the coupling resistance R_{12}, since R_{11} includes the resistance of the signal and ground TSV. The skin-effect resistance and transition from dc to ac resistance is very well captured using the presented model.

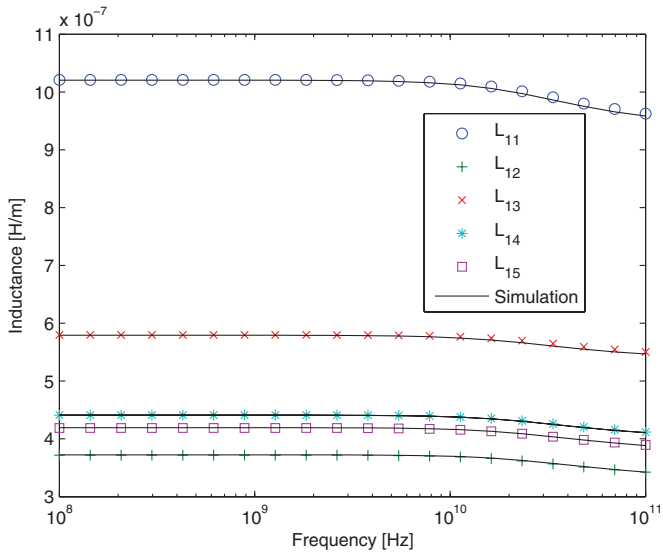

Fig. 10. Inductance matrix elements for six coupled TSVs. Solid lines show 2-D COMSOL simulations, markers show the analytical result.

V. Full Coupled TSV Model

The presented capacitance, conductance, resistance, and inductance models are combined in Fig. 12, which is a general coupled TSV model similar to the representation of a multiconductor transmission line in terms of its per unit length parameters. Based on this model, configurations with multiple return TSVs with arbitrary assignments in the TSV array can also be represented. One way of achieving this is by changing the reference TSV in the inductance matrix and reducing the size of the inductance matrix using matrix operations as described in [50].

For verification of the presented approach with full-wave electromagnetic simulations, scattering parameters based on this model are compared with full-wave simulations from Ansys HFSS as shown in Fig. 13. The TSV parameters are the same as

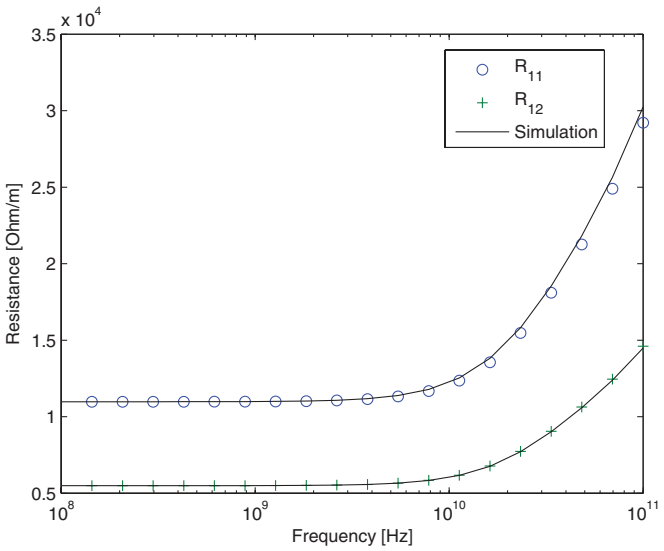

Fig. 11. Resistance matrix elements for six coupled TSVs. Solid lines show 2-D COMSOL simulations, markers show the analytical result.

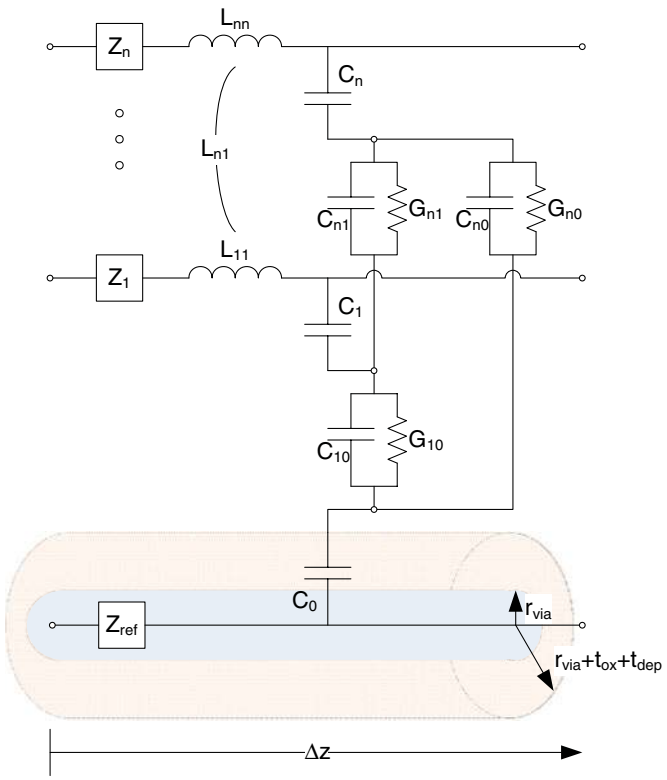

Fig. 12. Multiconductor transmission line model for coupled TSVs. All the circuit elements in the figure can be obtained from per unit length RLGC matrix elements by multiplying them with Δz.

the example in Fig. 4. The length of the vias was 10 μm, resulting in a small insertion loss. In HFSS simulations, a depletion region was included. There is a very good agreement between HFSS and the analytical model. The analytical model was also calculated without the depletion region to see its impact. We observe a difference around the transition frequency f_e between

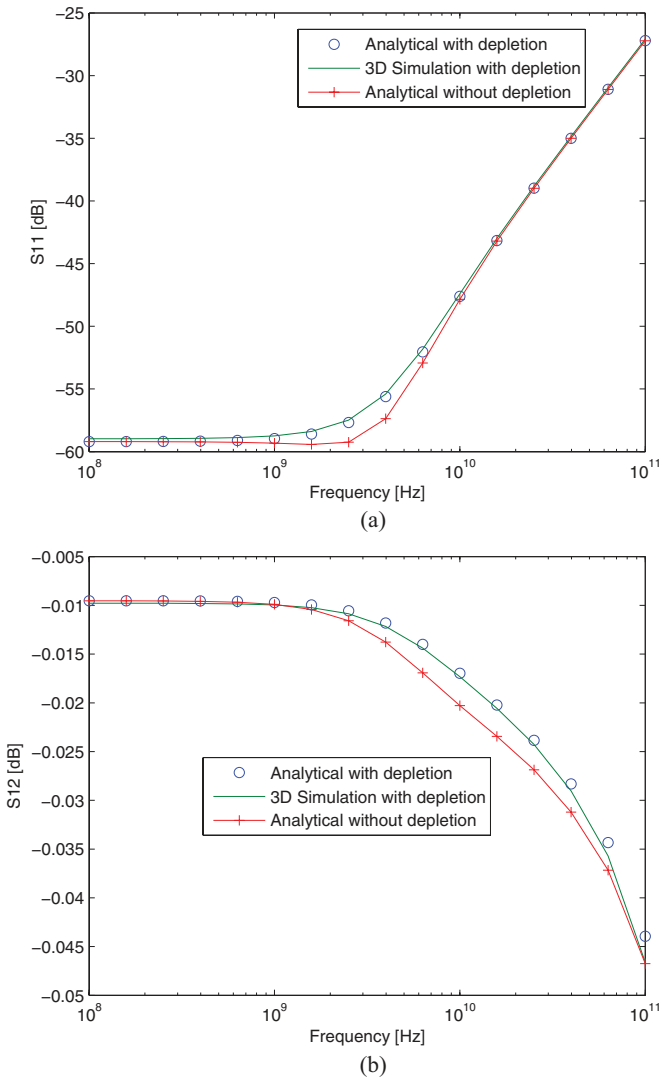

Fig. 13. HFSS simulation versus analytical model with and without the depletion region for a single TSV pair.

the slow-wave and dielectric quasi-TEM modes. A deviation is expected especially at low frequency (i.e., the slow-wave mode region), where the effective capacitance is solely the side-wall capacitance [51]. However, this is not the case, and the scattering parameters become flat at a similar level at lower frequencies. This indicates that the via resistance, and not the capacitance, is the dominant factor in the scattering parameters at the considered frequency range. For larger vias, the depletion capacitance would have an impact at lower frequencies as in [51].

Next, three coupled TSVs were simulated by removing the top row in Fig. 8 to validate the accuracy of the analytical model for TSV crosstalk simulation as shown in Fig. 14. For these simulations, port 1 and port 2 were defined at the top side of the vias, whereas port 3 and port 4 were at the bottom. Hence, S_{11} is the reflection coefficient, S_{12} represents the near-end crosstalk, S_{13} is the transmission coefficient, and S_{14} represents the far-end crosstalk. All the scattering parameters agree well as shown in the figure.

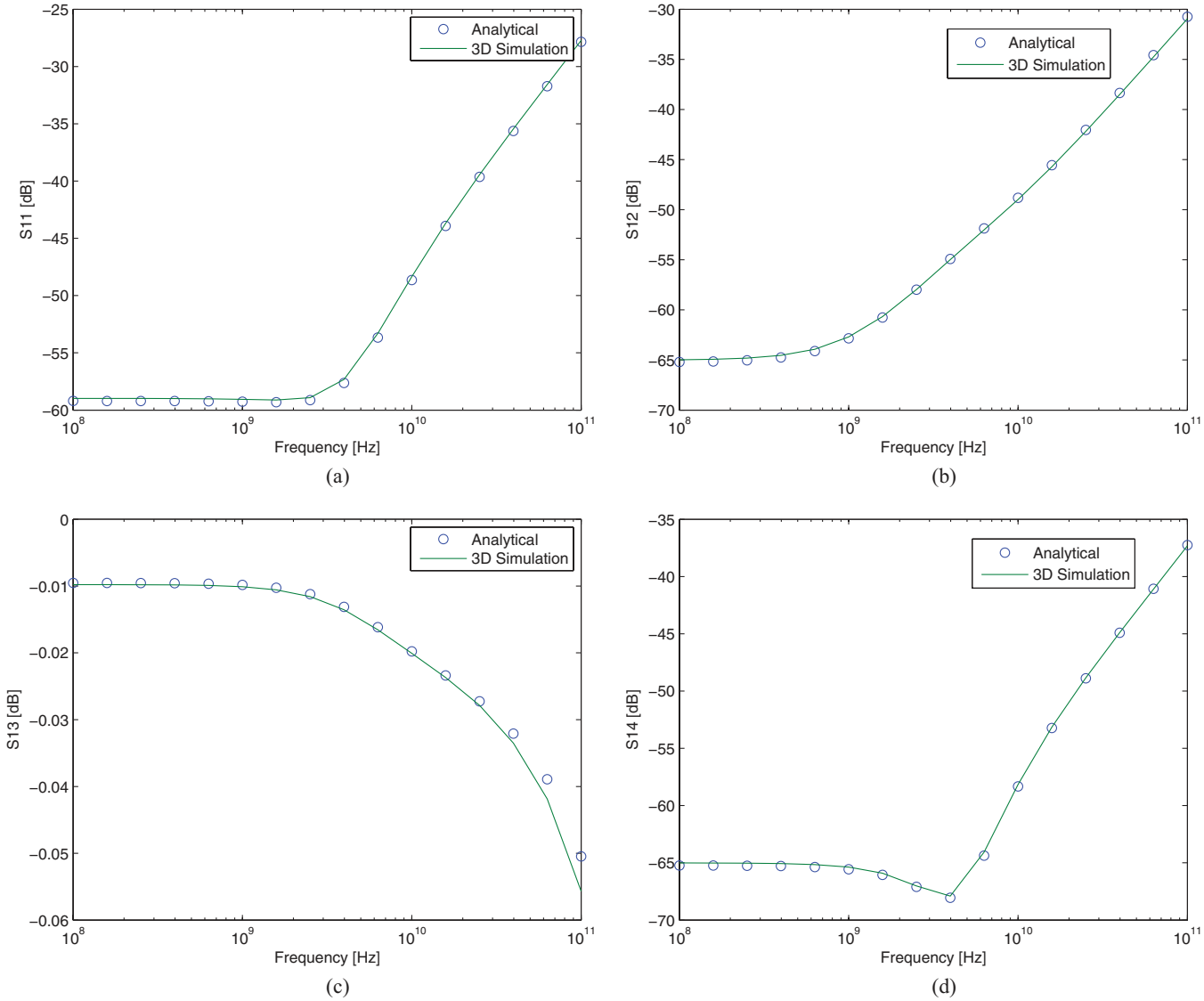

Fig. 14. Analytical results versus HFSS simulation for three colinear TSVs. The TSV in the center is the ground TSV. S_{11} is the reflection coefficient, S_{12} represents the near-end crosstalk, S_{13} is the transmission coefficient, and S_{14} represents the far-end crosstalk.

VI. Conclusion

An analytical approach for obtaining the per unit length RLGC matrices of TSVs was presented. The external inductance matrix is calculated using a simple formula that has been applied before in modeling crosstalk in ribbon cables. The internal inductance and resistance matrices are calculated based on the internal impedance formula for a round wire. The capacitance and conductance matrices are calculated in two steps. In the first step, cylindrical capacitance formulas are used assuming an equipotential surface at the edge of the depletion region. In the second step, capacitance and conductance through silicon is calculated based on the inverse of the inductance matrix of an equivalent problem. Hence, all of the elements of the RLGC matrices of coupled TSVs are obtained using an analytical approach. Comparisons with quasi-static 2-D and full-wave 3-D simulations show good agreement with the presented approach. With this approach, it is possible to account for the MOS capacitance effect as well as the MIS transmission line effects including slow-wave and quasi-TEM dielectric mode wave propagations. To analyze signal integrity and crosstalk behavior of coupled TSVs, a standard π or T-model based on lumped segmentation of the presented multiconductor transmission line model can be used. For more accurate simulations, the extracted RLGC matrices can be used in circuit simulators that support multiconductor transmission lines with frequency-dependent RLGC parameters.

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