Modeling of IC power supply and I/O ports from measurements

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Abstract: This paper addresses the generation of behavioral models of digital ICs for signal and power integrity simulations. The proposed models are obtained by external port measurements and by the combined application of specialized state-of-the-art modeling techniques. The proposed approach is demonstrated on the I/O buffers and the core power supply ports of a commercial 90nm flash memory.

1 Introduction

Nowadays, the modeling of the power supply and I/O ports of ICs is of paramount importance for the simulation of many advanced electronic applications. The modeling from measured transient responses, in particular, is a key resource to handle ICs whose suppliers provide low-order or partial models only. Besides, when power supply ports are involved, the modeling from measured responses can be the best option to cope with the complexity of the problem.

Parametric modeling of I/O ports from measured transient responses has been addressed in [1] and the modeling of power supply ports is addressed in [2, 3, 4]. In this paper, we demonstrate those methods by developing models for both I/O and power supply ports for an high-speed IC memory, that is a 512Mb NOR Flash memory in 90nm technology produced by Numonyx. As shown in the schematic of Fig. 1, the test device has 16 high-speed I/O buffers (DQn terminals) for data communication and separate - weakly coupled - supply ports for the core logic (VDD-VSS terminals) and the high-speed I/O buffers (VDDQ-VSSQ terminals). This device is a medium complexity IC for System-in-Package (SiP) application and is therefore a good test case for the modeling approach being addressed.

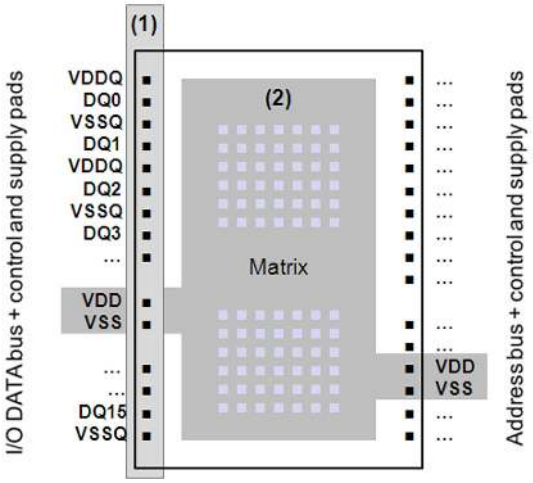

Figure 1: Simplified structure of the example IC highlighting the data bus (*i.e.,* the I/O buffers DQn in the scheme) and the different sub-networks VDDQ-VSSQ (1) and VDD-VSS (2) composing the power delivery network of a digital memory.

The test board that has been developed to carry out the transient measurements used in the modeling process is also described. The test board allows accurate measurements of the IC supply currents as well as of the voltage and currents of the I/O ports at the same time. Besides, the developed board can be easily adapted to test different ICs.

2 Model structures

This paper focuses on the modeling of the I/O ports (DQn) and of the core power supply port (VDD-VSS). The structure of the models and the data required for the estimation of the model parameters are shortly outlined in this Section.

2.1 VDD-VSS core power supply

According to [2, 3, 4], the models for the core power supply of ICs are defined by simplified - physically inspired - circuit equivalents that attempt to describe the different blocks involved in the power delivery network of the digital IC. A common assumption in these approaches is the description of the power delivery network of the IC by means of a Norton equivalent where the short-circuit current generator accounts for the internal switching activity of the

device and the equivalent impedance accounts for the passive interconnect structure (see Fig. 2). It is ought to remark that this assumption holds when the physical dimension of the silicon die and the frequency bandwidth of interest are compatible with lumped modeling and the effects of possible nonlinearities in the supply port behavior are negligible. When these conditions are met, this simplification is the best solution to estimate the model parameters from external measurements.

The estimation of the Norton model of the core power supply port, however, requires care in collecting, interpretating and processing the measured data. The estimation of the equivalent impedance has been proven to be best achieved via on-chip two-port scattering parameter measurements as suggested in [4]. In contrast to measurements based on fixtures including package and external interconnects, this solution generates responses free from resonant effects, leading to improved accuracy levels. Once the port impedance at die-level is known, the actual impedance at the IC port is obtained by taking into account the package effects via electromagnetic modeling.

For the test IC of this paper, the measurement and estimation of the impedance of the model is addressed in [4]. Here we concentrate on the estimation of the equivalent current source via the measurement of the switching activity. This measurement must be carried out with the device mounted on a board and operating in nominal conditions, as it is explained in the next Section.

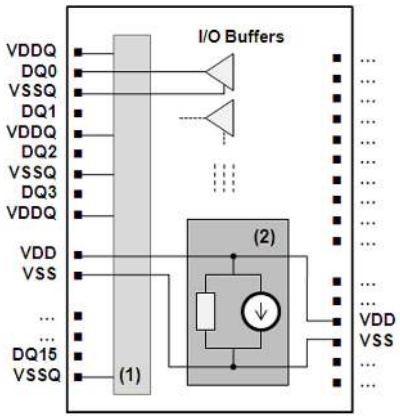

Figure 2: IC structure with highlighted the different blocks representing the different behavioral models considered in this study.

2.2 I/O buffers

According to [1, 6], the models of the output buffers DQn exploit the following two-piece parametric relation:

$$i(t) = w_H(t) i_H(v(t), d/dt) + w_L(t) i_L(v(t), d/dt) \tag{1}$$

where i and v are the buffer output port voltage and current variables, with associated reference directions, w_H and w_L are switching signals accounting for the device state transitions and i_H and i_L are nonlinear parametric relations accounting for the device behavior in the fixed high and low logic states, respectively.

The estimation of model (1) amounts to computing the parameters of submodels i_H and i_L and the weighting signals w_H and w_L from suitable port voltage $v(t)$ and current $i(t)$ responses. These estimation responses must be recorded while the buffer drives different loads and performs state switchings. Model parameters are then computed by minimizing suitable error functions between the model and the measured responses, which are used as references to be fitted.

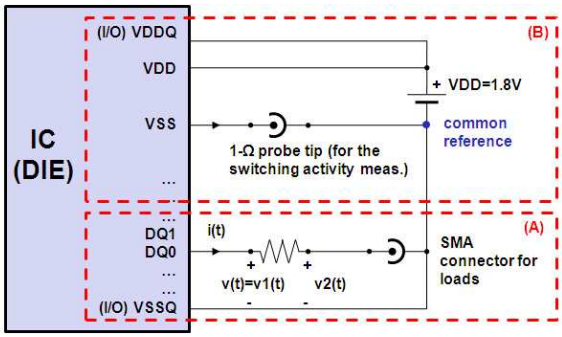

Figure 3: Schematic of the test setup for the measurement of the core switching activity (box A) and of the buffer port voltage and currents waveforms (box B).

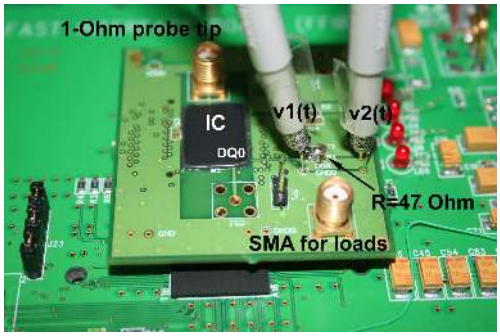

Figure 4: Measurement board for recording the core switchig activity and the buffer waveforms for the example IC. The key elements of the setup can be recognized.

3 Test board

As outlined in the previous Section, the transient measurement required for the modeling study of this paper, are the switching activity at the core power supply port and the voltage and currents waveform at the buffer ports recorded during state switching and for different loads. The ideal schematic of a setup for the measurement of these quantities is shown in Fig. 3. In this setup, the switching current of the core power supply port is measured by means of a 1-Ω current probe that has been suitably designed and series connected to the VSS pad. This method and the probe design follows the guidelines of [5].

The buffer voltage waveform is obtained by direct measurement, whereas the current waveform is obtained by means of the series resistor of Fig. 3. The connector on the buffer output is used to plug-in the different loads needed to generate the estimation waveforms [1].

In order to implement this setup, a test board composed of a general purpose control circuitry for the operation of the device under test and of a measurement board holding the IC under test and the measurement fixture has been developed. The measurement board is connected to the control board via a pair of 40-pin QTE connectors, and can be replaced to test different ICs. A close-up of the measurement board for the example IC of this paper is shown in Fig. 4.

In all the measurements carried out within this activity, a LeCroy WavePro 7300A scope (3GHz bandwidth, 10GS/s) and two single-ended passive voltage probes P6158 (3GHz bandwidth, 1 kΩ, 1.5 pF, 20x attenuation) have been used to collect the transient waveforms. To reduce the effects of the measurement noise, the memory buffers have been forced to produce a periodic bit pattern and the averaging feature of the scope has been set (16 waveforms are considered for the average).

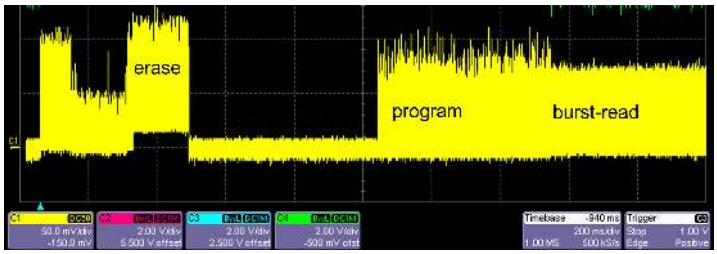

Figure 5: Measured power supply current obtained while the memory is driven to perform the three basic cycles (*i.e.,* the erase, programn and burst-read programs).

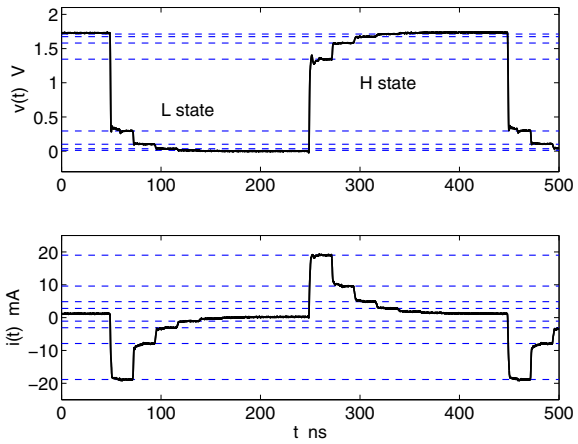

Figure 6: Responses obtained by driving the buffer DQ0 in Fig. 3 to produce a periodic '010' bit pattern on suitable transmission line load. The dashed lines highlight the steps of the voltage and current responses that allows for the extraction of the static parts of submodles i_H and i_L.

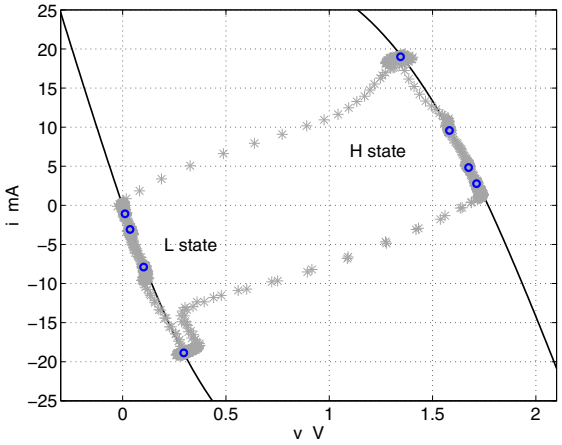

Figure 7: Static characteristics of the DQ0 buffer. Solid lines: transistor-level response; gray stars: region explored by the $v(t)$,$i(t)$ samples of the transient responses of Fig. 6; Circles: static points extracted from the curves of Fig. 6.

4 Results

This Section illustrates measurements and models developed in this study.

Figure 5 shows an example of the switching current recorded as explained in the previous Section. The different patterns corresponding to the basic erase, program and read cycles can be clearly distinguished. Supplemental study based on numerical simulations allowing for the package effects proved that the value of the signal-to-noise ratio of this measurement is good for frequencies up to $500\,\mathrm{MHz}$. Besides, the relation between the impedance of the supply network of our test board and the Norton model impedance guarantees that the measured switching current is close to the equivalent current source of Fig. 2. The cross-validation of the complete model obtained in this way is currently under development.

The model of the output buffers is based on i_H and i_L submodels (see eq. 1) defined as sum of a static and a dynamic part. The static parts is extracted form the measured responses of Fig. 6, that are obtained by driving the buffer to produce a periodic '010' sequence on a transmission line load. The $\{i, v\}$ pairs corresponding to the flat parts of the waveforms of Fig. 6 are shown in Fig. 7, which proves the excellent accuracy of the static behavior extracted by this approach. The remaining model parameters, including the dynamic parts of submodels and the weighting signals are estimated as suggested in [1] from the edges of the waveforms of Fig. 6.

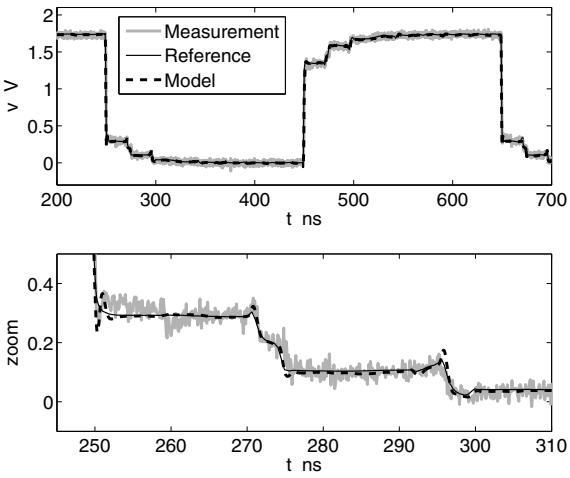

Figure 8: Port voltage and current responses of the DQ0 buffer for the validation test considered in the study (see text for details).

The waveforms of a validation of the complete buffer model built in this way are shown in Fig. 8. This Figure compares the measured and predicted response of the modeled buffer for a load different from those involved in the parameter estimation process. The load consists of the shunt connection of an open ended coaxial cable ($Z_0 = 50\,\Omega$, $L = 2.6\,m$) with a coaxial cable ($Z_0 = 50\,\Omega$, $L = 2\,m$) terminated by a $C = 15\,pF$. Both the response of the estimated model and the response of the high-order transistor level model of the buffer provided by the foundry are shown in the Figure.

The very good agreement among the curves of Fig. 8 confirms the strengths of the proposed methodology in generating accurate models from measured transient responses. Such models can be easily obtained by the proposed measurement setup and can effectively replace the hardly available and less efficient transistor-level models of ICs.

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