# Modeling of Lead-Frame Plastic CSPs for Accurate Prediction of Their Low-Pass Filter Effects on RFICs

Tzyy-Sheng Horng, *Member, IEEE*, Sung-Mao Wu, Hui-Hsiang Huang, Chi-Tsung Chiu, and Chih-Pin Hung

***Abstract*—This paper presents a direct extraction method to construct the electrical models of lead-frame plastic chip scale packages for RF integrated circuits (RFICs) from the measured $S$-parameters. To evaluate the package effects on the reciprocal passive components, the insertion and return losses for an on-chip 50-Ω microstrip line housed in a 32-pin bump chip carrier (BCC) package were analyzed based on the established package model. Excellent agreement with measurement has been found up to 15 GHz. When applied to the nonreciprocal active components, the gain variations for a heterojunction-bipolar-transistor array housed in an 8-pin BCC package have also been successfully predicted up to 22 GHz. Both cases have demonstrated that the package acts as a low-pass filter to cause a sharp cutoff for the RFIC components above a certain frequency.**

***Index Terms*—Integrated circuit packaging, package effects, package modeling techniques, plastic packaging.**

## I. Introduction

In TODAY'S wireless communications, there is a robust trend toward higher microwave frequencies for RF integrated circuits (RFICs) to meet the increasing bandwidth for higher data rate. Meanwhile, the package effects are more evident to degrade RFICs. The conventional lead-frame plastic packages like thin shrink small outline packages (TSSOPs) and thin quad flat packs (TQFPs) that are currently the most often used for RFICs have been pushed to their limits of bandwidth and are considered as a dominant barrier to RFICs operating above UHF band. Recently, lead-frame plastic chip scale packages (CSPs) such as small outline nonlead (SON), quad flat nonlead (QFN), leadless plastic chip carrier (LPCC), and bump chip carrier (BCC) packages are gaining in popularity. These CSPs offer a smaller size than TSSOPs and TQFPs with a promising better performance at higher frequencies.

In the past, quasi-static approaches have been given to construct the equivalent $L, C, R$ matrices for the plastic packages [1]–[3]. However, these matrices are mainly low-frequency results and possess difficulties in providing a full picture of the high-frequency phenomena such as resonance, mutual coupling, impedance mismatch, and frequency-dependent losses. Considering the package as a multiport microwave network, some literature have demonstrated extraction of the equivalent circuits for the conventional small-outline integrated-circuit (SOIC) packages from $S$-parameters based on full-wave simulations [4]–[6] and vector-network-analyzer measurements [7], [8]. The equivalent models established are mainly focused on the package structure itself. The interaction between package and chip was not yet explored and usually plays a more important role to affect RFIC performance. Our previous research [9] was devoted to direct extraction of the package models from the measured $S$-parameters and has deduced the electrical superiority of lead-frame plastic CSPs over TSSOPs in the applications to RFICs by comparing the resultant low-pass filter effects predicted from the models. In this paper, a more complete model for lead-frame plastic CSPs including the chip's bond-pad and common-ground parasitic effects has been proposed to characterize such a low-pass filter behavior over a wide frequency range. The theoretical predictions corresponding to several packaged test components prepared in the experiment agree quite well with the measured results.

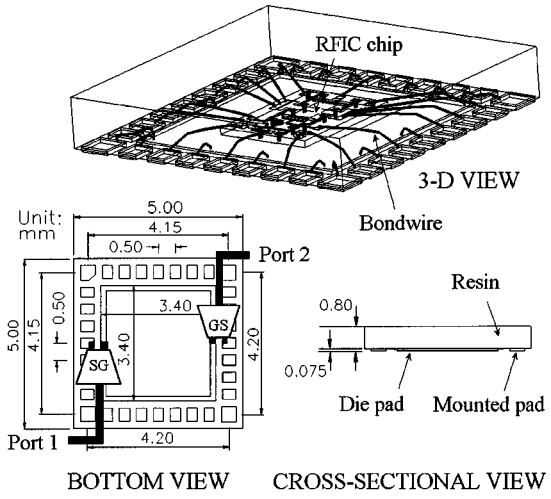


Fig. 1. Configuration of the 32-pin BCC$^{++}$ package and illustration of its measurement with microwave probes.

## II. Modeling Techniques

As an example, in Fig. 1, an electrically and thermally enhanced BCC (abbreviated as BCC$^{++}$) package with a pin count

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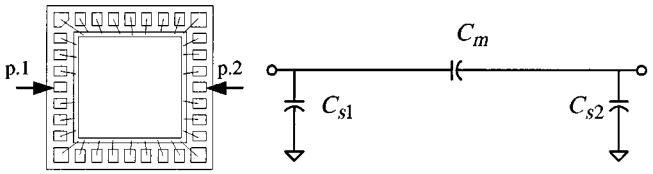



Fig. 2. Wire-bonding diagram and equivalent model of the 32-pin BCC$^{++}$ package sample under test for evaluating the mounted-pad capacitances.

of 32 has been modeled. In comparison with a 32-pin TQFP, this package measuring 25 mm$^2$ reduces almost one-half in the area of mounting footprint. As illustrated in the three-dimensional (3-D) sketch of Fig. 1, the plastic BCC$^{++}$ package seals the semiconductor chip within the molding resin and exposes the peripheral mounted pads and center die pad on the package underside. Electrical connection between the chip and mounted pads relies on bond wires only and such a leadless configuration can reduce the package inductance and capacitance substantially. In addition, the die pad can be soldered directly to a ground plane on the printed circuit board to provide excellent ground shield and thermal spread.

In the bottom view of the 32-pin BCC$^{++}$ package, as seen in Fig. 1, the center die pad often treated as a microwave ground is coplanar with the other peripheral mounted pads. The two-port $S$-parameters for an arbitrary pair of the I/O paths can be measured directly with a pair of fixed-pitch signal–ground/ground–signal (SG/GS)-type microwave probes connected to a vector network analyzer by landing the probe's signal and ground tip on the package's mounted and die pad, respectively. Therefore, unlike TSSOPs and TQFPs, there is no need to design an additional test fixture in consideration of the probe landing, which saves a great effort to calibrate the fixture parasitics. The modeling technique proposed here adopts a step-by-step procedure. In each step, we measure a package sample of different designs in wire bonding to extract the equivalent-circuit elements from impedance or admittance representation of the measured $S$-parameters. The results are also inserted into the subsequent extraction in the next step such that the measured data can be stripped during the extraction process yielding, step by step, a full set of circuit elements. Fig. 2 shows the wire-bonding diagram for a package sample with the fifth and twenty-first mounted pads under test open circuited and its equivalent circuit. Note that the other unused mounted pads are all connected to the ground by down bonding to the rim of the die pad. In the extraction, the measured $S$-parameters ($[S]^{\mathrm{op}}$) from 1 to 15 GHz are converted into the admittance parameters ($[Y]^{\mathrm{op}}$) from which the shunt and mutual capacitances can be found as

$$[Y]^{\mathrm{op}} = Z_0^{-1}\left([U] + [S]^{\mathrm{op}}\right)^{-1}\left([U] - [S]^{\mathrm{op}}\right) \quad (1)$$

$$C_{s1} = \mathrm{median}\left(\mathrm{Im}\,(Y_{11}^{\mathrm{op}} + Y_{12}^{\mathrm{op}})/\omega\right) \quad (2)$$

$$C_{s2} = \mathrm{median}\left(\mathrm{Im}(Y_{22}^{\mathrm{op}} + Y_{12}^{\mathrm{op}})/\omega\right) \quad (3)$$

$$C_m = \mathrm{median}\left(-\mathrm{Im}\,(Y_{12}^{\mathrm{op}})/\omega\right) \quad (4)$$

where a median of a frequency-dependent distribution $X(f)$ is defined by a value of $x$ such that the probability of $X(f) < x$ is less than or equal to 1/2 and the probability of $X(f) \geq x$ is also less than or equal to 1/2 for 1 GHz $\leq f \leq$ 15 GHz. The above

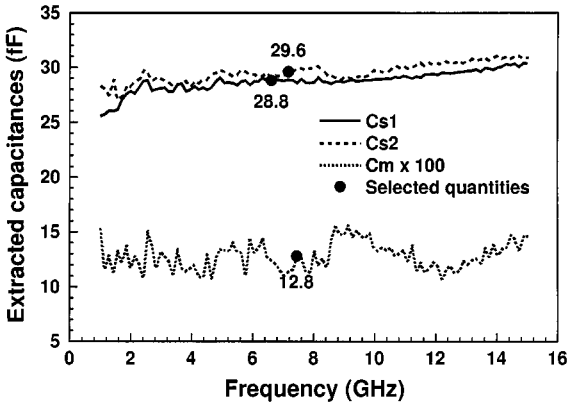
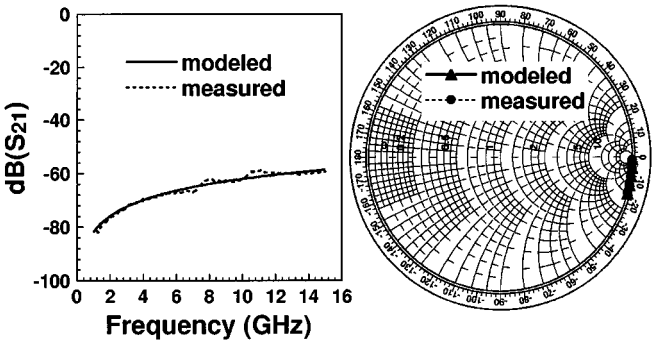



Fig. 3. Extracted and selected quantities of the mounted pad capacitances.




(a) (b)

Fig. 4. Comparison between modeled and measured results of: (a) $S_{21}$ in decibels and (b) $S_{11}$ on the Smith chart for the configuration of Fig. 2.

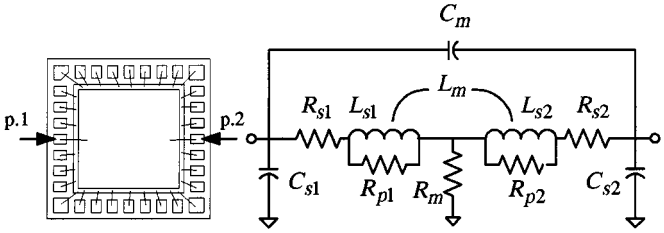



Fig. 5. Wire-bonding diagram and equivalent model of the 32-pin BCC$^{++}$ package sample under test for evaluating the bond-wire parasitic elements.

expressions assume a weak frequency dependence for each extracted element such that its medium value can be selected for use in the model. The impedance of this measurement system $Z_0$ is equal to 50 Ω. The extracted and selected capacitance quantities are shown in Fig. 3. The $S$-parameters generated with the selected quantities have been compared to the measured results, as shown in Fig. 4. Excellent agreement can be found.

Fig. 5 shows another package sample with the mounted pads under test wire bonded to the die pad, as well as the other unused mounted pads. In the equivalent circuit provided in Fig. 5, except the same $\pi$ model of three capacitances in the outer shell, two lossy inductances with mutual terms are included to account for the bond-wire parasitic effects. A series-parallel $LR$ model, as suggested in [9], has been used to approximate the bond wire's frequency-dependent losses in the frequency range from 1 to 15 GHz. In the equivalent circuit, the series resistances $R_{s1}, R_{s2}$ are selected by the quantities extracted

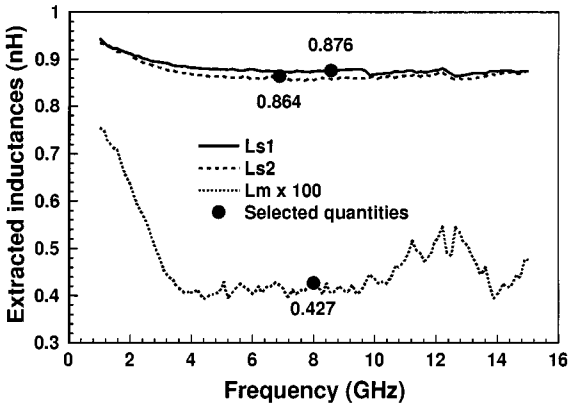



Fig. 6. Extracted and selected quantities of the bond-wire inductances.

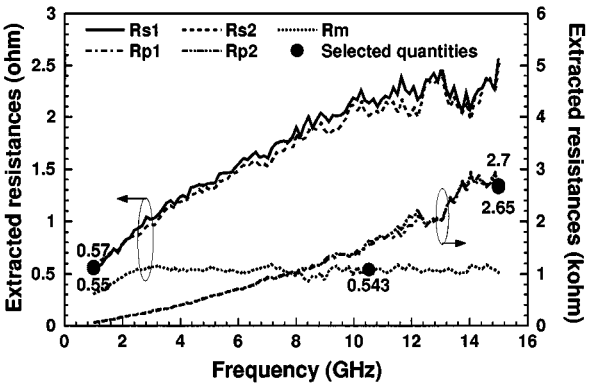
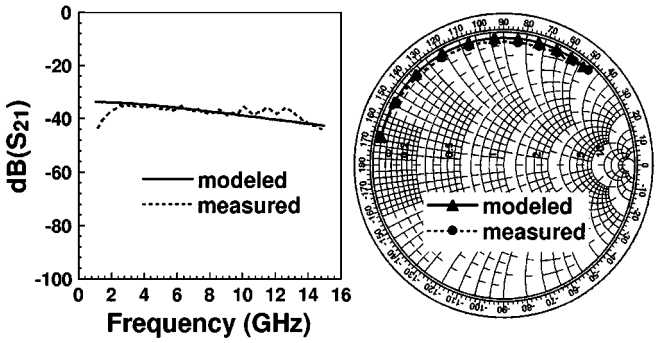



Fig. 7. Extracted and selected quantities of the bond-wire resistances.




(a) (b)

Fig. 8. Comparison between modeled and measured results of: (a) $S_{21}$ in decibels and (b) $S_{11}$ on the Smith chart for the configuration of Fig. 5.

from a series $LR$ model at 1 GHz while the parallel resistances $R_{p1}, R_{p2}$ are selected by the quantities extracted from a parallel $LR$ model at 15 GHz. A shunt resistance between two bond wires is also used to represent the mutual resistance. Before extracting these bond-wire parasitic elements, the measured $S$-parameters ($[S]^{\rm sp}$) are first expressed in the admittance matrix. After subtracting the admittance matrix ($[Y]^{\rm op}$) representing the mounted-pad capacitve effects, we convert the admittance matrix into impedance matrix ($[Z]^{\rm sp}$) whose parameters can determine the bond-wire parasitic elements by following the formulation given as

$$[Z]^{\rm sp} = \Big(Z_0^{-1}\big([U]+[S]^{\rm sp}\big)^{-1}\big([U]-[S]^{\rm sp}\big) - [Y]^{\rm op}\Big)^{-1} \tag{5}$$

$$L_{s1} = \text{median}\left(\text{Im}\left(Z_{11}^{\rm sp}\right)/\omega\right) \tag{6}$$

$$L_{s2} = \text{median}\left(\text{Im}\left(Z_{22}^{\rm sp}\right)/\omega\right) \tag{7}$$

$$L_{m} = \text{median}\left(\text{Im}\left(Z_{12}^{\rm sp}\right)/\omega\right) \tag{8}$$

$$R_{s1} = \text{Re}\big(Z_{11}^{\rm sp} - Z_{12}^{\rm sp}\big) \quad f = 1\,\text{GHz} \tag{9}$$

$$R_{s2} = \text{Re}\big(Z_{22}^{\rm sp} - Z_{12}^{\rm sp}\big) \quad f = 1\,\text{GHz} \tag{10}$$

$$R_{p1} = \Big(\text{Re}\big(Z_{11}^{\rm sp} - Z_{12}^{\rm sp}\big)^{-1}\Big)^{-1} \quad f = 15\,\text{GHz} \tag{11}$$

$$R_{p2} = \Big(\text{Re}\big(Z_{22}^{\rm sp} - Z_{12}^{\rm sp}\big)^{-1}\Big)^{-1} \quad f = 15\,\text{GHz} \tag{12}$$

$$R_{m} = \text{median}\Big(\text{Re}\big(Z_{12}^{\rm sp}\big)\Big). \tag{13}$$

Their extracted and selected quantities are shown in Figs. 6 and 7. Again, the modeled $S$-parameters using the selected element quantities agree quite well with the measured results, as shown in Fig. 8.

In Fig. 9, a chip with a number of bond pads on the periphery was used to characterize the bond-pad parasitic effects. The pair of bond pads to be characterized is wire bonded to package's mounted pads under test. The other chip's bond pads are treated as ground pads to all be connected by the on-chip $U$-shaped metallization patterns and then down bonded to the die pad.

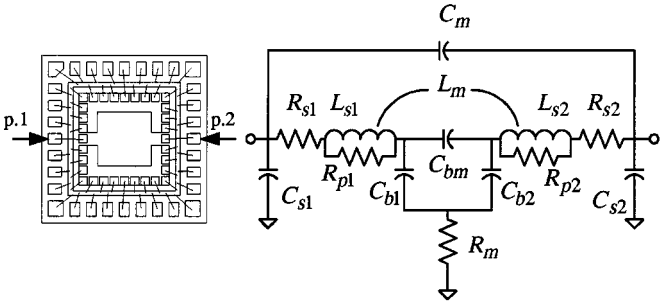



Fig. 9. Wire-bonding diagram and equivalent model of the 32-pin BCC$^{++}$ package sample under test that houses a chip with a specified layout for evaluating the bond-pad capacitances.

The chip was implemented on a 10.8-mil-thick GaAs substrate. Each bond pad has a dimension of 8 mil × 8 mil × 0.2 mil. The spacing between the two bond pads is 2 mil. Their parasitic elements include shunt and mutual capacitances that can be extracted from the measured $S$-parameters ($[S]^{\rm bp}$) for the configuration of Fig. 9 using the following expressions:

$$[Y]^{\rm ob} = \Big(\big(Z_0^{-1}([U]+[S]^{\rm bp})^{-1}([U]-[S]^{\rm bp}) - [Y]^{\rm op}\big)^{-1} - [Z]^{\rm sp}\Big)^{-1} \tag{14}$$

$$C'_{b1} = \text{Im}\left(Y_{11}^{\rm ob} + Y_{12}^{\rm ob}\right)/\omega \tag{15}$$

$$C'_{b2} = \text{Im}\left(Y_{22}^{\rm ob} + Y_{12}^{\rm ob}\right)/\omega \tag{16}$$

$$C_{bm} = \text{median}\left(-\text{Im}\left(Y_{12}^{\rm ob}\right)\Big/\omega\right). \tag{17}$$

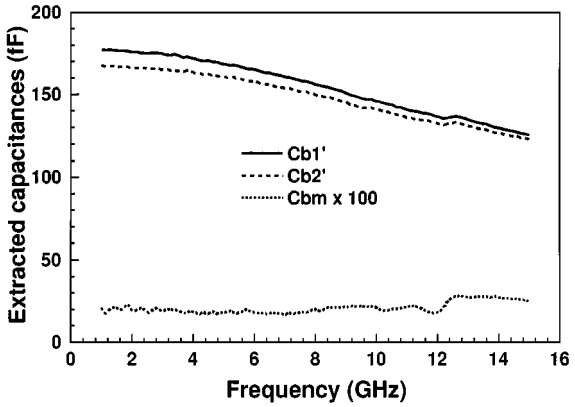



Fig. 10. Extracted quantities of the bond-pad capacitances including the bond wire's distributed capacitances.

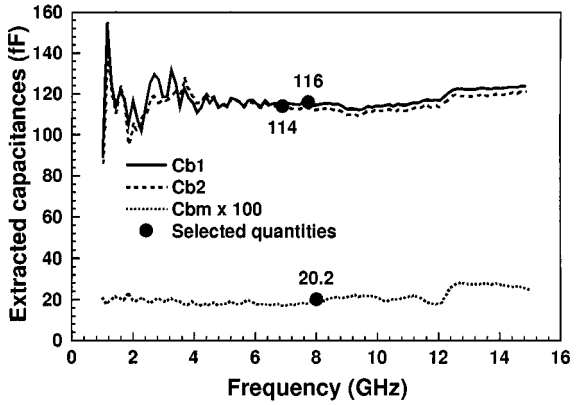



Fig. 11. Extracted and selected quantities of the bond-pad capacitances excluding the bond wire's distributed capacitances.

The extracted results are presented in Fig. 10. It can be seen that the shunt capacitances (denoted by $C'_{b1}$ and $C'_{b2}$) decrease as frequency increases, which fails to satisfy our expectation to have a weak dependence on frequency. This is because the equivalent circuit shown in Fig. 9 does not include the bond wire's distributed capacitances. When a segment of bond wire is treated as a lossless uniform transmission line, its connection to a bond pad with an equivalent shunt capacitance $C_b$ has an input impedance expressed as

$$Z_i = Z_{0w}\frac{(j\omega C_b)^{-1} + jZ_{0w}\tan\beta_w l_w}{Z_{0w} + j(j\omega C_b)^{-1}\tan\beta_w l_w} \tag{18}$$

where $Z_{0w}, \beta_w$, and $l_w$ represent the bond wire's characteristic impedance, phase constant, and length, respectively. When the bond wire's electrical length is small, the following approximations, i.e., (1) $\tan\beta_w l_w \approx \beta_w l_w$, (2) $Z_{0w} \approx \sqrt{L_s/C_w}$, and (3) $\beta_w \approx \omega\sqrt{L_s C_w}/l_w$, can be applied to simplify (18) in the form

$$Z_i = \frac{1-\omega^2 C_b L_s}{j\omega(C_b + C_w)} \tag{19}$$

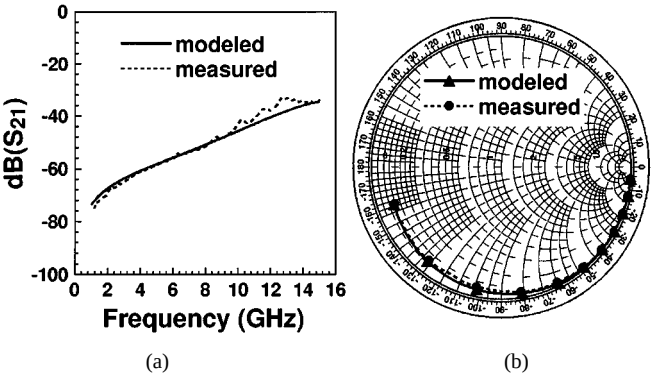
where $L_s$ and $C_w$ denote the bond-wire inductance and capacitance, respectively. From the equivalent-circuit point-of-view, $Z_i \approx j\omega L_s + (j\omega C'_b)^{-1}$. Thus, equating this relation to (19), one can find

$$C'_b = \frac{C_b + C_w}{1+\omega^2 L_s C_w}. \tag{20}$$

When the second term in the denominator of (20) is ignored at low frequencies, $C'_b$ is equivalent to an amount of $C_b$ and $C_w$. As frequency increases, $C'_b$ decreases according to (20), which can account for the frequency dependence of the results shown in Fig. 10. The relation between $C'_b$ and its low-frequency quantity ($C''_b$) can be used to eliminate $C_w$ in (20) such that the pure bond-pad capacitances can be found as

$$C_{b1} = \text{median}\left(\frac{L_{s1}C'_{b1}C''_{b1}\left(\omega^2-\omega_1^2\right)+\left(C'_{b1}-C''_{b1}\right)}{L_{s1}\left(\omega^2 C'_{b1}-\omega_1^2 C''_{b1}\right)}\right) \tag{21}$$

$$C_{b2} = \text{median}\left(\frac{L_{s2}C'_{b2}C''_{b2}\left(\omega^2-\omega_1^2\right)+\left(C'_{b2}-C''_{b2}\right)}{L_{s2}\left(\omega^2 C'_{b2}-\omega_1^2 C''_{b2}\right)}\right) \tag{22}$$




(a) (b)

Fig. 12. Comparison between modeled and measured results of: (a) $S_{21}$ in decibels and (b) $S_{11}$ on the Smith chart for the configuration of Fig. 9.

where $C''_{b1} = C'_{b1}(\omega_1)$ and $C''_{b2} = C'_{b2}(\omega_1), \omega_1 = 2\pi \times 1$ GHz. Note that (21) and (22) are regarded as the modified expressions of (15) and (16), respectively, by removing the influence of the bond wire's distributed capacitances, and can yield the results with a certain degree of frequency independence, as shown in Fig. 11. When the selected quantities of $C_{b1}, C_{b2}$, and $C_{bm}$, shown in Fig. 11, are used to regenerate the $S$-parameters, the frequency-dependent capacitances $C'_{b1}$ and $C'_{b2}$ calculated from (20) with $C_w \approx C''_{b1} - C_{b1} \approx C''_{b2} - C_{b2}$ have been used instead of $C_{b1}$ and $C_{b2}$ in the circuit simulation. This can result in better agreement with measurements, as shown in Fig. 12. In real applications, the bond pads in the I/O paths will not be left open ended, but connected to a device with low impedance, say, 50 Ω. Under this situation, the influence due to the bond wire's distributed capacitances becomes much slighter and can just be ignored.

## III. Evaluation of Package Effects

To evaluate the complete package effects on RFICs, one can import $S$-parameters for the core RFIC circuitry as a black box when cascaded with the package parasitic elements. For demonstration, a 50-Ω microstrip line was implemented on a 10.8 mil thick GaAs substrate and then housed in a 32-pin BCC$^{++}$ package with the specified wire-bonding diagram shown in Fig. 13. The $S$-parameters ($[S]^{\text{lp}}$) for the packaged microstrip line can be calculated based on the equivalent circuit in Fig. 13 by following the procedure in (23)–(26), shown at

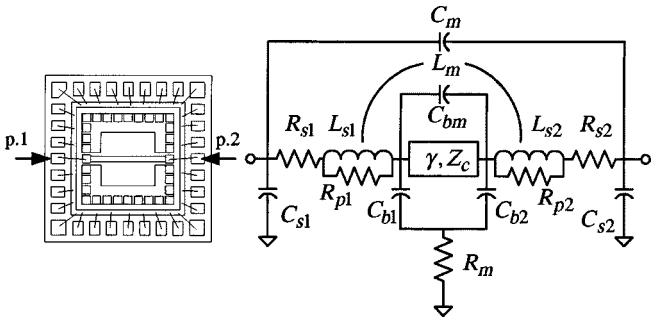



Fig. 13. Wire-bonding diagram and equivalent model of the 32-pin BCC$^{++}$ package sample under test that houses an on-chip 50-$\Omega$ microstrip line for evaluating the resultant low-pass filter effects.

the bottom of this page, where $\ell = 88$ mil is the microstrip length. The parameters $\gamma$ and $Z_c$ represent microstrip's complex-valued propagation constant and characteristic impedance, respectively, which can be generally expressed in terms of the distributed parameters

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{27}$$

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{28}$$

where

$$L \approx \sqrt{\varepsilon_{\text{eff}}}(Z_0/c) \tag{29}$$

$$C \approx \sqrt{\varepsilon_{\text{eff}}}/(Z_0 c) \tag{30}$$

$$R \approx 2R_s/w \tag{31}$$

$$G \approx \omega \tan\delta \sqrt{\varepsilon_{\text{eff}}}/(Z_0 c). \tag{32}$$

In (29)–(32), $c$ and $\varepsilon_{\text{eff}}$ denote the speed of light in free space and the microstrip effective dielectric constant, respectively, and $R_s = \sqrt{\omega\mu_0/2\sigma_c}$ is the surface resistivity of gold with $\sigma_c = 4.11 \times 10^7$ S/m. The on-chip microstrip line can be considered embedded in an inhomogeneous structure with a GaAs substrate $(\varepsilon_r = 12.9)$ and a molding-resin superstrate $(\varepsilon_r = 3.9)$. To realize a $Z_0 = 50\ \Omega$ line, the simulated microstrip width $(w)$ and effective dielectric constant $(\varepsilon_{\text{eff}})$ using spectral-domain approaches applied to the multilayered microstrip structure [10], [11] are equal to 5.5 and 9.28 mil, respectively. The filling factor, representing the percentage of the electromagnetic fields distributed in the substrate region, is estimated close to 0.6. The loss tangent in (32) can be approximated as a weighted average

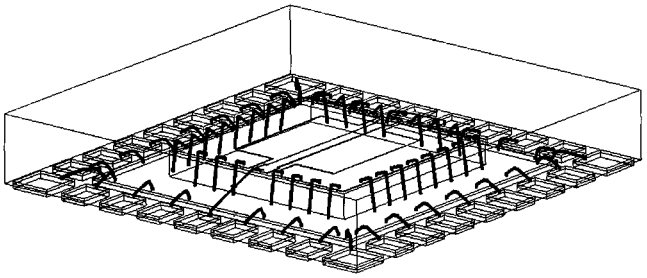


Fig. 14. Simulation configuration in Ansoft's HFSS for an on-chip 50-$\Omega$ microstrip line housed in a 32-pin BCC$^{++}$ package.

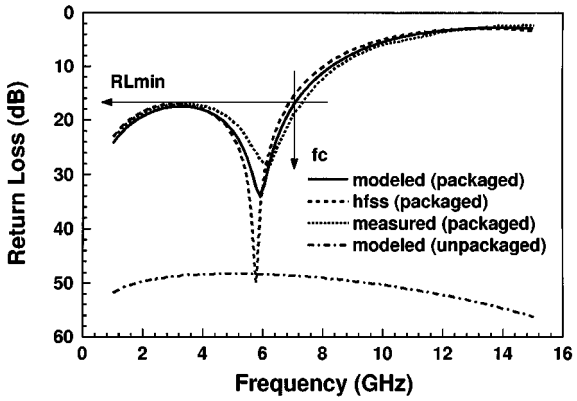



Fig. 15. Comparison between simulated and measured return losses for an on-chip 50-$\Omega$ microstrip line housed in a 32-pin BCC$^{++}$ package.

of the values for the GaAs substrate $(\tan\delta = 6 \times 10^{-4})$ and molding-resin superstrate $(\tan\delta = 0.018)$ with the filling factor and, thus, evaluated as $6 \times 10^{-4} \times 0.6 + 0.018 \times (1 - 0.6) = 7.56 \times 10^{-3}$.

As a result, the insertion and return losses for the packaged microstrip line have been calculated from (26) and compared to Ansoft's HFSS simulation results based on the constructed 3-D configuration in Fig. 14. When all the simulated and measured data are collected and plotted in Figs. 15 and 16 for the return and insertion losses, respectively, excellent agreement has been observed up to 15 GHz for the results corresponding to the packaged microstrip line. Comparing the calculated insertion loss for the on-chip microstrip line, one can see that the package adds a slight loss to the line below 7 GHz, but causes a sharp cutoff above that frequency. Such a low-pass filter effect results from the impedance mismatch due to the package

$$[Y]^{\text{lb}} = \begin{bmatrix} Z_c^{-1}\coth\gamma\ell + j\omega(C_{b1} + C_{bm}) & -Z_c^{-1}\operatorname{csch}\gamma\ell - j\omega C_{bm} \\ -Z_c^{-1}\operatorname{csch}\gamma\ell - j\omega C_{bm} & Z_c^{-1}\coth\gamma\ell + j\omega(C_{b2} + C_{bm}) \end{bmatrix} \tag{23}$$

$$[Z]^{\text{lw}} = \left([Y]^{\text{lb}}\right)^{-1} + \begin{bmatrix} R_{s1} + R_m + \frac{j\omega L_{s1} R_{p1}}{R_{p1} + j\omega L_{s1}} & R_m + j\omega L_m \\ R_m + j\omega L_m & R_{s2} + R_m + \frac{j\omega L_{s2} R_{p2}}{R_{p2} + j\omega L_{s2}} \end{bmatrix} \tag{24}$$

$$[Y]^{\text{lp}} = \left([Z]^{\text{lw}}\right)^{-1} + \begin{bmatrix} j\omega(C_{s1} + C_m) & -j\omega C_m \\ -j\omega C_m & j\omega(C_{s2} + C_m) \end{bmatrix} \tag{25}$$

$$[S]^{\text{lp}} = \left(Z_0^{-1}[U] + [Y]^{\text{lp}}\right)^{-1}\left(Z_0^{-1}[U] - [Y]^{\text{lp}}\right) \tag{26}$$

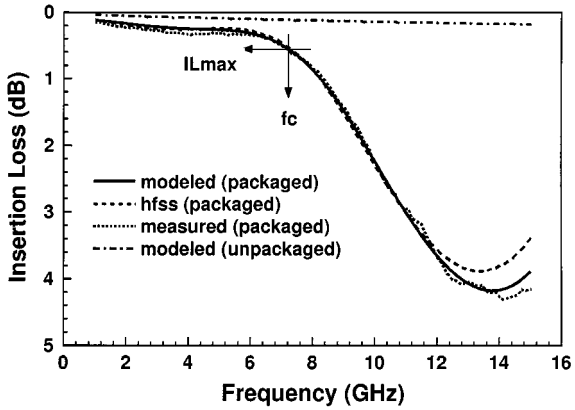



Fig. 16. Comparison between simulated and measured insertion losses for an on-chip 50-Ω microstrip line housed in a 32-pin BCC$^{++}$ package.

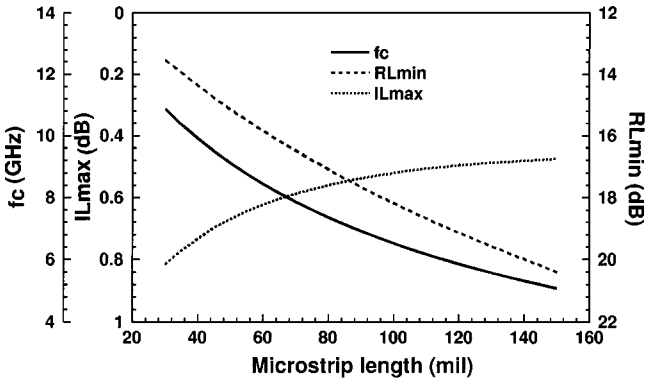



Fig. 17. Simulated low-pass filter parameters versus the microstrip length for an on-chip 50-Ω microstrip line housed in a 32-pin BCC$^{++}$ package.

parasitic elements. As illustrated in Figs. 15 and 16, three parameters $f_c, \mathrm{RL}_{\min}$, and $\mathrm{IL}_{\max}$ that represent the cutoff frequency, minimum return loss, and maximum insertion loss in the passband, respectively, have been used to describe such a low-pass filter response. In the passband, the minimum return loss $\mathrm{RL}_{\max} = 17$ dB, which occurs at the cutoff frequency $f_c = 7$ GHz and also at 3.5 GHz. The maximum insertion loss $\mathrm{IL}_{\max} = 0.6$ dB at the cutoff frequency. From the simulation, we can vary the microstrip length to change the low-pass filter characteristics. As shown in Fig. 17, a longer microstrip line housed in the package has smaller insertion loss and larger return loss in the passband than a shorter line. However, these improvements in the passband are at the cost of lower cutoff frequencies.

Unlike the microstrip line treated as a two-terminal device when cascaded with the package parasitic elements, a microwave transistor in the common emitter (source) configuration for amplifier applications should be regarded as a three-terminal device with the additional terminal connected to the chip's common ground. In RFICs, the common ground is usually implemented by designing a metallization pattern connecting all ground pads on the chip together. When the chip is housed in a BCC$^{++}$ package, down bonding is performed to connect the ground pads directly on the chip to the die pad. A measurement set up is illustrated in Fig. 18 for extracting the common-ground parasitic elements in an equivalent parallel

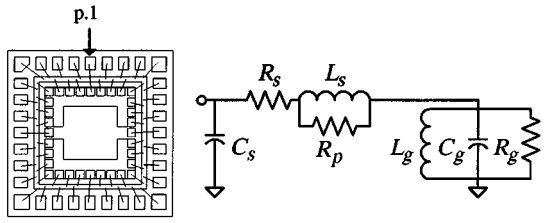



Fig. 18. Wire-bonding diagram and equivalent model of the 32-pin BCC$^{++}$ package sample under test that houses a chip with specified layout for evaluating the common-ground parasitic elements.

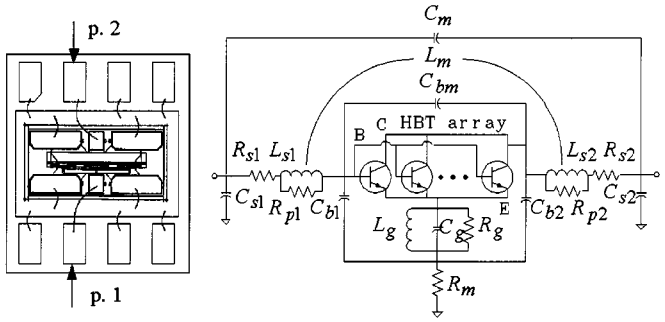



Fig. 19. Wire-bonding diagram and equivalent model of the 8-pin BCC$^{++}$ package sample under test that houses an HBT array for evaluating the resultant low-pass filter effects. The package parasitic elements have been extracted with the following selected quantities: $C_{s1} \approx C_{s2} \approx 22$ fF, $C_m \approx 0.8$ fF, $L_{s1} \approx L_{s2} \approx 1.6$ nH, $L_m \approx 29$ pH, $R_{s1} \approx R_{s2} \approx 0.9\ \Omega$, $R_{p1} \approx R_{p2} \approx 3.6$ kΩ, $R_m \approx 0.5\ \Omega$, $C_{b1} \approx C_{b2} \approx 37$ fF, $L_g \approx 0.39$ nH, $C_g \approx 162$ fF, $R_g \approx 322\ \Omega$.

$RLC$ resonant circuit. The formulation to determine the circuit elements from the measured reflection coefficient $(S_{11}^g)$ is given as

$$Z_g = Y_g^{-1} = Z_0 \left( \frac{1 - S_{11}^g}{1 + S_{11}^g} - j\omega C_s Z_0 \right)^{-1} - R_s - \frac{j\omega L_s R_p}{R_p + j\omega L_s} \tag{33}$$

$$R_g = \mathrm{median}\big(1/\mathrm{Re}(Y_g)\big) \tag{34}$$

$$L_g = \mathrm{median}\left( \left( \frac{\omega}{\omega_r^2} - \frac{1}{\omega} \right) \Big/ \mathrm{Im}(Y_g) \right) \tag{35}$$

$$C_g = \left(\omega_r^2 L_g\right)^{-1} \tag{36}$$

where $\omega_r$ denotes the radial resonant frequency estimated according to $\mathrm{Im}(Y_g(\omega_r)) = 0$.

To study the package effects on the nonreciprocal active components, an n-p-n AlGaAs/GaAs heterojunction-bipolar-transistor (HBT) array has been housed in an 8-pin BCC$^{++}$ package, as shown in Fig. 19. It comprises several unit cells of HBTs in an array form, which is commonly used for power amplification. Each unit cell of HBT has an emitter size of 60 $\mu$m$^2$. The bias conditions are set at $V_{ce} = 3$ V and $J_c = 5$ kA/cm$^2$. By following the same extraction procedure, we have found almost all the equivalent-circuit elements for the 8-pin BCC$^{++}$ package shown in Fig. 19. The only exception is the feedback capacitance $C_{bm}$, whose quantity can be extracted more accurately from the $S$-parameters measured when the HBT array is reverse biased [12]. Such a feedback capacitance resulting primarily from mutual coupling between the interconnections in the base and collector of the HBT array increases

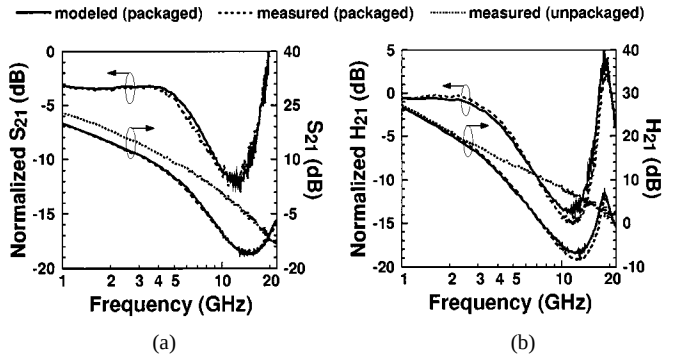



Fig. 20. Comparison between modeled and measured magnitude of: (a) $S_{21}$ and normalized $S_{21}$ and (b) $H_{21}$ and normalized $H_{21}$ in decibels for an HBT array with a total emitter area of $6 \times 60$ $\mu$m$^2$ housed in an 8-pin BCC$^{++}$ package. $C_{bm} = 64$ fF for this case.

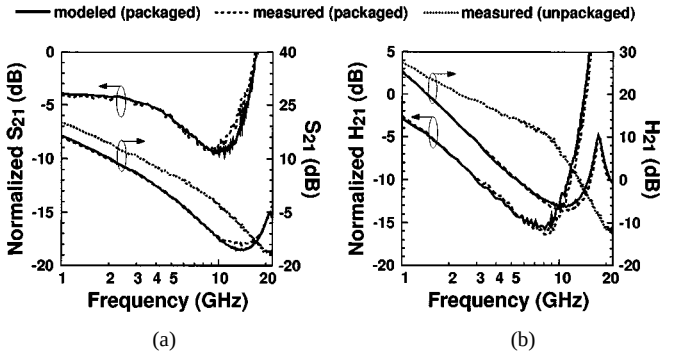



Fig. 21. Comparison between modeled and measured magnitude of: (a) $S_{21}$ and normalized $S_{21}$ and (b) $H_{21}$ and normalized $H_{21}$ in decibels for an HBT array with a total emitter area of $18 \times 60$ $\mu$m$^2$ housed in an 8-pin BCC$^{++}$ package. $C_{bm} = 172$ fF for this case.

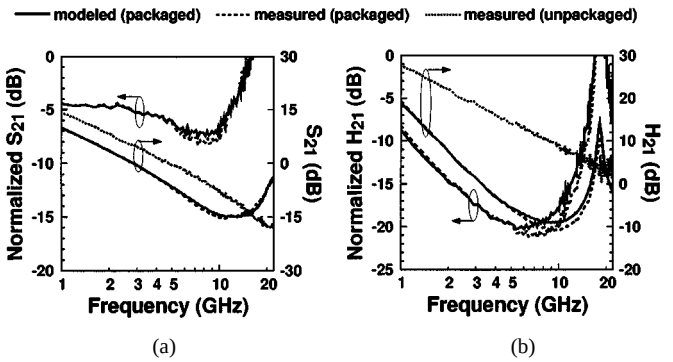



Fig. 22. Comparison between modeled and measured magnitude of: (a) $S_{21}$ and normalized $S_{21}$ and (b) $H_{21}$ and normalized $H_{21}$ in decibels for an HBT array with a total emitter area of $18 \times 60$ $\mu$m$^2$ housed in an 8-pin BCC$^{++}$ package. $C_{bm} = 586$ fF for this case.

dramatically after packaging. Figs. 20–22 show the variations of gain in two representations, $S_{21}$ and $H_{21}$, from 1 to 22 GHz for the HBT array with a total emitter area of $6 \times 60$ $\mu$m$^2$, $18 \times 60$ $\mu$m$^2$, and $48 \times 60$ $\mu$m$^2$, respectively. The feedback capacitance evaluated corresponds to 64, 172, and 586 fF, respectively. One can see the low-pass filter characteristics clearly when the packaged HBT gains are normalized by the unpackaged HBT gains. In the passband, two factors have been found to dominate the gain reduction. One is due to the ground inductance $(L_g)$, the so-called emitter degeneration effect. The other is due to the feedback capacitance $(C_{bm})$ based on the well-known Miller effect. The losses due to bond wires become a minor part in comparison with the above effects. The cutoff frequency is determined primarily by the bond-wire inductances $(L_{s1}, L_{s2})$ and the shunt capacitances $(C_{s1}, C_{s2}, C_{b1}, C_{b2})$ associated with the mounted and bond pads. Above the cutoff frequency, the gain drops at a certain rate until a turnaround appears. This can be explained by the common-ground coupling due to the ground parasitic elements $(L_g, C_g, R_g)$. The maximum coupling in the stopband occurs at ground's resonant frequency, which is about 20 GHz. From Figs. 20–22, one can compare to see that the low-pass filter effects on a packaged HBT array with a larger emitter area have a trend of lower cutoff frequency, more gain reduction in the passband, and lower attenuation rate in the stopband. The modeled results have predicted all the phenomena successfully from the good agreement with measurements.

## IV. Conclusion

A complete methodology for modeling and evaluating lead-frame plastic CSPs in housing RFICs has been presented in this paper. Two examples, an on-chip 50-$\Omega$ microstrip line and an HBT array housed in a 32- and 8-pin BCC$^{++}$ package, respectively, have been examined. It was concluded that the packages caused a low-pass filter effect on both components. The associated passband and stopband characteristics can be predicted accurately from the established package models.

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