Modeling of Multi-Layered Power Distribution Planes Including Via Effects Using Transmission Matrix Method

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Abstract

This paper presents a method for analyzing multi-layered power distribution networks in the frequency domain. Using a two dimensional array of distributed RLCG circuits, multi-layered power distribution planes are represented. Each plane pair is connected by vias, which are modeled as partial self and mutual inductors. For the efficient computation of the power distribution impedances at specific points in the network, a multi-input and multi-output transmission matrix method has been used, which is much faster than Spice and reduces memory requirements. This method has been compared with the cavity resonator method simulated in Spice.

1. Introduction

A major problem in power distribution networks is simultaneous switching noise (SSN) induced by power and ground inductance. As a result, an important area in high-speed digital systems is the design of the power and ground planes arising in power distribution networks. A major challenge in the design of planes, which forms an integral part of the power delivery system (PDS) for gigahertz (GHz) packages and board, is the supply of clean power to the switching circuits. As clock speeds increase, and signal rise time and supply voltages decrease, the transient current injected into the power distribution planes builds up energy due to the resonant cavity; as a result, it can cause voltage fluctuations and circuit delays [1]. This leads to unwanted effects on the PDS such as ground bounce, power supply compression, and electromagnetic interference. Hence, it is required that the PDS should have a low impedance and less resonant frequencies over the entire bandwidth of the signal so that the transient current does not cause excessive noise on the power distribution network. For the design of the reliable PDS to suppress the SSN, efficient noise prediction methods are necessary.

In a realistic package/board, since the PDS consists of numerous vias, decoupling capacitors, signal lines, irregular geometries, and multiple plane layers, the number of transmission line segments required may become very large. As a result, large memory requirements and a considerable CPU run time are required for analysis. The transmission matrix method discussed in this paper offers a more efficient technique for solving these kinds of problems. In [2], [3], for the analysis of an arbitrary shaped power/ground plane pair, the transmission matrix showed the following efficiency: small memory requirements, large savings in computer run time, and flexibility and versatility in applications. It is because the transmission matrix method is based on a multi-input, multi-output transfer function which enables the matrix for the entire power distribution network ($N \times M$ unit cells) to be computed as the product of the individual square matrices formed by 2N-port networks having N input ports and N output ports [2]. Once the unit cell parameters are computed, the transmission matrix method can be efficiently applied to any arbitrary shaped plane geometry.

In this paper, the transmission matrix has been extended to a third dimension, which is made up of two-dimensional plane pairs connected by vertical vias. From the via inductance extraction program FastHenry, which was developed at MIT, partial self and mutual inductances between vias have been extracted and added to the transmission matrix method. This paper discusses the use of the transmission matrix method with Π model unit cells shown in [3] for computing impedances between 2 or more ports; however, each individual square matrix is based on a pair of power/ground planes while it was based on a column of unit cells in [2], [3]. Where applicable, the results have been compared with Spice, in which the cavity resonator model was used for simulation [4]. Multi-layered power/ground planes have also been

modeled without vias (as short circuits), with vias as partial self inductances, and with vias coupled to each other.

2. Modeling of plane layers using unit cells

Figure 1 shows the structure of multi-layered power distribution planes, which are commonly used in computer applications. Each two-dimensional plane pair is connected through vertical vias.

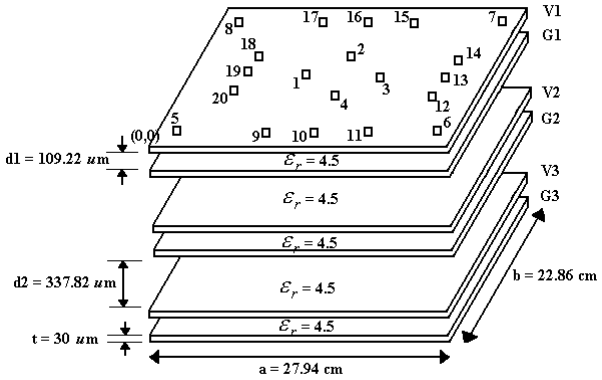


Figure 1. Multi-layered power/ground plane structure

From quasi-static approximations where the dielectric separation (d) is much less than the metal dimensions (a, b) and the wavelength (λ) [5], which is true for power/ground plane pairs, each power/ground plane can be divided into unit cells with a lumped element model for each cell, as described in [6]. Each cell consists of an equivalent circuit with R, L, C, and G components, as shown in Figure 2.

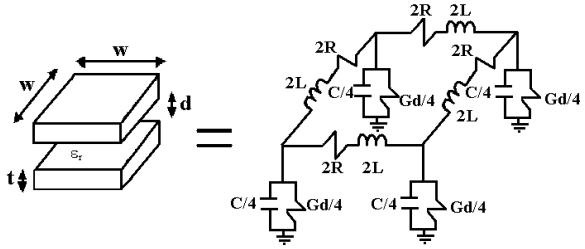


Figure 2. Unit cell and equivalent circuit

Using the equations for a parallel plate [5], from the lateral dimension of a unit cell (w), separation between planes (d), dielectric constant (ε), loss tangent of dielectric ($\tan(\delta)$), metal thickness (t), and metal conductivity (σ_c), the equivalent circuit parameters of a unit cell can be computed as:

$$C = \varepsilon_o \varepsilon_r \frac{w^2}{d} \qquad L = \mu_o d \qquad R_{dc} = \frac{2}{\sigma_c t}$$
$$R_{ac} = 2\sqrt{\frac{\pi f \mu_o}{\sigma_c}}(1+j) \qquad G_d = \omega C \tan(\delta) \tag{1}$$

In the above equation, ε_o is the permittivity of free space, μ_o is the permeability of free space, and ε_r is the relative permittivity of the dielectric. The parameter R_{dc} is the resistance of both the power and ground planes for a steady D.C. current where the planes are assumed to be of uniform cross section. The ac resistance R_{ac} accounts for the skin effect on both conductors. The shunt conductance G_d represents the dielectric loss in the material between the planes.

Using the unit cell, a distributed network of RLCG elements can be generated for the multi-layered planes, as shown in Figure 1. Since this is a circuit model, it can be simulated in Spice by generating the Modified Nodal Analysis (MNA) equations or using the transmission matrix method. To obtain good accuracy, a unit cell size that is 10 times less than the wavelength at the highest frequency of interest was used.

3. Transmission matrix method

3.1. Power/ground planes

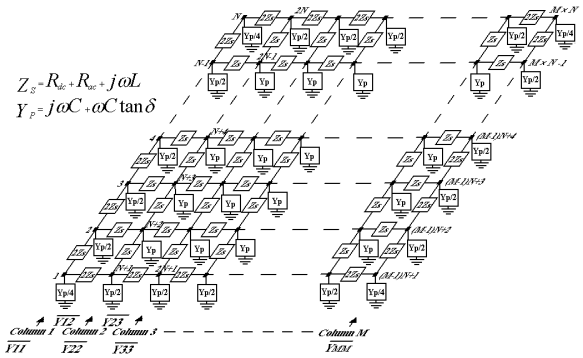


Figure 3. Equivalent circuit for a pair of power/ground planes

As shown in Figure 1, using a distributed network of RLCG elements, each rectangular plane pair can be divided into $(M-1)\times(N-1)$ unit cells. The $(M-1)\times(N-1)$ unit cells can be represented as a $2(M\times N)\times 2(M\times N)$ matrix formed by $(M\times N)$ input ports and $(M\times N)$ output ports. This is shown in Figure 3 for the Π equivalent circuits for the unit cells, which are cascaded to represent a pair of power/ground planes shown in Figure 2.

From Figure 3, the input ports are indexed as 1 to $(M\times N)$, and the output ports are indexed as $(M\times N)+1$ to $2(M\times N)$. The transmission matrix for the $2(M\times N)$-port network can be derived in terms of the node voltages and port currents. Using the 2×2 block matrix representation, the transmission matrix can be represented to relate the voltages and currents as:

$$\overline{V_{in}} = [A_p]\overline{V_{out}} + [B_p]\overline{I_{out}}$$
$$\overline{I_{in}} = [C_p]\overline{V_{out}} + [D_p]\overline{I_{out}} \quad (2)$$

where $\overline{V_{in}} = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_{M\times N} \end{bmatrix}$ $\overline{I_{in}} = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_{M\times N} \end{bmatrix}$ $\overline{V_{out}} = \begin{bmatrix} V_{M\times N+1} \\ V_{M\times N+2} \\ \vdots \\ V_{2(M\times N)} \end{bmatrix}$ $\overline{I_{out}} = \begin{bmatrix} I_{M\times N+1} \\ I_{M\times N+2} \\ \vdots \\ I_{2(M\times N)} \end{bmatrix}$

The above transmission matrix of a power/ground plane pair can be rewritten in the simpler form:

$$T_p = \begin{bmatrix} A_p & B_p \\ C_p & D_p \end{bmatrix} = \begin{bmatrix} I & 0 \\ C_p & I \end{bmatrix} \quad (3)$$

where $[I]$ (identity matrix), $[0]$ (zero matrix), and $[C_p]$ are $(M\times N)\times(M\times N)$ matrices. In Eq. (3), the matrix $[C_p]$ is of the form:

$$[C_p] = \begin{bmatrix} \overline{Y}_{11} & -\overline{Y}_{12} & 0 & 0 & \cdots \\ -\overline{Y}_{12} & \overline{Y}_{22} & -\overline{Y}_{23} & 0 & \cdots \\ 0 & -\overline{Y}_{23} & \overline{Y}_{33} & -\overline{Y}_{34} & \cdots \\ \vdots & \vdots & \vdots & \vdots & \cdots \\ 0 & 0 & 0 & 0 & \cdots \overline{Y}_{MM} \end{bmatrix} \quad (3A)$$

where $N\times N$ matrix, $\overline{Y}_{11} = \overline{Y}_{MM} = 0.5\overline{Y}_{22} = 0.5\overline{Y}_{33} = \cdots\cdots = 0.5\overline{Y}_{(M-1)(M-1)} =$

$$\begin{bmatrix} \frac{Y_p}{4}+\frac{1}{Z_s} & -\frac{1}{2Z_s} & 0 & \cdots & 0 & 0 \\ -\frac{1}{2Z_s} & \frac{Y_p}{2}+\frac{2}{Z_s} & -\frac{1}{2Z_s} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & \ddots & \frac{Y_p}{2}+\frac{2}{Z_s} & -\frac{1}{2Z_s} \\ 0 & 0 & \cdots & & -\frac{1}{2Z_s} & \frac{Y_p}{4}+\frac{1}{Z_s} \end{bmatrix}$$

$\overline{Y}_{12} = \overline{Y}_{23} = \cdots\cdots = \overline{Y}_{(M-1)M} =$

$$\begin{bmatrix} \frac{1}{2Z_s} & & & & 0 \\ & \frac{1}{Z_s} & & & \\ & & \ddots & & \\ & & & \frac{1}{Z_s} & \\ 0 & & & & \frac{1}{2Z_s} \end{bmatrix}$$

As can be seen in Eq. (3A), the transmission matrix for a power/ground plane pair is sparse, which enables reduction in memory and CPU time when applied to realistic structures.

3.2. Vias and via coupling

Multi-layered power distribution planes can be represented as a cascade of a power/ground plane pair connected by vias. In a realistic structure, there are thousands of via connections to reduce the via inductances and for thermal dissipation. These effects are not totally negligible in the high frequency range as clock speeds increase. Figure 4 shows the side view of three conductor planes, which can be separated into two pairs of power/ground planes with vias.

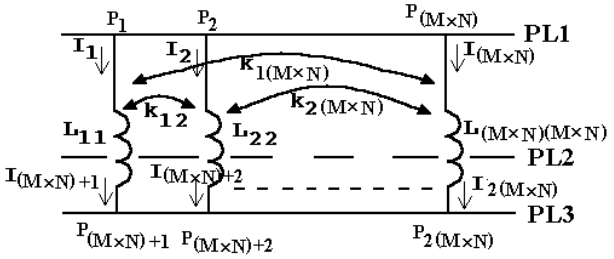


Figure 4. Side view of power/ground planes with vias

It is assumed that there are $(M\times N)$ vias, which can be decomposed into partial self and mutual inductances as shown in Figure 4.

In terms of PL1 and PL3 conductor planes, the node voltage and port current between point P_1 and $P_{(M\times N)+1}$, shown in Figure 4, can be represented as follows:

$$V_{p_1 p_{(M\times N)+1}} = jwL_{11}I_1 + jwM_{12}I_2 + \cdots + jwM_{1(M\times N)}I_{(M\times N)}$$
$$I_1 = I_{(M\times N)+1} \quad (4)$$

where mutual inductance $M_{ij} = k_{ij}\sqrt{L_{ii}L_{jj}}$. Other node voltages and port currents follow Eq. (4). In Eq. (4), the inductances of the vias represent partial inductances.

From Eq. (4), in the transmission matrix method, partial self and mutual inductances, which can be extracted from FastHenry, can easily be included into the matrices. Actually, FastHenry gives losses and inductances; and polarity (dot convention). These real (loss) and imaginary (inductance) values are frequency-dependant. To apply static values with a good approximation, two frequency data points are sampled; namely, low-frequency data and high-frequency data. Since inductance values are dominant in the high frequency range, the high frequency inductances are used in the entire frequency band. However, the loss (real) parts can be approximated as $(R_{dc} + R_{ac}\sqrt{f})$. From the two real parts of data, the two unknown values can be found and represented using the following equation.

$$R_{dc} = \frac{D_1\sqrt{f_2} - D_2\sqrt{f_1}}{\sqrt{f_2} - \sqrt{f_1}}$$
$$R_{ac} = \frac{D_2 - D_1}{\sqrt{f_2} - \sqrt{f_1}} \quad (5)$$

where D_1 is the data at the frequency f_1 and D_2 at the frequency f_2. From these values, the transmission matrix for vias in terms of input ports on PL1 and PL2; and output ports on PL3 and PL2 planes can be represented as follows:

$$[T_{via}] = \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix} \quad (6)$$

where $[B_{via}]=\begin{bmatrix} Z_{via,11} & Z_{via,12} & Z_{via,13} & \cdots & Z_{via,1(M\times N)} \\ Z_{via,12} & Z_{via,22} & Z_{via,23} & \cdots & Z_{via,2(M\times N)} \\ Z_{via,13} & Z_{via,23} & Z_{via,33} & \cdots & Z_{via,3(M\times N)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ Z_{via,1(M\times N)} & Z_{via,2(M\times N)} & Z_{via,3(M\times N)} & \cdots & Z_{via,(M\times N)(M\times N)} \end{bmatrix}$

In Eq. (6), $Z_{via,ij} = R_{dc,ij} + R_{ac,ij}\sqrt{f} + j\omega L_{ij}$. As seen in Eq. 6, the transmission matrix loses the sparsity as the number of vias increases. The negligible coupling coefficients (k_{ij}) can be eliminated in the matrix to enable sparsity using the transmission matrix method.

3.3. Decoupling capacitors

In the transmission matrix method, decoupling capacitors can readily be included into the matrices. The impedance of a decoupling capacitor is represented using the following equation.

$$Z_{cap} = R + j\omega L + \frac{1}{j\omega C} \tag{7}$$

where 'R' is the Equivalent Series Resistance (ESR), 'L' is the Equivalent Series Inductance (ESL), and 'C' is the capacitance. The transmission matrix for decoupling capacitors can be represented as follows:

$$[T_{cap}]=\begin{bmatrix} I & 0 \\ C_{cap} & I \end{bmatrix} \quad \text{where} [C_{cap}]=\begin{bmatrix} Y_{cap1} & & & & \\ & \ddots & & 0 & \\ & & Y_{capi} & & \\ & 0 & & \ddots & \\ & & & & Y_{capM\times N} \end{bmatrix} \tag{8}$$

where $Y_{cap,i} = \frac{1}{Z_{cap,i}}$ and if there is no decoupling capacitor in the i^{th} row, then $Y_{cap,i} = 0$.

3.4. Overall Networks

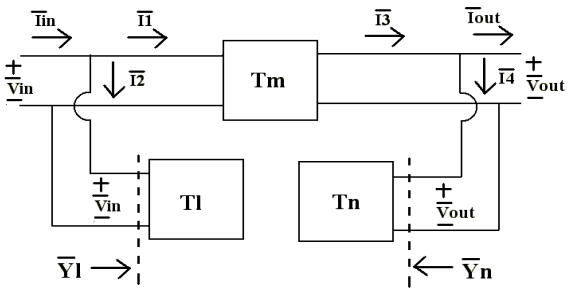


Figure 5. Block diagram of entire system

The $2(M\times N)\times 2(M\times N)$ transmission matrix for the overall power distribution network which consists of a cascade of two or more networks can now be obtained by multiplying the individual matrices [2], [3]. For the rectangular multi-layered planes in Figure 1, since all the matrices for planes, via, and decoupling capacitors have the same size, the response of the entire geometry can be obtained as a single $2(M\times N)\times 2(M\times N)$ matrix. The block representation of the cascade connection of $2(M\times N)$-port networks is shown in Figure 5 using the [T] matrix representation. As seen in Figure 5, the entire system can be simplified into 3 parts of block diagrams in term of input and output ports, which have input voltage and current variables; and output voltage and current variables, respectively. The transmission matrix for the block diagrams can be represented as follows:

$$\begin{aligned} [T_l]&=\begin{bmatrix} A_l & B_l \\ C_l & D_l \end{bmatrix}= \\ &\begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_1 \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{1,2} \times \begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_2 \times\cdots\times \begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_l \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l,l+1} \\ [T_m]&=\begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix}= \\ &\begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_{l+1} \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+1,l+2} \times \begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_{l+2} \times\cdots\times \begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_{l+m} \\ [T_n]&=\begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix}= \\ &\begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+m,l+m+1} \times \begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_{l+m+1} \times \begin{bmatrix} I & B_{via} \\ 0 & I \end{bmatrix}_{l+m+1,l+m+2} \times\cdots\times \begin{bmatrix} I & 0 \\ C_p+C_{cap} & I \end{bmatrix}_{l+m+n} \end{aligned} \tag{9}$$

where l, m, and n represent the number of power/ground plane pairs. From Figure 5, two inversions of a $2(M\times N)\times 2(M\times N)$ matrix are needed to obtain the overall transmission matrix, and one inversion of a matrix is needed to convert to the $2(M\times N)\times 2(M\times N)$ impedance matrix [Z] of the network [2], [3]. However, since most of the computational time is taken to invert a matrix, the number of matrix inversions needs to be minimized. Using one inversion of a matrix, it is possible to convert to the impedance matrix from Eq. (9). The overall $2(M\times N)\times 2(M\times N)$ impedance matrix for the multiple input and output ports can be computed as follows:

$$\begin{aligned} &[Z_A]=R_n\times C_{inv}\times D_l \quad [Z_D]=A_n\times C_{inv}\times R_l \\ &[Z_B]=[Z_C]=A_n\times C_{inv}\times D_l \\ &\text{where} \quad C_{inv}=([C_l \quad D_l]\times\begin{bmatrix} A_m & B_m \\ C_m & D_m \end{bmatrix}\times\begin{bmatrix} A_n \\ C_n \end{bmatrix})^{-1} \\ &R_n = A_m\times A_n + B_m\times C_n \quad R_l = C_l\times B_m + D_l\times D_m \end{aligned} \tag{10}$$

During the design of the power delivery system, the impedance at specific points on the network is often desired. This can either be the self impedance at a port or the trans-impedance between ports. This can reduce about half the computations during the matrix multiplications. Only the C matrix, which can be computed by multiplications of the transmission matrix from Plane 1 to Plane (l+m+n), the rows of R_n and A_n, and the columns of R_l and D_l at the specific points are needed.

4. Test vehicle description

The test structure consists of five 27.94 cm by 22.86 cm rectangular pairs of power/ground planes with FR4

dielectric with relative permittivity $\varepsilon_r = 4.5$. Figure 1 shows the details of the plane layers. The conductor planes are made of copper ($\sigma_c = 5.8\times10^7$ S/m) with a thickness of 30 μm and dielectric loss tangent $\tan(\delta) = 0.02$ at 1 GHz. Using a unit cell size of 7.62 mm by 7.62 mm, the PDS was divided into 37×30 unit cells, which require a 2356×2356 matrix size for the transmission matrix. An excitation point (Port 1) was located at (x = 13.8 cm, y = 11.25 cm) and an observation point (Port 2) at (x = 2 cm, y = 2 cm) between V1 and G1 planes. Three kinds of 32 decoupling capacitors (C = 47 nF, ESL = 1 nH, ESR = 0.1 Ω; C = 10 nF, ESL = 1 nH, ESR = 0.1 Ω; and C = 20 μF, ESL = 10 nH, ESR = 0.1 Ω), with locations as shown by the rectangular dots in Figure 2, were incorporated between V1 and G1 planes. Twenty vias, which have the same locations as the decoupling capacitors, were vertically connected from power plane to power plane and from ground plane to ground plane.

5. Results

5.1. Comparison of the transmission matrix and cavity resonator method

To check the accuracy of the transmission matrix method, the results have been compared with the cavity resonator model for the structure shown in Figure 1. Figure 6 shows the transfer impedance between Port 1 and Port 2. In this section, via inductances were not included. Each plane pair is connected by a small value of resistors ($1\,\mu\Omega$), so that the resistors mimic a short circuit. For comparison, the propagating modes were set to m = 6, and n = 5 in the cavity resonator model described in [4]. As shown in Figure 6, both the methods show good agreement.

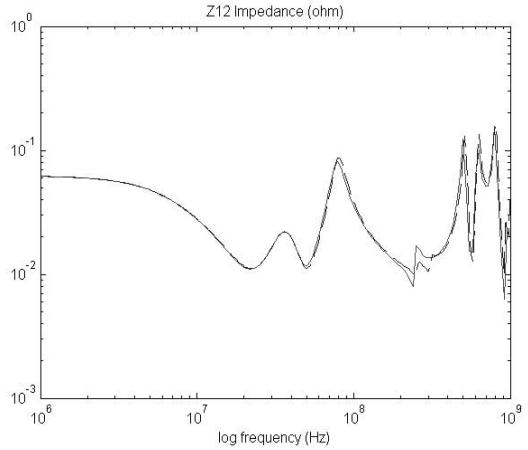
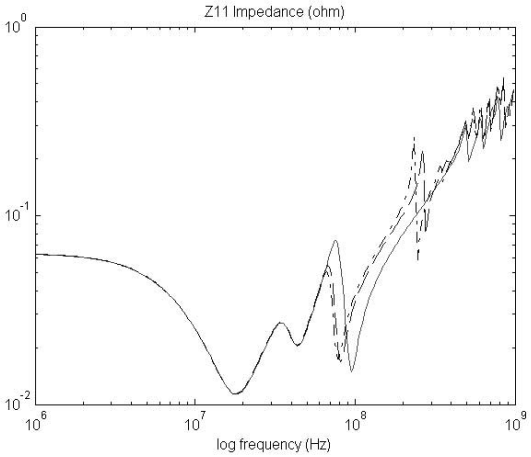


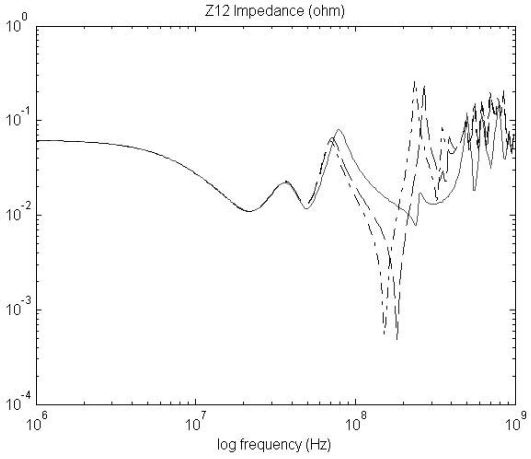
Figure 6. Impedance without via effects
solid line: transmission matrix
dashed line: cavity resonator

5.2. Comparison of vias with no inductance, self inductance, and self and mutual inductance

As the cut-off frequency on the PDS increases, the effects of vias are no longer negligible. Since vias are characterized as inductances, impedance values are varied in the high frequency range, and the null resonant frequencies move to lower frequencies. To check the effect of vias, three cases were compared: effect of no inductances (as short circuits), effect of partial self inductances, and effect of partial self and mutual inductances. The diameter of the via holes is 0.3556 mm and the value of the partial self inductances is around 110 pH. Since the via couplings between the different layers, which were computed as a very small value using FastHenry, are negligible [7], they were neglected. Figure 7 shows the differences for the three cases.



(a)



(b)

Figure 7. Impedance with and without via effects
solid line: no via inductance
dashed line: self inductance
dash-dot line: self and mutual inductance

As shown in Figure 7, via inductances affects the null resonant frequencies and magnitudes of plane impedances

as the frequency range increases. However, while multi-layered power/ground planes with via inductances have the same peak resonant frequencies of the planes without inductances, they have additional resonant frequencies since via inductances are coupled with the capacitances of the planes. As the PDS has more planes with the parallel connections of vias, the plane impedances can be more seriously affected by vias. The impedance magnitude with partial self and mutual inductances are very close to the magnitude with partial self inductances. This means that the coupling coefficients are secondary effects to the PDS.

In [3], a transient response in the time domain was generated from the frequency domain data. Using Inverse Discrete Fourier Transform (IDFT), ground bounce in PDS was captured. The simulation results in the time domain for the three cases, which have been mentioned previously, were also compared.

6. CPU time and memory requirement comparison

As per the comparison of CPU time between Spice and the transmission matrix method in [2], a speed-up in the range 7X-13X was obtained for a pair of power/ground planes by using the transmission matrix method. Compared with Spice, it is believed that a larger speed-up can be obtained for the multi-layered planes than for a single plane pair. Moreover, as shown in Eq. (9), the number of decoupling capacitors does not affect CPU time since only additions are required. To compute the impedances of the planes with the decoupling capacitors and vias for the test structure, a CPU time of 717 seconds for 300 sampling frequency points was required using MATLAB. In addition, the transmission matrix method enables large memory savings that enable the analysis for any numbers of plane pairs. Table 1 shows the number of circuit elements and the matrix size between Spice and the transmission matrix method for the amount of memory storage required in computation. These numbers were estimated only for the plane RLCG circuit elements as an example, which is shown in Figure 1. Most of the computational time is required to invert a matrix, as mentioned in the previous section. Hence, the smaller the matrix, the smaller is the computation time. As shown in Table 1, the small size of the transmission matrix leads to savings in CPU time.

Table 1. Comparison of matrix size

Number of unit cells	Parameter	Spice (MNA)	Transmission matrix
37×30×5	Elements	57,520	57,520
	Nodes	40,195	5,890
	Matrix size	**63,410×63,410**	**2,356×2,356**

7. Conclusion

The transmission matrix method has been discussed for analyzing multi-layered power distribution with decoupling capacitors and vias. This paper described the physical principle, formulation and implementation of the transmission matrix method. This method is computationally more efficient than Spice, which is commonly used for most power delivery system analysis. The transmission matrix leads to small memory requirements and large savings in computer run time. In addition, even the most complicated power plane structure can be analyzed using the transmission matrix method.

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