Compact Modeling of SOI-LDMOS Transistor including Impact Ionization, Snapback and Self Heating

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THESIS CERTIFICATE

This is to certify that the thesis titled **Compact Modeling of SOI-LDMOS Transistor including Impact Ionization, Snapback and Self-heating**, submitted by **Ujwal Radhakrishna**, to the Indian Institute of Technology, Madras, for the award of the degree of **Master of Technology and Bachelor of Technology (Dual Degree)**, is a bona fide record of the research work done by him under our supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

KEYWORDS: LDMOS; SOI Technology; Compact model; Impact ionization; Snapback; Self-heating.

In recent times, interest towards lateral double diffused MOSFETs (LDMOS) has been increasing considerably due to their ease of integration with low voltage circuitry to form high voltage integrated circuits (HVICs). Accurate design of HVICs requires LDMOS models which predict device behavior accurately over wide ranges of bias and temperatures. Modeling effects like impact ionization and snapback is the key to achieve a comprehensive model of such devices. Fabrication of LDMOS structure on silicon-on-insulator (SOI) platform has become a norm in the industry due to advantages like better isolation, lower leakage, high packing density and reduced parasitics compared to bulk devices. This inadvertently leads to device self-heating which tends to modify device characteristics. Hence a model which accounts for device self-heating is essential.

In this thesis, a physics-based compact model including impact ionization, associated snapback, and self-heating in SOI-LDMOS is presented. The model explains the snapback effect observed in these devices which is due to the turn-on of lateral parasitic bipolar transistor (BJT). Compact model described in [31] is used for channel current and Chynoweth's law [32] is used for the avalanche ionization rates. The model includes the effect of device self-heating using resistive thermal network with explicit formulations and minimum nodes.

Thus the model has the advantages of both minimum computation time and reasonable accuracy. Comparison of model results with device simulation data show that the model exhibits excellent accuracy over a wide range of bias voltages and temperatures.

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ABBREVIATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon On Insulator
LDMOS	Lateral Double Diffused MOS
VDMOS	Vertical Double Diffused MOS
HVIC	High Voltage Integrated Circuit
PIC	Power Integrated Circuit
BJT	Bipolar Junction Transistor
JFET	Junction Field Effect Transistor
PMOS	P-channel MOSFET
DC	Direct Current
AC	Alternating Current
BOX	Buried Oxide
EHP	Electron hole pair
SOL1	Solution 1 corresponding to pre-snapback region
SOL2	Solution 2 corresponding to snapback region
SCE	Short channel effect
CLM	Channel length modulation
DIBL	Drain induced barrier lowering
FoM	Figure of merit

NOTATION

V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
V_{DiS}	Voltage drop across channel
$V_{D'D_i}$	Voltage drop across drift region under gate oxide
$V_{DD'}$	Voltage drop across drift region under field oxide
$V_{sat,ch}$	Channel saturation voltage
$V_{sat,dr}$	Reg-II saturation voltage
$V_{DiS,eff}$	Effective voltage drop in channel
$V_{D'Di,eff}$	Effective voltage drop in Reg-II
V_{BS}	Base to source voltage
V_{BD}	Base to drain voltage
I_{DS}	Drain to source current
I_{ch}	Channel region current
I_{dr}	Current in Reg-II
I_{dr1}	Current in Reg-III
I_f	Forward diode current
I_r	Reverse diode current
I_T	Transfer current of BJT
I_{AVL}	Avalanche current
L_{ch}	Length of channel region
L_{dr}	Length of Reg-II
L_{LC}	Length of Reg-III
L_{pw}	Length of p-well region
C_{ox}	Capacitance of oxide
W	Width of LDMOS
A	Cross section area of LDMOS
t_{Si}	Silicon film thickness

t_{BOX}	Thickness of buried oxide
N_D	Doping concentration in Reg-II
N_{dr1}	Doping concentration in Reg-III
V_T	Thermal voltage
K	Boltzman's constant
ϵ_{Si}	Permitivity of silicon
E_G	Bandgap of silicon
v_{sat}	Saturation velocity of electrons
ψ_s	Surface potential in channel
Q_{inv}	Inversion charge per unit area in Reg-I
Q_n^{dr}	Total drift region charge per unit area in Reg-II
Q_{acc}^{dr}	Accumulation charge per unit area in Reg-II
Q_{dep}^{dr}	Depletion charge per unit area in Reg-II
V_{FB}^{ch}	Flat band voltage in channel
V_{FB}^{dr}	Flat band voltage in Reg-II
μ_{ch}	Effective mobility in channel
μ_{dr}	Effective mobility in Reg-II
μ_{dr1}	Zero field mobility in Reg-III
μ_{pw}	Zero field mobility in p-well region
$\theta_{3,ch}$	Velocity saturation parameter in channel
θ_1	Channel mobility reduction parameter
θ_2	Channel mobility reduction parameter
$\theta_{3,dr}$	Velocity saturation parameter in Reg-II
θ_{dr1}	Velocity saturation parameter in Reg-III
λ_{ch}	Channel length modulation parameter
λ_{dr1}	Drift length modulation parameter
β_f	Current gain of BJT in forward active mode
β_r	Current gain of BJT in inverse active mode
M	Impact ionization multiplication factor
α	Impact ionization coefficient
ρ_{pw}	Resistivity of p-well region
R_B	Resistance of base region

R_{ch}	Thermal resistance of channel
R_{dr}	Thermal resistance of Reg-II
R_{dr1}	Thermal resistance of Reg-III
P_{ch}	Power dissipated due to channel current
P_{dr}	Power dissipated due to Reg-II current
P_{dr1}	Power dissipated due to Reg-III current
$P_{dr1,BJT}$	Power dissipated due to BJT currents
k_{BOX}	Thermal conductivity of buried oxide
dT_{ch}	Temperature update in MOSFET thermal subcircuit in channel
dT_{dr}	Temperature update in MOSFET thermal subcircuit in Reg-II
dT_{dr1}	Temperature update in MOSFET thermal subcircuit in Reg-III
$dT_{dr1,BJT}$	Temperature update in BJT thermal subcircuit

CHAPTER 1

INTRODUCTION

1.1 An overview of power semiconductor devices

Today, power semiconductor devices have become industry's choice while designing high voltage integrated circuits (HVICs). This current status enjoyed by power semiconductor devices is the result of remarkable advances in silicon fabrication technology and development efforts to create new novel device structures. Since the inception of the bipolar junction transistor and subsequent development of thyristor, power semiconductor devices have come a long way.

It took almost a decade for power semiconductor devices to find practical application in HVICs, since the device was first commercially introduced by Texas Instruments in 1954. Thyristors-the first class of power semiconductor devices suffered from limitations like difficulty of integration and poor switching speed. It was the introduction of power MOSFETs in late seventies [1], which led to the development of new generation power devices. Initially high voltage MOSFETs were developed by converting the regular lateral MOSFET into an asymmetric device, thus increasing the reverse blocking capability of the device [2]. This trend ultimately led to the creation of lateral double diffused metal oxide semiconductor (LDMOS) transistors.

These LDMOS devices can be easily integrated with low voltage circuitry and continue to be industry standard even today for medium voltage (less than 100 V) power applications. The main disadvantages of LDMOS transistors are its low current ratings and breakdown voltage-specific on-resistance tradeoff. The reverse voltage in such devices is dropped across a lightly doped extended drain region. So, to sustain higher reverse breakdown voltages, the length of this region has to be large, thus increasing the area requirement of the device. In order to circumvent these problems, vertical double diffused MOS (VDMOS) technology was developed. Though VDMOS technology

provides larger current ratings and higher breakdown voltages compared to its lateral counterpart [3], it requires complicated process steps and its integration with low voltage circuitry is a challenge. Thus VDMOS devices find market in high current and high power applications, while medium power industry is still dominated by LDMOS devices.

Today, HVICs and power integrated circuits (PICs) are replacing discrete circuits in automotive and consumer applications like switch mode power supplies (SMPS), DC-DC converters and power amplifiers [4][5][6]. Integration of high and low voltage circuits on the same chip results in improved performance as well as reduced size. In general, HVICs are designed to give low output currents even at high supply voltages while PICs are designed for higher currents [7][8]. In smart PICs, high voltage circuits act as interface between the power load and low voltage digital control logic [9][10]. The LDMOS devices are integral part of many of these interesting applications.

1.2 Current scenario in LDMOS transistor modeling

As PICs and HVICs with LDMOS technology are finding use in consumer applications like SMPS and convertors, there is an increasing need to model LDMOS transistors. Another recent trend is the processing of LDMOS devices on silicon on insulator (SOI) platform. LDMOS devices fabricated on an SOI substrate has several advantages like reduced latch up, higher packing density and lower leakage currents [11]. An essential requirement needed in smart power ICs is isolation between power devices and low voltage circuitry. This is possible in SOI technology and hence SOI-LDMOS transistors are increasingly being used in smart power ICs. Thus compact models for SOI-LDMOS transistors capable of modeling device characteristics over wide range of bias and for various device dimensions, are needed for the optimal failsafe design of these power integrated circuits. The structure of SOI-LDMOS is different from that of a conventional MOSFET because of the presence of an extended drift region between the channel and the drain region which gives an asymmetry to the structure. It is this region which sustains the high reverse voltages in the device which qualifies it to be called as a high voltage device. In addition, the channel doping in such devices is also non-uniform

due to double diffusion process, which results in increased complexity in SOI-LDMOS modeling compared to modeling a conventional MOSFET.

There have been many efforts in modeling SOI-LDMOS especially in low drain voltage regime. The two main approaches used are (i) macro-modeling and (ii) compact modeling. The macro-modeling approach consists of discrete elements or modules connected together to synthesize a new circuit which models both AC and DC regime. As the number of effects needed to be modeled rises, the number of elements in the circuit rises, the parameters needed to be extracted increase and the extraction process becomes lengthy and complex. Increased number of internal nodes also increases simulation time and results in convergence problems. There are many existing LDMOS macro models based on SPICE which consider SPICE models for MOSFETs, JFETs and diodes to model LDMOS [12][13][14]. Another macro model BSIM4 uses JFET to model drift region and shorted PMOS transistors to model capacitance behavior of drift region [15]. All these models have a large number of non-physical model parameters.

The compact modeling approach, on the other hand maintains device unity by a set of self-consistent expressions which are able to produce device behavior. It can be easily used when implementation is needed in complex circuits, where accuracy and robustness of model are critical. All internal nodal equations in such a model are solved in the model itself, thereby reducing computation time. Compact models have clear advantage over macro models due to better convergence behavior, reduced number of parameters and possibility of physical tuning of parameters. EKV model is an example of such a compact model for LDMOS devices [16][17][18]. Though the model is simple and has been validated for both VDMOS and SOI-LDMOS in low V_{DS} regime, its inaccuracy in capacitance modeling and convergence problems in modeling substrate current has limited its use. The most popular compact model for SOI-LDMOS devices is the MOS model 20 (MM20) [19] by NXP semiconductors. It is a surface potential based model and takes into account the channel and drift region under the gate oxide. It does not however, model the drift region under field oxide and thus cannot be used for higher voltage devices. The effect of quasi-saturation in drift region under field oxide is considered in [31]. However, it does not model any secondary effects in such devices. It accurately describes the low V_{DS} regime and hence is taken as starting point

for the model developed in this thesis.

A device model is of use to industry only when it can model actual device characteristics exhibited by the device on a chip. To achieve this, the model must be comprehensive and must account for any secondary effects that might influence the device characteristics in a real-life scenario. High voltage devices like SOI-LDMOS transistors are affected by three such effects namely, impact ionization, snapback and self heating.

High voltage SOI-LDMOS devices are prone to impact ionization driven snapback due to triggering on of lateral parasitic BJT. On a typical drain-voltage dependent drain current curve ($I_D - V_{DS}$) at a given gate voltage (V_{GS}) (Ref Fig. 1.1), as operating point is moved towards higher V_{DS}, the slope of the curve increases and eventually becomes infinite at a point termed as 'snapback point'. Beyond this point the device exhibits negative resistance and is said to be operating in the snapback region.

Although impact ionization driven snapback breakdown is reversible, operation of devices in this region is generally avoided as it can lead to secondary thermal breakdown which can result in device damage [20]. There have been several efforts to avoid snapback and thus extend the safe operating area (SOA) of these devices [20]. This notion of excluding snapback region from SOA in these devices has resulted in lack of interest in modeling snapback. So far, snapback modeling has been of interest only to designers of EPROMS where it constitutes an acute constraint. However in recent times, snapback has found useful applications in input/output electro static discharge (ESD) protection circuits [21][22] thus increasing the need for reliable snapback model.

In literature, there are few detailed studies on snapback in devices similar to SOI-LDMOS and few of them have resulted in model development [22][23][24][25][26][27] [28]. Most of them model snapback using the well known subcircuit model (also known as macromodel) approach. Although the subcircuit models in [23][24][25][26] include the parasitic BJT which is responsible for snapback, the main aim seems to be to accurately determine snapback point and hence SOA, rather than modeling snapback region itself. The snapback model in [27] for a floating body SOI-MOSFET cannot be extended to SOI-LDMOS as it does not model the impact ionization coefficient (M) and has convergence problems in circuit simulators due to discontinuities in model expres-

sions. SPICE Model in [28] for NMOS transistor cannot be directly applied to model snapback in SOI-LDMOS. When implemented in Verilog-A, model in [28] will always converge to pre-snapback solution and not to snapback solution. It also does not consider the effect of self-heating on device characteristics.

Self heating is a persistent problem in SOI-LDMOS devices as the active drift layer is sandwiched between field oxide and thick buried oxide. So, models for these devices must account for temperature rise due to device self-heating for reliable results. Thermal networks containing resistive elements are the standard way of modeling self-heating in such devices [29][30]. Self-heating gains even more significance in the snapback region where current levels are high. It results in lowering of snapback voltage and reduction in SOA. A model describing self-heating, especially in snapback region in SOI-LDMOS has not been developed previously. Thus compact models, in addition to accurately modeling device characteristics over normal operating range of bias, must also model several secondary effects such as impact ionization, snapback and self-heating effects which are prominent in SOI-LDMOS devices and significantly affect device characteristics.

The need for a comprehensive model which accounts for aforementioned effects is clear from Fig. 1.1. Device simulations are performed with and without considering device self heating. These are compared with results from existing models in literature. Models, such as [31] do not consider any secondary effects and hence are able to model only low V_{DS} region accurately. Models in [27][28] account for impact ionization but not snapback, hence are able to predict device characteristics upto snapback point. They do not yield the snapback solution. In addition, the models do not consider device self heating. Thus the actual device characteristics shown with self heating are not modeled by any of these models. A comprehensive model including all the above effects is currently not available in literature.

In this thesis, a comprehensive model to describe static characteristics of SOI-LDMOS is proposed. MM20 based model in [31] serves as a starting point for describing low current region where parasitic BJT is off. In low current regime, the model considers field dependant mobility reduction, velocity saturation in channel and quasi saturation in drift region. In high current regime, the new model incorporates the ef-
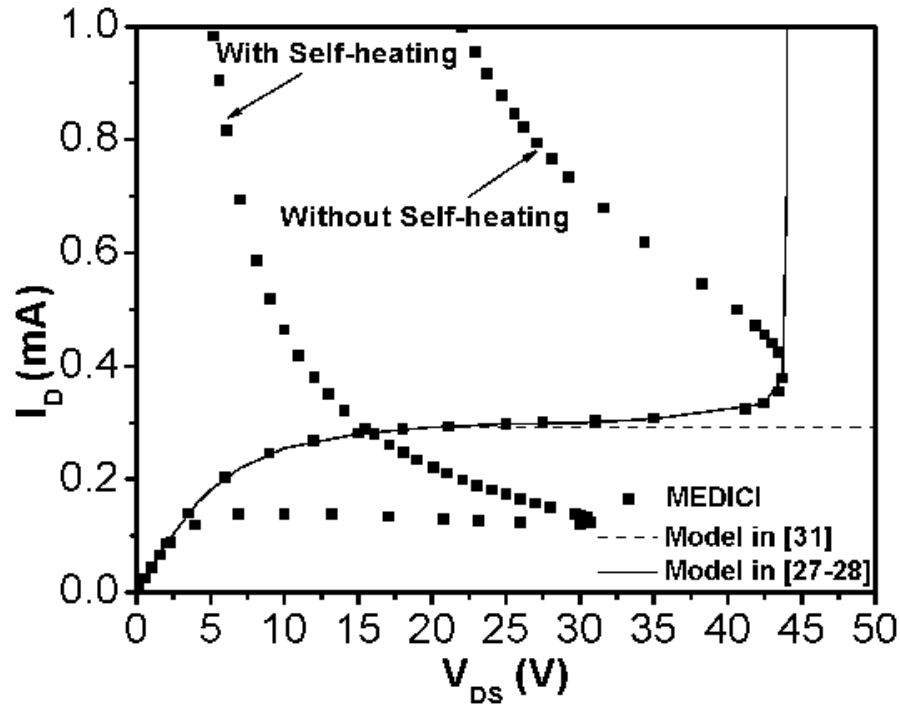
Figure 1.1: $I_D - V_{DS}$ plots for V_{GS}=15V from existing models [27][28],[31] compared with device simulation results from the 2-D device simulator MEDICI.

fects of impact ionization triggered snapback as well as self-heating in channel and drift layers due to both MOSFET and parasitic BJT currents.

1.3 Objectives

The main objectives of the thesis are outlined below.

- To analyze the behavior of SOI-LDMOS in channel, drift region under gate oxide and drift region under field oxide for different gate and drain bias voltages.

- To analyze the device under impact ionization regime and develop a physics based model to explain the phenomenon.

- To understand snapback mechanism in these devices and develop a physics based model which can be implemented in Verilog-A.

- To understand and model device self-heating occurring in such devices.

1.4   Structure of the thesis

The thesis is organized as follows.

- **Chapter 2: Analysis of physical effects**

  This chapter deals with analysis of low voltage region along with aspects of impact ionization, subsequent snapback and self-heating in the device. The device behavior is analyzed with the aid of MEDICI [36] simulation results.

- **Chapter 3: Static model and Verilog-A implementation**

  In this chapter, compact model to include these effects is proposed and Verilog-A [34] implementation of the model is explained. The model uses MM20 model for channel and drift region under gate oxide. quasisaturation model to model drift region under field oxide. Chynoweth's law to model impact ionization and thermal networks to model device self-heating.

- **Chapter 4: Results and discussions**

  Static model results are compared with MEDICI simulation results. A way for the optimum design of SOI-LDMOS with the help of these results is described.

- **Chapter 5: Conclusions**

  The contributions and perspectives offered by this work are presented. Scope for future work is listed.

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CHAPTER 2

ANALYSIS OF PHYSICAL EFFECTS

High voltage (HV) lateral MOS devices, where the gate electrode works as a field plate is an interesting structure in mainstream HV technology. In particular HV SOI-LDMOS device with its extended drain region and lateral non-uniformly doped channel increases model complexity. In addition it includes a plethora of effects like quasi saturation in drift region, parasitic BJT turn on, self heating due to poor thermal conductivity of buried oxide (BOX) and so on which offer considerable challenge to device model developers.

In this chapter, focus is mainly on analysis of physical effects which appear in SOI-LDMOS transistor under static conditions. Firstly, The effect of gate and drain bias on voltage drop in different regions and its subsequent impact on currents in these regions are analyzed. This is used to explain the current formulations of the model in [31] which will be used in low V_{DS} regime. Next, the analysis of impact ionization and carrier generation rates and resulting increase in current densities will be studied to explain avalanche process. The electric field distribution in the device is taken into account to explain avalanche driven snapback. Finally, temperature rise with bias and its distribution within device geometry is analyzed to account for device self-heating. For the purpose of these studies commercially available two-dimensional (2-D) device simulator MEDICI [36] is used.

2.1 Device structure

SOI-LDMOS is an asymmetric structure with a drift region located between the channel and the drain contact. Schematic of the cross-section of high voltage SOI-LDMOS used in this investigation is shown in Fig. 2.1. The channel region is self aligned to the gate and is formed by p-type diffusion creating a p-well under the gate. Thus the doping concentration in the channel is non-uniform with gradual reduction from source to

drain end. The source is then formed by n^+ diffusion. Since the channel and source are formed by successive diffusion steps, these devices are called double-diffused MOSFETs. The LDMOS uses lateral double diffusion which makes it possible to achieve shorter channels without hindrance from photolithographic process. The n-drift region sustains the reverse voltage and hence is lightly doped in comparison to channel. The depletion region thus extends more into the drift region which holds the reverse breakdown voltage. The gate electrode covers the surface of the channel and a part of the drift region. The active part of the device is separated from the substrate by a thick buried oxide (BOX). This provides dielectric isolation and minimizes parasitics. It is a planar device and since drain, source and gate contacts are taken from the surface, integration of SOI-LDMOS devices with low voltage SOI-CMOS based circuitry is made easy.
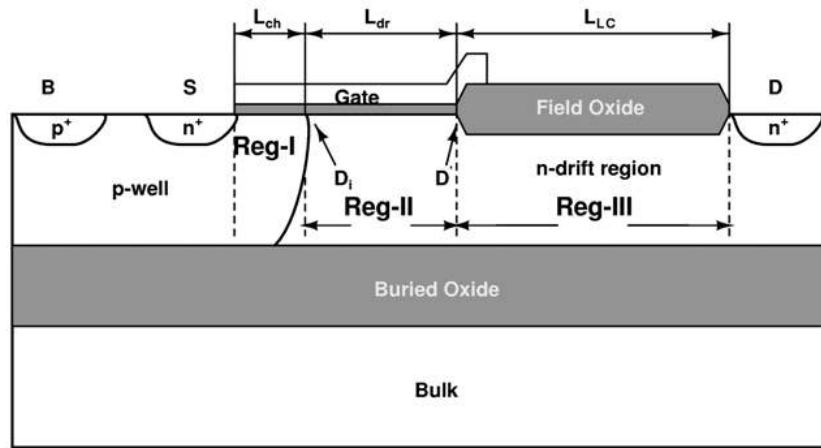
Figure 2.1: Schematic of the cross section of SOI-LDMOS.

From the schematic of the cross section of the device in Fig 2.1, it is clear that there are three regions of importance in the active area of the device. The p-well i.e. the channel region (Reg-I), the drift region with the gate oxide at its surface (Reg-II) and the long drift region sandwiched between top field oxide and bottom BOX (Reg-III). The abrupt transition between Reg-I and Reg-II is defined by the point D_i. The transition between Reg-II and Reg-III is defined by the point D'. Since the field oxide is thick, variation of gate voltage does not influence behavior of device in Reg-III.
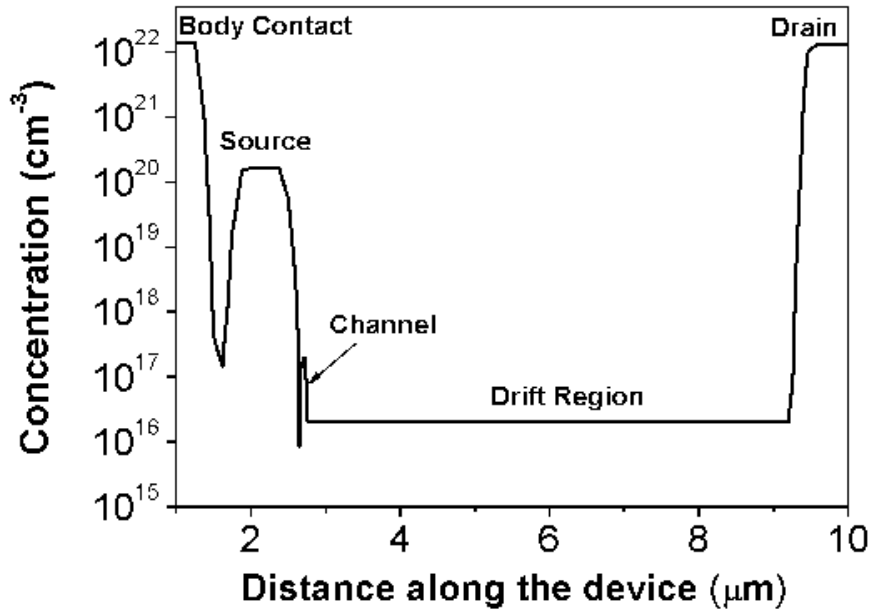
Figure 2.2: Doping profile along silicon surface showing doping in channel, drift region and all contacts.

The doping profile of the device along a lateral cutline close to the silicon-silicon dioxide interface is shown in Fig. 2.2. Even though for a practical device, the channel doping is non uniform due to double diffusion technology, here it is assumed to be uniform for simplicity. It is also clear that the drift region has the lowest doping levels in the structure to sustain applied voltage.

For the device under discussion, p-well forming the channel has a uniform doping concentration of $2 \times 10^{17} cm^{-3}$. Entire transistor is isolated from the bulk by a buried oxide of thickness 2 μm. The device has a very long lightly n-type doped drift region to withstand externally applied high voltages. The doping concentration in the region is $2 \times 10^{16} cm^{-3}$. The length of the channel (L_{ch}) is 0.125 μm, length of drift layer under gate oxide (L_{dr}) is 0.325 μm and length of drift layer under thick field oxide (L_{LC}) is 6.5 μm. The total device length is 10 μm. The gate oxide thickness is 3.8 nm, field oxide thickness is 100 nm.

2.2 MOSFET static currents

[31] In order to provide accurate model for the SOI-LDMOS, its electrical behavior needs to be analyzed and understood. This requires the separation of the device structure into specific regions i.e. Reg-I, Reg-II and Reg-III. This separation is not physical but only to understand the device behavior in a better way. It helps in modeling MOSFET currents in the low bias regime and serves as basis for the model even in high bias regime where BJT is active.

When V_{GS} is greater than the threshold voltage of the channel (Reg-I), electrons are attracted to the surface to form an inversion layer. The gate extends over a portion of the drift region to form Reg-II, where the applied voltage causes accumulation condition under the gate oxide. Now, if V_{DS} is applied, electrons from source will move through inversion layer in Reg-I into Reg-II and will drift through the accumulation layer into Reg-III and finally into drain contact.

The LDMOS transistor is similar to conventional MOSFETs in Reg-I. So LDMOS can be considered as a low voltage MOSFET in series with the drift region. The advantage of this approach is that, already available surface potential based models for Reg-I can be used and focus could be directed at modeling phenomenon arising out of drift layers in Reg-II and Reg-III. To understand the operation of the device, the operating bias range is divided into two regimes, high V_{GS} and low to moderate V_{GS}. Potential drops across Reg-I, Reg-II and Reg-III are studied for both high V_{GS} and low V_{GS} regimes in order to explain the I_d-V_{DS} characteristics of the device, simulated using MEDICI, shown in Fig. 2.3.
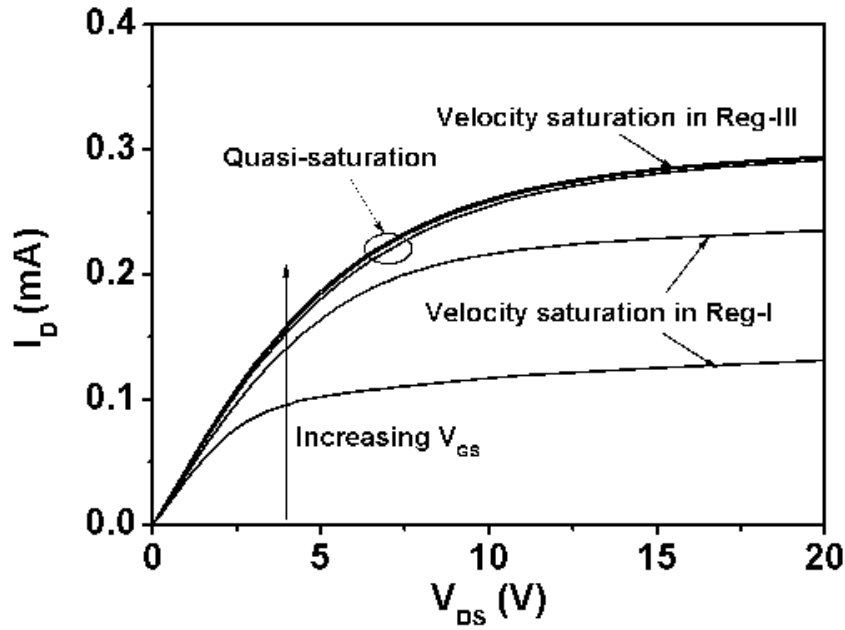
Figure 2.3: I_d-V_{DS} plots simulated for V_{GS} = 3V, 5V, 10V, 15V and 20V, in MEDICI.

2.2.1 Potential drop in Reg-I

Low to moderate V_{GS}

Figure 2.4 shows the potential drop across the channel for different V_{GS}. It can be observed that as V_{DS} increases, the drop across Reg-I increases. This is because even at low V_{GS}, Reg-II is in accumulation condition and its conductivity is high due to large accumulation of electrons. As V_{DS} is increased further, the lateral electric field in the region increases and reaches the critical value. Beyond this point, the voltage across Reg-I saturates. This can be observed for V_{GS}=5V in Fig. 2.4. This is velocity saturation in Reg-I which leads to current saturation. Current saturation due to velocity saturation in Reg-I can be seen in Fig. 2.3 for V_{GS}=3V and 5V. The increase in saturation current with V_{DS} seen in Fig. 2.3, is due to short channel effects (SCE) like channel length modulation (CLM) and drain induced barrier lowering (DIBL).
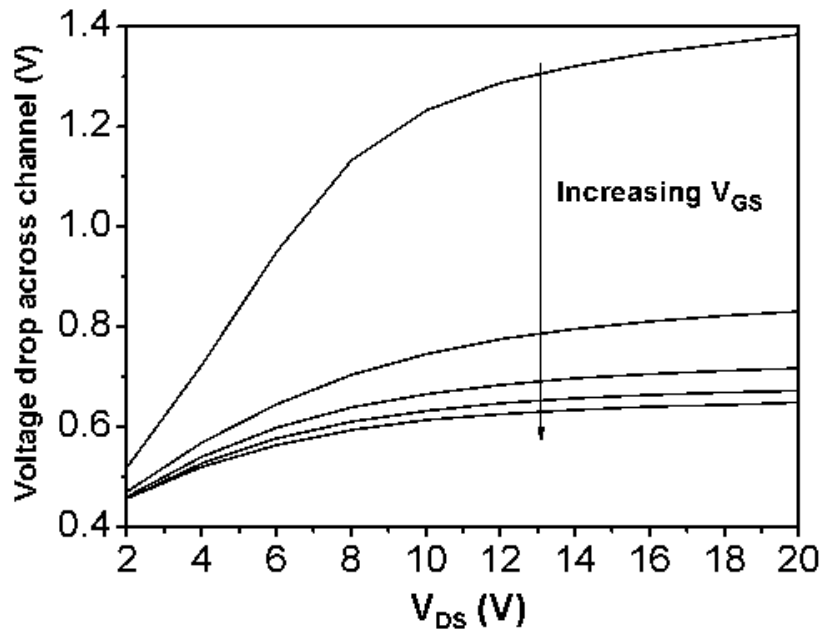
Figure 2.4: Voltage drop across channel obtained from MEDICI at V_{GS}= 5V, 10V, 15V, 20V and 25V.

High V_{GS}

At high V_{GS}, conductivity of both Reg-I and Reg-II is very high. As field oxide is very thick and gate overlap with Reg-III is not significant, the conductivity of Reg-III remains fairly unaffected even by this high V_{GS}. The voltage drop across Reg-I reduces at high V_{GS}, due to increased conductivity of the channel. At high V_{GS}, saturation velocity is never attained in the channel as the critical field is never reached due to lower voltage drop across the channel. As V_{GS} is further raised, the potential drop across the channel keeps reducing. Thus while saturation of current is due to velocity saturation in Reg-I upto V_{GS}=5V in Fig. 2.3, for high V_{GS}, current saturation is not governed by Reg-I.
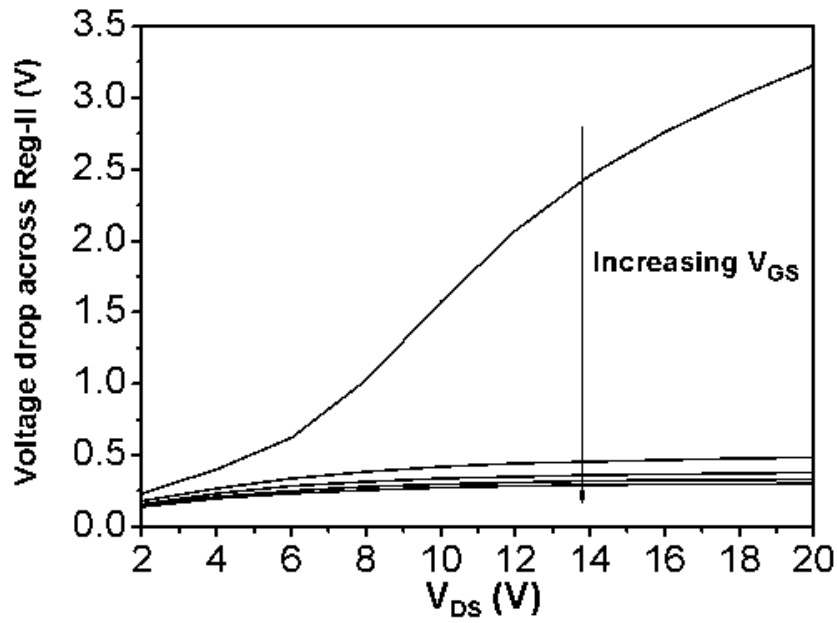
Figure 2.5: Voltage drop across Reg-II obtained from MEDICI at V_{GS}= 5V, 10V, 15V, 20V and 25V.

2.2.2 Potential drop in Reg-II

Low to moderate V_{GS}

The potential drop across Reg-II for different V_{GS} is shown in Fig. 2.5. The drop across Reg-II increases with increasing V_{DS}, but at a reduced slope compared to that in Reg-I. This is due to higher conductivity of Reg-II even at lower V_{GS} due to accumulation in the region. After velocity saturation occurs in Reg-I, the voltage drop across Reg-I saturates and the remaining voltage drops across Reg-II. Thus, the slope of the potential drop across Reg-II increases after voltage saturates in Reg-I. This can be observed in Fig. 2.5 for V_{GS}=5V at about V_{DS}=8V . The voltage drop across this region increases and does not saturate even for V_{DS}=20V, as seen in Fig. 2.5, for V_{GS}=5V. So current saturation is controlled only by Reg-I and not Reg-II for low to moderate V_{GS}.

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High V_{GS}

At high V_{GS}, conductivity of Reg-II is very high. with low voltage drop across the region. The velocity never saturates as critical field is never achieved in the region. This can be observed for V_{GS} >10V in Fig. 2.5.

2.2.3 Potential drop in Reg-III
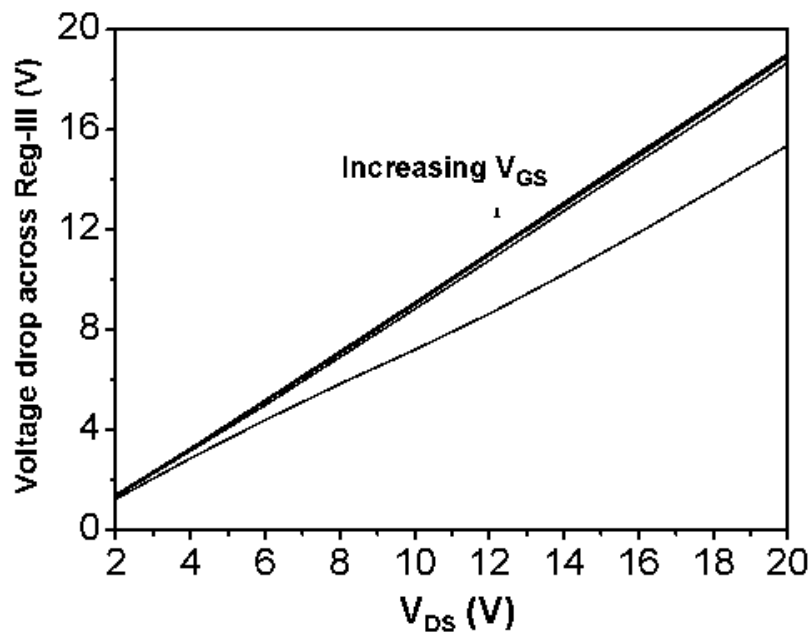
Figure 2.6: Voltage drop across Reg-III obtained from MEDICI at V_{GS}= 5V, 10V, 15V, 20V and 25V.

Low to moderate V_{GS}

The potential drop across Reg-III for different V_{GS} is shown in Fig. 2.6. As can be observed from the figure, the voltage drop across Reg-III for V_{GS}=5V, increases with V_{DS} but at reduced slope at lower V_{DS}. However as V_{DS} is increased, after about V_{DS}=10V, the voltage drop increases at a faster rate, since at such higher V_{DS}, Reg-I voltage drop would have saturated and voltage drop across Reg-II is small. The velocity of electrons in Reg-III never saturates for lower V_{GS}.

High V_{GS}

As V_{GS} rises, the voltage drops across both Reg-I and Reg-II reduce and most of the applied voltage drops across Reg-III as can be seen in Fig. 2.6 for V_{GS} >10V. The carrier velocity in Reg-III increases and reaches saturation values for high V_{DS}. Thus, it is Reg-III which is responsible for current saturation for high V_{GS}. This is shown in Fig. 2.3, for V_{GS} >10V. As can be seen from Fig. 2.3, any further increase in V_{GS} will not increase saturation current as Reg-III is not influenced by V_{GS}. This effect is termed as quasi-saturation effect and is dominant in high voltage LDMOS devices. At high V_{GS}, velocity saturation occurs at drain end of Reg-III and with increased V_{DS} the saturation point moves towards source side. This results in drift length modulation and subsequent slight increase in drain current with V_{DS} as seen in Fig. 2.3 for V_{GS} >10V.

Thus current saturation in LDMOS transistor can occur due to two mechanisms.

- **Velocity saturation in channel:** For medium V_{GS}, as V_{DS} is increased, the lateral electric field in channel becomes greater than critical field and velocity saturation occurs leading to current saturation. This phenomenon is common to short channel devices. The device structure used for the purpose of this thesis has a channel length of $0.125\mu m$ and so velocity saturation in channel is responsible for current saturation at lower V_{GS}. However, for long channel LDMOS devices at very low V_{GS}, as V_{DS} is increased channel gets depleted and current saturates. This is called pinch-off which is normal saturation mechanism for long channel MOSFETs.

- **Velocity saturation in Reg-III:** At high V_{GS}, a second saturation mechanism is possible in HV-LDMOS transistors. It is velocity saturation in Reg-III. The intrinsic MOSFET is still in linear region while Reg-III is saturated, hence this is not real saturation. Above this critical V_{GS} at which saturation in Reg-III occurs, V_{GS} will not have any impact on current. This phenomenon is termed as quasi-saturation and limits the maximum current carrying capability in such devices.

2.3   Impact ionization and snapback

At higher bias conditions, high current density in the device coupled with large lateral electric field can result in impact ionization. Electrons from source, move through the inversion layer into the drift region and will drift through the accumulation layer. These electrons under the influence of the lateral electric field due to V_{DS}, gain sufficient energy to cause impact ionization, thereby creating secondary electron hole pairs (EHPs). The secondary electrons move towards the drain contact while the secondary holes move towards the p-well contact and form p-well hole current. Since EHPs created due to impact ionization further cause impact ionization, there is an avalanche multiplication of carriers. The whole process acts as a positive feedback mechanism and the total output current builds up to large values.
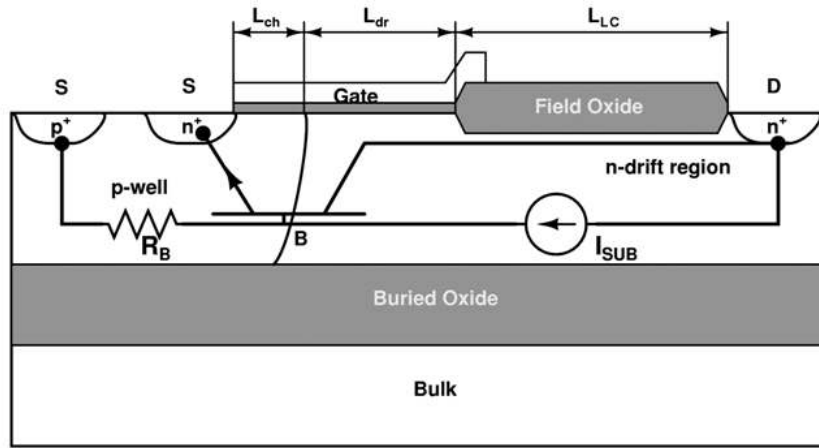
Figure 2.7: Schematic of the cross section of SOI-LDMOS.

In the SOI-LDMOS structure, in addition to avalanche multiplication of carriers due to impact ionization, there is another impact ionization driven effect termed as snapback due to the presence of parasitic lateral npn BJT transistor. In the device, n^+ source, p-well and n drift region constitute a lateral parasitic npn BJT as shown in Fig. 2.7. As V_{DS} is increased, impact ionization process builds up and the generated hole current flows towards p-well. This is represented by I_{SUB} in Fig. 2.7. Since p-well contact is sufficiently far from the p well – n drift region junction, the secondary hole current (also called substrate curent) flowing to p-well contact has to flow through a resistive p-well region shown as R_{B} in Fig. 2.7. This creates a voltage drop (V_{BS}) across p-well.

In the structure, both p well and source contacts are grounded and hence V_{BS} is the base emitter voltage (V_{BE}) of the BJT. If secondary hole current flowing through resistive p-well is large enough, V_{BS} becomes greater than about 0.7 V and BJT turns on.

After the turn on of parasitic BJT, the gate of the LDMOS transistor starts to lose control over output current as the BJT transfer current becomes a major component of the total drain current. The substrate current generated due to impact ionization, increases with both the output current and the lateral electric field (which is determined by V_{DS}). The transfer current of the BJT provides an additional current source for multiplication and increases the output current after turn on. Thus in order to generate the same substrate current, the required V_{DS} is less. V_{DS} now is only required to sustain V_{BS} so that BJT is kept in the turn on state. This V_{DS} needed to keep the BJT on, reduces as more and more impact ionization occurs and total drain current increases. Thus even though the output current increases, the required V_{DS} to generate this increasing output current reduces. This phenomenon is called snapback. The applied V_{DS} is equivalent to collector to emitter voltage (V_{CE}) of the BJT. In the limiting case, the V_{DS} drops to the collector to emitter saturation voltage ($V_{\text{CE, sat}}$) of the npn BJT, where the BJT is pushed to saturation condition. Impact ionization and snapback can limit the SOA of SOI-LDMOS devices. In order to analyze impact ionization and snapback in such devices, bias conditions can be divided into high V_{GS} and low to moderate V_{GS} condition.

2.3.1 Low to moderate V_{GS}

At low to moderate V_{GS}, Reg-I and to a certain extent Reg-II conductivities are lower and hence applied V_{DS} is mostly dropped across these regions. Since channel region is very short, even if V_{DS} is low, lateral electric field strength is high enough in Reg-I and Reg-II to cause impact ionization. Fig. 2.8, shows the electron hole pair generation rate (EHPs $cm^{-3}s^{-1}$) in the form of impact ionization contours. Each coloured region between the contours signifies region with the same generation rate (Regions with highest generation rate are depicted in red color and regions with the least generation rate are depicted in yellow). From Fig. 2.8 it is clear that impact ionization is initiated at Reg-I and Reg-II at lower V_{DS}.

Figure 2.8: Impact ionization contours (EHPs $cm^{-3}s^{-1}$) in log scale for V_{DS} of 20 V and V_{GS} of 5 V.

At higher V_{DS}, impact ionization spreads over to Reg-III as potential drop across this region and hence lateral electric field start to increase with V_{DS}. This is shown in Fig. 2.9. Although, lateral field in Reg-I and Reg-II is high, the saturation current governed by channel is still very low to cause significant avalanche multiplication at low to moderate V_{GS}. Thus even though impact ionization does occur near Reg-I, Reg-II and in Reg-III (at higher V_{DS}), it is not significant enough to cause current rise for lower V_{GS}.

Figure 2.9: Impact ionization contours (EHPs $cm^{-3}s^{-1}$) in log scale for V_{DS} of 50 V and V_{GS} of 5 V.

The impact ionization generation rates across a lateral cutline in the device in Fig. 2.10 show that even at a large bias of V_{DS}=50V, the EHPs generated is about $6\times10^{24}s^{-1}cm^{-3}$, which is much lower than the rates for higher V_{GS}, shown in next section.

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Figure 2.10: Impact ionization rates across Y=0.3 μm lateral cutline of the device obtained from MEDICI at V_{GS}= 5V and V_{DS}= 5V, 10V, 20V, 30V, 40V and 50V.
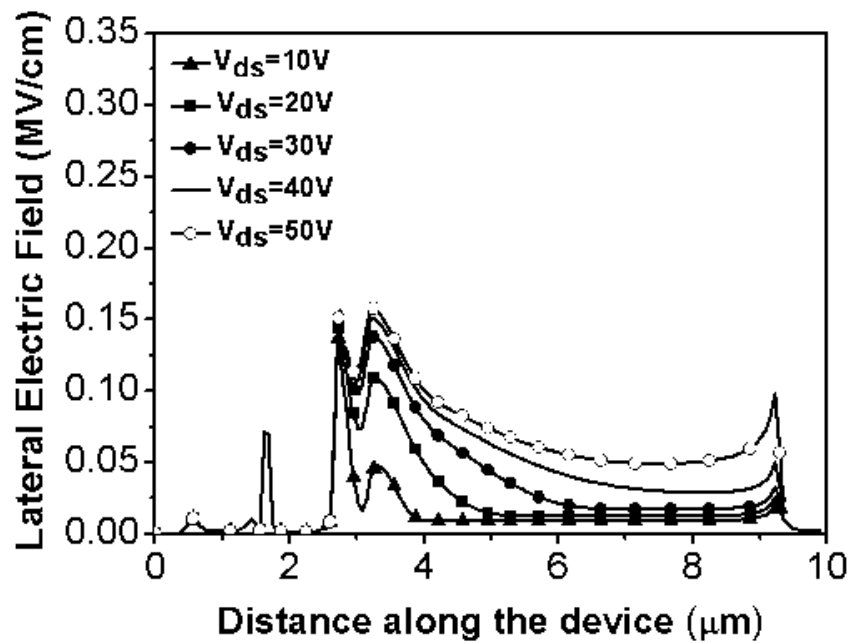
Figure 2.11: MEDICI simulations of electric field strength at Y=0.3 μm lateral cut line at V_{DS}= 10V, 20V, 30V, 40V and 50V and V_{GS}=5V.

Since at lower V_{GS}, the channel current is not sufficiently large enough to cause significant impact ionization, snapback effect is noticeably absent or occurs at very high V_{DS}. The electric field distribution shown in Fig. 2.11 across a lateral cutline in the device shows that even though the field peaks near the channel-drift region junction, this field, together with low MOSFET current is insufficient to generate significant substrate current that can turn on the BJT.
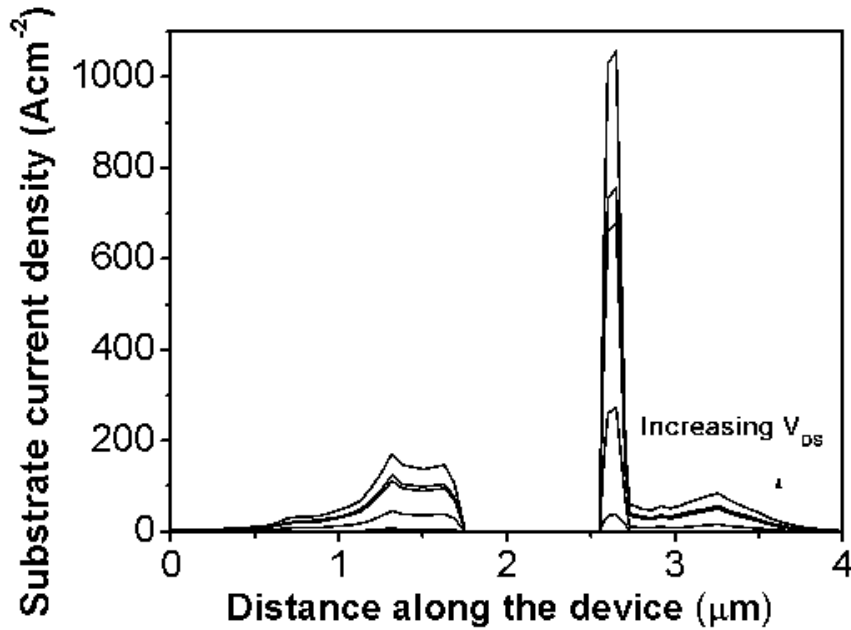
Figure 2.12: MEDICI simulations of substrate current density at Y=0.3 μm lateral cut line at V_{DS}= 10V, 20V, 30V, 40V and 50V and V_{GS}=5V.

The substrate current density shown in Fig. 2.12, across the same cutline as in Fig. 2.11, also peaks at Reg-I-Reg-II interface confirming that impact ionization occurs in this region of the device. The low substrate current density also reiterates the hypothesis that impact ionization is insufficient to cause snapback in low V_{GS} regime.

2.3.2 High V_{GS}

At higher V_{GS}, most of the applied voltage is dropped across Reg-III as conductivities of both Reg-I and Reg-II are very high. The current saturates due to quasi-saturation in Reg-III and not due to Reg-I. Thus, high lateral electric field is present in Reg-III near the drain contact. The impact ionization contours depicting the electron hole pair generation rate (EHPs $cm^{-3}s^{-1}$) in Fig. 2.13 show that impact ionization mostly occurs in Reg-III near drain contact (Region in red in the Figs. 2.13 and 2.14), even at low V_{DS}.
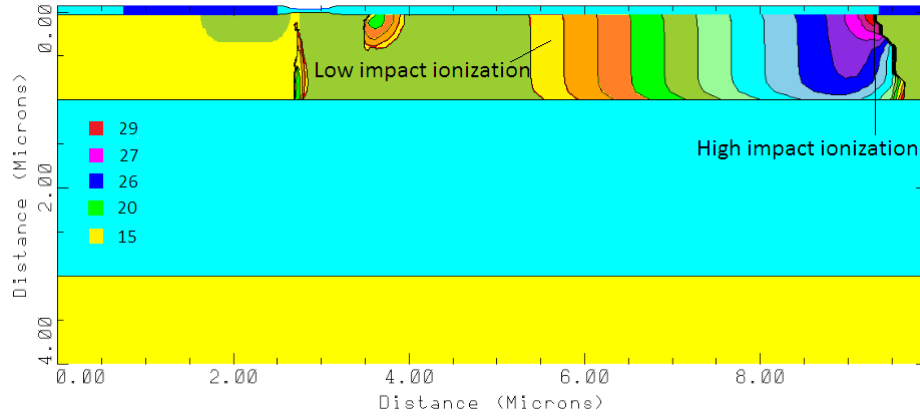
Figure 2.13: Impact ionization contours (EHPs $cm^{-3}s^{-1}$) in log scale, at V_{DS} of 20 V and V_{GS} of 15 V in pre-snapback region.
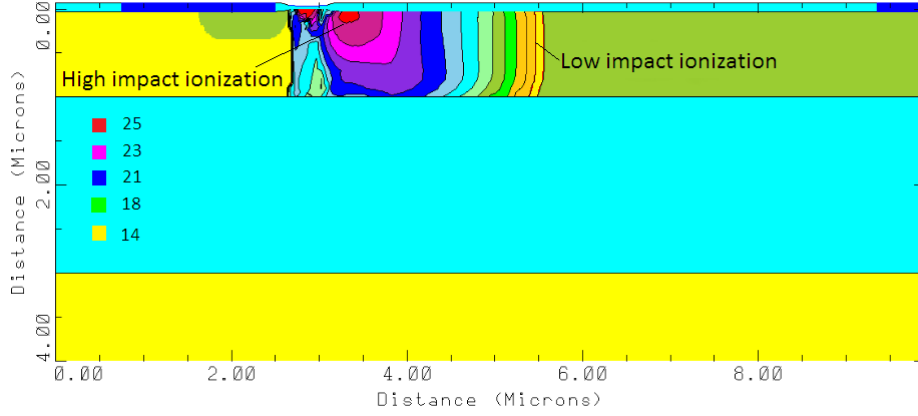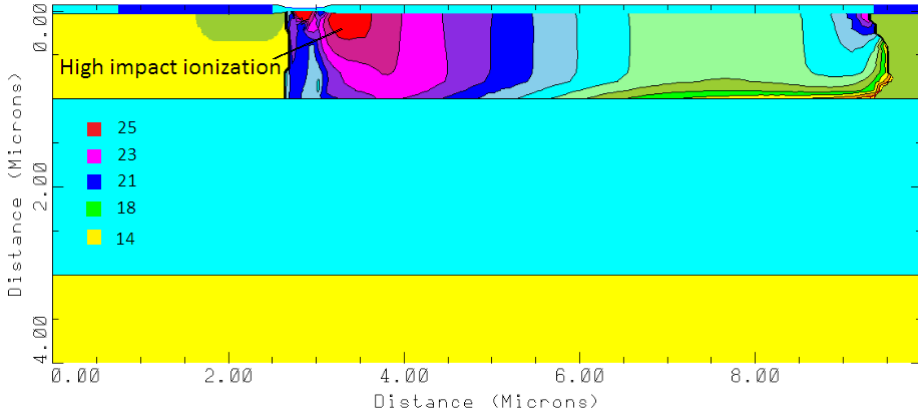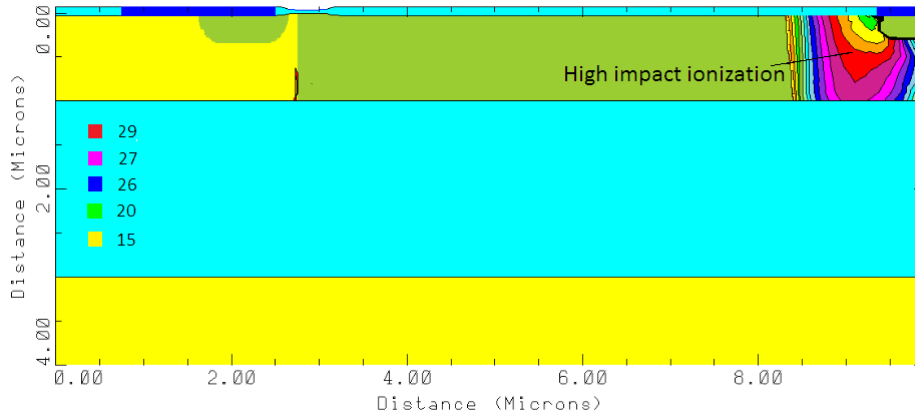

Figure 2.14: Impact ionization contours (EHPs $cm^{-3}s^{-1}$) in log scale for V_{DS} of 20 V and V_{GS} of 15 V in post-snapback region.

As V_{DS} is increased, in the high V_{GS} regime, carrier velocity saturation occurs in the drift region under field oxide resulting in quasi-saturation of current. This current is large enough to cause impact ionization at higher V_{DS} and produces secondary hole

current in the p-well, which turns on the npn BJT and snapback is observed. Due to snapback, for each applied V_{DS} there are two solutions for total drain current, namely pre-snapback (SOL1) solution and post-snapback (SOL2) solution. The transfer current of the parasitic BJT becomes the major component of drain current in SOL2 regime. At such high current levels, there is the well known base push-out or Kirk effect which causes the depletion region in drift layer to be pushed closer to drain contact. Thus the electric field in the drift region near the drain increases heavily and impact ionization rises drastically. The area over which there is substantial impact ionization is pushed closer to $n - n^+$ interface as shown in Fig. 2.14.
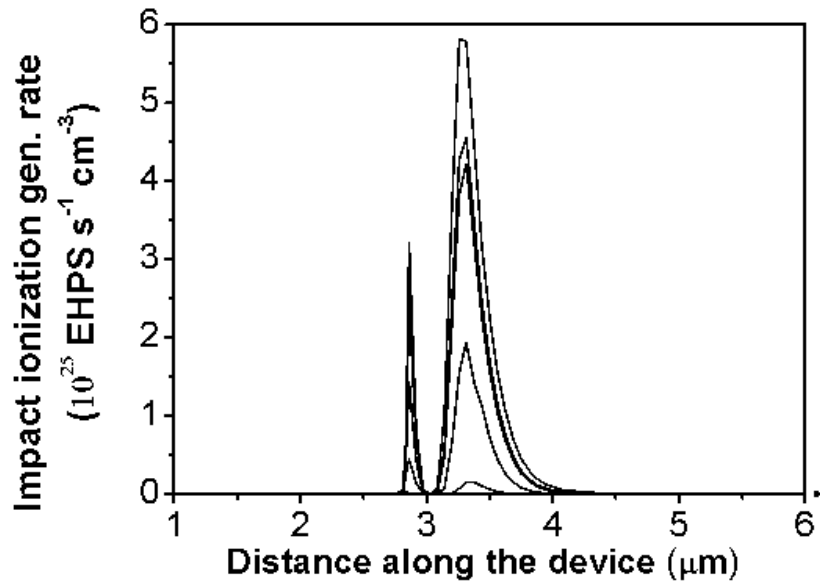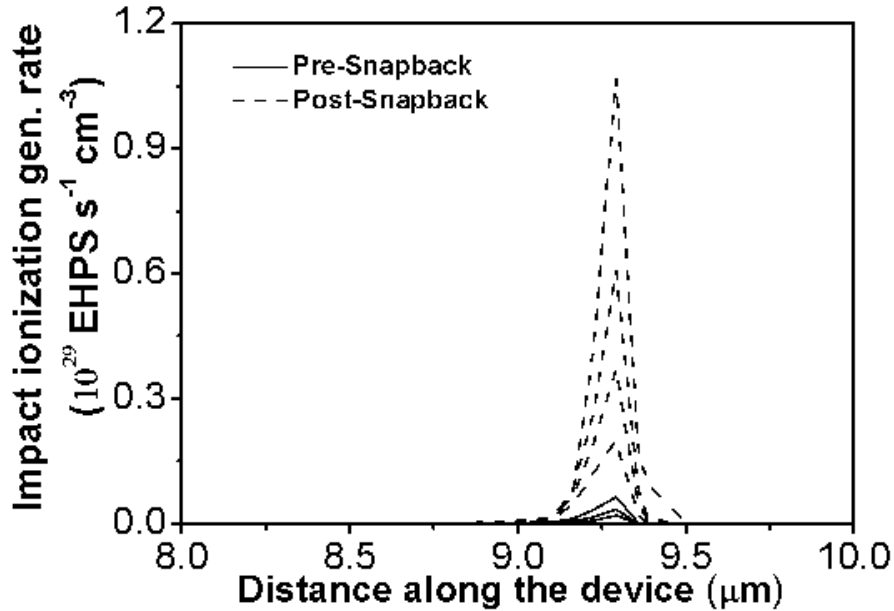

Figure 2.15: Impact ionization rates across Y=0.3 μm lateral cutline of the device obtained from MEDICI at V_{GS}= 15V and V_{DS}= 5V, 10V, 20V, 30V and 40V in SOL1 and SOL2 regions.

The impact ionization generation rates across lateral cutline of the device, for high V_{GS} case, is shown in Fig. 2.15. Impact ionization is dominant near drain contact and the generation rates are of the order of $1 \times 10^{29} s^{-1} cm^{-3}$ which is much larger than that for low to moderate V_{GS}.

The peak electric field distribution is shown across the device along a lateral cutline in Fig. 2.16. The peak lateral electric field responsible for impact ionization is different for SOL1 and SOL2. The field corresponding to SOL2 is much higher than that

corresponding to SOL1 due to Kirk effect in SOL2 regime. Due to this effect, there is reduction in the effective drift length over which V_{DS} is dropped, leading to higher peak electric field and greater impact ionization. The electric field distribution in Fig. 2.16, is for bias points spanning both SOL1 and SOL2. From the figure, Kirk effect and the resulting rise in peak electric fields in SOL2 regime, compared to electric fields of SOL1, for the same V_{DS} can be clearly observed.
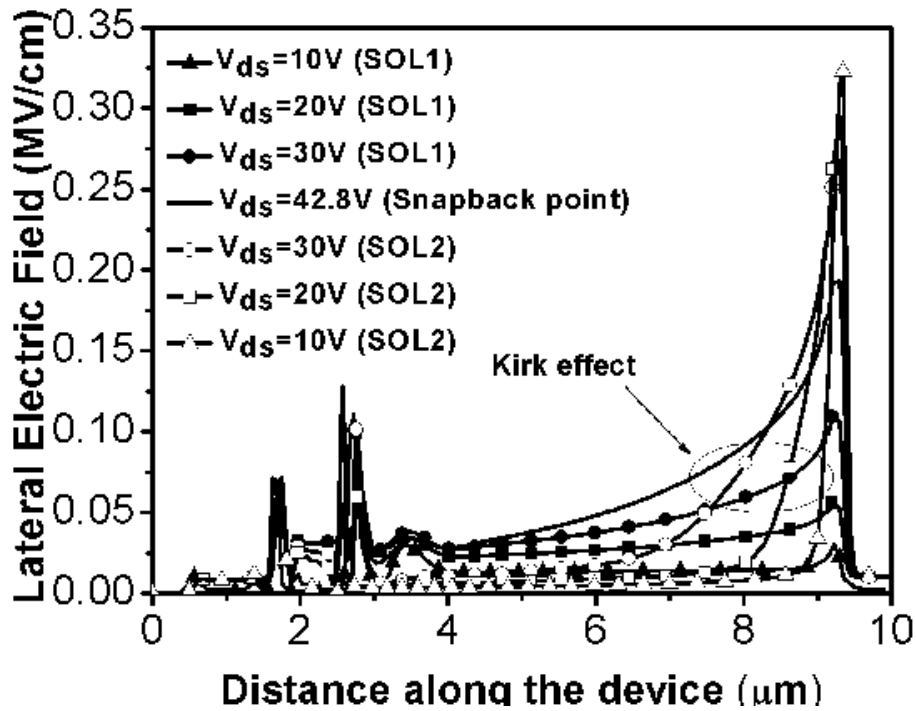
Figure 2.16: MEDICI simulations of electric field strength at Y=0.03 μm lateral cut line for V_{DS}= 10V, 20V, 30V and 42.8V for both SOL1 and SOL2 at V_{GS}= 15V .

Thus, even if applied V_{DS} is the same for SOL1 and SOL2 regimes, the peak electric field corresponding to SOL2 is much higher. i.e, For a given V_{DS}, even if area under the curve in Fig. 2.16 between X=4 μm and X=10 μm is the same for SOL1 and SOL2, the peak of the sawtooth-like electric field profile is higher for SOL2, as the base of the profile is much smaller in SOL2 due to Kirk effect. Since it is the peak electric field which governs the magnitude of substrate current and hence the transfer current of BJT (via V_{BS}), the output current of the device is higher for SOL2 even if V_{DS} is the same as in SOL1. The high value of the substrate current density responsible for forward biasing BE junction of the BJT is also shown along the cutline, in Fig. 2.17.
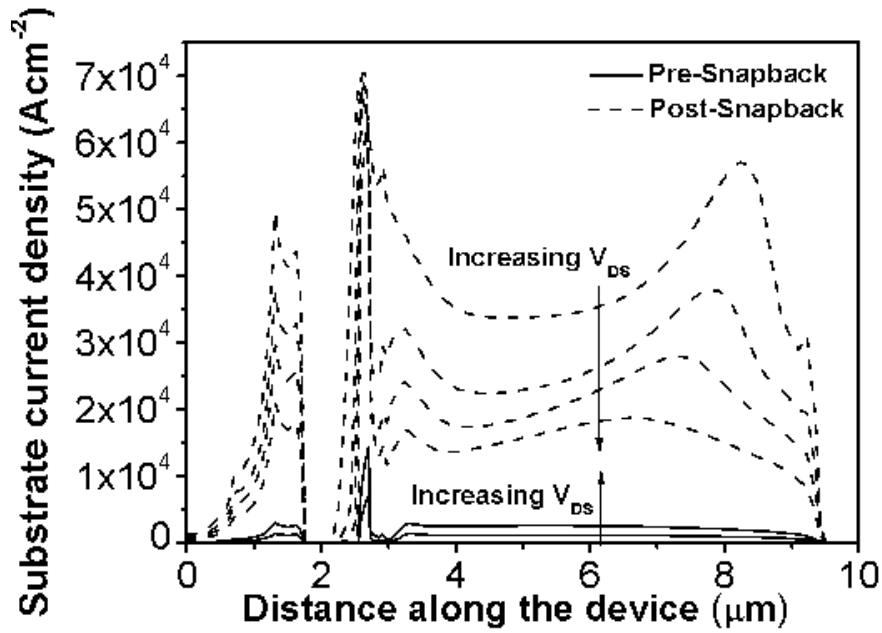
Figure 2.17: MEDICI simulations of substrate current density at Y=0.3 μm lateral cut line at V_{DS}= 10V, 20V, 30V and 40V (SOL1 and SOL2) and V_{GS}=5V.

2.4 Device self heating

High current densities in LDMOS devices result in considerable power dissipation, which coupled with low thermal conductivity of buried oxide leads to significant temperature rise. Due to this, the output current in SOL1 reduces with increasing V_{DS}, yielding a negative differential resistance. This is because carrier mobility reduces due to lattice scattering and threshold voltage increases with temperature. As power dissipation and temperature, increase with V_{DS}, the output MOSFET current reduces. Bipolar junction transistors on the other hand are known to suffer from the problem of thermal runaway which results in increased currents with temperature. Thus snapback is initiated by the parasitic BJT at much lower voltages and at lower current levels due to self heating. There is reduction in $V_{Snapback}$ with temperature and so the SOA decreases due to self-heating.

The temperature distribution in the device under high snapback condition is shown in Fig. 2.18. Here X-axis spans the length of the device from source to drain electrode and Y-axis is along the depth of the device spanning from active silicon film to BOX

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until substrate. The substrate is taken to be the thermal electrode for the purpose of sim-
ulation as it reflects the actual scenario where the top surface of the device is thermally
insulated, while cooling is ensured from substrate. As can be seen, the peak tempera-
ture occurs at drain electrode near the field oxide and falls along the drift region from
drain to source. The temperature falls inside the BOX ($1\mu m < Y < 3\mu m$) until it reaches
room temperature of 300K in the substrate.
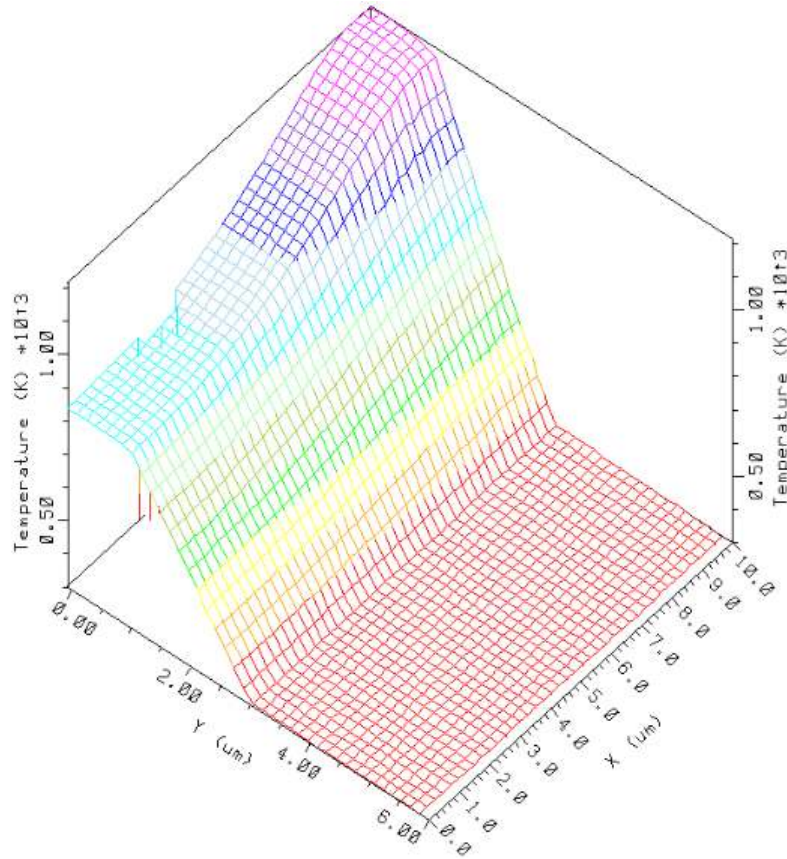
Figure 2.18: Typical temperature distribution in the device in snapback region; V_{DS}=
10V and V_{GS}= 15V.

Fig. 2.19 gives the temperature variation with bias, spanning both SOL1 and SOL2
across a lateral cutline in the device. It can be observed from Fig. 2.19 that in SOL1, the
temperature rise is more or less uniform throughout the length of the device. MOSFET
currents active in SOL1 are thus affected by thermal resistances corresponding to Reg-I,
Reg-II and Reg-III and must be taken into account in the thermal network model. In
SOL2, the temperature distribution is non-uniform, with temperature peaking at drain
electrode. This is valid, considering the current density and potential drop is highest
near the drain contact in SOL2 which results in huge power dissipation in the region.

The BJT currents dominating total current in SOL2 are thus influenced mainly by thermal resistance corresponding to Reg-III and are modeled accordingly in the thermal network, used to model self-heating.
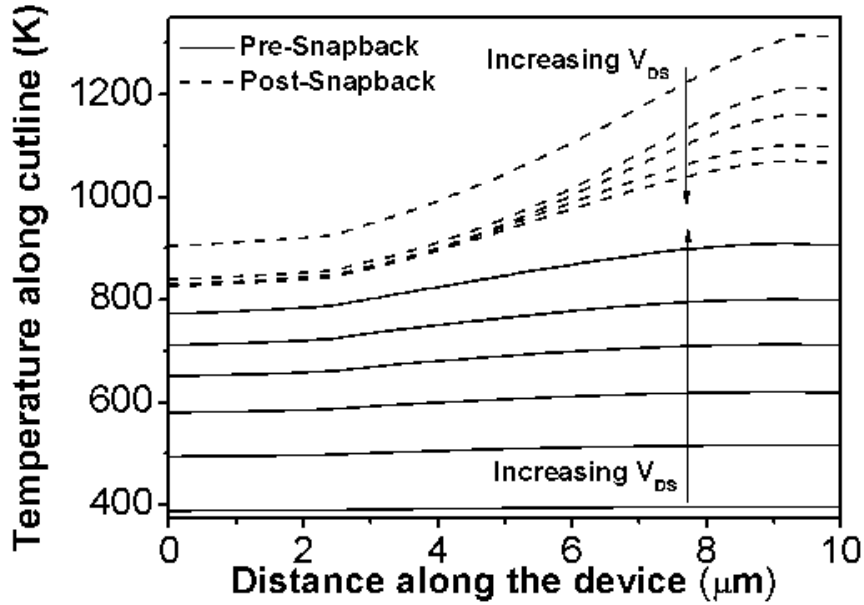
Figure 2.19: MEDICI simulations of temperature at Y=0.5 μm lateral cut line at V_{DS}= 10V, 20V, 30V and 40V (SOL1 and SOL2) and V_{GS}=15V.

From the analysis carried out in this chapter, the following conclusions can be made. These observations are taken into account while developing a comprehensive model for SOI-LDMOS in chapter 3.

- MOSFET current saturation is due to velocity saturation in Reg-I at lower V_{GS} and due to quasi-saturation at higher V_{GS}.

- Impact ionization is not high enough to cause rise in current levels at lower V_{GS} but is significant at higher V_{GS} and generates sufficient substrate current to turn on the parasitic BJT. The BJT transfer current increases even if V_{DS} is reduced in SOL2 due to Kirk effect and this is the reason for snapback.

- Device self-heating in SOL1 is in all 3 regions due to MOSFET currents, while in SOL2 it is highest in Reg-III due to BJT currents.

CHAPTER 3

MODEL AND VERILOG-A IMPLEMENTATION

A comprehensive model for any device must be capable of describing device performance over wide range of biases, temperatures and device geometries. SOI-LDMOS forms an integral part of HVICs used for automotive and consumer applications and hence accurate modeling of these devices is essential for fail-safe design of HVIC circuits.

Any LDMOS model should have following features.

- Accurate modeling of AC/DC terminal currents and nodal charges in linear, saturation and off modes.

- Continuity in device models over different regions and continuity in their derivatives.

- Capability to model impact ionization in drift region.

- Capability to model snapback and in turn predict SOA.

- Capability to model self heating which requires temperature dependence of model quantities.

- Scalability over wide range of bias, geometries and temperatures.

- Modeling various types of noise i.e. 1/f noise, thermal noise etc.

- Conservative nature of charge model.

- Accurate modeling of capacitances required to model dynamic behavior.

In this chapter, a new comprehensive static model for SOI-LDMOS is presented. The developed model is a compact model and thus has reduced number of internal nodes which are solved in the model itself. Device unity is retained by using a set of

self-consistent expressions to model device behaviour. The model incorporates surface potential based approach to model MOS transistor current including quasi-saturation in drift region. It takes into account of impact ionization in drift region to model parasitic BJT activation and resulting snapback. It also models temperature scaling and device-self heating. The equations describing device behavior are functions of terminal voltages and hence the device behavior is accurately described in all regions of operation namely accumulation, depletion, weak inversion and high current regime.

3.1   Model for static MOSFET currents

In the low bias regime, only MOSFET behavior is dominant as both impact ionization and device self heating are negligible. The MOSFET current is affected by Reg-I, Reg-II and Reg-III of the device. From the analysis carried out in section 2.2 of chapter 2, it is clear that Reg-I is responsible for current saturation at lower V_{GS} and quasi-saturation in Reg-III is responsible for current saturation at high V_{GS}. Potential drops across individual regions were explained in section 2.2 of chapter 2. The MOSFET current model to explain these observations are given in this section.
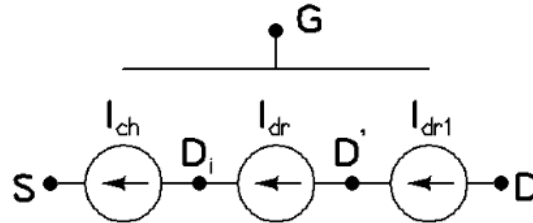
Figure 3.1: EC model for static MOSFET currents.

The MOSFET current is modeled using three current sources [31] as shown in Fig. 3.1. Here, I_{ch} is the current in the channel which is a function of the potential drop across channel, given by V_{DiS}. The potential drop across Reg-II is given by $V_{D'Di}$ and it determines the current through Reg-II, given by I_{dr}. The current through Reg-III is I_{dr1}, which is determined by potential drop across Reg-III, given by $V_{DD'}$. Each of the current source models is explained in following sub-sections.

3.1.1 Formulation of channel current

Channel current in Reg I is modeled using a surface potential based approach. The current has drift and diffusion components given by

$$I_{ch} = \frac{W \mu_{ch}}{L_{ch}} \left(\int_{\psi_{s,0}}^{\psi_{s,L}} (-Q_{inv}) d\psi_s + V_T (Q_{inv,L} - Q_{inv,0}) \right) \tag{3.1}$$

where W is channel width, μ_{ch} is channel mobility taking into effect of mobility reduction due to lateral and vertical electric fields. Channel length is given by L_{ch}, ψ_s is surface potential, V_T is thermal voltage and Q_{inv} is inversion layer charge per unit area which is given as $Q_{inv} = -C_{ox} V_{inv}$ with $Q_{inv,L}$ and $Q_{inv,0}$ being its values at drain and source side respectively. Inversion potential V_{inv} is given by

$$V_{inv} = V_{GB} - V_{FB,ch} - \psi_s - k_o \sqrt{\psi_s}. \tag{3.2}$$

Here, $V_{FB,ch}$ is the channel flat band voltage, V_{GB} is the applied gate to substrate voltage, k_o is body effect coefficient in Reg-I. This V_{inv} is approximated by Taylor series expansion around $\psi_s = \psi_{s,0}$ for simplicity and is written as

$$V_{inv} = V_{inv,0} - \zeta (\psi_s - \psi_{s,0}) \tag{3.3}$$

with $\zeta = \left(1 + \frac{k_o}{2\sqrt{\psi_{s,0}}} \right)$ and inversion potential at source side is given by

$$V_{inv,0} = V_{inv}|_{\psi_s=\psi_{s,0}} = V_{GB} - V_{FB,ch} - \psi_{s,0} - k_o \sqrt{\psi_{s,0}} + m_{DIBL} V_{DiS} \tag{3.4}$$

where $\psi_{s,0}$ is the surface potential at source side and is given by $\psi_{s,0} = 2V_T ln \left(\frac{N_{ch}}{n_i} \right)$, N_{ch} is doping concentration of channel. m_{DIBL} accounts for drain induced barrier lowering in the short channel of SOI-LDMOS. Using (3.2), (3.3) and (3.4), (3.1) can be simplified as

$$I_{ch} = \frac{W \mu_{ch} C_{ox}}{L_{ch}} \left(V_{inv,0} - \frac{1}{2} \zeta \nabla \psi_s + \zeta V_T \right) \nabla \psi_s \tag{3.5}$$

where $\nabla \psi_s = \psi_{s,L} - \psi_{s,0}$. The mobility reduction due to lateral electric field which accounts for velocity saturation is given by [33]

$$\mu_{ch} = \frac{\mu_{eff,ch}}{(1 + \theta_{3,ch} \nabla \psi_s)} \tag{3.6}$$

where $\theta_{3,ch} = \frac{\mu_{0,ch}}{L_{ch} v_{sat}}$ is the parameter which takes account of velocity saturation in channel, with v_{sat} being the saturation velocity in channel and $\mu_{0,ch}$ being the zero field mobility. $\mu_{eff,ch}$ accounts for mobility reduction due to vertical field and is given by [33]

$$\mu_{eff,ch} = \frac{\mu_0}{\left(1 + \theta_1 V_{inv,0} + \theta_2 \left(\sqrt{\psi_{s,0}} - \sqrt{\psi_{s,0}|_{V_{SB}=0}}\right)\right)} \tag{3.7}$$

with θ_1 and θ_2 taken as model parameters. Substituting (3.6-3.7) in (3.5) and replacing $\nabla \psi_s = \psi_{s,L} - \psi_{s,0}$ by V_{DiS}, gives the channel current as

$$I_{\text{ch}} = \frac{W \mu_{\text{ch}} C_{\text{ox}}}{L_{\text{ch}}} \left(V_{inv,0} - 0.5\zeta V_{DiS} + \zeta V_T\right) V_{DiS}. \tag{3.8}$$

This current model is till the onset of channel saturation. To model saturation, the channel saturation potential is computed from $\frac{\delta I_{Ch}}{\delta V_{DiS}}|_{V_{DiS}=V_{sat,ch}} = 0$. This gives the channel saturation potential ($V_{sat,ch}$) as

$$V_{sat,ch} = \frac{\frac{2V_{inv,0}}{\zeta}}{1 + \sqrt{1 + \frac{2\theta_{3,ch} V_{inv,0}}{\zeta}}}. \tag{3.9}$$

The final expression of channel current that is used by the model then becomes

$$I_{\text{ch}} = (1 + \lambda_{ch} V_{DiS}) \frac{W \mu_{\text{eff,ch}} C_{\text{ox}}}{L_{\text{ch}}} \frac{(V_{inv,0} - 0.5\zeta V_{DiS,eff} + \zeta V_T) V_{DiS,eff}}{(1 + \theta_{3,ch} V_{DiS,eff})} \tag{3.10}$$

where λ_{ch} is the channel length modulation parameter and $V_{\text{DiS,eff}}$ is effective potential drop across channel which is the minimum of V_{DiS} and $V_{sat,ch}$. The diffusion component of channel current in the model is significant in sub-threshold regime.

3.1.2 Formulation of current in drift region under gate oxide

Reg-II current unlike Reg-I current is dominated by drift current and hence the diffusion component is neglected. The drift current in Reg-II can then be written as

$$I_{dr} = \frac{W\mu_{dr}}{L_{dr}} \int_{V_{D'}}^{V_{Di}} (-Q_n^{dr}) dV_c \qquad (3.11)$$

where W is drift region width, μ_{dr} is Reg-II mobility taking into effect of mobility reduction due to lateral and vertical electric fields. L_{dr} is length of Reg-II. Like in Reg-I, Reg-II also undergoes velocity saturation due to lateral electric field, however in addition there is accumulation condition created because of vertical electric field due to V_{GS}. This is accounted in Q_n^{dr} which is the total drift region charge in Reg-II per unit area including both depletion and accumulation components and is given by

$$-Q_n^{dr} = qN_{dr}t_{si} - Q_{acc}^{dr} - Q_{dep}^{dr} \qquad (3.12)$$

where N_{dr} is Reg-II doping concentration, t_{si} is silicon film thickness, Q_{acc}^{dr} is the accumulation charge per unit area valid for $V_{GC} > V_{FB,dr}$ and is given by

$$Q_{acc}^{dr} = -C_{ox}(V_{GC} - V_{FB,dr}) \qquad (3.13)$$

and Q_{dep}^{dr} is the depletion charge per unit area valid for $V_{GC} < V_{FB,dr}$ and is given by

$$Q_{dep}^{dr} = k_{dr}C_{ox}\left(-0.5k_{dr} + \sqrt{(0.5k_{dr})^2 - (V_{GC} - V_{FB,dr})}\right) \qquad (3.14)$$

where $V_{FB,dr}$ is the flatband voltage of Reg-II, V_{GC} is the voltage drop between gate and Reg-II and k_{dr} is the body effect coefficient in Reg-II. The mobility reduction due to lateral and vertical fields is modeled akin to that of channel mobility reduction as [33]

$$\mu_{dr} = \frac{\mu_{eff,dr}}{(1 + \theta_{3,dr}V_{D'Di})} \qquad (3.15)$$

where $\theta_{3,dr} = \frac{\mu_{0,dr}}{L_{dr}v_{sat}}$ is the parameter which takes account of velocity saturation in Reg-II, with v_{sat} being the saturation velocity and $\mu_{0,dr}$ being the zero field mobility.

$\mu_{eff,dr}$ accounts for mobility reduction due to vertical field and is given by [33]

$$\mu_{eff,dr} = \frac{\mu_{0,dr}}{(1 + \theta_{acc}(0.5V_{GS} + 0.5V_{GD'} - V_{FB,dr}))} \qquad (3.16)$$

with θ_{acc} taken as model parameter. Substituting (3.10-3.14) in (3.9) gives the Reg-II current as

$$I_{dr} = \frac{W\mu_{dr}C_{ox}}{L_{dr}} \left(V_n^{dr}|_{V_c=V_{Di}} - 0.5V_{D'Di}\right) V_{D'Di} \qquad (3.17)$$

which is obtained by Taylor series expansion of V_n^{dr} similar to the expansion of channel inversion potential in previous section. Here, $V_n^{dr} = -\frac{Q_n^{dr}}{C_{ox}}$ and for $V_{GDi} > V_{FB,dr}$ is given by

$$V_n^{dr}|_{V_c=V_{Di}} = \frac{qN_{dr}t_{si} - Q_{acc}^{dr}|_{V_c=V_{Di}}}{C_{ox}}. \qquad (3.18)$$

For $V_{GDi} < V_{FB,dr}$ it is given by

$$V_n^{dr}|_{V_c=V_{Di}} = \frac{qN_{dr}t_{si} - Q_{dep}^{dr}|_{V_c=V_{Di}}}{C_{ox}}. \qquad (3.19)$$

This current model is till the onset of saturation. To model saturation, the drift saturation potential is computed from $\frac{\delta I_{dr}}{\delta V_{D'Di}}|_{V_{D'Di}=V_{sat,dr}} = 0$. This gives the Reg-II saturation potential ($V_{sat,dr}$) as

$$V_{sat,dr} = \frac{2V_n^{dr}|_{V_c=V_{Di}}}{1 + \sqrt{1 + 2\theta_{3,dr}V_n^{dr}|_{V_c=V_{Di}}}}. \qquad (3.20)$$

The final expression of Reg-II current that is used by the model is

$$I_{dr} = \frac{W\mu_{eff,dr}C_{ox}}{L_{dr}} \frac{\left(V_n^{dr}|_{V_c=V_{Di}} - 0.5V_{D'Di,eff}\right) V_{D'Di,eff}}{\left(1 + \theta_{3,dr}V_{D'Di,eff}\right)} \qquad (3.21)$$

where $V_{\text{DiS,eff}}$ is effective potential drop across Reg-II which is the minimum of $V_{D'Di}$ and $V_{sat,dr}$.

3.1.3 Formulation of current in drift region under field oxide

Although the drift region under field oxide shows resistive behavior under low gate voltages, at higher gate voltages velocity saturation occurs in this region resulting in

quasi-saturation. Due to quasi-saturation, the saturation current levels do not increase with further increase in V_{GS}. After the onset of quasi-saturation, drift length modulation also takes place resulting in increase in current with drain voltage. These effects are taken into consideration in the drift current formulation given by

$$I_{\mathrm{dr1}} = \frac{\left(1 + \lambda_{dr1} V_{DD'}\right) q N_{dr1} \mu_{\mathrm{dr1}} V_{DD'} W t_{\mathrm{si}}}{L_{LC} \left(1 + \theta_{l,dr1} \left(\frac{V_{DD'}}{L_{LC} E_C}\right)^{\theta_{dr1}}\right)^{1/\theta_{dr1}}} \tag{3.22}$$

where μ_{dr1} is effective mobility, N_{dr1} is drift layer doping concentration, $V_{DD'}$ is effective potential drop across the drift region and t_{si} is effective thickness of this region. The drift length modulation parameter is given by λ_{dr1}. The critical field at velocity saturation is given by $E_C = \frac{v_{\mathrm{sat}}}{\mu_{\mathrm{dr1}}}$. Model parameters $\theta_{l,dr1}$ and θ_{dr1} account for velocity saturation in the region.

The expressions for currents I_{ch}, I_{dr} and I_{dr1} derived in (3.10),(3.21) and (3.22) are used in the model circuit shown in Fig. 3.1. Since the current sources in the circuit are in series, at any given bias, the currents must converge to the same value. Hence, the MOSFET current (I_{MOS}) at any bias is equal to I_{ch}, I_{dr} or I_{dr1}. The potential drops across Reg-I, Reg-II and Reg-III, given by V_{DiS}, $V_{D'D_i}$ and $V_{DD'}$ respectively get adjusted such that I_{ch}, I_{dr} and I_{dr1} have the same value in accordance with equations (3.10),(3.21) and (3.22).

3.2 Model for static parasitic BJT currents

The parasitic lateral BJT in SOI-LDMOS is primarily responsible for snapback. So model formulation of SOI-LDMOS is incomplete without including it in the model. From the analysis carried out in section 2.3 of chapter 2, it is clear that n^+ source, p-well and n drift region constitute the lateral parasitic npn BJT (Refer Fig. 2.7). Since the p-well forming the base of the BJT is sufficiently wide, the BJT has low current gain. Nonetheless, even this low gain BJT is sufficient to sustain large transfer current which dominates the total output LDMOS current in the snapback regime. The p well - n drift region junction forming the BC junction of the BJT is reverse biased due to

applied V_{DS} and the BE junction formed between p well-n^+ source, is forward biased by the potential drop in p-well due to substrate hole current flowing through it. Thus the BJT is driven into forward active mode due to impact ionization in the snapback regime.
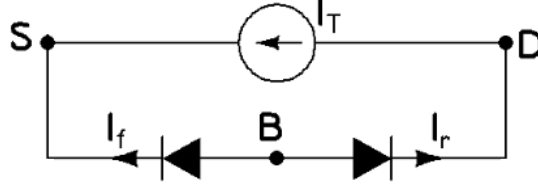
Figure 3.2: EC model of parasitic BJT.

The BJT is modeled using a simple equivalent circuit containing a transfer current source and two diode elements as shown in Fig. 3.2 The node B in the circuit of Fig. 3.2 corresponds to the p-well - n drift region junction. The source of LDMOS transistor is also the emitter of the parasitic BJT. Hence in Fig. 3.2, the emitter terminal corresponds to source node S, which is the same node S in Fig. 3.1. Similarly collector terminal corresponds to node D, which is the same node D in Fig. 3.1. The forward diode current (I_f) in Fig. 3.2, is given by the well known diode equation

$$I_{\mathrm{f}} = \frac{Aqn_i^2 V_T \mu_{pw}}{N_{pw} L_{pw}} \left(e^{\frac{V_{BS}}{m_p V_T}} - 1 \right) \tag{3.23}$$

where μ_{pw} is the mobility in p-well region, N_{pw} is doping of p-well and L_{pw} is effective length between p-well-n drift junction and body contact, A is the device area, V_{BS} is the voltage difference between base and source nodes. Here since n^+ source is heavily doped, diffusion component due to this region is neglected. The reverse diode current (I_r) is similarly given by

$$I_{\mathrm{r}} = \frac{Aqn_i^2 V_T \mu_{dr}}{N_{dr} L_{dr}} \left(e^{\frac{V_{BD}}{m_{dr} V_T}} - 1 \right) \tag{3.24}$$

where μ_{dr} is mobility in n drift region, N_{dr} is doping of n drift region, L_{dr} is effective length between p-well-n drift junction and drain contact and V_{BD} is the voltage difference between p-well base and drain nodes. For almost the entire device operation region, this current can be neglected as V_{BD} is negative because of reverse biased BC junction for LDMOS operation.

Transfer current is modeled by the Moll-Ross relation as

$$I_T = \beta_f I_f - \beta_r I_r \qquad (3.25)$$

where β_f and β_r are forward and reverse current gains which need to be extracted from device simulation data. It is this I_T that is the major component of output current through the drain electrode after impact ionization and subsequent snapback set in. The substrate current which turns on the BJT is generated due to impact ionization which is modeled in the next section.

3.3   Model for impact ionization
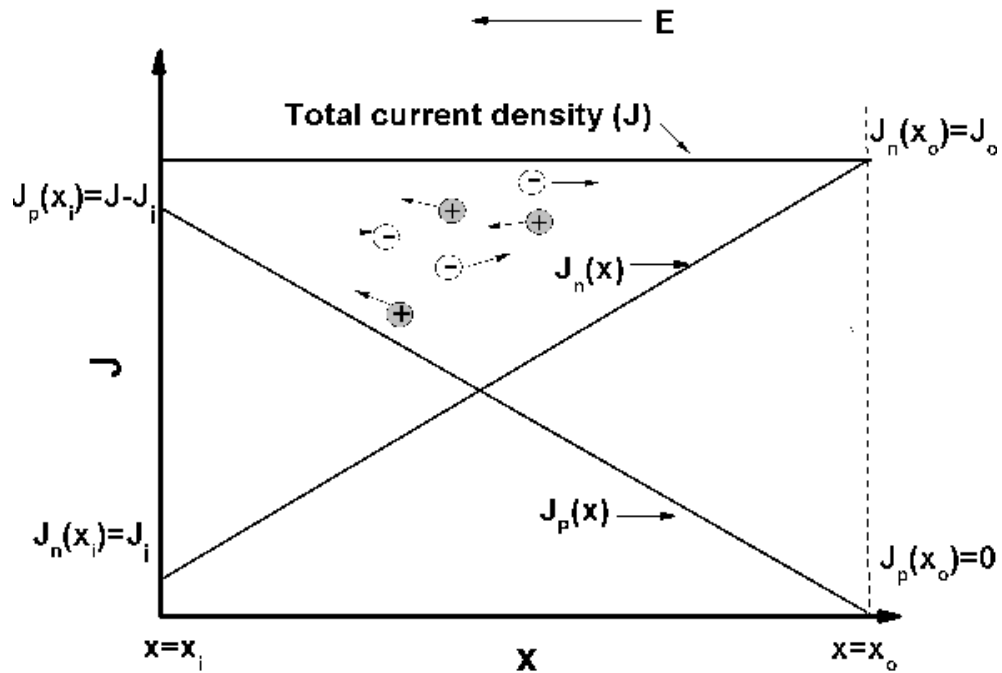
Figure 3.3: Illustration of impact ionization phenomenon in space charge region in drift region of LDMOS transistor.

From the analysis of impact ionization in section 2.3 of chapter 2, it can be inferred that at high V_{GS}, there is significant impact ionization in Reg-III near the drain contact. Impact ionization leads to rise in drain current levels and ultimately causes snapback. At sufficiently large V_{DS}, high energy electrons moving through space charge layer (SCR)

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of the drift region, under the influence of electric field collide with valence band electrons. These valence band electrons gain sufficient energy to move to conduction band thereby creating EHPs. This process builds up due to subsequent collisions, resulting in an avalanche like phenomenon. The resulting current is many times greater than the current which initiates the avalanche process. The multiplication factor is defined for each type of carrier as the ratio of output current density of that carrier, leaving avalanche region to the input current density of that carrier, entering the region. For electrons, which in the present case initiate impact ionization, it is given by (Refer Fig. 3.3)

$$M = \frac{J_{\mathrm{o}}}{J_{\mathrm{i}}}. \tag{3.26}$$

If α is the probability that one new EHP is created over an interval dx due to a carrier collision, then αndx and αpdx are absolute number of electrons and holes created in the interval [37]. Here α_{n} and α_{p} are assumed equal for simplicity. Due to impact ionization, the increase in electron current density over a region dx in the drift space charge region is given by [37]

$$dJ_n = \alpha q(v_p p dx - v_n n dx) \tag{3.27}$$

where v_p and v_n are electron and hole velocities in SCR. Since $J_p(x) = qv_p p$ and $J_n(x) = -qv_n n$, (3.27) can be rewritten as

$$dJ_n = \alpha(J_p(x) + J_n(x))dx = \alpha J dx. \tag{3.28}$$

The total current density is spatially independant and hence spacial integration yields

$$J_{\mathrm{o}} - J_{\mathrm{i}} = J \int_{x_i}^{x_o} \alpha dx \tag{3.29}$$

where x_i and x_o define boundaries of avalanche region. From Fig. 3.3, $J_{\mathrm{o}} = J$ and $J_{\mathrm{i}} = \frac{J_{\mathrm{o}}}{M}$ from (3.26). The resulting expression then is

$$1 - \frac{1}{M} = \int_{x_i}^{x_o} \alpha dx. \tag{3.30}$$

The integration on LHS of (3.30) is quite small for weak avalanche and M can be approximated to be

$$M \approx 1 + \int_{x_i}^{x_o} \alpha dx. \tag{3.31}$$

The SOI-LDMOS under consideration has a reasonably large drift region. Thus it is valid to assume local impact ionization mechanism where instant acceleration of carriers occur at any given location x, due to the local field at that location E(x). This assumption is valid for long SCR cases like in the present case. Both local and non-local impact ionization models in MEDICI yielded the same results for the structure thus justifying the assumption. The ionization coefficient then is given according to Chynoweth's law [32] as

$$\alpha = a e^{-\frac{b}{|E(x)|}} \tag{3.32}$$

where values of parameters a and b are experimentally found to be $0.703 \times 10^6 cm^{-1}$ and $1.231 \times 10^6 V cm^{-1}$ respectively [32]. Using this expression for α and assuming weak avalanche process M is given by

$$M \approx 1 + \int_{x_i}^{x_o} a e^{-\frac{b}{|E(x)|}} dx. \tag{3.33}$$

From Fig. 2.16 in section 2.3 of chapter 2, it can be observed that the electric field profile in drift region is almost a sawtooth-like profile. The electric field peaks at one end of the depletion layer near the drain contact (x= 9 μm) and goes to zero at the other edge of the depletion region (x= 4 μm). Thus the electric field can be approximated to be

$$|E(x)| \approx E_P \left(\frac{x - x_i}{x_o - x_i}. \right) \tag{3.34}$$

Here, both the peak field (E_P), and the depletion layer width are functions of bias as will be explained shortly. Substituting (3.34) in (3.33) and upon simplification, M turns out to be

$$M = 1 + \frac{a}{b} V_{DS} e^{-\frac{b}{E_P}}. \tag{3.35}$$

With reference to Fig. 3.3, the electron current (I_i) entering the SCR at x_i in Reg-III which is the cause of avalanche process, is the sum of MOSFET current and transfer

current of BJT and is given by

$$I_i = I_{MOS} + I_T. \tag{3.36}$$

The avalanche substrate current shown in the EC model in Fig. 3.4, is the hole current leaving SCR at x_i as seen in Fig. 3.3 and is given by

$$I_{\text{AVL}} = (M - 1)(I_{\text{T}} + I_{MOS}) \tag{3.37}$$

where I_{MOS} is determined by I_{ch}, I_{dr} and I_{dr1}. This I_{AVL} is the substrate hole current which flows towards the p-well contact under the influence of the lateral electric field. As it flows through the resistive p-well region, it forward biases the BE junction of parasitic BJT. The p-well resistance R_B can be written as

$$R_B = \frac{L_{pw}\rho_{pw}}{A} \tag{3.38}$$

where ρ_{pw} is the resistivity of the p-well region and L_{pw} is effective length of p-well. current flowing through R_B forward biases BE junction of BJT and turns it on.

At high bias conditions, impact ionization gains significance and BE junction forward bias is sufficient to generate large I_T. High values of I_T, together with I_{MOS} inject large amount of carriers into n-drift region at the BC junction of the BJT. Thus the BC junction is pushed towards the drain end or p-well forming the base is pushed out. This is the well known Kirk effect common in BJTs under high injection conditions. Thus, the effective width of the depletion layer in drift region, reduces in SOL2, for the same V_{DS} as in SOL1 and E_P increases heavily. This large field in SOL2, prompts more impact ionization which increases BE junction forward bias and rises I_T. This is a self-sustaining cycle. Even if V_{DS} is reduced in SOL2 regime, I_T and hence I_D increases. This phenomenon is nothing but snapback. E_P still increases marginally in SOL2 regime due to the base push-out effect as can be seen from Fig. 2.16 of chapter 2.

For SOL1 regime, E_P in (3.35) is given by

$$E_P = \frac{2V_{DD'}}{L_{LC}} \tag{3.39}$$

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assuming a sawtooth-like electric field profile in the drift region. In SOL2, base push out effect becomes prominent. Thus the actual depletion layer width is much lesser than the length of Reg-III (L_{LC}) unlike in SOL1 regime. The actual depletion layer width is a complex function of I_D and V_{DS}. Therefore, E_P in (3.35) is modeled by a cubic polynomial in SOL2. E_P in SOL2 is given by

$$E_P = \frac{2V_{DD'}}{L_{LC,eff}} \tag{3.40}$$

where $L_{LC,eff}$ is effective depletion width in drift region which can be approximated as

$$L_{LC,eff} = L_{LC}\left(1 - \xi_0 \frac{\nabla V}{V_{snapback}}\right) \tag{3.41}$$

where $\nabla V = V_{snapback} - V_{DS}$ and ξ_0 is a constant. Equation (3.40) can then be approximated as

$$E_P = \frac{2V_{DS}}{L_{LC}}\left(1 + \xi_1 \frac{\nabla V}{V_{snapback}} + \xi_2 \left(\frac{\nabla V}{V_{snapback}}\right)^2\right) \tag{3.42}$$

where ξ_1 and ξ_2 are parameters to be extracted from device simulation data.
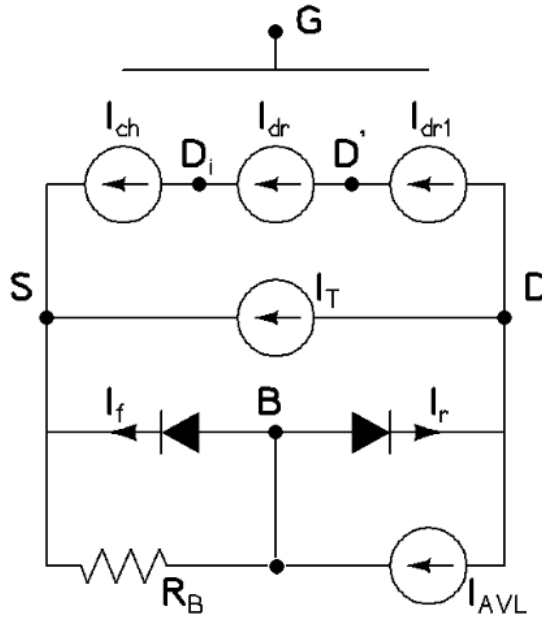

Figure 3.4: EC model of SOI-LDMOS to explain impact ionization and snapback.

The equivalent circuit (EC) model of SOI-LDMOS which can explain impact ionization and associated snapback is shown in Fig. 3.4. The LDMOS transistor action is modeled by the current sources I_{ch}, I_{dr} and I_{dr1} [31] as in the previous section 3.1.

The parasitic BJT is modeled as given in section 3.2 and impact ionization generated substrate current is modeled as described in this section.

Direct implementation of this circuit in model simulator like Verilog-A [34] will require an extra node (due to node 'B') than in [31] and will always converge to SOL1 for any V_{DS}, even when SOL2 is desired. To avoid this, voltage at node B (V_B) must be explicitly solved as will be shown in the next section.

3.4   Model implementation in Verilog-A

Implementation of the model is carried out in Verilog-A and tested using Spectre [35]. Any circuit simulator solves nodal equations assuming zero initial condition or takes the previous solution as initial condition. Thus, direct implementation of the EC in Fig. 3.4 in Verilog-A always yields SOL1 for any V_{DS}, while SOL2 is never obtained. This is because for any given V_{DS}, computation begins from zero bias condition and converges to SOL1 first. Once convergence is achieved, simulation stops, having encountered a valid solution. In order to make the simulator reach the second valid solution SOL2, the voltage at node B is found from Fig. 3.4 as

$$V_{BS} = R_B \left(I_{AVL} - I_{\text{f}} - I_r \right). \tag{3.43}$$

Substituting equations (3.23), (3.24) and (3.36) in (3.43) and upon further simplification, the above equation will be of the form

$$V_{BS} = C_1 + C_2 e^{\frac{V_{BS}}{V_T}} \tag{3.44}$$

where C_1 and C_2 ($C_1 \gg C_2$) are constants for a given external bias given by

$$C_1 = R_B(M - 1)I_{MOS}, \tag{3.45}$$

$$C_2 = R_B \left((M - 1)\beta_f - 1 \right) I_o \tag{3.46}$$

where I_o is the reverse saturation current of the forward biased diode as given in (3.23). (3.44) has two solutions, one corresponding to SOL1 and another corresponding to SOL2. This can be graphically visualized as shown in Fig. 3.5.
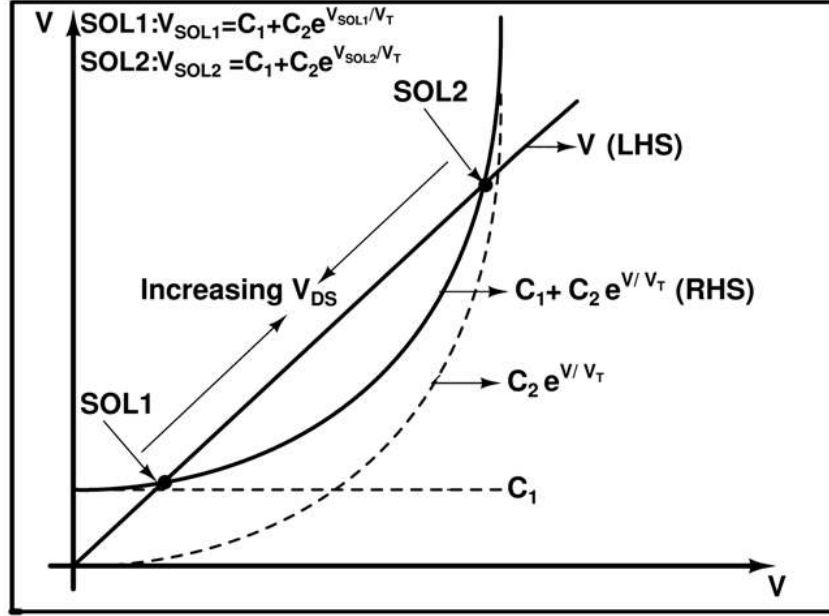
Figure 3.5: Graphical representation of solution of equation (3.44).

From Fig. 3.5, it can be observed that SOL1 solution is mainly determined by C_1. In SOL1 regime, as V_{DS} is increased from 0V upto $V_{snapback}$, I_{MOS} increases marginally and M increases due to impact ionization. Thus from (3.44), C_1 increases with V_{DS}. (This can also be noticed by comparing C_1 in Fig. 3.5 and Fig. 3.6.) This means that as V_{DS} is increased from 0V upto $V_{snapback}$, the solution point corresponding to SOL1, moves up along V(LHS) line as illustrated in Fig. 3.5.

As V_{DS} is reduced from $V_{snapback}$ to lower voltages in SOL2 regime, E_P increases only marginally as shown in Fig. 2.16 of chapter 2 and given by (3.42). Then, from (3.35), M reduces as V_{DS} is reduced from $V_{snapback}$ to lower voltages. In other words, as V_{DS} is increased from low values upto $V_{snapback}$, M increases. From (3.45), it implies that C_2 increases with V_{DS}. As C_2 increases with V_{DS}, the slope of the exponential $C_2 e^{\frac{V_{BS}}{V_T}}$, shown in Fig. 3.5 increases. (This can also be noticed by comparing the exponential in Fig. 3.5 and Fig. 3.6.) From Fig. 3.5, it can also be noticed that the solution point corresponding to SOL2, is mainly determined by this exponential. Since the slope of the exponential increases, it cuts V(LHS) line at lower voltages. Hence as V_{DS} is in-

creased, the solution point of SOL2, moves down along V(LHS) line as illustrated in Fig. 3.5.

Thus SOL1 and SOL2 solution points approach each other as V_{DS} is increased and at $V_{snapback}$, the two solutions become identical. This is illustrated in Fig. 3.6. Hence in the output characteristics of the device, there are two solutions for currents at any given $V_{DS} < V_{snapback}$. At $V_{snapback}$, the two currents are identical. From Fig. 3.6, it can also be visualized that beyond $V_{snapback}$, the curve $C_1 + C_2 e^{\frac{V_{BS}}{V_T}}$ (RHS) does not cut V(LHS) line. Thus, beyond $V_{snapback}$, there is no solution for drain current.
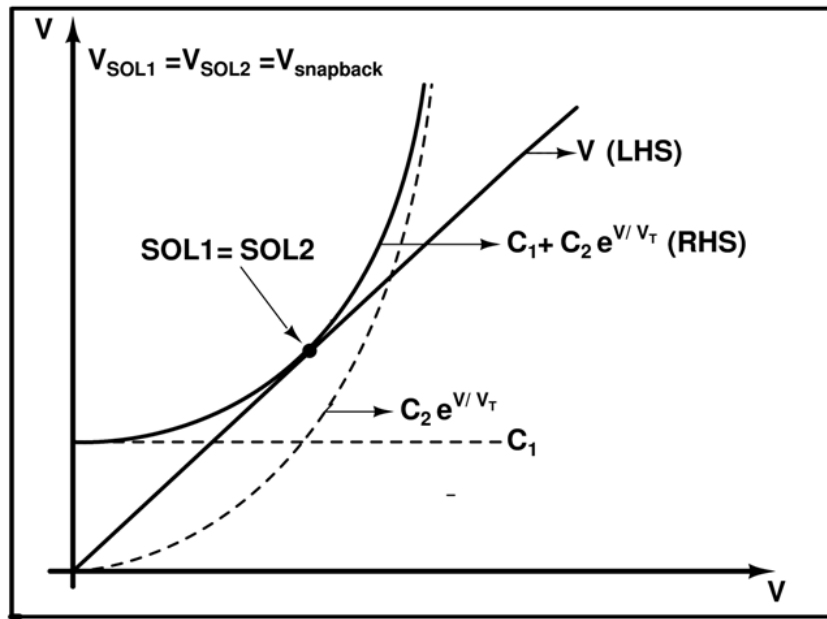
Figure 3.6: Graphical representation of solution of equation at snapback point (3.44).

The procedure to find the second solution for V_{BS}, corresponding to SOL2, is illustarted in Fig. 3.7. Here equation (3.44) is rewritten in the form given in (3.47) and solved iteratively until convergence criterion is met.

$$V_{BSnew} = V_T ln\left(\frac{V_{BSold} - C_1}{C_2}\right). \tag{3.47}$$

A large value for V_{BS} like 1 V, can be taken as initial condition (V_o corresponding to SOL2 in Fig. 3.7). Thus, from Fig. 3.7, $V_2 = V_T ln\left(\frac{V_1 - C_1}{C_2}\right)$, $V_3 = V_2$, $V_4 = V_T ln\left(\frac{V_3 - C_1}{C_2}\right)$ and so on.
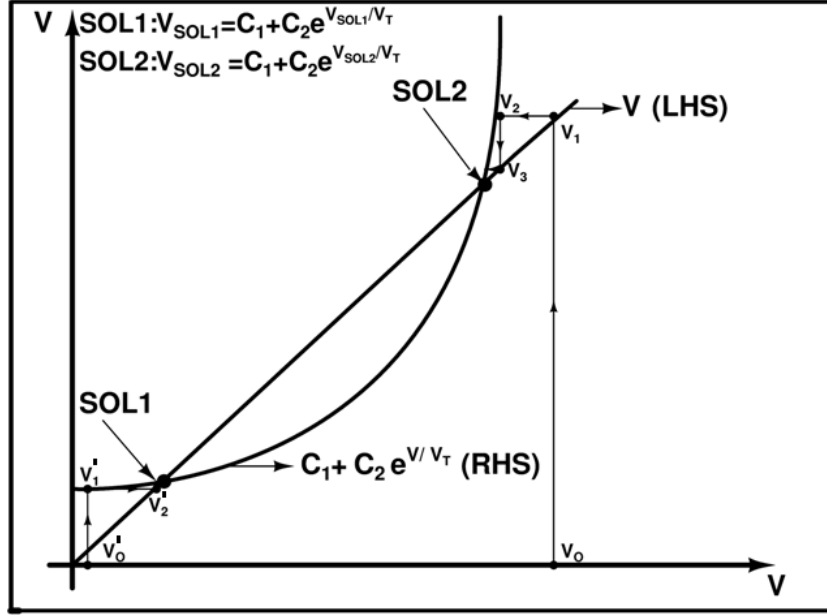
Figure 3.7: Graphical representation of the method used to find SOL2 point.

Once V_{BS} is computed, the total drain current (I_D), given by

$$I_D = M(I_T + I_{MOS}),\qquad(3.48)$$

can be obtained. For each V_{DS}, the simulator gives two values of I_D corresponding to SOL1 and SOL2. Both solutions together give the complete I_D-V_{DS} characteristics of SOI-LDMOS including snapback. Depending on circuit requirement one of the solutions could be chosen. The model developed in this and previous section is for the case when device self-heating is absent. In reality however, self-heating in power devices is a serious issue which requires modeling. Based on the analysis carried out in chapter 2, a model for device self-heating is presented in the next two sections of this chapter.

3.5 Model for temperature dependence

The model developed in previous sections assumes that the operation of device is at an ambient temperature of 300K. In reality, however this temperature can vary drastically depending on device operating condition. To account for this, the LDMOS model parameters must be scalable with temperature. Several of the parameters of LDMOS

model are temperature dependant. To avoid complexity in modeling, temperature dependence of some of these parameters need only be considered.

Considering the most important mechanisms of lattice and impurity scattering, the temperature dependance of carrier mobility can be expressed as [37]

$$\mu_T = \mu_{T_o} \left(\frac{T}{T_o} \right)^{-k} \tag{3.49}$$

where μ_T is effective mobility at a temperature T, μ_{T_o} is effective mobility at reference temperature T_o and k is model parameter which is a function of doping. In the device, doping concentration in drift region is low and mobility decreases with temperature due to lattice scattering. The intrinsic charge carrier concentration is modeled as [37]

$$n_{i,T} = n_{i,T_o} \left(\frac{T}{T_o} \right)^{1.5} exp \left(\frac{E_G(T_o)}{2KT_o} - \frac{E_G(T)}{2KT} \right) \tag{3.50}$$

where $n_{i,T}$ and n_{i,T_o} are intrinsic charge carrier concentrations at T and T_o respectively. The material bandgap is given by E_G. The bandgap of the material, together with flat-band voltage and surface potential are assumed to linearly vary with temperature as [37]

$$E_G(T) = E_G(T_o) + k_1 \left(\frac{T}{T_o} - 1 \right), \tag{3.51}$$

which is quite justifiable. The impact ionization rates are assumed to have linear dependence with temperature as well and are given by

$$a_n(T) = a_n(T_o) + \zeta_{an} \left(\frac{T}{T_o} - 1 \right), \tag{3.52}$$

$$b_n(T) = b_n(T_o) + \zeta_{bn} \left(\frac{T}{T_o} - 1 \right). \tag{3.53}$$

The coefficients ζ_{an} and ζ_{bn} have been extracted for Si [37]. An empirical model [31] is used for describing temperature dependence of v_{sat}, which is expressed as

$$v_{sat} = \frac{2.4 \times 10^7}{1 + 0.8415\frac{T}{T_o}}. \tag{3.54}$$

Critical field is then defined in terms of mobility and carrier saturation velocity. Mobil-

ity reduction due to vertical electric field is assumed to have weak temperature dependence and its effect is ignored. The base resistance variation is modeled by taking into account of mobility and charge carrier variation with temperature. With these temperature dependant parameters, the model given in sections 3.3 and 3.4 become temperature scalable. This model can be extended to model device self-heating as will be shown in next section.

3.6   Model for device self heating

Modeling of device self-heating in high voltage SOI-LDMOS is essential since self heating alters device performance. Due to presence of low conducting buried oxide and high power dissipation, local temperature of the device rises with increasing voltage and current levels in the device. This modifies the device model parameters such as mobility, flat band voltage and Fermi potential etc. as described in previous section. Measurement of drain characteristics show a significant reduction in current levels with negative slope in the plot between I_{DS} and V_{DS} in SOL1 and a premature snapback leading to reduced SOA.

The procedure to model device self-heating is to use a thermal network together with the electrical network [30]. For any given bias, the electrical network's output of dissipated power is fed as input to the thermal network which inturn gives back the temperature update. Temperature dependant quantities in electrical network are re-calculated with the new temperature and is fed back to electrical network. The cycle repeats until convergence is achieved.

From the analysis carried out on device self-heating in section 2.4 of chapter 2, it was concluded that the temperature rise in the device can be studied in SOL1 and SOL2 regimes separately. In both regimes, the heat generated due to device currents in silicon film is dissipated through the substrate across the BOX layer (Refer Fig. 2.18). The substrate is maintained at room temperature and the silicon film is at a high temperature. This reflects the practical scenario, where the chip is cooled from the bottom. The present case, then becomes a classic problem of heat conduction through a material connecting two reservoirs at different temperatures. The thermal network modeling

self-heating takes these observations into account. In the model, heat loss in Si-substrate is neglected.

From Fig. 2.19, it is clear that in SOL1 regime, the temperature rise across the device is uniform and is mainly due to MOSFET current. Since MOSFET current is modeled using three current sources viz. I_{ch}, I_{dr} and I_{dr1}, with each source causing power dissipation, the thermal network, modeling device self heating due to MOSFET currents has 3 sub-circuits as shown in Fig. 3.8.
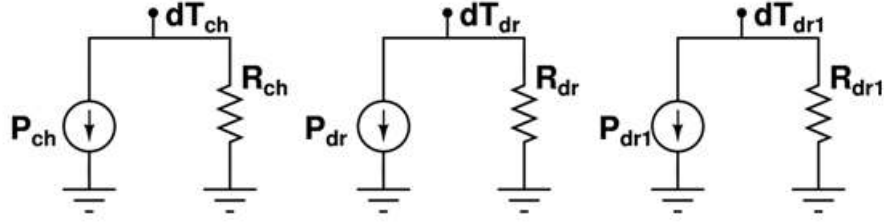
Figure 3.8: Thermal network to model self-heating due to MOSFET currents.

The network has 3 sub-circuits, one for each current source. The thermal resistance for the channel sub-circuit is given as

$$R_{ch} = \frac{t_{BOX}}{k_{BOX}\, W_{BOX}\, L_{ch}} \tag{3.55}$$

where k_{BOX}=1.4 W/mK [30], is the thermal conductivity of oxide, W_{BOX} and t_{BOX} are the width and thickness of BOX layer respectively and L_{ch} is the channel length. The power dissipated by I_{ch} is given by

$$P_{ch} = V_{DiS}\, I_{ch} \tag{3.56}$$

where dT_{ch} is the temperature rise in the channel region above 300K, due to heat dissipation by I_{ch} and is given by

$$dT_{ch} = P_{ch}\, R_{ch}. \tag{3.57}$$

The thermal resistance for the sub-circuit corresponding to Reg-II(Reg-III) is similarly given as

$$R_{dr(dr1)} = \frac{t_{BOX}}{k_{BOX}\, W_{BOX}\, L_{dr(LC)}} \tag{3.58}$$

where $L_{dr(LC)}$ is the length of Reg-II(Reg-III). The power dissipated by $I_{dr(dr1)}$ is given by

$$P_{dr(dr1)} = V_{D'Di(DD')} \, I_{dr(dr1)} \tag{3.59}$$

where $dT_{dr(dr1)}$ is the temperature rise in Reg-II(Reg-III) above 300K, due to heat dissipation by $I_{dr(dr1)}$ and is given by

$$dT_{dr(dr1)} = P_{dr(dr1)} \, R_{dr(dr1)}. \tag{3.60}$$

Since $L_{ch}<L_{dr}<L_{LC}$ for the device structure, $R_{ch}>R_{dr}>R_{dr1}$ from (3.55) and (3.58). However since $V_{DiS}<V_{D'Di}<V_{DD'}$ for most of the bias range in SOL1, where self-heating is prominent, $P_{ch}<P_{dr}<P_{dr1}$ from (3.56) and (3.59). These two opposing effects result in temperature rise dT_{ch}, dT_{dr} and dT_{dr1} to be almost uniform across the silicon film in SOL1 regime. As V_{DS} becomes closer to $V_{snapback}$, dT_{dr1} is slightly more than dT_{ch} and dT_{dr} as seen in Fig. 2.19. $dT_{ch}+300$ is the new temperature which is used to compute parameters corresponding to I_{ch}. Similarly the temperatures affecting parameters of I_{dr} and I_{dr1} are given by $dT_{dr}+300$ and $dT_{dr1}+300$ respectively.

In SOL2 regime, the temperature rise is non uniform across the silicon film. From Fig. 2.19, it can be observed that, the temperature rise in Reg-I and Reg-II are more or less uniform, while temperature rise in Reg-III is much higher. This is expected as in SOL2, impact ionization and parasitic BJT transfer currents dominate over MOSFET current and heat dissipation due to these currents is mainly in Reg-III. The thermal network for modeling self-heating due to BJT currents is given in Fig. 3.9.
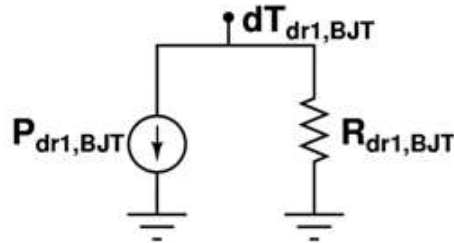

Figure 3.9: Thermal network to model self-heating due to BJT currents.

This network gives temperature rise in Reg-III only. The parameters of Fig. 3.9 are given as follows. $P_{dr1,BJT}$ is the power dissipated by impact ionization and parasitic BJT transfer currents in Reg-III and is given by

$$P_{dr1,BJT} = V_{DD'}\, I_T + V_{DB}\, I_{AVL} \tag{3.61}$$

where $dT_{dr1,BJT}$ is the temperature rise in Reg-III above 300K, due to heat dissipation by impact ionization and parasitic BJT transfer currents and is given by

$$dT_{dr1,BJT} = P_{dr1,BJT}\, R_{dr1}. \tag{3.62}$$

The temperature in Reg-III affects I_{dr1}, I_T and I_{AVL} and is given by $dT_{dr1}+dT_{dr1,BJT}+300$. The temperature rise in Reg-I and Reg-II in SOL2 regime, only affects I_{ch} and I_{dr} respectively. They are computed from subcircuits of Fig. 3.8 as before, except now,

$$P_{ch(dr)} = (I_{ch(dr)} + I_T + I_{AVL})\, V_{DiS(D'Di)}. \tag{3.63}$$

In the self-heating model, temperature rise in any region of the device is computed from power dissipation occuring in that region. Thermal coupling between regions is ignored for model simplicity. This assumption is justifiable for the current LDMOS structure since it has a long drift region. However, if length of Reg-III is significantly reduced, thermal coupling becomes a major factor for temperature rise in different regions and must be modeled by using thermal coupling resistive networks.

In this chapter, a comprehensive static model of SOI-LDMOS structure has been developed to include quasi-saturation, impact ionization, snapback and self-heating. In order to validate the developed model, the results obtained from model implementation are compared with the results obtained from 2D simulator MEDICI, which is discussed in chapter 4.

CHAPTER 4

RESULTS AND DISCUSSION

Device simulations are carried out for HV SOI-LDMOS structure with doping profile shown in Fig. 2.2, using commercially available device simulator TCAD MEDICI. The developed model is implemented in Verilog-AMS and simulated using Spectre from Cadence. In this chapter, the model results from Verilog-A are compared against MEDICI results for model validation. The model is implemented with and without self-heating to include quasi saturation in Reg-III, impact ionization and snapback.
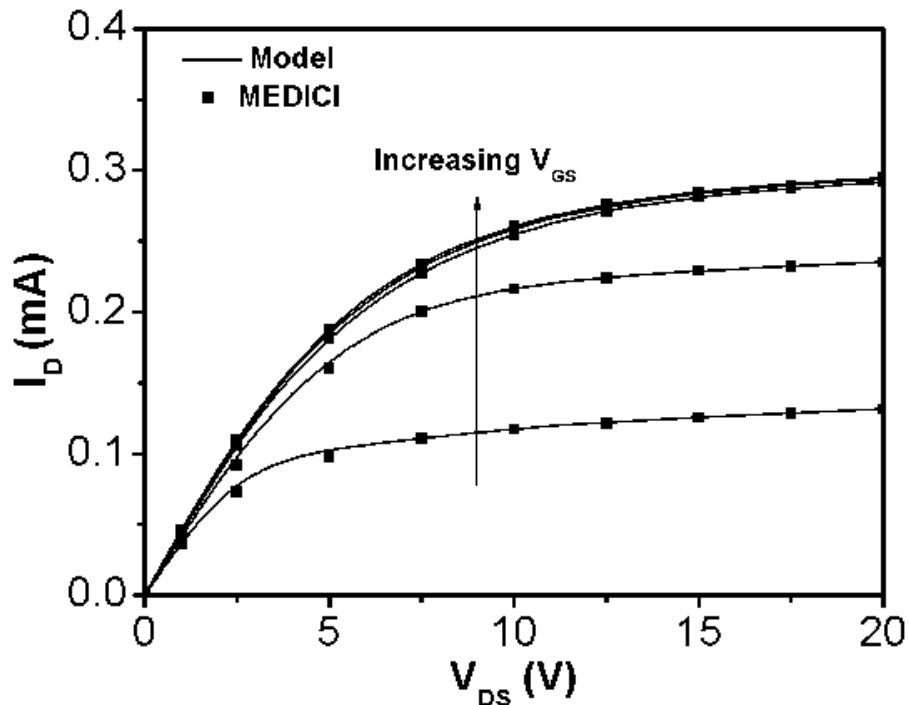
4.1 Static MOSFET currents

Figure 4.1: Comparison of I_D-V_{DS} plots simulated for V_{GS} = 3V, 5V, 10V, 15V and 20V, in MEDICI with the model.

Figure 4.2: Comparison of I_D-V_{GS} plots simulated for V_{DS} = 5V, 10V, 15V and 20V, in MEDICI with the model.

Figures 4.1 and 4.2 show drain currents plotted against drain and gate voltages respectively in low drain bias regime where total current is dominated by MOSFET current due to negligible impact ionization. Upto $V_{GS} = 10V$, it is velocity saturation in Reg-I which is responsible for current saturation. For lower V_{GS}, due to the short length of the channel, short channel effects (SCE) like channel length modulation (CLM) and drain induced barrier lowering (DIBL) are prominent. This results in rise in saturation current level at larger V_{DS} as seen for V_{GS} of 3V in Fig 4.1. Beyond V_{GS} of 10V, current saturation is due to quasi-saturation in Reg-III. This results in negligible increase in drain current with V_{GS} as can be seen from Figs 4.1 and 4.2. The slight increase of drain current with V_{DS} is due to drift length modulation.

From Fig 4.1 and Fig 4.2 it can be seen that drain current from the model shows excellent agreement with MEDICI results. The output conductance and transconductance are also shown in Figs 4.3 and 4.4. They show reasonably good match with MEDICI results. This confirms differentiability of the model.
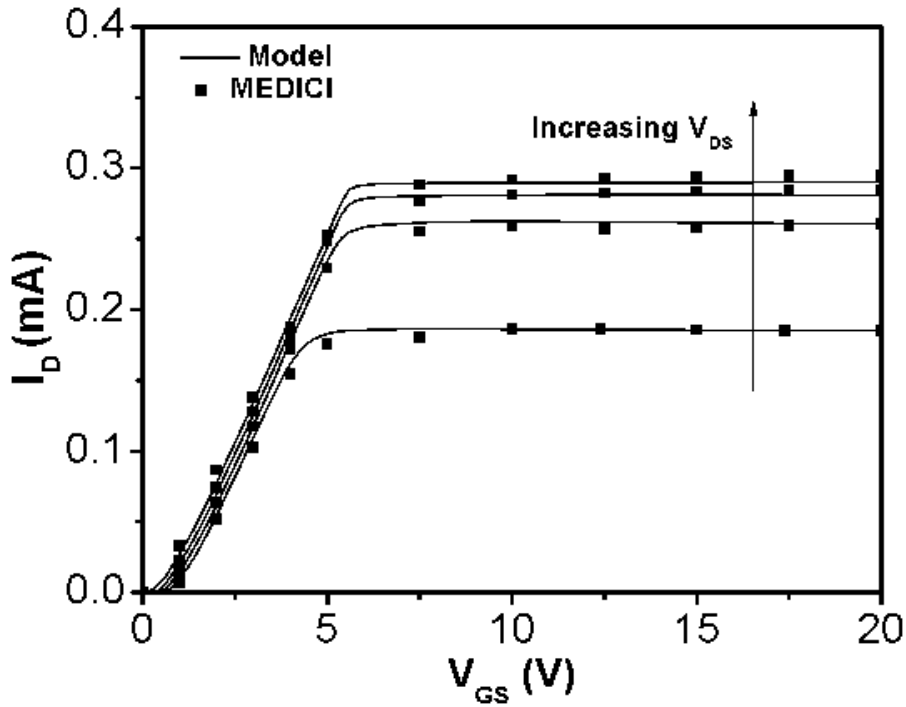
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Figure 4.3: Comparison of g_{DS}-V_{DS} plots simulated for V_{GS} = 5V, 10V, 15V and 20V, in MEDICI with the model.
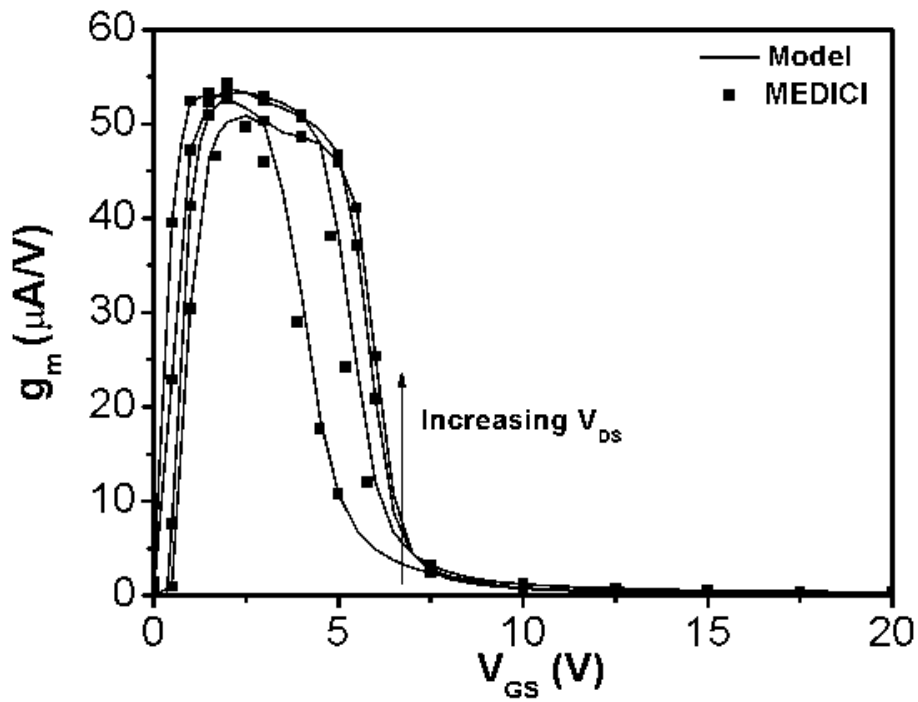
Figure 4.4: Comparison of g_m-V_{GS} plots simulated for V_{DS} = 5V, 10V, 15V and 20V, in MEDICI with the model.

4.2   Impact Ionization and snapback

Impact ionization is modeled by including elements for impact ionization generated avalanche current and parasitic BJT. The activation of the parasitic BJT also results in snapback which is modeled and implemented as described in section 3.5 of chapter 3. In this section, device characteristics with impact ionization and snapback but without self-heating are shown.

Device characteristics, without self heating can be obtained by setting thermal resistances in the thermal networks shown in chapter 3 equal to zero. Fig. 4.5 shows output characteristics of SOI-LDMOS under no self-heating condition. Device simulator output characteristics are generated with self heating turned off. From Fig. 4.5, it can be observed that the model results match with MEDICI device simulation results (with self heating turned off) for the entire V_{DS} range and over wide range of gate bias.
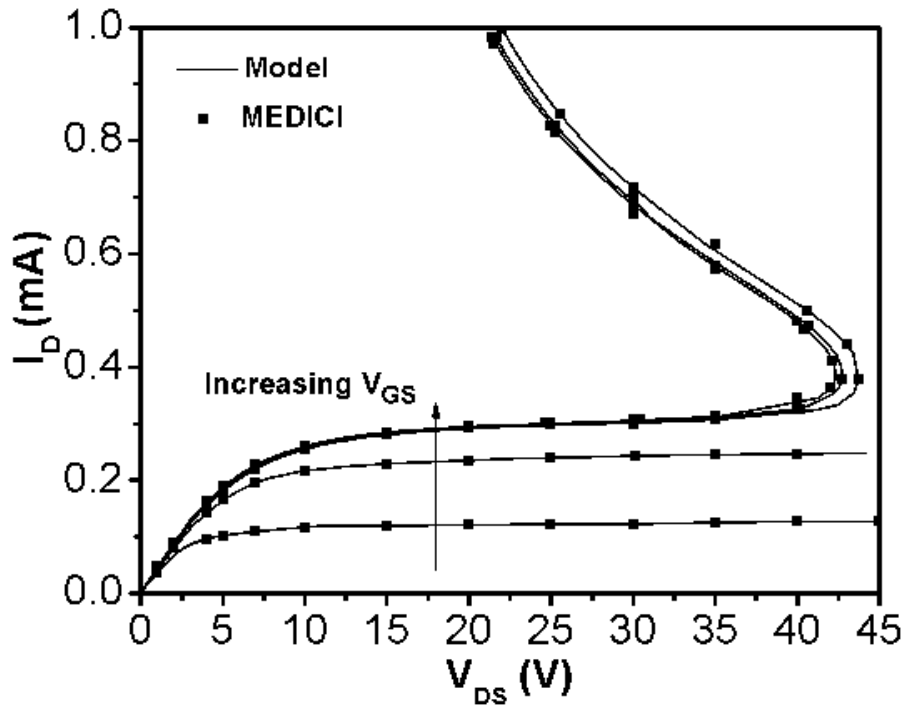
Figure 4.5: Comparison of I_D-V_{DS} plots simulated for V_{GS} = 3V, 5V, 10V, 15V and 20V, in MEDICI with the new model without self-heating.

For lower gate voltages, the saturation current and lateral electric field are not large enough to cause sufficient impact ionization. The resulting avalanche current is too weak to turn on the parasitic BJT and hence snapback is absent even at high V_{DS}. From Fig. 4.5, it can be seen that for V_{GS} of 3V and 5V, snapback is absent even when V_{DS}=45V. While for V_{GS} above 10V, snapback occurs at about 45V.

4.3 Device self heating
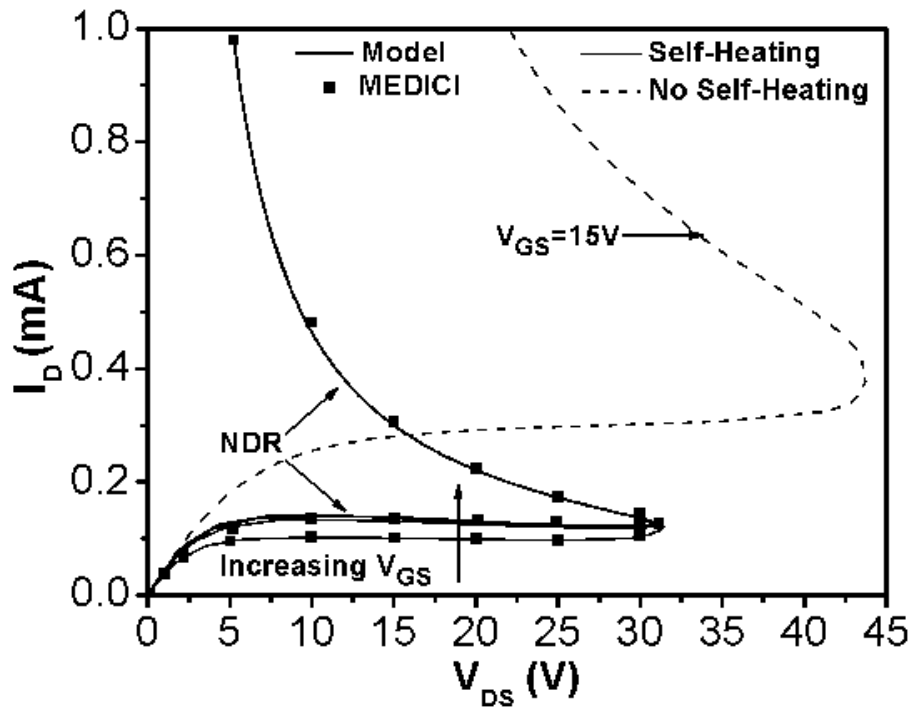
Figure 4.6: Comparison of I_D-V_{DS} plots simulated (Including self-heating effect) for V_{GS}= 3V, 5V, 10V, 15V and 20V, in Verilog-A with MEDICI results.

Fig. 4.6 gives the output characteristics of SOI-LDMOS under impact ionization and self-heating. It can be observed that the Verilog-A results match with MEDICI device simulation results for the entire V_{DS} range and over wide range of gate bias. The I_D-V_{DS} curves tend to merge above V_{GS}=5V, due to quasi-saturation coupled with self-heating effect. The current levels and the snapback voltage are greatly reduced due to device self-heating. This can be seen from Fig 4.6 by comparing drain current curves for V_{GS}=15V, simulated with and without self-heating.
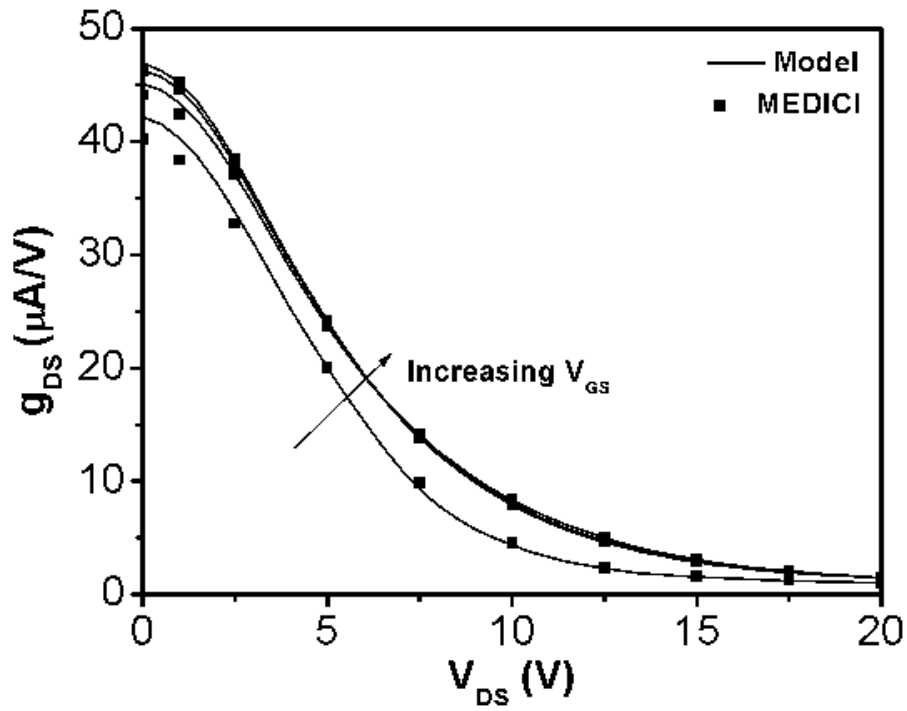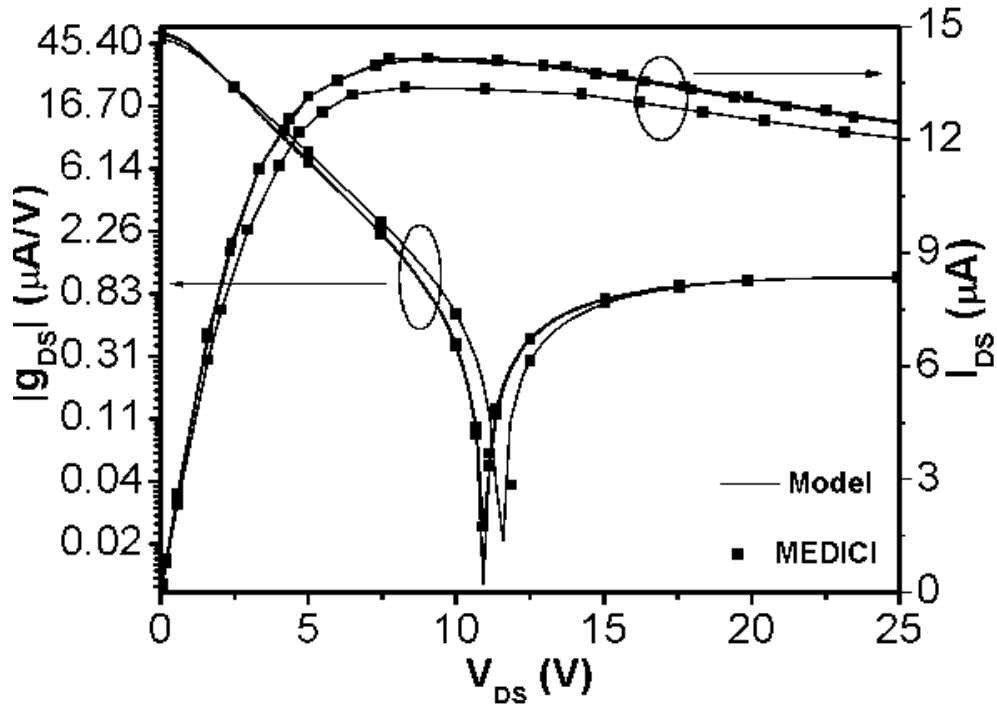
Figure 4.7: Comparison of g_{ds}-V_{DS} plots simulated for V_{GS} = 5V, 10V, 15V and 20V, in MEDICI with the model.

In the model, parameters like mobility, flatband voltage and so on which vary with device temperature as described in section 3.5 of chapter 3, will result in negative differential resistance in I_D-V_{DS} plot even in pre-snapback region in addition to post-snapback region. The drain current increases with V_{DS} in the linear region till the onset of saturation, resulting in positive g_{DS}. After the onset of saturation, short channel effects (SCE) like CLM and DIBL would normally result in further increase of drain current with V_{DS}. However due to predominance of self-heating in the saturation region, there is mobility reduction (as given in equation 3.49) which tends to reduce the drain current with V_{DS}. Thus, there are two opposing factors which influence the nature of change of I_D with V_{DS}. At higher V_{DS}, mobility reduction dominates, resulting in a net reduction in drain current with V_{DS}. This can be observed from Figs. 4.6 and 4.7. The absolute values of output conductance when plotted against drain voltage on a log scale will show a notch at V_{DS} of about 10V, as seen in Fig. 4.7. At the notch, the output conductance goes to zero as the effect on drain current due to SCE and the effect due to mobility reduction tend to balance each other at this point. The I_D-V_{DS} plot in Fig. 4.7 shows that I_D is flat at this point. Beyond this point, self-heating dominates and

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mobility reduction takes precedence over SCE resulting in a reduction in drain current with V_{DS} giving rise to negative g_{DS}.

Device simulations have shown that, for large V_{GS} and V_{DS}, device temperature peaks at $n - n^+$ junction below field oxide close to drain contact. This is because I_{AVL}, I_T and I_{MOS} reach drain contact through this small region creating high current density and hence large power dissipation. Since the region is insulated on both sides by thick field and buried oxides, the dissipated heat causes a very high local increase in temperature. This region's temperature is critical as it initiates thermal breakdown induced device failure. The self-heating model developed can be used to give a fairly accurate estimate of this temperature with bias and the result is shown in Fig. 4.8. It is important to note that though the temperature rise is very high, it is only local to the top of $n - n^+$ junction. Most regions of the device are at temperatures much below these levels as thermal coupling between regions is negligible.
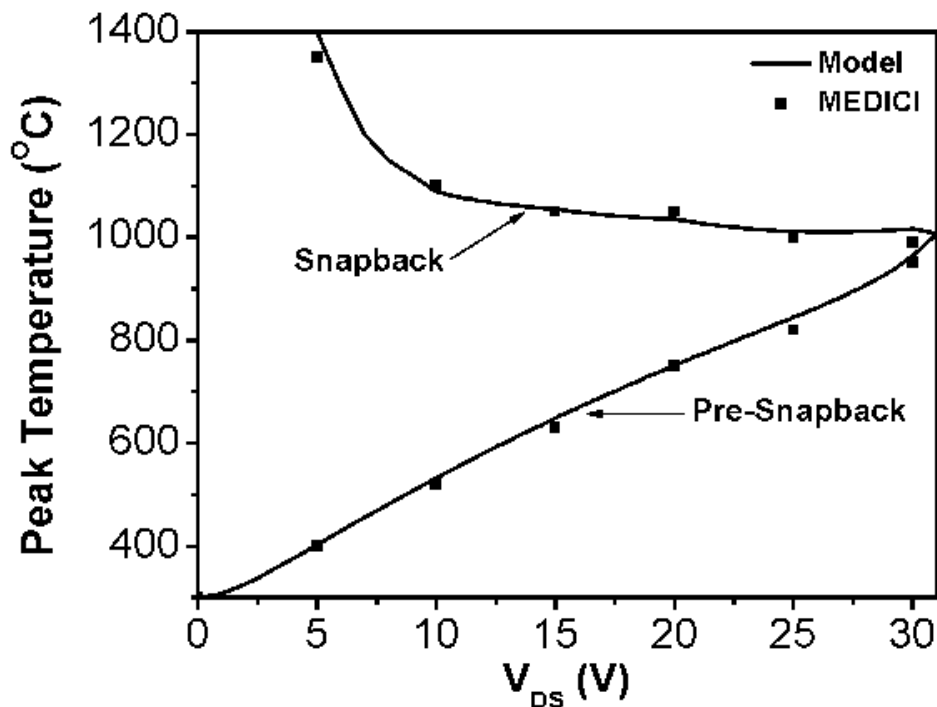
Figure 4.8: Peak temperature at $n - n^+$ junction vs. V_{DS}, for V_{GS}= 15V, given by Verilog-A model and MEDICI.

In this chapter, the results obtained from model implementation in Verilog-A are analyzed and compared with MEDICI simulations. The results obtained in this chapter can be summarized as follows.

- The model for static MOSFET current gives reasonably good match with MEDICI simulations. The output and transfer current characteristics show good accuracy. The transconductance and output conductance plots match reasonably well with MEDICI simulations showing model differentiability.

- The output current characteristics of the device under impact ionization and snap-back match with MEDICI simulations accurately over wide range of gate and drain bais voltages. These simulations and model results assume no self-heating in the device.

- The output current characteristics and output transconductance plots of the device under self-heating match accurately with MEDICI simulations. The model also gives a fairly accurate estimate of temperature rise in Reg-III.

CHAPTER 5

CONCLUSIONS AND SCOPE FOR FUTURE WORK

5.1   Findings of the thesis

In this work, the operation of HV SOI-LDMOS has been analyzed using results obtained from MEDICI simulations and a comprehensive physics based static model to include impact ionization, snapback and device self-heating has been proposed. The developed model is implementable in Verilog-A.

 The major contributions of the work can be listed as following:

1. **Explanation of static MOSFET current model**

   Static MOSFET current model has been explained by region-wise analysis of HV-LDMOS in chapter 2. The device is separated into three regions viz. channel, drift region under gate oxide and drift region under field oxide. Potential drops across each of the region gives insight into the cause for current saturation. It has been concluded that current saturation is mainly due to velocity saturation in channel at lower gate voltages, while it is due to quasi-saturation in drift region under field oxide at higher gate voltages.

2. **Explanation of impact ionization and snapback**

   Impact ionization phenomenon in this device has been studied in detail using MEDICI simulations in chapter 2. The results reveal that impact ionization is significant to cause an increase in static MOSFET currents only under high bias regime. The ionization process is local, due to the long drift region and occurs mainly near the drain contact. By analyzing the resulting substrate currents and field distribution patterns it is concluded that impact ionization driven turn-on of parasitic BJT is responsible for snapback observed in device characteristics.

3. **A physics based compact model for impact ionization and snapback**

   In chapter 3, a new model is developed for explaining the effects of impact ioniza-
   tion and subsequent snapback. The model reuses the model in [31] for MOSFET
   currents and uses impact ionization coefficient model of Chynoweth's law [32].
   The implementation of this developed model in Verilog-A with minimum node
   count is also explained in the chapter. The option to choose either pre-snapbak or
   post-snapback current depending on circuit constraints is an added advantage of
   the model. Results obtained from the model implementation are verified against
   plots obtained from MEDICI simulations and are found to be accurate.

4. **Temperature scalability**

   The physical parameters of the model are scalable with temperature and hence
   the model can describe the device behavior at different temperatures.

5. **Model for device self-heating**

   Modeling self-heating is important in SOI-LDMOS devices as high temperatures
   inside these devices tend to modify device performance. The model for including
   self-heating is developed using resistive thermal networks as given in chapter 3.
   Results show that the model correctly predicts device behavior under self-heating
   conditions at room temperature.

5.2   Scope for future work

1. The model assumes uniform doping concentration in channel for simplicity. However, in practical LDMOS devices, the doping is highest at the source end and decreases towards drain end. This effect of non-uniform doping in channel must be included for an efficient model.

2. The electric field required for impact ionization is presently modeled as a polynomial function of terminal voltages. An analytical expression for the electric field is desirable for the ease of parameter extraction and device scalability.

3. Device scalability is the true floor test for any model. The model equations for physical quantities, used in the developed model are easily scalable with lengths of Reg-I, Reg-II and Reg-III. Hence it is possible to include device scalability into the model. Work in this direction is yet to be carried out.

4. The developed model is a static model. A dynamic model to explain non-quasi static and dynamic behavior of the device needs accurate description of node charges and capacitances.

5. Insights of device performance obtained through analysis and model development could be used to design an optimum SOI-LDMOS structure with a good figure of merit (FoM) in terms of reduced specific on resistance and increased breakdown voltage.

APPENDIX A

MEDICI SOURCE CODE

Medici program of SOI-LDMOS with impact ionization, snapback and self-heating

```
LOOP STEPS=1

ASSIGN NAME=SIFILM N.VALUE=1 DELTA=0.5

ASSIGN NAME=SIFIFILE C1=MESH1


LOOP STEPS=1

ASSIGN NAME=BOX N.VALUE=2 DELTA=0.5

ASSIGN NAME=BOXFILE C1=BOXMESH1


LOOP STEPS=1

ASSIGN NAME=TOTWIDTH N.VALUE=10 DELTA=1

ASSIGN NAME=TOTFILE C1=TOTWIDTH1


MESH SMOOTH=1

X.MESH X.MAX=2.5 H1=0.125

X.MESH X.MIN=2.5 X.MAX=@TOTWIDTH-0.8 H1=0.05 H2=0.125

X.MESH X.MIN=3 X.MAX=@TOTWIDTH H1=0.125

Y.MESH N=1 L=-0.038

Y.MESH N=3 L=0

Y.MESH DEPTH=@SIFILM H1=0.1

Y.MESH DEPTH=@BOX H1=0.1

Y.MESH DEPTH=3 H1=0.1


ELIMIN COLUMNS Y.MIN=@SIFILM+0.1

ELIMIN COLUMNS Y.MIN=@SIFILM+0.3 X.MIN=2.5 X.MAX=@TOTWIDTH-0.8
```

```
SPREAD LEFT WIDTH=2.625 UP=1 LO=3 THICK=0.1 ENC=2

SPREAD RIGHT WIDTH=@TOTWIDTH-3.117 UP=1 LO=3 THICK=0.1 ENC=2

SPREAD LEFT WIDTH=100 UP=3 LO=4 Y.LO=.1


REGION SILICON Y.MIN=0 Y.MAX=@SIFILM X.MIN=0 X.MAX=@TOTWIDTH

REGION OXIDE Y.MIN=@SIFILM Y.MAX=@SIFILM+@BOX X.MIN=0

+ X.MAX=@TOTWIDTH

REGION SILICON Y.MIN=@SIFILM+@BOX Y.MAX=@SIFILM+@BOX+3 X.MIN=0

+ X.MAX=@TOTWIDTH

REGION OXIDE IY.MAX=3


ELECTR NAME=GATE X.MIN=2.625 X.MAX=3.117 TOP

ELECTR NAME=SUBSTRATE BOTTOM

ELECTR NAME=HEATSINK BOTTOM THERMAL

ELECTR NAME=SOURCE X.MAX=2.5 X.MIN=0.7 IY.MAX=3

ELECTR NAME=DRAIN X.MIN=@TOTWIDTH-0.6 IY.MAX=3


PROFILE N-TYPE N.PEAK=2E16 UNIFORM Y.MIN=0 Y.MAX=@SIFILM

+ X.MIN=2.75+0 X.MAX=@TOTWIDTH OUT.FILE=M1

PROFILE P-TYPE N.PEAK=2E17 UNIFORM Y.MIN=0 Y.MAX=@SIFILM

+ X.MIN=0 X.MAX=2.75+0

PROFILE P-TYPE N.PEAK=3E15 UNIFORM Y.MIN=@SIFILM+@BOX Y.MAX=50

+ X.MIN=0 X.MAX=@TOTWIDTH

PROFILE N-TYPE N.PEAK=2E20 Y.JUNC=0.34 X.MIN=1.9 WIDTH=0.5

+ XY.RAT=0.75

PROFILE P-TYPE N.PEAK=2E22 Y.JUNC=0.34 X.MIN=0.75 WIDTH=0.5

+ XY.RAT=0.75

PROFILE N-TYPE N.PEAK=2E22 Y.JUNC=0.34 X.MIN=@TOTWIDTH-0.5

+ WIDTH=0.5 XY.RAT=0.75


REGRID DOPING LOG IGNORE=OXIDE RAT=2 SMOOTH=1 IN.FILE=M1

PLOT.2D GRID TITLE="DOPING REGRID" FILL SCALE
```

```
CONTACT NAME=GATE N.POLY

MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB IMPACT.I

SYMB CARRIERS=0

METHOD ICCG DAMPED

SOLVE


REGRID POTEN IGNORE=OXIDE RAT=0.2 MAX=1 SMOOTH=1 IN.FILE=M1

+ OUT.FILE=M2

PLOT.2D GRID TITLE="POTENTIAL REGRID" FILL SCALE

PLOT.2D DEPL SCALE FILL TITLE="DEPLETION"


LOOP STEPS=2

ASSIGN NAME=HEAT L.VAL=(T,F)

ASSIGN NAME=LOCLOG C1=@SIFIFILE@BOXFILE"SOL1"

+ C2=@SIFIFILE@BOXFILE"SOL2"


LOOP STEPS=1

ASSIGN NAME=GATEVOL N.VALUE=5 DELTA=5

ASSIGN NAME=GATVOL C1=GATVOL5


IF COND=@HEAT

MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB IMPACT.I

SYMB CARRIERS=0 LAT.TEMP COUP.LAT

ELSE

MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB IMPACT.I

SYMB CARRIERS=0

IF.END

METHOD ICCG DAMPED

SOLVE V(GATE)=0 V(SUBSTRATE)=0 V(SOURCE)=0 V(DRAIN)=0 INITIAL

SOLVE V(GATE)=@GATEVOL OUT.FILE=TEMPSOL
```

```
ASSIGN NAME=LOGFIL C1=@LOCLOG@TOTFILE@GATVOL

LOAD IN.FILE=TEMPSOL

IF COND=@HEAT

MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB IMPACT.I

SYMB CARRIERS=2 NEWTON LAT.TEMP COUP.LAT

ELSE

MODELS ANALYTIC FLDMOB CONSRH AUGER BGN PRPMOB IMPACT.I

SYMB CARRIERS=2 NEWTON

IF.END

METHOD ^AUTONR STACK=10

LOG OUT.FILE=@LOGFIL

SOLVE V(SUBSTRATE)=0

SOLVE V(SOURCE)=0

SOLVE V(DRAIN)=0

SOLVE ELEC=DRAIN CONTINUE C.VMAX=50 C.VSTEP=0.01

+ C.TOL=0.05 C.IMAX=3E-3


L.END

L.END

L.END

L.END

L.END


PLOT.1D IN.FILE=MESH1BOXMESH1SOL1TOTWIDTH1GATVOL5 X.AXIS=V(DRAIN)

+ Y.AXIS=I(DRAIN) LEFT=0 RIGHT=20 BOTTOM=0 TOP=10E-4  COL=1

+ ^ORDER OUT.FILE=iv5.DAT


PLOT.1D IN.FILE=MESH1BOXMESH1SOL2TOTWIDTH1GATVOL5 X.AXIS=V(DRAIN)

+ Y.AXIS=I(DRAIN) LEFT=0 RIGHT=20 BOTTOM=0 TOP=10E-4  COL=2

+ ^ORDER OUT.FILE=ivsh5.DAT
```

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