Hindawi Publishing Corporation
Modelling and Simulation in Engineering
Volume 2014, Article ID 635803, 7 pages
http://dx.doi.org/10.1155/2014/635803

Hindawi

Research Article

Modeling of Temperature-Dependent Noise in Silicon Nanowire FETs including Self-Heating Effects

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Received 7 January 2014; Accepted 23 April 2014; Published 21 May 2014

Academic Editor: Agostino Bruzzone

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Silicon nanowires are leading the CMOS era towards the downsizing limit and its nature will be effectively suppress the short channel effects. Accurate modeling of thermal noise in nanowires is crucial for RF applications of nano-CMOS emerging technologies. In this work, a perfect temperature-dependent model for silicon nanowires including the self-heating effects has been derived and its effects on device parameters have been observed. The power spectral density as a function of thermal resistance shows significant improvement as the channel length decreases. The effects of thermal noise including self-heating of the device are explored. Moreover, significant reduction in noise with respect to channel thermal resistance, gate length, and biasing is analyzed.

1. Introduction

As the device size scaling continues, many critical issues such as increased leakage current, short-channel effect, high-field effects, variability, reliability, noise, and parasitic impacts may pose more obstruction for highly scaled devices. Therefore, device structure and material innovation have attracted more attention as the primary enabler for performance enhancement in CMOS technology.

The gate-all-around (GAA) silicon nanowire transistor (SNWT) is considered as one of the promising candidates for ultimate scaling, due to its excellent electrostatic control capability, improved transport property, and feasible device design [1–4]. This kind of device has the unique structural nature, with quasi-one-dimensional and strongly confined nanowire channel, three-dimensional surrounding gate-stack of multiple crystallographic interface orientations, and sharp transition from the large source/drain region to the narrow part (of source/drain extension). Thus, some of the above mentioned critical issues may be even more complicated that would give rise to new challenges in device engineering of SNWTs.

Channel thermal noise is the most dominant noise source of short-channel MOSFETs at high frequencies. As the MOSFET is scaled down, short-channel effects increase and it causes serious problems in device operation. Gate-all-around silicon nanowire MOSFET is one of the strong candidates, which has high performance even in short-channel devices [5–7]. As well as the short-channel effects, channel thermal noise is also increased as the MOSFET is scaled down. Thus, it is necessary to predict channel thermal noise in silicon nanowire MOSFET [8]. To compare the channel thermal noise in nanowire MOSFET with temperature-dependent model, analytical power spectral density (PSD) equation is used. The cross-sectional view of a silicon nanowire MOSFET is shown in Figure 1.

2. DC Characterization of Silicon Nanowires

Before analyzing the channel thermal noise, the DC characteristics of SNWFET are analyzed. From Figure 1, the drive current, threshold voltage, subthreshold swing, and DIBL are calculated by TCAD simulations. Here, different channel lengths are chosen and correspondingly the threshold voltage is noted. Here, the threshold voltage varies from 0.24 to 0.27 V; the subthreshold swing and DIBL are 71 mV/decade and 18.4 mV/volt, respectively. The drain current values are varied from 0.31 mA to 0.51 mA. It is predicted that channel thermal noise is much higher in devices with higher drain currents and increases with scaling.

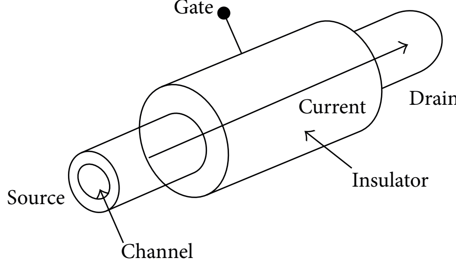


Figure 1: Structure of SNWFET.

3. Channel Thermal Noise Modeling

In this work, channel thermal noise of the silicon nanowire MOSFET (SNWFET) is derived from the analytic thermal noise model, by including short-channel effects [9, 10]. Power spectral density of the noise current is defined by

$$S_{\mathrm{id}} = 4KT\frac{1}{R}. \tag{1}$$

Here, K is Boltzmann constant, T is temperature (K), and R is resistance (ohm).

Using (1), we can find the power spectral density of channel thermal noise in SNWFET [11]:

$$S_{\mathrm{id}} = 4K_BT\frac{\mu\left(-Q_{\mathrm{inv}}\right)}{L^2}. \tag{2}$$

Here, μ is mobility of charge carriers, L is channel length (nm), and Q_{inv} is inversion charge.

Considering the short-channel effects, the power spectral density of channel thermal noise is validated for short-channel transistors as follows:

$$S_{\mathrm{id}} = 4K_BT\cdot I_{\mathrm{ds}}\cdot\left(\frac{1}{V_{\mathrm{ds}}}+\frac{1}{E_cL_c}\right). \tag{3}$$

Here, E_c is critical electric field, L_c is channel length (nm), and V_{ds} is drain source voltage (V).

4. Temperature-Dependent Model

Special design approaches are derived for SNWT circuits by using the thermal model; the effect can be analyzed for the devices with the following relationship between temperature dependence and power dissipation [12] given by

$$T - T_0 = R_{\mathrm{th}}V_{\mathrm{ds}}I_{\mathrm{ds}}. \tag{4}$$

Here, T is actual temperature, T_0 is the ambient (substrate) temperature, and R_{th} is a thermal resistance

$$S_{\mathrm{id}} = 4K_B\left(T-T_0\right)\cdot I_{\mathrm{ds}}\cdot\left(\frac{1}{V_{\mathrm{ds}}}+\frac{1}{E_cL_c}\right), \tag{5}$$

$$S_{\mathrm{id}} = 4K_BR_{\mathrm{th}}I_{\mathrm{ds}}^2\left\{1+\left(\frac{V_{\mathrm{ds}}}{E_cL_c}\right)\right\}; \tag{6}$$

$$R_{\mathrm{th}} = \frac{d}{A\lambda_{\mathrm{th}}}, \tag{7}$$

$$S_{\mathrm{id}} = \frac{4K_BdI_{\mathrm{ds}}^2}{A\lambda_{\mathrm{th}}}\left\{1+\left(\frac{V_{\mathrm{ds}}}{E_cL_c}\right)\right\}. \tag{8}$$

Equation (8) represents the power spectral density of channel thermal noise with temperature-dependent model. Here, A is the area and d is the thickness of silicon nanowire, respectively. λ_{th} is the thermal conductivity.

5. Self-Heating Effects (SHE)

Once the temperature dependence of the device parameters is extracted, the same approach can be used for describing the self-heating effects of the device:

$$G_{\mathrm{SEH}} = \frac{\partial I_{\mathrm{ds}}}{\partial T}\cdot\frac{\partial T}{\partial V_{\mathrm{ds}}}, \tag{9}$$

$$\frac{\partial T}{\partial V_{\mathrm{ds}}} = R_{\mathrm{th}}I_{\mathrm{ds}}, \tag{10}$$

$$R_{\mathrm{th}} = \frac{G_{\mathrm{SHE}}}{I_{\mathrm{ds}}\cdot\left(\partial I_{\mathrm{ds}}/\partial T\right)}, \tag{11}$$

$$C_{\mathrm{th}} = \frac{1}{2\pi f_{\mathrm{th}}R_{\mathrm{th}}}. \tag{12}$$

From (12), C_{th} is the thermal capacitance, f_{th} is the thermal frequency, and G_{SHE} is the transconductance including self-heating effects (SHE) at the particular point. We use the AC drain output conductance (g_{ds}) data at one bias point to characterize both R_{th} and C_{th}. The SHE can be subtracted from the DC data and a SHE-free device model can be extracted as [13, 14]

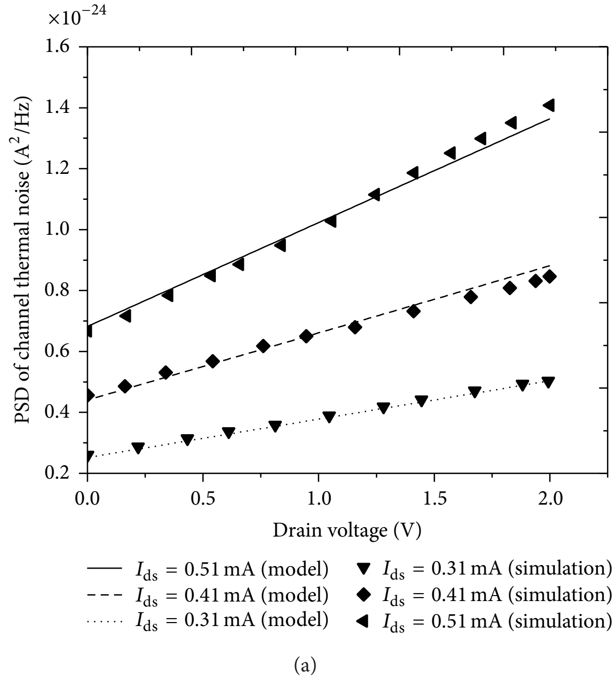
$$\Delta T\left(f\right) = \frac{I_{\mathrm{ds}}V_{\mathrm{ds}}R_{\mathrm{th}}}{\sqrt{1+\left(2\pi fR_{\mathrm{th}}C_{\mathrm{th}}\right)^2}}. \tag{13}$$

Temperature variation depending on the frequency ($\Delta T(f)$) is calculated.

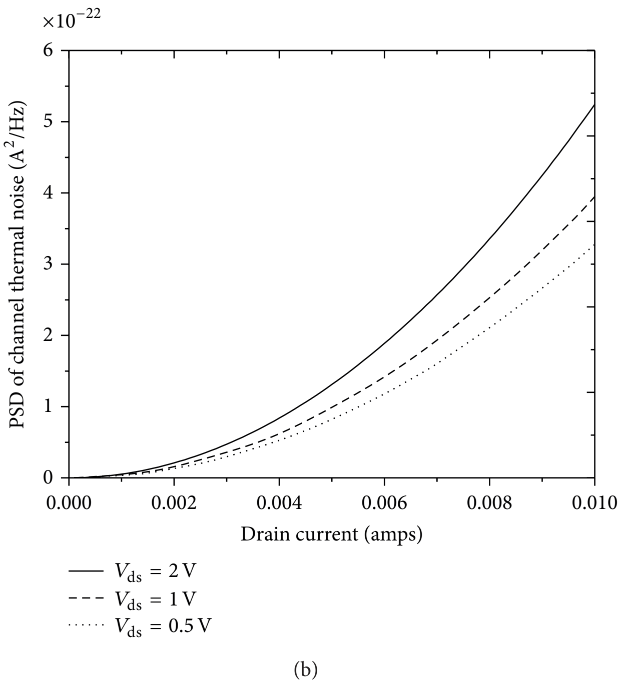
Substituting self-heating effect in power spectral density equation of channel thermal noise,

$$S_{\mathrm{id}} = 4K_B\Delta T\left(f\right)I_{\mathrm{ds}}\left\{\frac{1}{V_{\mathrm{ds}}}+\frac{1}{E_cL_c}\right\} \tag{14}$$

$$S_{\mathrm{id}} = 4K_B\cdot\frac{I_{\mathrm{ds}}^2d}{\sqrt{\left(A\lambda_{\mathrm{th}}\right)^2+\left(2\pi fdC_{\mathrm{th}}\right)^2}}\left\{1+\frac{V_{\mathrm{ds}}}{E_cL_c}\right\}. \tag{15}$$



(a)



(b)

Figure 2: (a) Power spectral density of channel thermal noise versus drain source voltage of the SNWMOSFET. (b) Power spectral density of channel thermal noise versus drain current of the SNWMOSFET.

Equation (15) is derived for power spectral density of channel thermal noise.

In SNWTs, the self-heating problem may be even worse due to their ultrasmall and strongly confined nanowire channels. Therefore, a simple and accurate analytical channel thermal noise model for SNWTs is developed and optimized for future applications.

6. Numerical Noise Model Calibration

In recent years, some effort has been devoted to the numerical simulation of noise phenomena in physics based device simulators. In most cases, the noise simulation is founded on Shockley's impedance field method [15] and its variations and generalizations. Bonani et al. [16] reported a numerically efficient Green function approach to the Langevin equation based simulation of the impedance field method (IFM) which is the basis for the implementation in the multidimensional, mixed-mode device simulator Synopsys TCAD described here. It is a variation of the direct impedance field method (DIFM). The so-called adjoint impedance field method (AIFM) (e.g., [17]) is limited to one-carrier devices and had been earlier implemented into Dessis-ISE [18].

6.1. Numerical Diffusion Noise. Diffusion noise is due to fluctuations of the velocities of the carriers, caused by collisions with phonons, impurities, temperatures, and so forth. The following expression for the electron diffusion noise source can be derived (e.g., [17]):

$$K_{\text{diff}} = 4qnK_B T\mu, \quad (16)$$

where n is the electron density, μ is the electron mobility, and T is one of lattice temperature, e temperature, h temperature, or e h temperature; the used temperature in the expression can be chosen with default lattice temperature. For example, e temperature uses the electron temperature for the electron noise source, while the lattice temperature is used for the hole noise source; the specification e h temperature uses for the carrier noise source the corresponding carrier temperature.

7. Results and Discussion

Figure 2(a) shows the power spectral density of channel thermal noise versus drain voltage of the SNWMOSFET for different drain currents. It is evident that the channel thermal noise increases with increasing drain current because as the electrons approach the drain, its velocity increases simultaneously increasing the temperature of the carriers under the influence of high drain field thereby increasing the PSD of the carriers. This proportionality of PSD channel thermal noise with drain current is checked and verified with noise simulation data in Figure 2(a).

The effect of drain current with PSD of channel thermal noise is modeled in Figure 2(b). It is evident that the channel thermal noise increases with increasing drain current as shown in (3).

Figure 3(a) shows the power spectral density of channel thermal noise versus channel length of the SNWMOSFET. It is observed that as the channel length is increased, thermal noise decreases due to the fact that aggressive scaling causes increased channel thermal noise and is verified by simulation results.

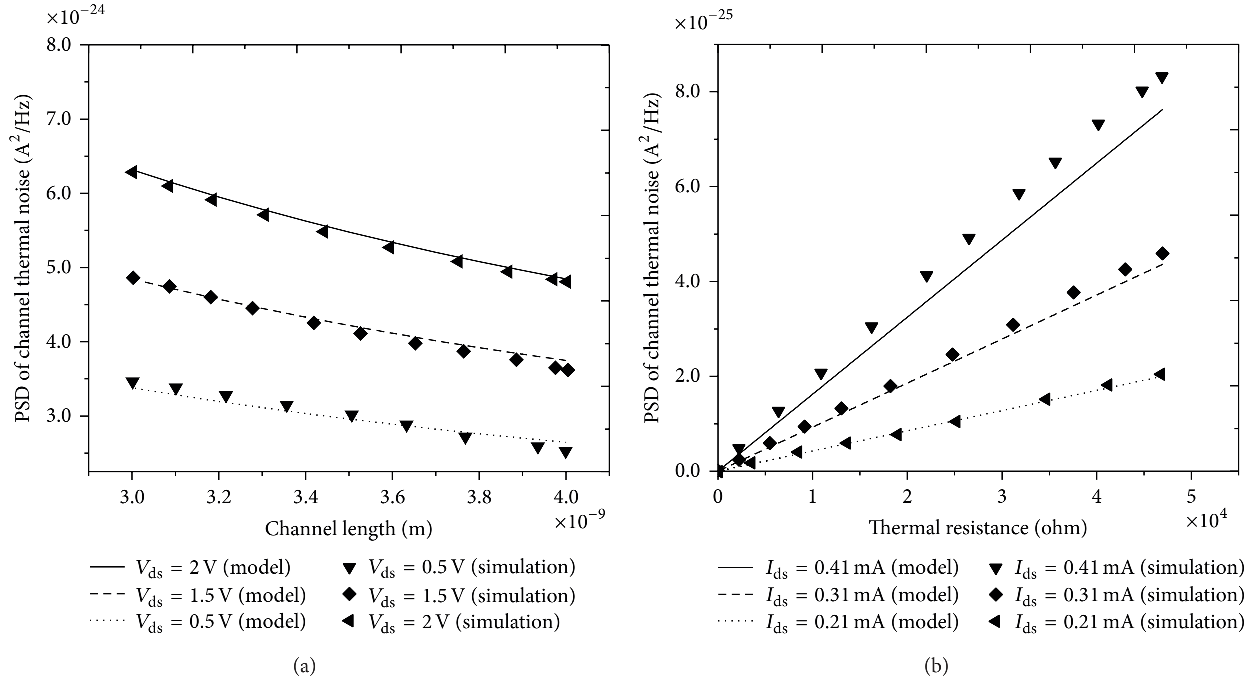


Figure 3: (a) Power spectral density of channel thermal noise versus channel length of the SNWMOSFET. (b) Power spectral density of channel thermal noise versus thermal resistance of the SNWMOSFET.

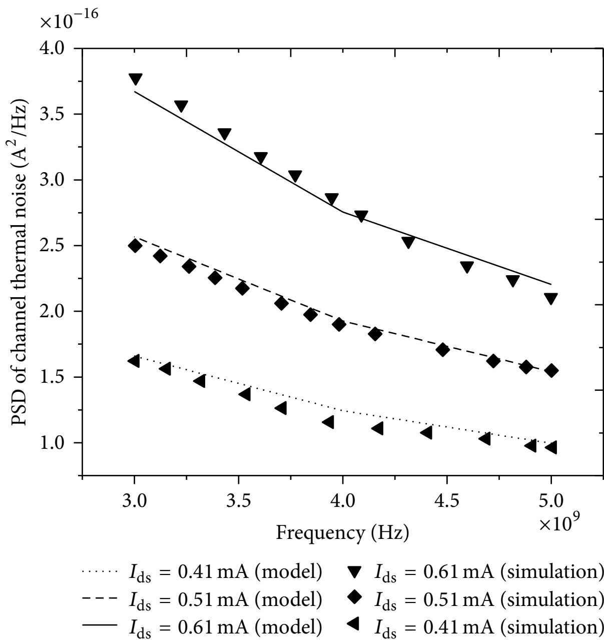


Figure 4: Power spectral density of channel thermal noise versus thermal resistance of the SNWMOSFET.

Figure 3(b) shows the variation of PSD channel thermal noise for different thermal resistance values. Due to uniform scaling, the resistances at the source and drain tend to increase with temperature which in turn increases the thermal noise. For channel length below 65 nm, the thermal resistance effects could not be ignored.

Figure 4 shows the power spectral density of channel thermal noise versus frequency of the SNWMOSFET for various drain current values. From the figure, it is clear that PSD of the channel thermal noise decreases at high frequency showing significant improvement in noise figure. This is because as the frequency increases, the parasitics increase, thereby increasing the reactance effects at high frequencies. The results are verified with simulations and are found to be matching each other.

Figure 5(a) shows the variation of minimum noise factor with respect to gate length for different frequencies. As the MOSFET is scaled down from 0.1 to 0.03 μm for increased F_t, the minimum noise factor increases since N_f is proportional to KTB and as temperature increases with the increase of F_t, the noise factor N_f also increases. The results are also verified using simulations.

Figure 5(b) shows the variation of noise factor with the drain voltage as the factor of gate length. N_f decays exponentially with increased drain voltages as the gate length is decreased.

Figure 6(a) shows the effect of temperature on the drive current for increased drain voltages. The drain current increases as the drain voltage approaches V_{dd} also increasing the temperature of the device (hot carrier effects). This is verified by using simulation results.

Figure 6(b) shows the variation of temperature over the area of the silicon nanowire for increased drain current. The temperature decays exponentially with the area of the silicon nanowire for increased drain current. As the area

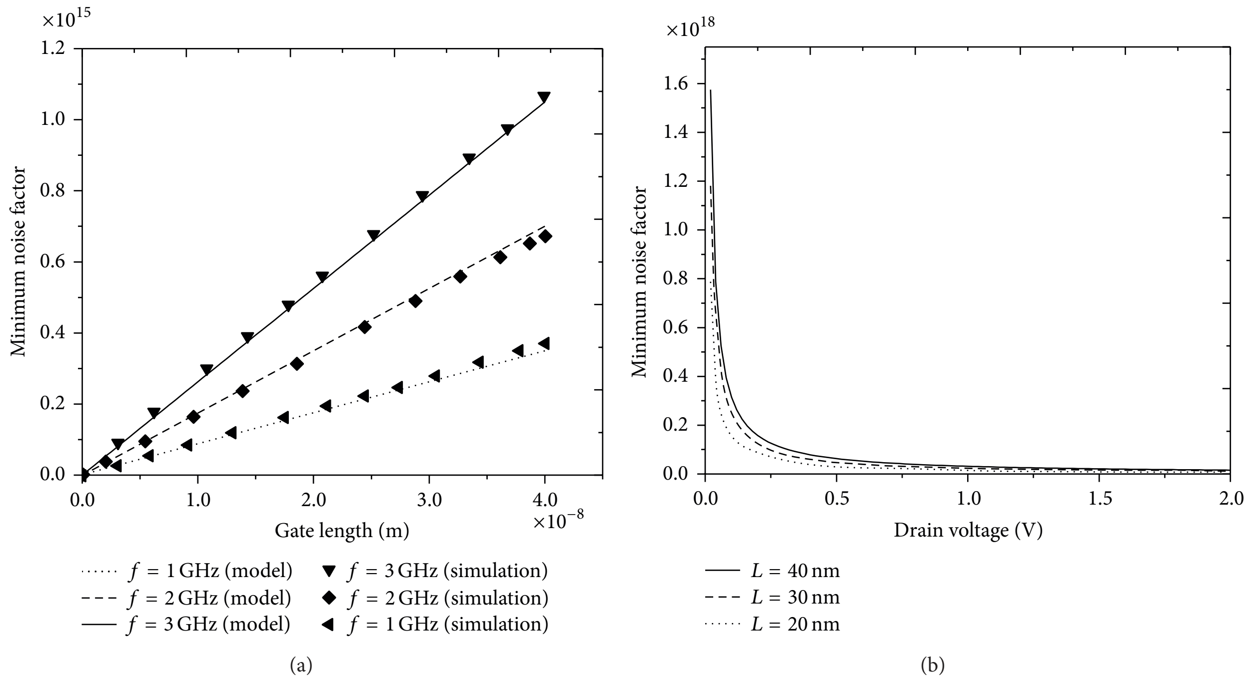


Figure 5: (a) Characteristic of minimum noise factor versus gate length. (b) Characteristic of minimum noise factor versus drain voltage.

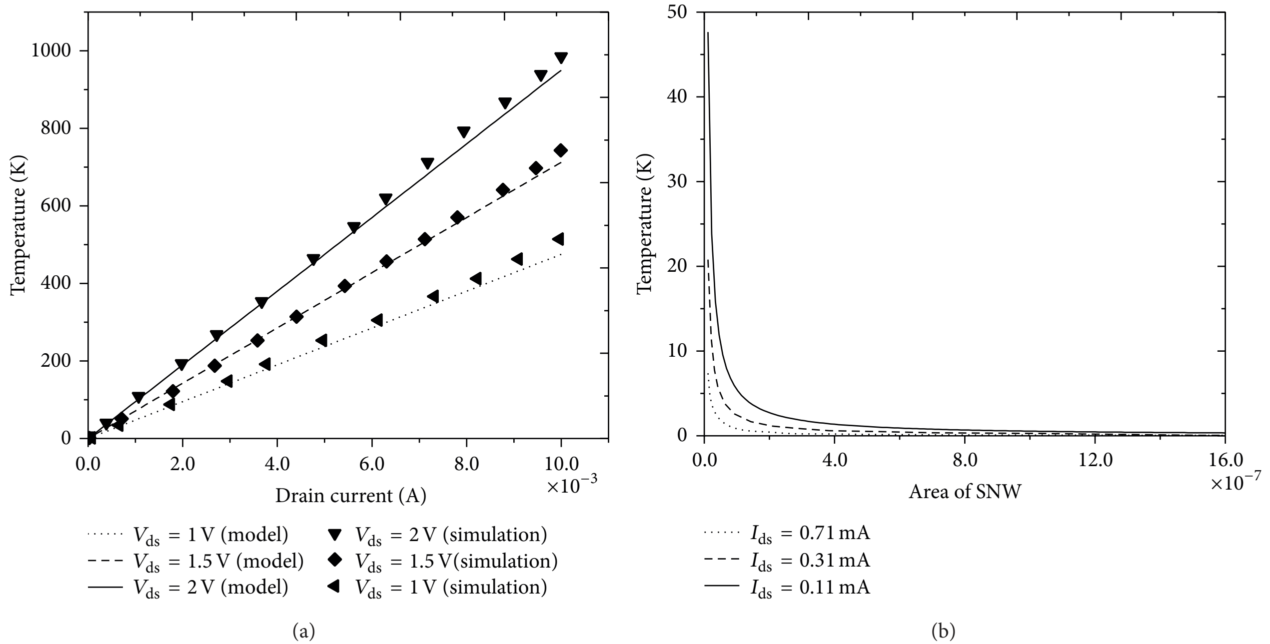


Figure 6: (a) Characteristic of temperature versus drain current. (b) Characteristic of temperature versus area of SNW.

of the nanowire is increased the hot electron at the drain ends will have enough space for scattering within the channel increasing thermal conductivity and thereby decreasing the temperature.

Figure 7 shows the PSD of channel thermal noise as the function of temperature. It is evident that for increased drain voltages the drain current increases simultaneously increasing the channel thermal noise which in turn increases the temperature since $P_n = KTB$, where P_n is the signal to noise power, T is temperature, K is Boltzmann's constant, and B is the bandwidth. This is verified by simulation results.

8. Conclusion

This paper analyses the modeling of thermal noise in silicon nanowire MOSFET including the self-heating effects.

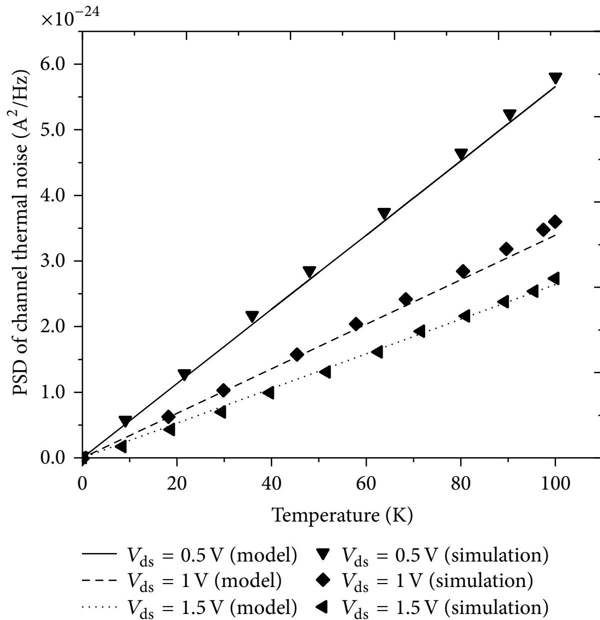


Figure 7: Characteristic of PSD of channel thermal noise versus temperature.

The variations of thermal noise with respect to various device oriented parameters are observed for improved performances of the device. The channel thermal noise is predicted using noise factor in silicon nanowire MOSFET at high frequencies. Improvement in noise figure owing to reduce area in case of effectively scaled Nanowires.

An analytical formulation of the thermal noise in short-channel MOSFETs, working in the saturation region, is presented. Hence, the noise characteristic is analyzed by noise factor and the performance of the noise characterized by TCAD shows significant improvement in case of suitably scaled nanowires. The effects of thermal noise with respect to device geometry are discussed in detail.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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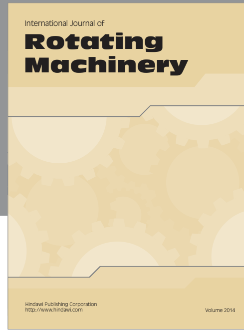
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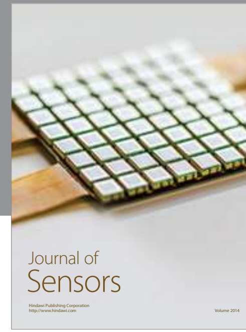
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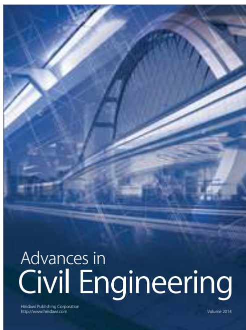
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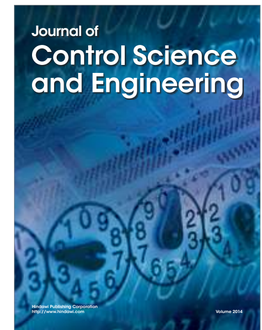
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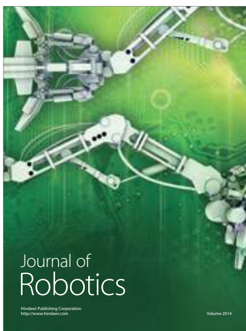
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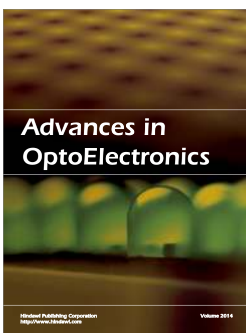
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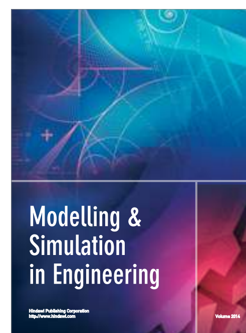
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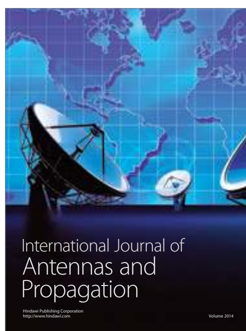
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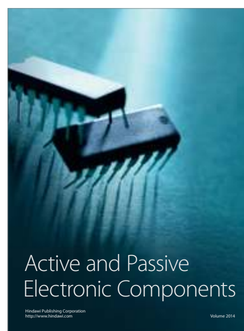
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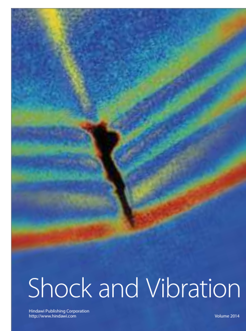
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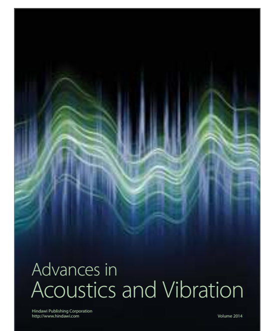
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