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Modeling Op Amp Nonlinearity in Switched-Capacitor Sigma-Delta Modulators[1]

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Abstract

A system-level methodology for the inclusion of op amp nonlinearity in discrete-time integrators and ΣΔ modulators is proposed that consists of a hyperbolic tangent model for the input/output characteristic of op amps and a recursive solution of nonlinear integrators. Simulations at different levels of abstraction indicate that the methodology incurs an error of no more than 1.1 dB in the magnitude of harmonics while providing a 50x advantage in the simulation speed with respect to transistor-level implementations.

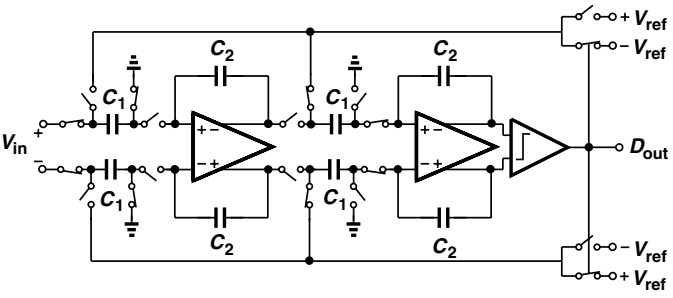
I. Introduction

The design of high-performance ΣΔ modulators is characterized by two trends. First, low oversampling ratios (e.g., 8-16) along with multibit quantizers are sought so as to accommodate greater signal bandwidths for a given clock frequency [1-3]. Second, the design of the constituent op amps becomes increasingly more difficult as the device dimensions and the supply voltage scale down. Fortunately, ΣΔ modulators can tolerate a relatively low op amp gain (e.g., a few times the oversampling ratio or as determined by the integrator leakage in single-stage or cascade architectures [4, 5]). Unfortunately, the nonlinearity of op amps manifests itself if the open-loop gain is not sufficiently high, requiring that the designer determine the minimum allowable open-loop gain that leads to negligible closed-loop distortion.

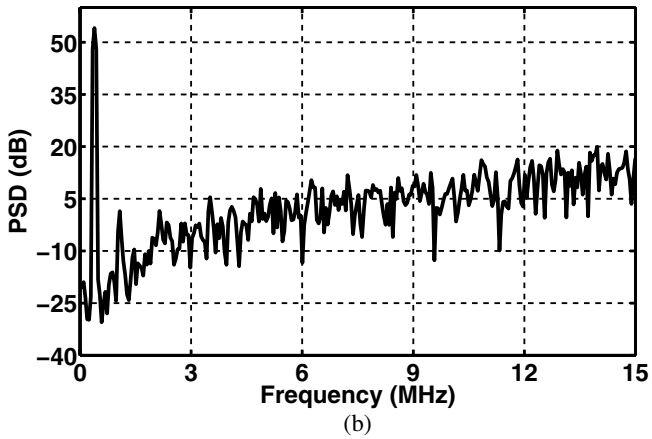
This paper introduces a methodology for modeling the nonlinearity of op amps in a ΣΔ modulator environment. Section II describes the modeling issues and Section III presents the methodology. Section IV provides a detailed study of the results at different levels of abstraction.

II. Nonlinearity Modeling Issues

Consider the generic 1-bit second-order ΣΔ modulator shown in Fig. 1(a). With a simple cascode op amp, ideal switches, and a behavioral comparator model, this modulator requires a simulation time of about one hour in Cadence (with low accuracy settings) to reveal the harmonic content of the output [Fig. 1(b)]. Of course, this simulation time increases further as multibit quantizers, DAC linearization techniques, and other functions are included in the design. For example, a cascade of two second-order modulators consisting of cascode op amps, three-bit behavioral quantizers, and ideal switches requires a simulation time of several hours. It therefore becomes extremely difficult to perform simulations, develop intuition, and try new concepts.



(a)



(b)

Fig. 1. (a) Second-order 1-bit ΣΔ modulator, (b) output spectrum.

The principal challenge in the modeling of integrator nonlinearity in platforms such as Matlab stems from the dependence of the integrator output upon its previous values. That is, the nonlinearity of the op amps makes the *instantaneous* transfer of charge in the integration phase depend on the previous output voltage. Thus, even if the input/output characteristic of the op amp is expressed as $V_{out} = f(V_{in})$, that of the integrator does not lend itself to such a form.

III. Proposed Methodology

The methodology introduced here consists of four steps:

[1] This work was supported by Skyworks, Inc., and Realtek Semiconductor.

1. Based on behavioral simulations of the modulator, determine the maximum required output swing of the op amp and the corresponding input swing, $V_{in,max}$.
2. Using transistor-level dc simulations, extract the input/output characteristic of the op amp, $f(V_{in})$, for the maximum required output swing.
3. Approximate the op amp characteristic with a hyperbolic tangent ($tanh$) expression.
4. Construct a recursive integrator model in Matlab that incorporates the $tanh$ approximation.

The following sections elaborate on these steps.

A. Op Amp Model

While the input/output characteristic of op amps can be ported as a lookup table to Matlab, it is desirable to employ an analytical approximation and hence allow variation of gain and nonlinearity in behavioral simulations. Fortunately, a simple hyperbolic tangent of the form $g(V_{in}) = a\tanh(bV_{in})$ can serve this purpose. The parameters a and b are chosen to minimize the error between $g(V_{in})$ and the actual characteristic, $f(V_{in})$. Rather than applying global minimization, we simply select a and b such that:

1. $g(V_{in})$ and $f(V_{in})$ provide equal small-signal gains in the vicinity of $V_{in} = 0$:

$$a.b = \frac{d}{dV_{in}} f(V_{in})|_{V_{in}=0} \tag{1}$$

2. $g(V_{in})$ and $f(V_{in})$ are equal at the extremes of the input difference, $\pm V_{in,max}$:

$$a\tanh(\pm bV_{in,max}) = f(\pm V_{in,max}). \tag{2}$$

(The op amps are fully differential and hence exhibit odd-symmetric characteristics.) Even with only two parameters, the $tanh$ model approximates the characteristics of typical op amps with reasonable accuracy. Plotted in Figs. 2(a) and (b) are the $tanh$ and the actual characteristics of a 1.2-V cascode op amp for an output swing of ± 0.3 V in 0.13-μm CMOS technology. Fig. 2(c) shows that the error, $a\tanh(bV_{in}) - f(V_{in})$, reaches a maximum of 0.3 mV ($\approx 0.1\%$). (If fitted for an output range of ± 0.5 V, the $tanh$ approximation incurs a maximum error of ± 0.84 mV).

As expected, such a small error leads to accurate prediction of harmonic components in closed-loop circuits. For example, the simple continuous-time amplifier depicted in Fig. 3(a) exhibits the output spectra shown in Figs. 3(b) and (c) with a $tanh$ approximation and a cascode op amp, respectively. The error in the harmonic magnitudes is less than 0.2 dB.

B. Recursive Nonlinear Integrator

Fig. 4 illustrates a switched-capacitor integrator in sampling and integration phases, where C_p denotes the input capacitance of the op amp. The charge stored on C_1 at time $n-1$ is given by $C_1V_{in}(n-1)$ and transferred to C_2 and C_p to produce a new value at the output, $V_{out}(n)$. Assuming that the

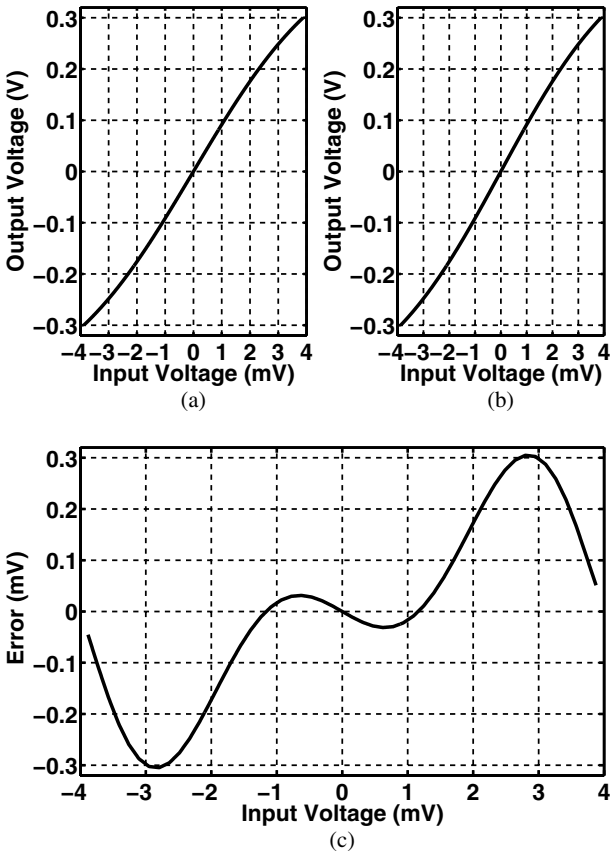


Fig. 2. (a) $Tanh$ approximation function, (b) op amp dc characteristic, (c) error function.

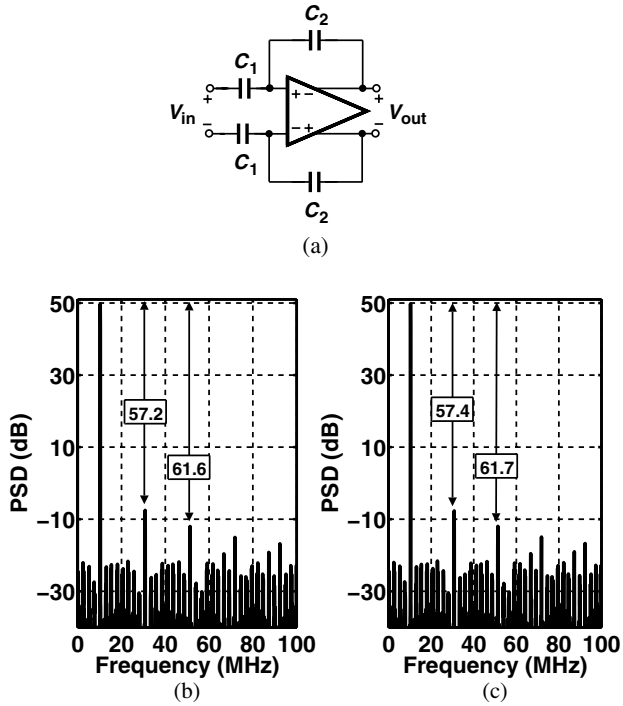


Fig. 3. (a) Continuous-time amplifier, (b) output spectrum with the $tanh$ approximation, (c) output spectrum with cascode op amp.

open-loop input/output characteristic of the op amp is approx-

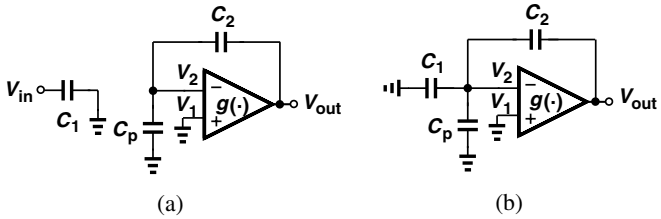


Fig. 4. Switched-capacitor integrator (a) sampling phase, (b) integration phase.

imated by $g(V_1 - V_2)$, we make the following observations:

1. The residual charge on C_1 in the integration phase is equal to $C_1 V_2(n) = -C_1 g^{-1}[V_{out}(n)]$;
2. The charge on C_2 in the integration phase is given by $C_2\{V_{out}(n) + g^{-1}[V_{out}(n)]\}$;
3. The charge on C_2 from the previous integration phase is equal to $C_2\{V_{out}(n-1) + g^{-1}[V_{out}(n-1)]\}$;
4. The change in the charge on C_p is given by $-C_p\{g^{-1}[V_{out}(n)] - g^{-1}[V_{out}(n-1)]\}$.

Equating the change in the charge on C_1 to the change in the charge on C_2 and C_p, we have:

$$\begin{aligned} C_1\{V_{in}(n-1) - g^{-1}[V_{out}(n)]\} = \\ C_2\{V_{out}(n) + g^{-1}[V_{out}(n)]\} - \\ C_2\{V_{out}(n-1) - g^{-1}[V_{out}(n-1)]\} + \\ C_p\{g^{-1}[V_{out}(n)] - g^{-1}[V_{out}(n-1)]\}. \end{aligned} \quad (3)$$

Regrouping the terms gives:

$$\begin{aligned} V_{out}(n) = V_{out}(n-1) + \frac{C_1}{C_2} V_{in}(n-1) \\ -(1 + \frac{C_1 + C_p}{C_2}) g^{-1}[V_{out}(n)] \\ +(1 + \frac{C_p}{C_2}) g^{-1}[V_{out}(n-1)]. \end{aligned} \quad (4)$$

Expressing the output of the integrator for any nonlinear characteristic, this equation can be solved using an iterative recursive procedure, e.g., the binary search iterative algorithm. For each time instance n, the algorithm begins with an initial guess equal to the ideal integrator output, i.e., if the op amp gain were infinite.

IV. Simulation Results

The proposed methodology serves as a powerful tool for analyzing $\Sigma\Delta$ modulators (and switched-capacitor filters), allowing the inclusion of various architectural concepts as well as circuit nonidealities in efficient platforms such as Matlab. Furthermore, the simple hyperbolic tangent approximation makes it possible to first determine the *minimum* acceptable op amp nonlinearity in Matlab before embarking on the design of the op amp.

In order to assess the accuracy of the proposed methodology at the integrator level, the circuit of Fig. 4 has been realized using a cascode op amp in Cadence and as a recursive behavioral model in Matlab. Fig. 5 shows the output spectra in response to an input sinusoid, indicating an error of 0.5 dB for the magnitude of the third harmonic. The Cadence and Matlab simulations take 25 minutes and 30 seconds, respectively.

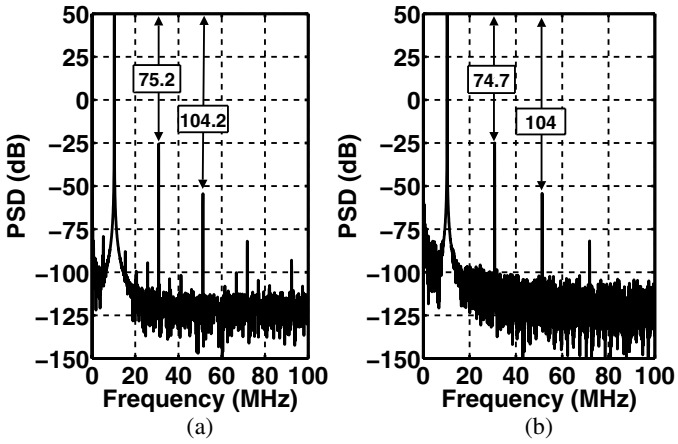


Fig. 5. Output spectrum of switched-capacitor integrator with (a) transistor-level implementation in Cadence, (b) iterative procedure in Matlab.

At the next abstraction level, we study the second-order modulator of Fig. 1 while including a five-bit quantizer to represent a more realistic case. Fig. 6(a) plots the Matlab simulation result for a behavioral model employing the $tanh$ op amp approximation and the recursive integrator solution, and Fig. 6(b) shows the output spectrum obtained from Cadence for a modulator with transistor-level implementation of both integrators. The behavioral simulation incurs an error of 0.3 dB in the magnitude of the harmonics while providing a 50x advantage in simulation speed (60 seconds versus 50 minutes).

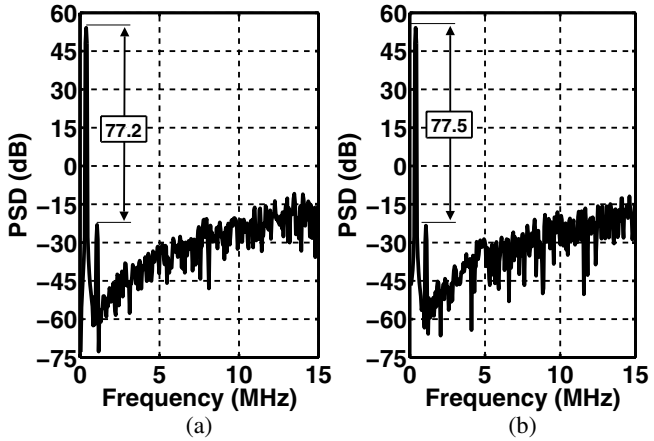


Fig. 6. Overall modulator output spectrum (a) Matlab procedure, (b) Cadence circuit simulation.

To demonstrate that the proposed methodology provides reasonable accuracies even for larger op amp nonlinearity, the cascode op amp in the first integrator is "stressed" by adjusting the output common-mode level and the above study is repeated. In each case, a $tanh$ approximation of the op amp is

created and ported to Matlab. Fig. 7 plots the relative magnitude of the output third harmonic as a function of op amp nonlinearity. (The nonlinearity is defined as the maximum deviation of the open-loop op amp characteristic from a straight line passed through the end points, normalized to the maximum output swing.) The error reaches a maximum of 1.1 dB. Fig. 8 plots the corresponding signal-to-(noise+distortion) ratio (SNDR).

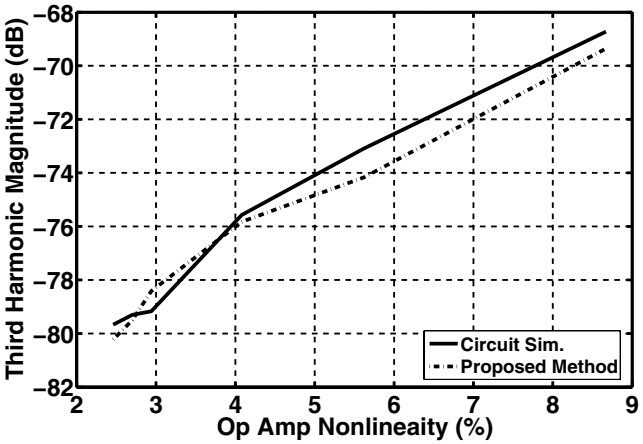


Fig. 7. Third harmonic magnitude as a function of the nonlinearity of the first op amp as predicted by transistor-level simulations and the proposed method.

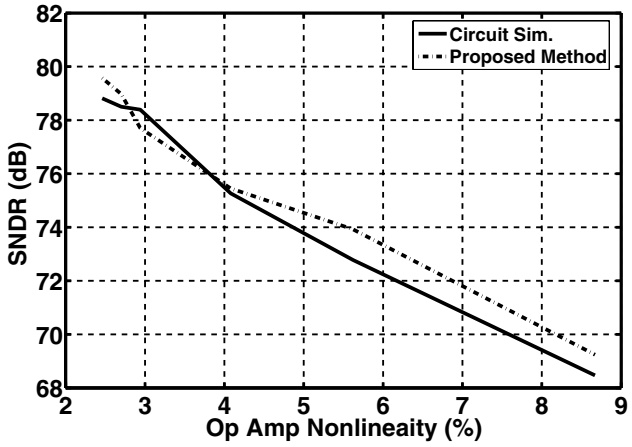


Fig. 8. Output SNDR as a function of the nonlinearity of the first op amp as predicted by transistor-level simulations and the proposed method.

The methodology allows further study of the effect of op amp nonlinearity upon the modulator performance. For example, the nonlinearity of the second integrator can be included while the first remains ideal. Fig. 9 plots the third harmonic observed at the output as a function of the nonlinearity of the second op amp. As expected, the nonlinearity in the second integrator degrades the performance to a much lesser extent, allowing a more relaxed design. Fig. 10 plots the corresponding SNDR, confirming the weak effect of the second integrator nonlinearity on the overall performance.

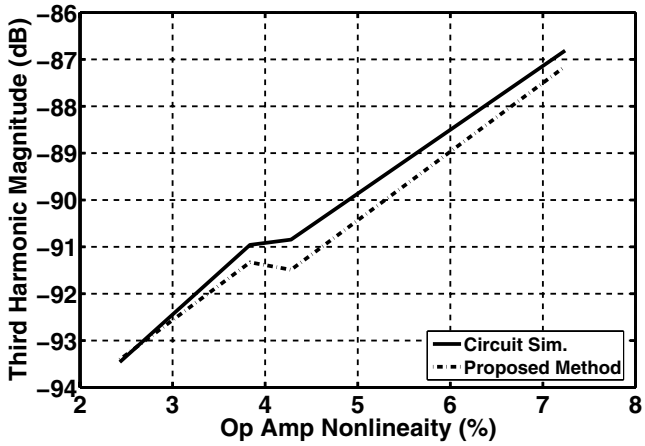


Fig. 9. Third harmonic magnitude as a function of the nonlinearity of the second op amp as predicted by transistor-level simulations and the proposed method.

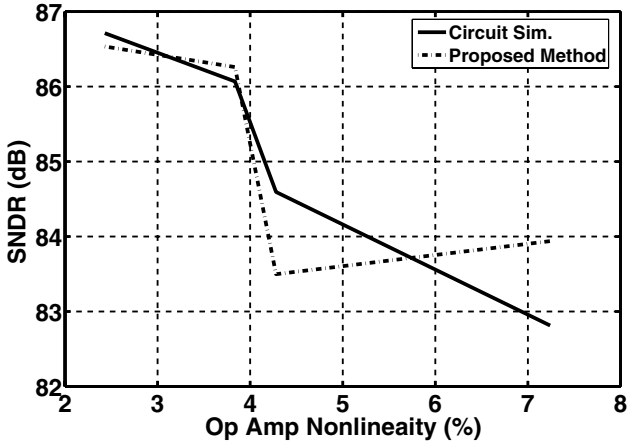


Fig. 10. Output SNDR as a function of the nonlinearity of the second op amp as predicted by transistor-level simulations and the proposed method.

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