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*Research Article*

# Modeling, Simulation, and Analysis of Novel Threshold Voltage Definition for Nano-MOSFET

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Threshold voltage ($V_{TH}$) is the indispensable vital parameter in MOSFET designing, modeling, and operation. Diverse expounds and extraction methods exist to model the on-off transition characteristics of the device. The governing gauge for efficient threshold voltage definition and extraction method can be itemized as clarity, simplicity, precision, and stability throughout the operating conditions and technology node. The outcomes of extraction methods diverge from the exact values due to various short-channel effects (SCEs) and nonidealities present in the device. A new approach to define and extract the real value of $V_{TH}$ of MOSFET is proposed in the manuscript. The subsequent novel enhanced SCE-independent $V_{TH}$ extraction method named "hybrid extrapolation $V_{TH}$ extraction method" (HEEM) is elaborated, modeled, and compared with few prevalent MOSFET threshold voltage extraction methods for validation of the results. All the results are verified by extensive 2D TCAD simulation and confirmed analytically at various technology nodes.

## 1. Introduction

Ceaseless curtailing of integrated circuit technology along with the accuracy of threshold voltage management methods and depletion in short-channel effects (SCEs) are emphasizing the threshold voltage to exceptionally low values. It is necessary to extract the precise threshold voltage ($V_{TH}$) for appropriate performance of the device. Flawlessly evaluated threshold voltage is mandatory to deliver correct and genuine gate control in channel conductivity and output characteristics of the device [1, 2]. Minor millivolt inaccuracy cannot be shirked because it may trigger grievous faults in the circuit practicality. Precisely for high-speed sturdy analog circuit nanoscale design, accurate threshold voltage evaluation is vital and crucial for accurate device behavior [3–5]. The extracted threshold voltage assists the process of device matching too. Threshold voltage is often exerted in evaluation and anticipation of device operation. The value of $V_{TH}$ is often utilized in examining the discrepancy because of manufacturing process technological parameter fluctuations. Additional utilizations of threshold voltage value are compiled as to appraise reliability elements like radiation damage, hot carrier, stress, temperature instability, and ageing degradation.

Generally, the $V_{TH}$ value is extracted specifically from the device transfer characteristics [6, 7]. The functional drain voltage ($V_{DS}$) exaggerates several SCEs like DIBL, $V_{TH}$ roll-off, punchthrough, surface scattering, velocity saturation, impact ionization, and hot electron effect. No particular evaluative analytic locus can be acknowledged as $V_{TH}$ in the device transfer characteristic curve due to subthreshold leakage phenomenon, hence causing ambiguity in the $V_{TH}$ extraction process. In the curve, weak inversion section demonstrates exponential divergence, whereas strong inversion section indicates linear/quadratic divergence. Conversely, the $V_{TH}$ is distinguished in the midst of weak and strong inversion transition sections. Threshold voltage likewise hinge on numerous device parameters (gate width, gate overlap, gate length, biased bulk, temperature, etc.) and process technology limitations ($C_{ox}$, $T_{ox}$, doping concentration, etc.), making the definition and extraction extrastrenuous [8].

In consideration of the above, the manuscript presents a new simple approach to define and extract the $V_{TH}$

of MOSFET. The corresponding novel enhanced SCE-independent $V_{TH}$ extraction method named "hybrid extrapolation extraction method" (HEEM) is further illustrated and compared with few prevalent customary MOSFET $V_{TH}$ extraction methods for validation of the results and claim the predominance of the HEEM over other extraction methods with minimum influence of short-channel effects (SCEs) and other second-order effects like DIBL, $V_{TH}$ roll-off, punch-through, surface scattering, velocity saturation, impact ionization, and hot electron effect. Rest of the paper is organized as follows. Section 2 presents the conventional threshold voltage definitions of MOSFET. Section 3 expounds the HEEM. Section 4 implements the HEEM concept on the test device and conventional MOSFET models. Furthermore, Section 5 presents the simulation results and validation of the proposed method and evaluation and analysis of discrete sub 45 nm technology nodes. Finally, concluding remarks and enhancement in the field are presented in Section 6.

## 2. Conventional Threshold Voltage Definitions of MOSFET

The conventional definition of the threshold voltage of doped semiconductor devices states that the gate voltage produces a surface potential equal to twice the fermi potential ($\varnothing_B$) in the bulk of the semiconductor [9]. Mathematically, the threshold surface potential ($\Psi_{TH}$) can be articulated as

$$\Psi_{TH} = 2\varnothing_B = \frac{1}{\beta}\ln\left(\frac{p_0}{n_0}\right) = \frac{2}{\beta}\ln\left(\frac{N_A}{n_i}\right), \quad (1)$$

where $\beta$ represents the inverse of thermal voltage and $p_0$ and $n_0$ are the equilibrium hole and electron densities, respectively [10, 11]. $N_A$ and $n_i$ are the substrate doping density and intrinsic free-carrier concentration, respectively.

Experimentally, it is observed that the modeled conventional definition does not agree well with the $V_{TH}$ value extracted from the transfer characteristic curve. Consequently, the enhanced definition was proposed for hot channel devices by including the MOSFET second-order effects. The proposed empirical term ($6/\beta$) was added to (1) for a typical range of MOSFET substrate doping concentrations and oxide thickness. The improved empirical definition is modeled as

$$\Psi_{TH} \approx 2\varnothing_B + \frac{6}{\beta}. \quad (2)$$

The conventional definition was also modified for long-channel devices by adding the corresponding empirical parameters to (1). The improved expression was developed by comparing the inversion and depletion charge terms of the device. Hence, the modified long-channel empirical definition is modeled as

$$\Psi_{TH} \approx 2\varnothing_B + \left(\frac{1}{\beta}\right)\ln\left(\frac{2\beta\varnothing_B}{\tau}\right), \quad (3)$$

where the empirical parameter $\tau = 10$ is valued for the typical range of substrate doping concentrations and oxide thickness analogous to long-channel devices. We can easily extract the subsequent threshold voltage ($V_{TH}$) from the threshold surface potential ($\Psi_{TH}$) of n-channel MOSFET using the standard basic threshold voltage MOSFET model expression.

The modified conventional definitions proposed in [10, 11] are based on the concept of intersection of the two asymptotes of the surface potential for the depletion and strong inversion region surface potential, whereas the enhanced HEEM concept is a current-based approach for evaluating $V_{TH}$ (elaborated in the Section 3). Hence, it is easier to model and simulate at nanolevel and more accurate to define even for upcoming slim ballistic transistors.

The concept proposed in [10, 11] works well for long-channel devices but deviates to give accurate results in extracting $V_{TH}$ for nano-MOSFETs with thin oxide layers and high doping densities. It also fails to generate sharp surface potential curves for nanodevices, hence asymptotic $V_{TH}$ point for nanodevices. The model equations of [10, 11] are approximate asymptotic $V_{TH}$ definition. It does not have an explicit expression for threshold voltage and gives considerable errors in predicting the $V_{TH}$ value at nanolevel technologies. Furthermore [10, 11], study includes only the classical effects with lot of approximations. The enhanced HEEM logic is applicable for both short-channel and long-channel devices and gives more accurate results. The HEEM logic generates sharp curves even working at nanotechnology node; hence, more accurate well-defined values are obtained. Simulation results validate the results shown in upcoming sections.

## 3. A Novel Approach: Hybrid Extrapolation $V_{TH}$ Extraction Method

The new simple straightforward approach of extracting the threshold voltage of nano-MOSFETs is based on globally accepted drift-diffusion model (DDM) and latterly developed ballistic, quasi-ballistic model. The transfer characteristics of MOSFET exemplify that the diffusion current governs the subthreshold region, while the drift current dominates in the linear-saturation region. The net entire current is equal to the summation of drift current and diffusion current. However, if potential across the drain to source terminals ($V_{DS}$) is zero, the net current flow is also nil as no current streams across the equipotential terminals even after biasing the gate terminal [12–14].

The constant current threshold voltage extraction method has an unclear description of critical drain current ($I_{DCRITICAL}$) liable on the technology employed. Linear extrapolation method, quadratic extrapolation method, and transition method results are highly influenced by many second-order effects like mobility degradation, short-channel effects, and extrinsic resistance effects [6, 7, 15]. Second derivative method, third derivative method, Ghibaudo method, reciprocal H-function method, and transconductance to current ratio method are extensively exaggerated by noise. The $V_{TH}$ definitions are also not based on ideal $V_{TH}$ definition condition [16]. The match point

method is seldom used as it is more laborious and more time-consuming. 5% deviation value is also an ambiguous definition of threshold voltage calculation in match point method [17]. In normalized mutual integral difference method and normalized reciprocal H-function method, the accurate evaluation of maxima in wide ranges makes the $V_{TH}$ extraction process tough and problematic [18, 19]. The HEEM has the competence to accurately determine the threshold voltage ($V_{TH}$) of MOSFET and totally remove or nullify the abovementioned flaws of the predefined existing extraction methods.

For simplicity, we have only considered the n-channel MOSFET to illustrate this unique HEEM approach. Similar analysis can be extended for p-channel MOSFET. Following assumptions are made purposely: the device is considered to be laterally symmetrical and the source, drain, and bulk terminals are considered to be grounded; hence, no potential exists amongst the corresponding terminals, the gate is made of n+ polysilicon with work function $q\varnothing_M = 4.24$eV, the immobile charge in the oxide near the oxide-semiconductor interface has the same dispersal over both p and n regions, and the interface traps or interface states have the same distribution for both the p and n parts of the device close to metallurgical junction.

With the drain and source terminals grounded, the gate terminal governs the charge in the channel. When a small positive-biased voltage is applied to the gate of n-channel MOSFET, the state within the channel will alter. The free holes present in p-type silicon are deterred, thus forming a depletion region in the channel. This depletion region is formed over both lateral and vertical directions, that is, across the length and width of the channel. Increasing the positive gate voltage further will eventually lead to the saturation of the depletion depth. Once the saturation of the depletion region is reached, additional gate voltage will entice negative mobile electrons to the channel surface [20]. When adequate electrons have accrued in the channel area, the surface of the channel alters from the hole-dominated to the electron-dominated silicon material and is said to have inverted. Under this condition, a steering n-channel or inversion layer is formed under the gate between the two n+ silicon materials, namely, source and drain regions. Additional upsurge in gate voltage will only increase the surface potential of the channel gradually beyond $2\phi_B$, whereby the increased gate voltage drops across the gate oxide. The minimum gate voltage required to form the conducting channel or an inversion layer underneath the surface is called as threshold voltage ($V_{TH}$). Figure 1 represents the 10 nm test device simulation results of drift current and diffusion current components versus gate voltage ($V_{GS}$) for $V_{DS} = 0.1$ V. We can further classify the four MOSFET operation states as depletion region, weak inversion, moderate inversion, and strong inversion in reference.

The drift-diffusion model (DDM) states that the total current across the channel is the sum of drift current and diffusion current as [21] $I_{TOTAL} = I_{DRIFT} + I_{DIFFUSION}$. The DDM and even the Landauer approach (Boltzmann transport equation) in ballistic, quasi-ballistic nano-MOSFET models advocate that with the source and drain terminals grounded ($V_{DS}$ = 0V), the total current flow is zero because of the zero potential drop across the terminals. However, if we plot the discrete components of the total current versus gate voltage, we see nonzero values and are exactly equal but opposite in direction of flow as both drift and diffusion currents balance each other [22]. The drift and diffusion current components literally equivalent but contrary in polarity can be termed as *junction current* 1 ($I_{JNSC}$) flowing between source and channel junction and *junction current* 2 ($I_{JNDC}$) flowing between drain and channel junction. Both the junction currents would be equal due to the symmetrical applied conditions and parameters. Hence, we can collectively denote both the junction currents $I_{JNSC}$ and $I_{JNDC}$ by $I_{JNC}$. Gradually increasing the gate voltage from zero to high bias ($V_{DD}$), the drift-diffusion current density and drift-diffusion current components ($I_{DRIFT}$ and $I_{DIFFUSION}$) also increase as shown in Figure 2. Consequently, we can conclude that $I_{JNC}$ also increases with the increase in gate bias

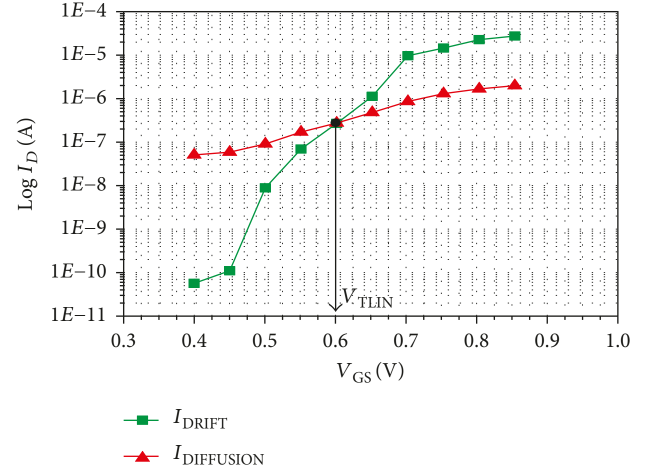


FIGURE 1: 10 nm test device simulation results of drift current and diffusion current versus gate voltage ($V_{GS}$) for $V_{DS} = 0.1$ V.

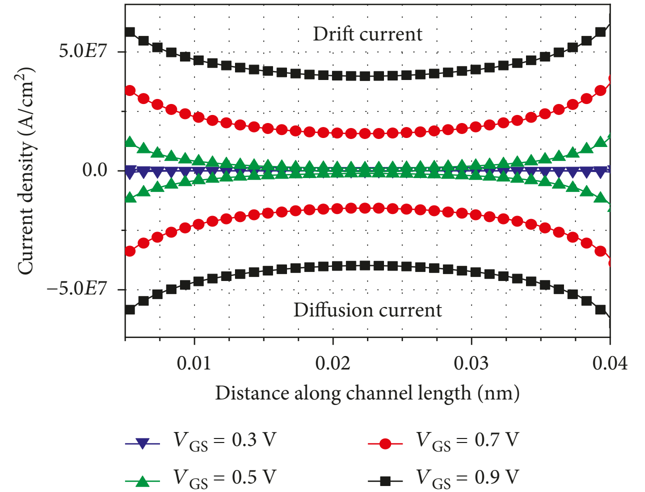


FIGURE 2: Drift-diffusion current density along the channel length for different gate voltages with $V_{DS} = 0$ V.

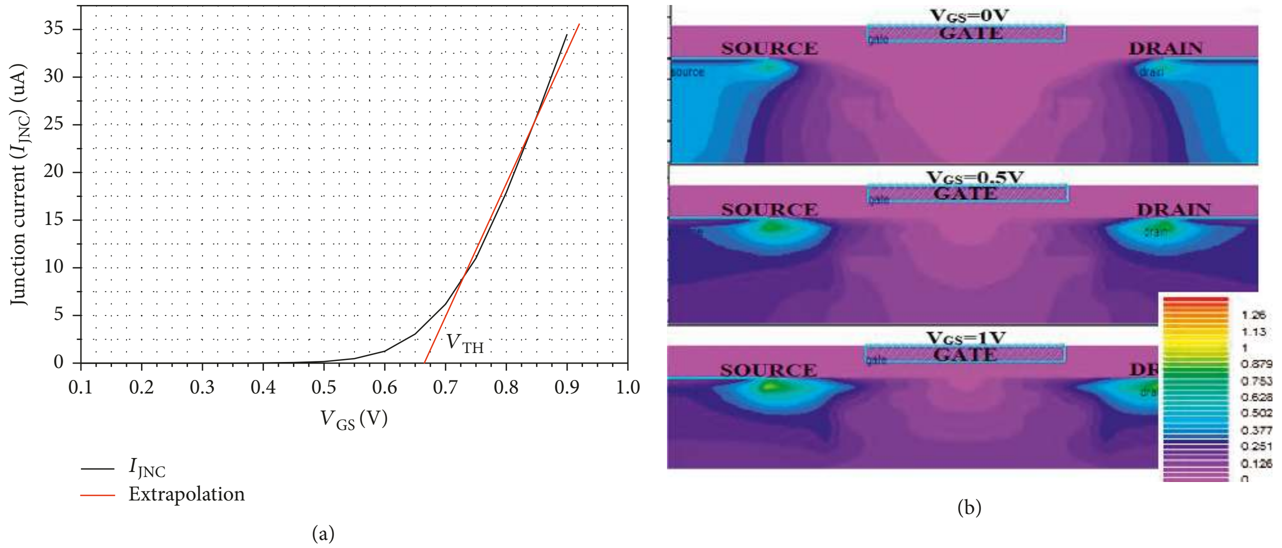


Figure 3: (a) Hybrid extrapolation $V_{TH}$ extraction method ($I_{JNC}$ value versus $V_{GS}$ plot). Extrapolation of the $I_{JNC}$ curve extracts the $V_{TH}$ value. (b) The $I_{JNC}$ flow density (A/cm$^2$) contour plots along the channel length ($L$) for distinct gate potentials ($V_{GS} = 0$ V, $V_{GS} = 0.5$ V, and $V_{GS} = 1$ V). Reference isoline represents the current flow density (A/cm$^2$).

terminal. However, $I_{TOTAL}$ remains zero because of the contrary flow direction of the distinct current components. Figure 2 justifies the logic as it can be seen that the drift current density is the same as the diffusion current density but opposite in polarity [23].

As per the assumptions and the applied conditions in our HEEM, the subsequent $I_{JNC}$ value is nearly zero (negligible) in the subthreshold region. A linear/quadratic increase is witnessed in the $I_{JNC}$ numerical value as the inversion layer is formed. Hence, we are able to efficiently extract vital $V_{TH}$ by plotting $I_{JNC}$ versus $V_{GS}$. Extrapolation of the $I_{JNC}$ versus $V_{GS}$ curve at the inflexion point gives an accurate threshold voltage. The threshold voltage is found at the intercept of the tangent in the inflexion point with the $V_{GS}$ axis. The linearity of the curve allows an easy extrapolation for better results as seen in Figure 3(a). The $I_{JNC}$ numerical value required for plotting the extraction curve is modeled in the subsequent section for reference. However, the $I_{JNC}$ value can be extracted easily from the TCAD simulation tools also. The $I_{JNC}$ flow density contour plots along the channel length for distinct gate potentials ($V_{GS}$) are simulated and shown in Figure 3(b) of 10 nm n-channel MOSFET test device. We can clearly see no current flow in the channel at $V_{GS} = 0$ V. However, contour of current flow is observed at the source-channel junction and drain-channel junction at $V_{GS} = 0.5$ V and increases with the gate bias ($V_{GS} = 1$ V). The current flow contour remains zero even at high gate bias (higher than the threshold voltage) exactly at the channel length position $x = L/2$ representing no current flow between source and drain terminals.

The extraction procedure is autonomous of drain-biased short-channel effects, extrinsic series resistances, mobility degradation, slope factor variations, and channel length modulation, allowing a direct accurate determination of the threshold voltage. Hence, it is more effective and fast in extracting $V_{TH}$ for both short-channel and long-channel devices. Exhaustive numerical simulations at various technology nodes and analytical results to demonstrate the extraction procedure are used to certify the proposed logic with conviction.

## 4. Implementation of Hybrid Extrapolation Extraction Method

The new hybrid extrapolation extraction method is implemented on test device and statistically evaluated using well-established MOSFET models. Comparison amid various conventional extraction methods and the new proposed method is performed on both technology CAD simulation and measurement in order to endorse the new enhanced extraction technique and related theory [10–12]. As described, the enhanced extraction method is independent of drain-biased short-channel effects, extrinsic resistances, channel length modulation, and mobility degradation. Hence, it is more effective in extracting $V_{TH}$ for both short-channel and long-channel devices.

*4.1. Execution of HEEM on Test Device.* A basic square-sized bulk NMOS structure is contemplated for TCAD execution. The nanodevice is modeled with channel length ($L_G$) = 10 nm, gate oxide thickness ($T_{ox}$) = 1 nm, bulk doping concentration ($N_{BULK}$) = $10^{17}$ cm$^{-3}$, and junction depth ($X_j$) = 8 nm. For generalization of the outcomes, uniform doping is deemed all through the bulk [24, 25]. Gaussian doping with the maximum limit of $10^{20}$ cm$^{-3}$ is modeled in source and drain regions for realistic results, whereas the extensions are planted and doped with the concentration of $10^{19}$ cm$^{-3}$ to reduce the GIDL consequences. Source-drain extensions expand 2 nm underlap, making the channel as an enhanced controlled and conductive path. Various parameters are considered to be steady in relation with the channel

Table 1: Comparison of $V_{TH}$ extraction methods for 10 nm test device.

| Method | $V_{DS}$ | $V_{TLIN}$ |
|---|---|---|
| Hybrid extrapolation extraction method | 0 V | 0.67 V |
| Linear extrapolation method (LEM) | 0.1 V | 0.68 V |
| Second derivative method (SDM) | 0.1 V | 0.675 V |
| Ghibaudo method (GM) | 0.1 V | 0.6 V |
| Match point method (MPM) | 0.1 V | 0.65 V |

length scaling (EOT = 1 nm, $N_{BULK} = 10^{17}$ cm$^{-3}$). The physical models deployed for unblemished outcomes include ballistic, quasi-ballistic, doping-dependent mobility with high-field saturation and degradation, Shockley-Read-Hall and tunneling models, and analytical model for efficacious temperature-dependent extractions. The model MOSFET incorporates the supply voltage of 0.9 V.

As per the set condition, $V_{DS} = 0$ V; hence, the proposed method will return a unique threshold value which can be considered as $V_{TH}$ of the device. The extracted threshold voltage value is independent of short-channel effects like DIBL and threshold voltage roll-off and many other second-order effects instigated due to drain bias.

The outcome of the hybrid extrapolation $V_{TH}$ extraction method for 10 nm test device and comparison with other predominant $V_{TH}$ extraction methods are shown in Table 1 (refer Figures 4(a)–4(d)).

$V_{TLIN}$ represents the threshold voltage with MOSFET operating in the linear region. The extracted value is found to accord with other recognized threshold extraction methods. The minor variation of the outcomes of the other predominant methods may be probably due to neglecting the SCE and second-order effects. The validity of this new proposed HEEM was verified for long-channel devices also. The test device considered for the long channel is a square-sized uniformly doped bulk-driven n-channel MOSFET with 180 nm channel length. Most common extraction methods were also applied to extract the threshold voltage in similar conditions. The extracted values using HEEM were found to accord with other recognized $V_{TH}$ extraction methods [24, 25]. The outcomes of various extraction methods for 180 nm test device are shown in Table 2.

The $V_{TH}$ extracted value using HEEM is very close to the few of the most popular $V_{TH}$ extraction methods. The overestimation of the other predominant methods may be probably due to neglecting the second-order effects. Hence, we can conclude that the HEEM is equally effective for both short-channel devices and long-channel devices [26, 27].

*4.2. Execution of HEEM on MOSFET Models.* Diffusion current is a type of current in a semiconductor instigated by the variance of charge carrier concentration (holes and/or electrons), whereas the drift current is due to the transport of charge carriers prompted by an electric field force exerted on them. Diffusion current can be in the same or conflicting direction of a drift current. The sum of diffusion current and drift current collectively are designated by the drift-diffusion equation [28].

Four autonomous current mechanisms in our n-type MOSFET test device are possible. These components are the majority carriers' electron drift current and diffusion current as well as the minority carriers' hole drift current and diffusion current. The complete current density is the summation of these four components. For one-dimensional instance, we can inscribe the concept as [4, 5]

$$J = \left[(nq\mu_n E_x) + (nq\mu_P E_x)\right] + \left[\left(qD_n\frac{dn}{dx}\right) - \left(qD_p\frac{dp}{dx}\right)\right]. \tag{4}$$

Equation can be generalized to three-dimensional format as

$$J = \left[(nq\mu_n E) + (nq\mu_P E)\right] + \left[(qD_n\nabla n) - (qD_p\nabla p)\right], \tag{5}$$

where $D_n$ and $D_p$ are electron and hole diffusion coefficients, respectively, $n$ is the number of electrons per unit volume, global symbol $q$ represents the electron charge, and $\mu_n$ and $\mu_p$ denote the electron and hole mobility in the medium, respectively. The electric field $E = -\frac{d\phi}{dx}$, where $\phi$ indicates the potential difference. The logic is expressed as

$$J_{TOTAL} = J_{DRIFT} + J_{DIFFUSION} = nq\mu E + qD\frac{dn}{dx}. \tag{6}$$

We also know $D = \mu\phi_t$ as Einstein relationship on electrical mobility. Thermal voltage $(\phi_t) = KT/q$, with $K$ as the Boltzmann coefficient and $T$ representing temperature in Kelvin. Thus, substituting $E$ for potential gradient in (6) and multiplying both sides with $e^{-\varnothing/\varnothing_t}$, we get

$$Je^{\frac{-\varnothing}{\varnothing_t}} = qD\left[\frac{-n}{\varnothing_t}\frac{d\varnothing}{dx} + \frac{dn}{dx}\right]e^{\frac{-\varnothing}{\varnothing_t}} = qD\frac{d\left(ne^{\frac{-\varnothing}{\varnothing_t}}\right)}{dx}. \tag{7}$$

Integrating (7) over depletion region of channel-source P-N junction assuming $xd$ as the depletion thickness, we get

$$J = \frac{qD_n e^{\frac{-\varnothing}{\varnothing_t}}}{\int\left(e^{\frac{-\varnothing}{\varnothing_t}}\right)dx} = \frac{qD_n N_a e^{\frac{-\varnothing_B}{\varnothing_t}}\left[\left(e^{\frac{V_{IN}}{\varnothing_t}}\right) - 1\right]}{\int\left(e^{\frac{-\varnothing_1}{\varnothing_t}}\right)dx}, \tag{8}$$

where $N_a$ and $N_d$ characterize the doping concentration of n region (source) and p region (channel), respectively. $\varnothing_B$ is built-in barrier potential and $V_{IN}$ denotes input voltage.

With $\varnothing_1 = \varnothing_B + (\varnothing_i - V_{IN})$, the denominator of (8) can be simplified. We know $\varnothing = -qN_d/2\varepsilon_s(x - x_d)^2$.

Therefore, the expression can be expressed as

$$\varnothing_1 = \frac{qN_d x\left(x_d - \dfrac{x}{2}\right)}{\varepsilon_s} = (\varnothing_i - V_{IN})\frac{x}{x_d}, \tag{9}$$

where $\epsilon_s$ denotes the permittivity of the material.

Since $x \ll x_d$, the term $(x_d - x/2) \approx x_d$.

Using the above approximation in (9), we get

$$\int\left(e^{\frac{-\varnothing}{\varnothing_t}}\right)dx = \frac{x_d(\varnothing_i - V_{IN})}{\varnothing_t}, \tag{10}$$

when $(\varnothing_i - V_{IN}) > \varnothing_t$; we obtain the current due to diffusion.

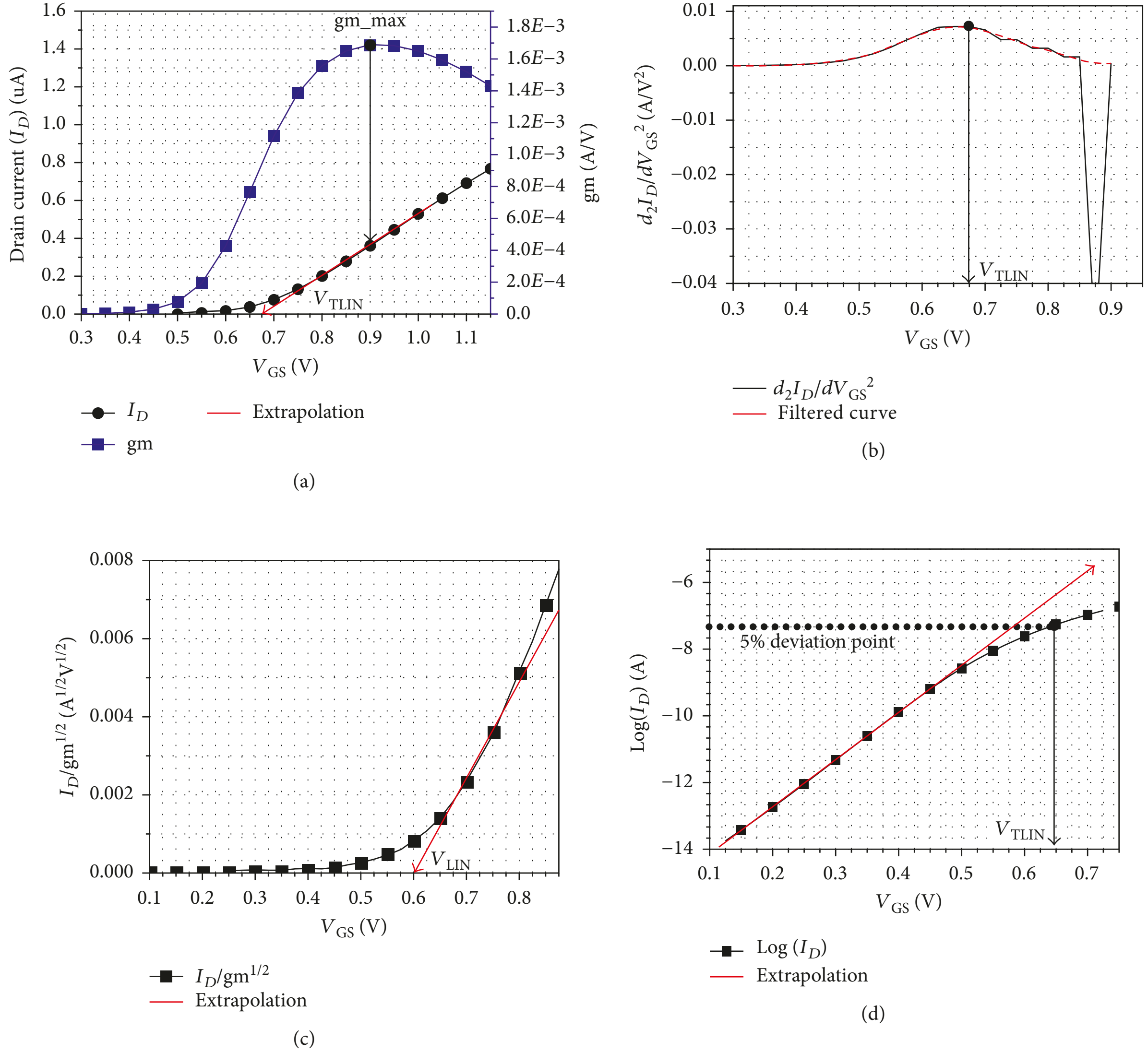


Figure 4: (a) Extraction of $V_{TLIN}$ using LEM for $V_{DS} = 0.1$ V. (b) Extraction of $V_{TLIN}$ using SDM for $V_{DS} = 0.1$ V. (c) Extraction of $V_{TLIN}$ using Ghibaudo method for $V_{DS} = 0.1$ V. (d) Extraction of $V_{TLIN}$ using match point method for $V_{DS} = 0.1$ V.

The net total current density can be described as

$$J = \frac{2qDN_a}{\varnothing_t}\sqrt{\frac{2q}{\varepsilon_s}(\varnothing_i - V_{IN})N_d}\left[e^{\frac{-\varnothing_B}{\varnothing_t}}\left(e^{\frac{V_{IN}}{\varnothing_t}} - 1\right)\right]. \quad (11)$$

From (11), we can observe that current depends exponentially on the input voltage ($V_{IN}$) and the barrier height ($\varnothing_B$). $V_{IN}$ can be written as a function of electric field intensity as

$$E_{max} = \sqrt{\frac{2q}{\varepsilon_s}(\varnothing_i - V_{IN})N_d}. \quad (12)$$

Manipulation and substitution in (11) gives

$$J = q\mu N_a E_{max}\left[e^{\frac{-\varnothing_B}{\varnothing_t}}\left(e^{\frac{V_{IN}}{\varnothing_t}} - 1\right)\right]. \quad (13)$$

From (13), one can observe that when zero input voltage ($V_{IN}$) is observed, the drift current entirely balances the diffusion current. Hence the net current flow density at zero potential $V_{IN}$ is always zero as the source and drain terminals are presumed to be grounded as per the assumptions and applied conditions in our HEEM.

Table 2: Comparison of $V_{TH}$ extraction methods for 180 nm test device.

| Method | $V_{DS}$ | $V_{TLIN}$ |
|---|---|---|
| Hybrid extrapolation extraction method | 0 V | 0.575 V |
| Linear extrapolation method (LEM) | 0.1 V | 0.585 V |
| Second derivative method (SDM) | 0.1 V | 0.585 V |
| Ghibaudo method (GM) | 0.1 V | 0.58 V |
| Match point method (MPM) | 0.1 V | 0.58 V |

The above outcome of HEEM can also be performed through the well-established MOSFET charge sheet model (CSM). We represent the CSM complete expression of drain current ($I_{DS}$) valid for all the operating regions and confirm

Table 3: Comparison of the simulation results of $V_{TH}$ extraction methods for various sub 45 nm technologies.

| Method | 10 nm TN | | 16 nm TN | | 22 nm TN | | 32 nm TN | | 45 nm TN | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{TLIN}$ | $V_{TSAT}$ | $V_{TLIN}$ | $V_{TSAT}$ | $V_{TLIN}$ | $V_{TSAT}$ | $V_{TLIN}$ | $V_{TSAT}$ | $V_{TLIN}$ | $V_{TSAT}$ |
| CCM | 0.355 V | 0.104 V | 0.463 V | 0.369 V | 0.479 V | 0.425 V | 0.440 V | 0.396 V | 0.433 V | 0.403 V |
| LEM | 0.683 V | N.A | 0.719 V | N.A | 0.706 V | N.A | 0.653 V | N.A | 0.634 V | N.A |
| SDM | 0.675 V | 0.437 V | 0.7 V | 0.6 V | 0.675 V | 0.6 V | 0.649 V | 0.552 V | 0.626 V | 0.578 V |
| GM | 0.59 V | 0.51 V | 0.645 V | 0.575 V | 0.645 V | 0.56 V | 0.6 V | 0.525 V | 0.6 V | 0.5 V |
| MPM | 0.7 V | 0.55 V | 0.7 V | 0.625 V | 0.7 V | 0.675 V | 0.65 V | 0.675 V | 0.65 V | 0.675 V |
| HEEM | 0.675 V | N.A | 0.675 V | N.A | 0.675 V | N.A | 0.625 V | N.A | 0.625 V | N.A |

the HEEM concept using the respective model. The model uses the source-end surface potential and drain-end surface potential to extract the complete drain current expression.

In the CSM, the channel depletion area is obtained under the assumption that the substrate is uniformly doped ($N_B$). We presume the source and drain junctions are geometrically symmetrical in shape with a radial junction depth ($X_j$), and the channel depletion area is linearized in terms of only source- and drain-end surface potentials. $X_{dms}$ and $X_{dmd}$ represent the depletion depth across the channel aside the source and drain regions, respectively. Thus, the bulk charge density can be obtained. Statistically, the CSM model equation of the net drain-to-source current can be represented as follows [4, 5].

Let $x$ be the horizontal position in the channel, measured from the source end. If inversion layer current in lateral direction at any position $x$ is denoted by $I(x)$, then we have

$$I(x) = I_{DRIFT}(x) + I_{DIFFUSION}(x). \quad (14)$$

$I_{DRIFT}(x)$ as drift current contribution and $I_{DIFFUSION}(x)$ as the diffusion current contribution at point $x$.

The intricate CSM drain current can be modeled as

$$\begin{aligned} I_{DS} = \left(\frac{W}{L}\right)\mu C'_{ox}(\Psi_{sL} - \Psi_{s0})\Bigg[ (V_{GB} - V_{FB}) - \frac{1}{2}(\Psi_{sL} - \Psi_{s0}) \\ - \frac{2\gamma}{3}\frac{\left(\Psi_{sL} + \sqrt{\Psi_{sL}\Psi_{s0}} + \Psi_{s0}\right)}{\left(\Psi_{sL}^{1/2} + \Psi_{s0}^{1/2}\right)} \\ - \phi_t\left(1 + \frac{\gamma}{\left(\Psi_{sL}^{1/2} + \Psi_{s0}^{1/2}\right)}\right)\left(\Psi_{sL}^{3/2} - \Psi_{s0}^{3/2}\right)\Bigg], \end{aligned} \quad (15)$$

with $\Psi_{s0}$ and $\Psi_{sL}$ expressing the surface potential at channel length $x = 0$ and $x = L$, respectively. $\gamma$ denotes the body effect coefficient. $W$ indicates the width of the channel. $C'_{ox}$ is oxide capacitance per unit area. $V_{GB}$ and $V_{FB}$ describe the gate-to-bulk voltage and flat band voltage, respectively.

As per the assumptions and the applied conditions in HEEM, $\Psi_{sL} = \Psi_{s0}$ (the source terminal and drain terminal are equipotential). The channel depletion region area is symmetrical across the channel length around the source and drain region area due to the assumed balanced doping and regular geometry. Hence, we can perceive from the model (15) that the net current is always zero in the described situation. Consequently, in this state, we can further conclude that the drift current totally balances the diffusion current; that is, the drift current value is exactly equivalent to the diffusion current value but with the contrary direction.

## 5. Simulation Results and Validation of the Proposed Method

The HEEM logic is explored and executed at 10 nm MOSFET IC technology along with discrete additional existing sub 45 nm IC technologies. The outcomes are corroborated through immense 2D TCAD simulation and analytically reaffirmed using industry standard tools. Discrete PT models developed by the Nanoscale Integrations and Modeling (NIMO) Group at Arizona State University (ASU) are employed to exemplify the outcomes [25]. The models are capable of capturing numerous second-order effects to forecast the accurate device characteristics [29–32].

The validation of the new proposed hybrid extrapolation extraction method was accomplished by two-dimensional (2D) numerical simulations, and brief analysis was carried out on both short-channel NMOS and long-channel NMOS devices. First, using numerical simulations, $I_{JNC}$ was monitored as a function of the gate voltage (Figures 2 and 3(a)). $I_{JNC}$ has an exponential behavior for positive low gate voltages less than $V_{TH}$, which corresponds to the weak inversion conferring to the MOS theory. Further increasing the gate voltage, we observe a linear/quadratic increase in $I_{JNC}$ corresponding to the transition of the surface from weak to moderate/strong inversion. This transition is considered as the definition of the threshold voltage of the device.

In the second phase of validation, the results of $V_{TH}$ extraction using HEEM was compared with other recognized threshold extraction methods, namely, CCM, LEM, SDM, GM, and MPM [15–18]. The HEEM's extracted $V_{TH}$ value was found to accord with the other referred extraction methods. The extracted $V_{TH}$ values are presented in Table 3. Compact meshing and larger added checkpoints can improve the extraction accuracy.

A number of existing $V_{TH}$ extraction methods were put forward, analyzed, and analytically compared their respective outcomes with the presented HEEM concept. The comparative extracted $V_{TH}$ values of presented extraction methods were simulated and analyzed in the same analogous conditions. Table 3 presents comparative $V_{TH}$ extraction values of HEEM along with largely applied threshold extraction methods, namely, CCM, LEM, SDM, GM, and MPM for bulk-driven

nano-MOSFETs at 10 nm IC technology along with discrete sub 45 nm IC technologies. The $V_{TH}$ value was also evaluated applying PT models on test device at various IC technologies, namely, 10 nm, 16 nm, 22 nm, 32 nm, and 45 nm IC technologies [25, 32]. The comparative outcome confirms that the HEEM extracts the accurate threshold voltage results for both short-channel and long-channel devices. $V_{TLIN}$ and $V_{TSAT}$ in Table 3 represent the threshold voltage with MOSFET operating in the linear region and saturation region, respectively.

## 6. Conclusion

The robust analysis and comparison of various existing $V_{TH}$ extraction methods were employed to determine the $V_{TH}$ value test device. HEEM $V_{TH}$ logic was also employed in similar conditions, manifesting the new extraction approach HEEM as the improved extraction method for direct determination of threshold voltage, superior with minimum influence of second-order effects like DIBL, short-channel effect, $V_{TH}$ roll-off, punchthrough, surface scattering, velocity saturation, impact ionization, and hot electron effect. It is very beneficial and convenient for accurate extraction of $V_{TH}$ for both short-channel and long-channel devices as it is based on the physics of the device. The other augmentation of this method can be listed as the threshold voltage outcome value is exclusive ($V_{TH}$) for all operating regions unalike outcomes of other extraction methods that normally generate $V_{TH}$ in the linear region ($V_{TLIN}$) and $V_{TH}$ in the saturation region ($V_{TSAT}$). The linearity of the $I_{JNC}$ versus $V_{GS}$ curve allows an easy extrapolation for better results. The HEEM is independent of drain-biased short-channel effects, extrinsic resistances, mobility degradation, channel length modulation, etc. Hence, it gives more precise results for both short-channel devices and long-channel devices.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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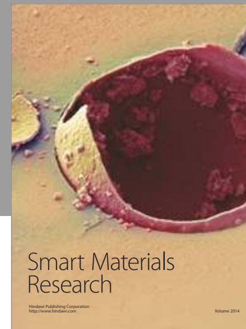
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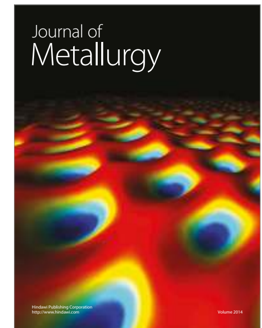
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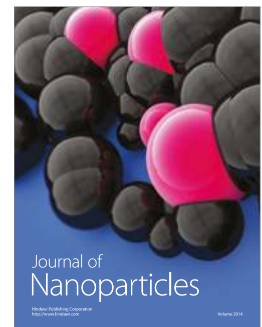
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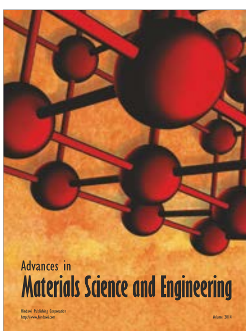
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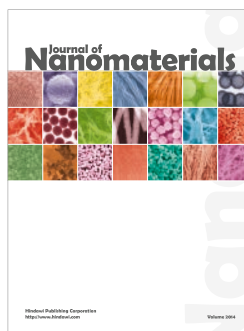
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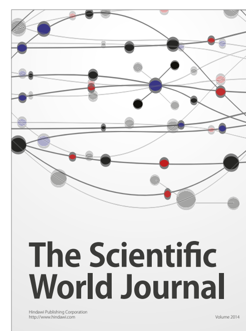
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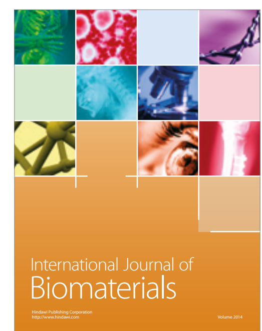
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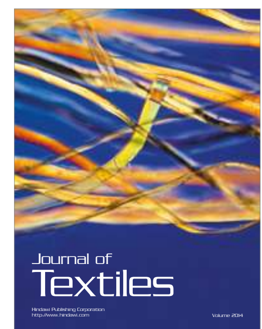
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