Modeling Snapback and Rise-time Effects in TLP Testing for ESD MOS Devices Using BSIM3 and VBIC Models

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ABSTRACT

A simple SPICE macro model has been created for ESD MOS modeling. The model consists of standard components only, mainly a MOS transistor modeled by BSIM3v3, a bipolar transistor modeled by VBIC, and a resistor for substrate resistance. It offers advantages of convenience in CAD implementation, high simulation speed, wider availability, and less convergence issues. The modeling approach has been used to investigate rise-time effects in TLP stress testing. The simulation, as well as measurement, demonstrated that the rising edge of TLP pulse affects snapback trigger voltage *Vt1* not only in gate coupled NMOS but also grounded gate NMOS devices. It implies that the base transit time and the junction capacitance of parasitic BJT have impact on trigger voltage *Vt1*.

***Key words*:** ESD, MOS, SPICE, macro model, snapback, rise-time

1. INTRODUCTION

ESD (Electro-Static Discharge) becomes a more serious reliability concern for IC chips as semiconductor devices scale toward smaller dimensions. On-chip protection circuits are widely used to protect IC chips from ESD damages. ESD protection circuits have interaction with I/O buffers and core circuitry. It is important to have integrated simulation for ESD and core function circuits to assure both ESD protection and core circuitry work properly and reduce design iteration. The main tool used by circuit designers is SPICE using compact models. SPICE can provide a circuit level simulation platform that incorporates ESD protection and core function parts into an integrated electronic circuit. The SPICE simulation also provides a way to monitor current flows inside of a circuit schematic, which provides helpful insight to circuit operation.

Conventional compact SPICE models are not designed for ESD simulation. Many effects important to ESD are not modeled at all or modeled insufficiently. MOS transistors operating in snapback mode are widely used as ESD protection in CMOS technology. The parasitic lateral bipolar transistor in the NMOS and its Collector/Base breakdown, are the key factors to snapback-based MOS ESD protection circuitry. BSIM3, the most widely used MOS model, like most other SPICE MOS models, does not include the lateral parasitic bipolar transistor and the junction breakdown effect [1].

Numerical SPICE modeling efforts on snapback-based MOS ESD simulation have been publicly reported (for example, [2,3,4]). These approaches extend main MOS with three additional components: a BJT, a current source and a substrate resistor. These models usually need special SPICE implementations, which may limit the availability of the models and/or have disadvantages of low simulation speed and possible convergence issue.

We have proposed a practical approach that uses SPICE macro models for the snapback of MOS ESD protection devices [5]. The macro model is constructed from standard circuit elements only. This paper will present using the modeling approach to investigate rise-time effects in pulse stress testing. The simulation demonstrated that the base transit time and the junction capacitance of parasitic BJT have impact on trigger voltage *Vt1*. The results explain the rise-time effects on *Vt1* observed in measurement.

2. SNAPBACK AND SPICE MODELS

2.1 Snapback Effect

Under a certain gate bias, MOS transistor behavior consists essentially of four stages. As the drain voltage V_d increases from 0, the device first enters the linear region and then the saturation region. The characteristic in these two regions is modeled well by standard SPICE MOS equations. Further increasing V_d, the device will enter the avalanche breakdown region that is influenced both by the MOSFET and the parasitic NPN bipolar transistor and then the snapback region which is dominated by the parasitic BJT. In ESD events, the device mostly operates in sanpback mode. Continuing increasing V_d will eventually lead to secondary snapback and device destruction.

Once V_d reaches the avalanche region, the electrical field in the depletion layer of the reverse-biased drain-substrate junction becomes high enough that many electron-hole pairs are generated by impact ionizations. The electrons are collected at the drain and the holes are injected into the substrate, contributing to the substrate current I_{sub}. The I_{sub} increases the voltage drop across the substrate resistance (V_{be} for the lateral BJT), which causes electrons emitted into the substrate from the source. When V_{be} reaches ~0.5V, the BJT turns on and the electron current reaching the drain

further increases the generated electron-hole pairs. Since a high electrical field is no longer needed to maintain the current level through impact ionization alone, the drain voltage decreases and snapback happens. The modeling accuracy of the voltage drop across the substrate resistance is critical since it determine when snapback occurs. Snapback effect is usually measured with transmission line pulse (TLP) technique, which is mostly regarded as a quasi-static event.

2.2 Basics of Snapback Models

A MOS model for snapback effect consists of four essential components: a main MOS, a parasitic BJT, a current source for the avalanche current, and a resistor for substrate resistance (Figure 1). The BJT is usually modeled with EM (Ebers-Moll) or GP (Gummel-Poon) equations. The avalanche current is modeled as [6]

$$Igen=(M-1)\cdot(Ids+Ic) \tag{1}$$

where M is the multiplication fact, Ids is the MOS surface drain current, and Ic is the BJT collector current. M is a function of the drain voltage and the saturation voltage $Vdsat$ of the MOS. It is often given by "Miller formula":

$$M = \frac{1}{1 - K1 \cdot \exp\left(-\frac{K2}{Vd - Vdsat}\right)} \tag{2}$$

where $K1$, $K2$ are fitting parameters related to drain depletion width and impact ionization coefficients. To overcome the discontinuity of M in equation (2), a continuous function was introduced in [7]:

$$M = \exp\left[k1(Vd - Vdsat - d1)\right] + \exp\left[k2(Vd - Vdsat - d2)\right] \tag{3}$$

where $k1$, $k2$, $d1$ and $d2$ are fitting parameters.

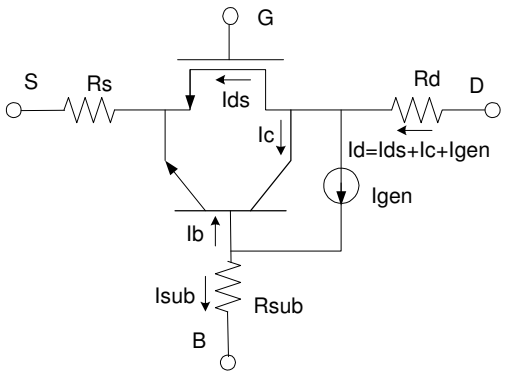

Figure 1: Basic Subcircuit of ESD Compact Model

There are some different versions, such as using two current sources for *Igen*, using a dynamic substrate resistance.

Special setups in CAD are needed to implement current source and/or substrate resistance. The models have to be implemented either as a new SPICE model [2], or using behavior languages Verilog-A [3]. The later could significantly lower simulation speed and may cause convergence problems. And both implementations may have limited availability and less accessible to circuit designers.

2.3 Macro Model Using BSIM3 and VBIC

The subcircuit we use is shown in Figure 3. In this subcircuit, all elements are standard SPICE devices and there are no explicit external current or voltage sources. The NMOS is modeled with BSIM3V3 and the BJT with three terminal VBIC model.

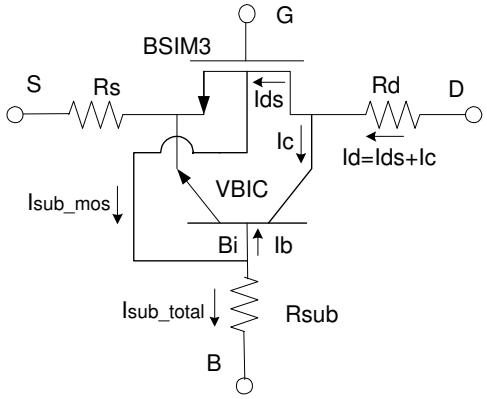

Figure 2: New subcircuit for ESD snapback simulation

We take the advantage of the substrate current modeling in BSIM3 and the collector base avalanche modeling in VBIC. The substrate current in BSIM3 model is given by

$$Isub = \left(\alpha 1 + \frac{\alpha 0}{Leff}\right)\cdot(Vds - Vdeff)\cdot e^{\left(-\frac{\beta 0}{Vds - Vdeff}\right)Idsa} \tag{4}$$

where $Idsa$ is the drain current without considering of impact ionization, $Leff$ is the effective channel length of the MOS, $Vdseff$ becomes $Vdsat$ in the saturation region, and $\alpha 0$, $\alpha 1$ and $\beta 0$ are fitting parameters[1].

The avalanche current of the collector-base junction in the VBIC model is equivalently given by

$$Iave = Ic \cdot AVC1 \cdot (PC - Vbci)\cdot e^{-AVC2\cdot(PC - Vbci)^{(MC-1)}} \tag{5}$$

where Ic is the collector current without avalanche, PC represents the junction built-in potential, MC is the junction grading coefficient, $Vbci$ the voltage drop over the junction, $AVC1$ and $AVC2$ are fitting parameters [8].

Equivalently, the subcircuit in Figure 2 has two parallel avalanche current sources between the drain and the substrate. The two avalanche current equations overcome the discontinuity problem that exists in equation (2) and

have similar computational stability as that offered by the new multiplication factor formulations in [7].

3. SIMULATION OF SNAPBACK

The model has been correlated with silicon dada. In model extraction, the BSIM3v3 model and the VBIC model were extracted first using regular methodology respectively, with emphasis on substrate current. Then the substrate resistance, R_{sub}, was extracted from the snapback curves measured with positive voltage pulse sequence that is regarded as equivalent to TLP pulses.

We developed a transient simulation program to simulate the snapback effect using a voltage pulse sequence as the input. Figure3 shows the plots of drain voltage *Vd*, drain current Id as well as pulse height *Vp*, as function of time in a single pulse. The input voltage linearly increases from 0 to *Vp* in a period of *Trise*, which is called rise time. The pulse length was 100ns. The stabilized *Vd* and *Id* values (in the time range 70~80ns) are picked as the simulation results that correspond to TLP data.

Transient simulation with pulse input and DC simulation have been run on ggNMOS and gcNMOS devices to analyse the *Vt1* impact of bulk/drain (base/collector) junction capacitance, gate drain overlap capacitance, BJT base transit time t_F and bulk/source (base/emitter) junction capacitance. In each simulation, only one parameter in the extracted model was modified. MOS parameters CGDO and CDGL were used for the impact of the gate drain overlap capacitance. In VBIC parameters, CJC was used for the bulk/drain junction capacitance, CJE for the bulk/source junction capacitance, and TF for the base transit time t_F. The t_F of the BJT model was estimated using inverter simulation, a method proposed by [9].

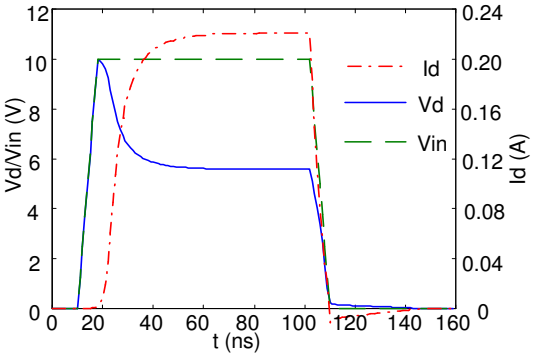

Figure 3: Input voltage *Vin*, drain voltage *Vd* and drain current *Id* vs. time *t* in a single pulse

4. RESULTS AND DISCUSSIONS

4.1 Snapback of ggNMOS

Figure 4 shows the snapback data of a ggNMOS device for two pulse sequences with different rise time. The data demonstrate that *Vt1* decreases as the rise time of the input pulses is reduced. The voltage step in measurement, as well as in simulation, was 0.1V. *Vt1* was 9.1V when *Trise*=8ns and 9.8V when *Trise*=20ns. Simulation with smaller voltage step (0.01V) has been carried out for the case of *Trise*=8ns and a more accurate value of *Vt1*=9.14V was obtained.

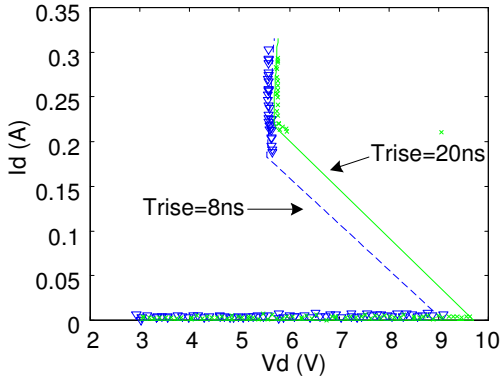

Figure 4: Snapback curves of a ggNMOS for different rise time pulses (lines: simulation, symbols: measurement)

A DC simulation, which correspond to quasi-static process, gave a result of *Vt1*=9.85V. It demonstrated that the rise time impact is negligible when *Trise*=20ns.

4.2 Vt1 Sensitivity

Figure 5 shows the results of *Vt1* sensitivity of CJC and t_F. The rise time was 8ns in the simulation. The results demonstrate that *Vt1* increases as the base transit time and the base/collect junction capacitance increase. The impact of CJC is more significant than t_F. When t_F increases from 150ps to 450ps, *Vt1* increases from 9.0 to 9.24V. While CJC varies 10% from its normal value, *Vt1* changes in the range of 8.76 to 9.48V.

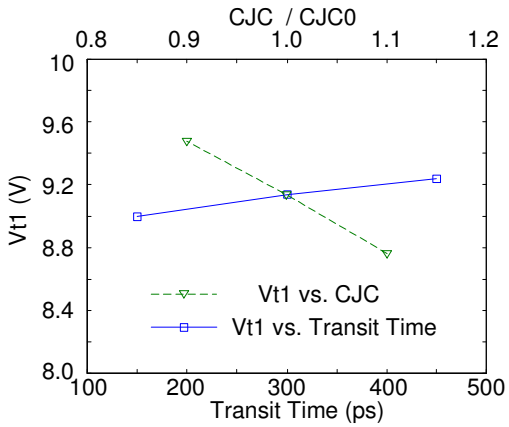

Figure 5: *Vt1* vs. CJC and t_F in a ggNMOS (Trise=8ns)

The results of simulation with varied gate/drain overlap capacitance and base/emitter capacitance parameters demonstrated that gate/drain overlap capacitance has no

impact on *Vt1* in ggNMOS structure. *Vt1* increases as base/emitter capacitance increases. The impact of CJE is less significant than CJC. The phenomenon can be explained that when base/emitter junction is forward biased, diffusion capacitance is more important than depletion capacitance, the latter is modeled by CJE.

4.3 Vbe Pike under ESD Pulse Stress

The key fact of snapback effect is that *Vbe* of the parasitic lateral NPN must be high enough to turn on the BJT. In quasi-static events, the *Vbe* is the voltage drop cross the substrate resistance caused by substrate current. In transient events, displacement currents due to *dV/dt* also contribute to the voltage drop and causes overshot in *Vbe*.

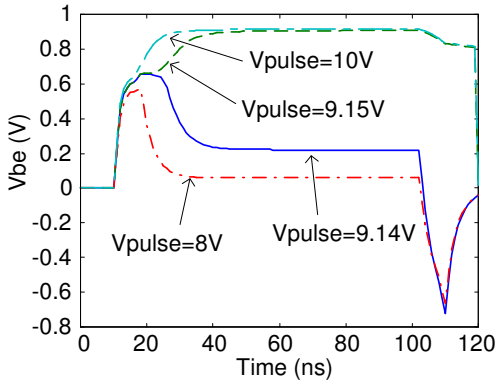

Figure 6: Vbe vs. Time in a single pulse for a ggNMOS

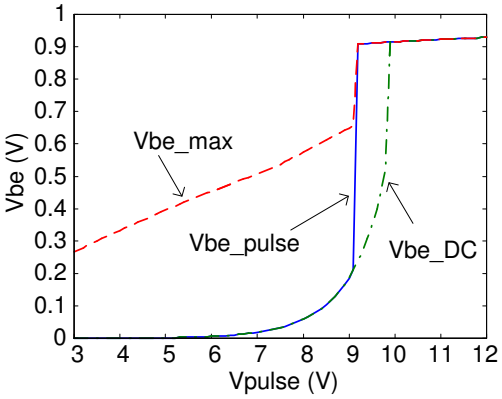

Figure 7: *Vbe* vs. ESD stress voltage in transient (*Vbe_pulse* and *Vbe_max*) and quasi-static (*Vbe_DC*) events

Figure 6 shows the intrinsic *Vbe* of the BJT in a single pulse for different pulse height *Vpulse*. *Vt1* was between 9.14 and 9.15V. The Vbe curves immediately before and after *Vt1* shows tremendous difference. *Vbe* curve has similar shape when *Vpulse*<*Vt1*. Not only does the height of *Vbe* pike increase, but the width of the pike increases more significantly as *Vpulse* increases.

Figure 7 is *Vbe* as function of ESD stress voltage, which is *Vpulse* in transient and *Vin* in DC simulations respectively. *Vbe_pulse* is the stabilized *Vbe* in transient simulation. Though *Vbe_pulse* has no visible difference from *Vbe_DC* before snapback is triggered, the peak of *Vbe* in transient event is significantly higher.

5. CONCLUSION

A practical macro model approach for modeling ESD MOS snapback is presented in this paper. It consists of standard components only and has no external current source, which makes the CAD implementation very straightforward. The fine-tuned algorithms in BSIM3v3 and VBIC make convergence issues much less likely happen. The sophisticated capacitance modeling in BSIM3v3 and VBIC makes the macro model suitable not only quasi-static process modeling but also simulation for transient events.

The modeling approach has been used to investigate the rise-time effects in pulse stress testing that was observed by measurement. The simulation demonstrated that the base transit time and the junction capacitance of parasitic BJT have impact on trigger voltage *Vt1* even in ggNMOS configuration. The cause of Vt1 drop in ggNMOS is the higher displace current under shorter TLP pulse rise-time.

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