Modeling the Channel Charge and Potential in Quasi-Ballistic Nanoscale Double-Gate MOSFETs

Anurag Mangla, Jean-Michel Sallese, Carlos Sampedro, Francisco Gamiz, and Christian Enz

***Abstract*— In this paper, we present an analytical semiempirical model of the profile of the channel charge and potential in quasi-ballistic double-gate (DG) MOSFETs. The charge model is based on the premise of separating the charge density in the quasi-ballistic channel into two hypothetical components: 1) exclusively ballistic (collision-free) and 2) collision-dominated components, which are governed by the same electrostatics. These components are related to each other through a ballisticity parameter whose values lie between 0 and 1. Varying the value of this parameter allows us to model the charge profile continuously between diffusive and purely ballistic devices. Using the proposed charge model and the DG MOSFET electrostatics, an analytical expression for the channel potential is derived which, like the charge model, is continuous between the diffusive and ballistic regimes.**

***Index Terms*— Compact model, double-gate (DG) MOSFET, quasi-ballistic.**

I. Introduction

BALLISTIC transport in semiconductors has been postulated since as long as a solution for low-power high-speed applications [1], [2], and it would start to manifest significantly in the contemporary nanometer scale CMOS devices. Even though it remains unclear whether 100% ballisticity can be achieved at room temperature in nanoscale silicon devices [3], [4], there is no doubt that such devices are quasi-ballistic, e.g., it has been demonstrated through simulations that even in a 200-nm device, a significant population of charge carriers injected from the source reaches the drain ballistically [5]. The exact definition of a quasi-ballistic device would imply such a device whose channel length is comparable with the carrier mean free path [6]. However, as is common in the literature, we use the term to denote any device in which non-negligible ballisticity can be detected, irrespective of the channel length.

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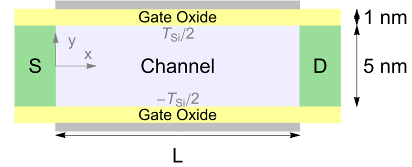

Fig. 1. Geometry of the DG-MOSFET used for the Monte-Carlo simulations.

The quasi-ballistic devices lie on the continuum between the ballistic and the diffusive devices and pose their own challenges to compact modeling; neither the ballistic models (which do not account for scattering [7]), nor the conventional drift-diffusion models (which do not take the nonlocal off-equilibrium nature of ballistic transport into account), are directly applicable. Evidently, a model for the quasi-ballistic devices would have to account for both collision-free and collision dominated transport thus remaining continuous between the ballistic and diffusive regimes. Several models for quasi-ballistic MOSFETs based on different approaches have been proposed in the literature: 1) backscattering coefficient-based [8], [9]; 2) scattering matrix-based [10]; 3) chain of ballistic MOSFETs [11], [12]; and 4) virtual-source-based [13], [14]. These and other models are based on the carrier flux transport over a barrier picture [15], [16], where the source-channel potential barrier plays an important role. However, the shape of the potential in the rest of the channel is generally approximated through parabolic [14], [17] or higher-power polynomial [8] functions. Though these polynomial functions approximate the channel potential profiles in the short-channel quasi-ballistic devices fairly well, they would not be able to model the potential profiles that are rather flat (constant potential) [7], [18], in the longer channel yet predominantly ballistic devices. A proper model of the potential profile is also needed to provide a physical description of channel length modulation and drain induced barrier lowering in the diffusive devices.

In this paper, drawing on the insights gained from multisubband ensemble Monte-Carlo simulations (MSB-EMC) on double-gate (DG) quasi-ballistic and ballistic MOSFETs, we propose a semiempirical analytical model of the channel charge. Subsequently, using the proposed charge model, an analytical model for the channel potential is derived. The charge and potential models could be used as precursors to a scalable compact model that would encompass the ballistic, quasi-ballistic, and drift-diffusion regimes.

II. Device Templates and Monte-Carlo Simulation

The symmetric DG MOSFET structure is used for the analyses and discussion in this paper. The geometry of an

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idealized device, shown in Fig. 1, consists of 5-nm thick silicon body and 1-nm thick SiO_2 gate oxide. A metal gate with work-function 4.61 eV is used. The source and drain extensions are each 10-nm long and are n-type doped to 1.2×10^{20} cm^{-3}. The channel is considered undoped with a residual doping of 1.2×10^{15} cm^{-3}. Two different channel lengths, 10 and 100 nm, are studied to evaluate the effect of channel length on the electrostatic potential profile.

The MSB-EMC simulations are used to study the electrostatics and transport. The MSB-EMC simulator used in this paper, which has been successfully applied for the study of different nanodevices, including bulk [19], DGSOI [20], and FDSOI [21], is based on the space-mode approach of quantum transport [22]. This approach treats the transport as semiclassical and solves 1-D Schrödinger equation for different slabs in the confinement direction. The electrostatics of the system is obtained from the coupled solution of 2-D Poisson and 1-D Schrödinger system. In this way, the evolution of the eigen-energies and wavefunctions for the ith valley and the νth subband is obtained along the transport direction. To evaluate the transport properties, the Boltzmann transport equation is solved by the ensemble Monte Carlo method considering a nonparabolic conduction band approximation in both confinement and transport directions [23]. The simulator provides one of the most detailed descriptions of carrier transport including the ballistic behavior of ultrashort devices.

For the purposes of this paper, the 10- and 100-nm devices are rendered artificially ballistic by turning off all the scattering mechanisms in the channel, but letting the charge carriers (electrons) thermalize completely in the source and drain regions. On application of suitable bias voltages on the source, drain, and gate terminals, the electrons are injected from the source into the channel where they undergo consecutive scatter-free random walks before being collected at the drain. The electrons do not scatter with each other or phonons, but they can backscatter at a potential barrier.

III. Channel Charge

The model of the channel charge that we will develop in this section is based on the premise that while traversing the channel in a quasi-ballistic device, a fraction of the carrier population injected from the source would remain ballistic, i.e., it would reach the drain, while having encountered exactly zero scattering events. This has been demonstrated for 200-nm devices [5] and for 25-nm devices [24]. Through our own simulations on 10- and 100-nm devices, as shown in Fig. 2, we observe that the ratio of ballistic carriers to the total number of carriers decreases monotonically from the source to the drain,[1] but it has a nonzero value at the drain end. This implies that even though the number of carriers scattered in the channel increases progressively from the source to the drain, a certain minimum number of carriers travel scatter-free from the source to the drain. This minimum number of ballistic carriers has to be a constant through the channel, being equal

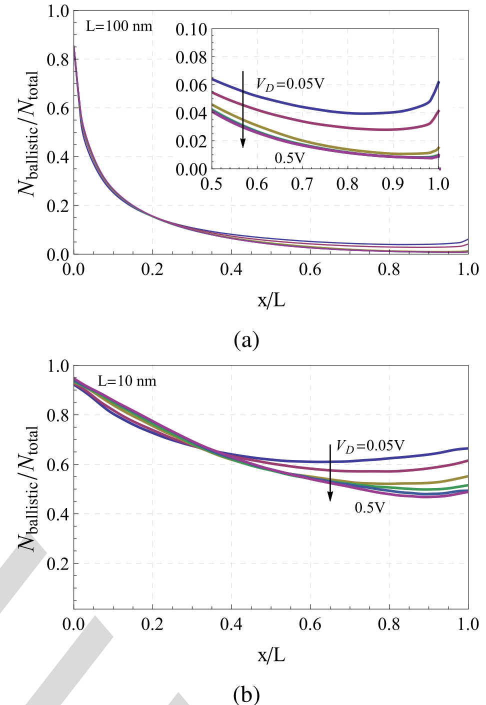

Fig. 2. Ratio of ballistic carriers to the total number of carriers along the channel in (a) 100-nm and (b) 10-nm devices. $V_G = 1$ V. Inset in (a): zoomed-in view on the second half of the channel.

to number of ballistic carriers collected at the drain, because any carrier that has encountered even one scattering event cannot be considered ballistic.

We propose to model the carrier density in the channel $n(x)$ in a similar way, as a sum of two components: 1) an intrinsically ballistic[2] component n_b whose magnitude remains constant throughout the channel and 2) a diffusive component n_d (which includes the carriers that are ballistic at the beginning, but scatter later) whose magnitude is position dependent, such that

$$n(x) = n_b + n_d(x). \quad (1)$$

In a diffusive device the x dependence of n can be described through the quasi-Fermi potential defined locally at each point in the channel. On the other hand, in the presence of ballistic transport (which is nonlocal and off-equilibrium [26]), the definition of a local quasi-Fermi level has no meaning [11]. Therefore, we account for the x dependence of $n_d(x)$ semiempirically as following:

$$n(x) = n_b + n_{d_0}\left(1 - \frac{2x^2}{L^2}\right). \quad (2)$$

Here, n_{d_0} is the magnitude of the carrier density at the source excluding the density of the carriers, which remain ballistic and L is the channel length. We note upfront that (2) would not be valid in close proximity of the source and drain extensions where, as can be observed in Fig. 3 [especially evident in Fig. 3(c) and (d)], the carrier density varies rapidly between the doping density in the source/drain extensions and the

[1]The slight increase in the number of ballistic carriers at the drain end, seen especially at low values of V_D, is due to the carriers injected from the drain.

[2]The percentage of carriers which are ballistic at the drain end is called intrinsic ballisticity [25].

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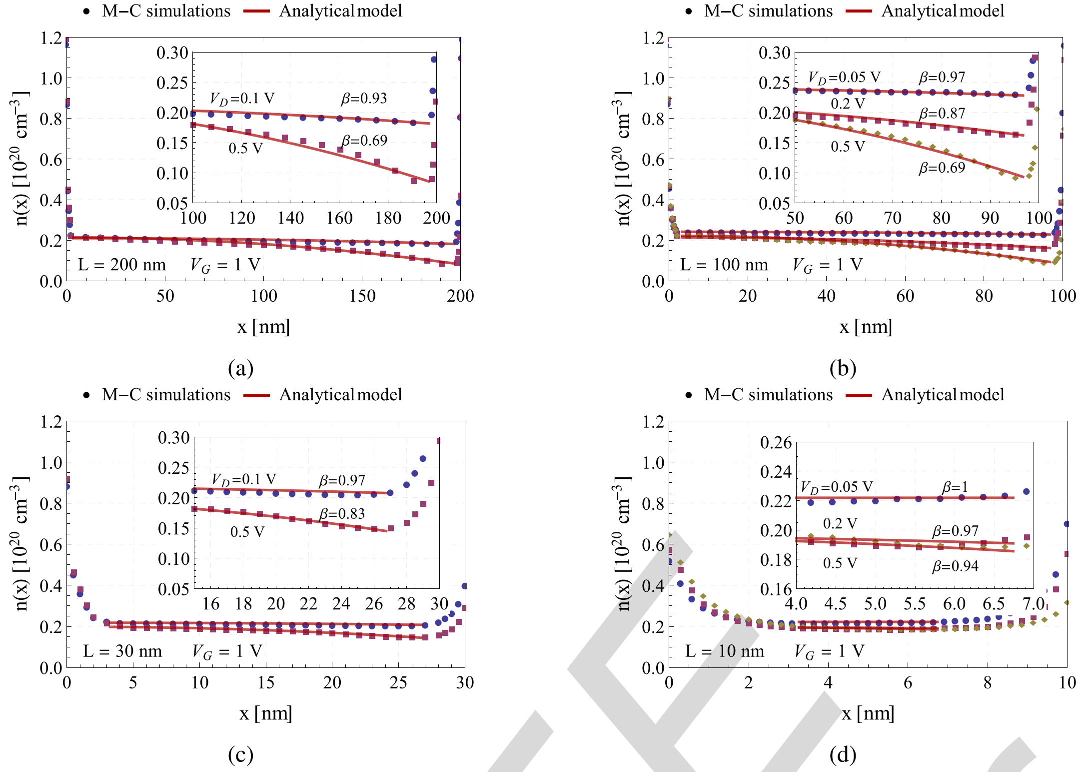

Fig. 3. Carrier density profile along the center of the channel for (a) 200-nm, (b) 100-nm, (c) 30-nm, and (d) 10-nm quasi-ballistic devices.

carrier density in the channel. In the vicinity of source/drain, this gradient of carrier density can be modeled using decaying exponential functions, with a decay factor characterized by the Debye length of electrons in the channel, and an expression for carrier density that is continuous from the source/drain into the channel can be obtained. However, since it will not modify the conclusions of this paper, this will not be covered in this paper to keep our analyses focused on the behavior in the part of the channel affected by ballistic transport.

Now, we define a parameter β as

$$\beta = \frac{n_b}{n_b + n_{d_0}} \tag{3}$$

using which, we can rewrite (2) as

$$n(x) = \frac{n_b}{\beta}\left(1 - (1-\beta)\frac{2x^2}{L^2}\right) \qquad (0 < \beta \leq 1). \tag{4}$$

In a fully ballistic device, $\beta = 1$, therefore, the charge density is

$$n(x) = n_b \qquad \text{(ballistic)} \tag{5}$$

whereas for a diffusive device, $\beta \to 0$ and $n_b \to 0$, therefore from (2)

$$n(x) = n_{d_0}\left(1 - \frac{2x^2}{L^2}\right) \quad \text{(diffusive)}. \tag{6}$$

Equation (4) can thus describe the carrier density from that in a fully ballistic device to that in a diffusive (quasi-ballistic) device, in a scalable manner. Nevertheless, it should be remarked that the separation of carrier densities into two components, as done in (1), is simply a conceptual formulation and we do not attempt to physically associate the two components to real ballistic and diffusive populations in the device.

To understand the meaning of β better, we evaluate (4) at $x = 0$, resulting in

$$n_{\text{QB}}(0) = \frac{n_b}{\beta} \tag{7}$$

for a quasi-ballistic device, and in

$$n_{\text{B}}(0) = n_b \tag{8}$$

for a fully ballistic device for which $\beta = 1$. From (7) and (8) we can interpret β to be a measure of the excess charge at the source end of a quasi-ballistic device, as compared with the amount of charge this same device would have had, had it been fully ballistic. In other words, a quasi-ballistic device would have $1/\beta$ $(0 < \beta \leq 1)$ times more charge at the source end than an identical ballistic device, at the same bias conditions. At a given bias, we would expect a shorter device to be more ballistic than a longer one; β for the shorter device would be greater than that for the longer one. Since ballisticity is also dependent on the applied biases [27], we would expect β to be dependent on the source, drain, and gate biases. At low V_{DS}, since the carriers do not gain energy that is required for phonon scattering, the scattering rate in the channel is diminished [7], [28]. As can be observed in Fig. 2, around the middle of the channel, the ratio of ballistic carriers to total carriers is higher at lower values of V_{DS}. Thus, for a given quasi-ballistic device, we would expect higher values of β at low V_{DS} and vice-versa. We have not yet been able to develop an analytical model to

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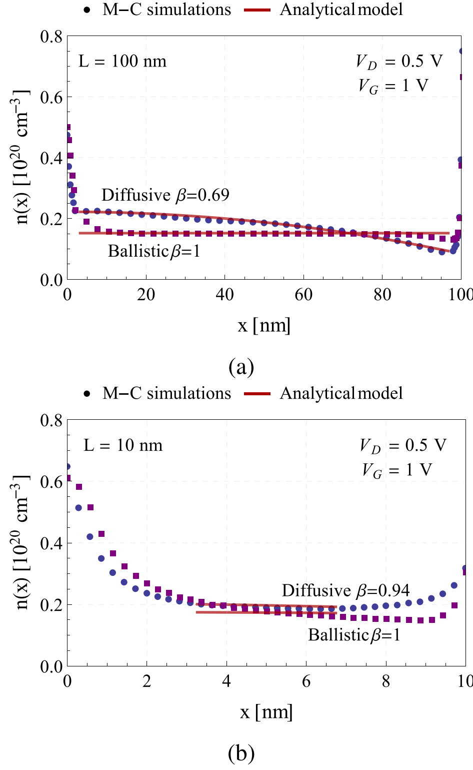

Fig. 4. Comparison of the carrier density profile along the center of the channel between the ballistic and quasi-ballistic cases in (a) 100-nm (b) 10-nm devices.

account for the length and bias dependence of β, so, for our purposes we will use it as a fitting parameter.

To determine n_b, we recall from (3) and (7) that the carrier density at the source is

$$n(0) = \frac{n_b}{\beta} = n_b + n_{d_0} \tag{9}$$

which constitutes the carriers that remain ballistic throughout the channel (n_b) and the carriers that are ballistic initially, but scatter later (n_d). This carrier density at the source can be calculated as a sum of two separate carrier populations, one that is in equilibrium with the source and the other that is in equilibrium with the drain [11]

$$n^*(0) = 2C_{\text{eff}}\, U_{\text{T}}\, \mathcal{W}\left(\frac{1}{2}e^{\frac{V_G-V_S-V_T}{U_T}} + \frac{1}{2}e^{\frac{V_G-V_D-V_T}{U_T}}\right) \tag{10}$$

$n^*(0)$ being the carrier density per unit area at the source. In (10), $\mathcal{W}(\cdots)$ is the Lambert-ω function and C_{eff}, V_T, and U_T are the effective gate capacitance, threshold voltage, and thermal equivalent voltage (kT/q), respectively. Assuming a uniform carrier distribution between the gates, we can determine n_b for the DG ballistic MOSFET as

$$nb = \beta\, n(0) = \beta\, \frac{n^*(0)}{T_{\text{si}}}. \tag{11}$$

In Fig. 3, we show the comparison of the analytical model of the carrier density, given by (4), with the carrier density obtained from Monte-Carlo simulations (in the center of the channel, i.e., $y = 0$), for four different devices with channel lengths 200, 100, 30, and 10 nm. Using β as a parameter, we obtain a good match between the model and the simulations at different values of V_D. The curves of the analytical model do not extend right upto the source and drain boundaries because (4) does not consider the charge spillover from the source and drain, which extends several nanometers into the channel. While this spillover region is quite negligible in longer devices, we remark that in the 10 nm one it consumes about two-thirds of the channel. It must be pointed out that in addition to β, a slight adjustment of C_{eff} in (10) was required to obtain the fit of model with the simulations at different values of V_D, while a constant value of threshold voltage $V_T = 0.65$ V was used. Fig. 4 shows the comparison of the carrier density profile along the center of the channel between the ballistic (all scattering mechanisms turned off in the simulations) and quasi-ballistic cases in 100- and 10-nm devices. By varying the value of the parameter β, both the quasi-ballistic and ballistic cases can be captured.

IV. Channel Potential

We start with the Poisson's equation that needs to be solved with appropriate boundary conditions to obtain the potential $\psi\,(x, y)$

$$\frac{\partial^2 \psi\,(x, y)}{\partial x^2} + \frac{\partial^2 \psi\,(x, y)}{\partial y^2} = \frac{q\, n(x, y)}{\varepsilon_{\text{si}}} \tag{12}$$

where q and $n(x, y)$ are the electronic charge and the carrier (electron) density, respectively. We assume a general parabolic shape in the y direction (perpendicular to the gates) to eventually simplify the 2-D Poisson's equation to a quasi 1-D equation [29], [30]. Using the boundary conditions

$$\frac{\partial \psi(y)}{\partial y} = 0 \quad \text{at } y = 0 \text{ (channel center)} \tag{13a}$$

$$\psi = \psi_{\text{s}}(x) \quad \text{at } y = \pm\frac{T_{\text{si}}}{2} \tag{13b}$$

and

$$\varepsilon_{\text{ox}} \frac{V_{\text{G}} - V_{\text{fb}} - \psi_{\text{s}}(x)}{T_{\text{ox}}} = \varepsilon_{\text{si}} \frac{\partial \psi(y)}{\partial y}\bigg|_{\text{y}=\pm\text{T}_{\text{i}}/2} \tag{13c}$$

where ε_{si} and ε_{ox} are the dielectric constants of silicon and silicon dioxide, respectively, V_G is the applied gate voltage, V_{fb} is the flat-band voltage, T_{ox} and T_{si} are the respective thicknesses of the oxide and silicon layers, and $\psi_{\text{s}}(x)$ is the surface potential, which varies along the channel depending on the applied voltages, we obtain

$$\psi\,(x, y) = -\frac{\varepsilon_{\text{ox}}\left(T_{\text{si}}^2 - 4y^2\right)\left(V_{\text{G}}' - \psi_{\text{s}}(x)\right)}{4\varepsilon_{\text{si}} T_{\text{ox}} T_{\text{si}}} + \psi_{\text{s}}(x) \tag{14}$$

where $V_{\text{G}}' = V_{\text{G}} - V_{\text{fb}}$. Evaluating $\psi(x, y)$ at $y = 0$ we obtain the center potential $\psi_{\text{c}}(x)$, using which we can rewrite (14) as

$$\psi\,(x, y) = -\frac{\left(T_{\text{si}}^2 - 4y^2\right)\left(V_{\text{G}}' - \psi_{\text{c}}(x)\right)}{8\lambda^2} + \frac{\left(\kappa^2 - 1\right)V_{\text{G}}' + \psi_{\text{c}}(x)}{\kappa^2} \tag{15}$$

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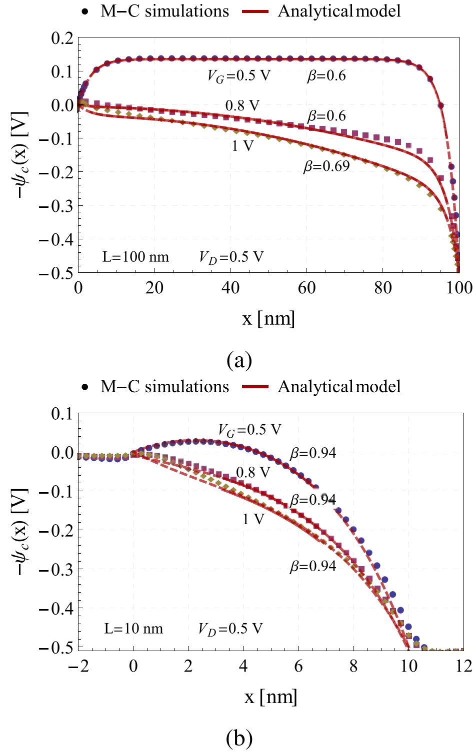

Fig. 5. Potential profile along the center of the channel in (a) 100-nm and (b) 10-nm quasi-ballistic devices, for different values of applied gate voltage V_G. The dashed lines extend the analytical model beyond the expected range of validity of (19).

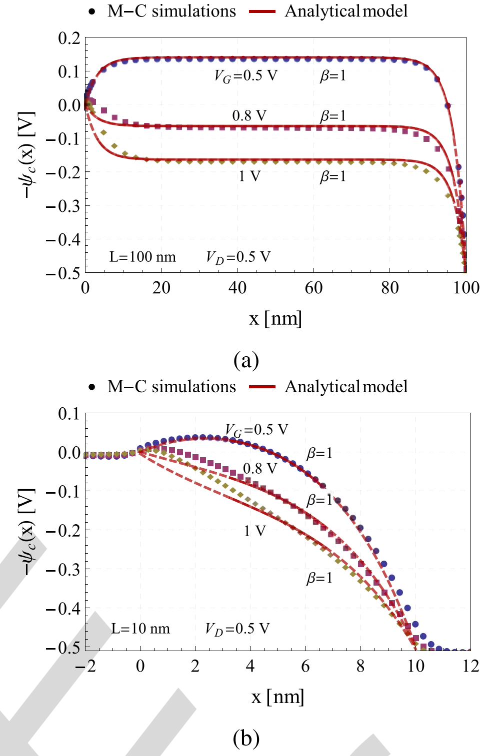

Fig. 6. Potential profile along the center of the channel in (a) 100-nm and (b) 10-nm fully ballistic devices, for different values of applied gate voltage. The dashed lines extend the analytical model beyond the expected range of validity.

where

$$\kappa^2 = 1 + \frac{\varepsilon_{\rm ox} T_{\rm si}}{4\,\varepsilon_{\rm si} T_{\rm ox}} \tag{16a}$$

and

$$\lambda^2 = \frac{\varepsilon_{\rm si} T_{\rm si} T_{\rm ox}}{2\,\varepsilon_{\rm ox}} \kappa^2. \tag{16b}$$

Using (15) in (12) and evaluating at the center of the channel, the Poisson's equation becomes

$$\frac{\partial^2 \psi_{\rm c}(x)}{\partial x^2} + \frac{V_{\rm G}^{'} - \psi_{\rm c}(x)}{\lambda^2} = \frac{q\,n(x)}{\varepsilon_{\rm si}} \tag{17}$$

which can be solved with the boundary conditions

$$\psi_{\rm c}(0) = V_{\rm S} \tag{18a}$$

$$\psi_{\rm c}(L) = V_{\rm D} \tag{18b}$$

to obtain the center potential

$$\begin{aligned}\psi_{\rm c}(x) = {} & V_{\rm D}\,\xi_x + V_{\rm S}\,\xi_{L\text{-}x} + V_{\rm G}^{'}\big(1 - \xi_x - \xi_{L\text{-}x}\big) \\ & - \frac{q\,\lambda^2}{\varepsilon_{\rm si}}\big(n(x) - n(L)\,\xi_x - n(0)\,\xi_{L\text{-}x}\big) \\ & + \frac{q\,\lambda^4}{\varepsilon_{\rm si}}\frac{4\,n_b(1-\beta)}{\beta\,L^2}\big(1 - \xi_x - \xi_{L\text{-}x}\big).\end{aligned} \tag{19}$$

Here, $n(x)$ is the carrier density as defined by (4), and $n(0)$ and $n(L)$ are the values of $n(x)$ evaluated at the source and the drain, respectively

$$n(0) = \frac{nb}{\beta} \tag{20a}$$

$$n(L) = \frac{nb}{\beta}\big(2\beta - 1\big) \tag{20b}$$

and the terms ξ_x and ξ_{L-x} are defined as follows:

$$\xi_x = \frac{e^{x/\lambda} - e^{-x/\lambda}}{e^{L/\lambda} - e^{-L/\lambda}} \tag{21a}$$

$$\xi_{L\text{-}x} = \frac{e^{(L-x)/\lambda} - e^{-(L-x)/\lambda}}{e^{L/\lambda} - e^{-L/\lambda}}. \tag{21b}$$

In (19), the factor λ, called the natural length of the DG SOI MOSFET [30] [defined in (16)], characterizes the distance over which the source and drain terminals influence the channel. The terms ξ_x and ξ_{L-x}, and consequently $V_D\,\xi_x$ and $V_D\,\xi_{L-x}$ in (19), decay rapidly (with the decay factor λ) on moving away from the drain and source, respectively. For the device dimensions under consideration in this paper $\lambda = 3.26$ nm, which is negligible in the long channel devices but not in the very short channel (e.g., 10 nm) devices, implying that the channel potential in the short devices would be significantly affected by the drain and source voltages even toward the middle of the channel.

The compact form of (19) permits us to see the individual contributions of the applied voltages, V_D, V_S, and V_G, to $\psi_{\rm c}$ more easily. The first, second, and third terms are the contributions of the applied drain, source, and gate voltages, respectively, weighted by the exponential factors defined in (21). The term $n(x)$ depicts a parabolic variation of $\psi_{\rm c}(x)$ through (4), which could serve as a basis for the parabolic approximations of the channel potential profile generally assumed for the analyses of nanoscale transistors, as discussed in Section I. It should be kept in mind that the carrier density terms in (9) are themselves dependent on the applied drain, source, and gate voltages through (10). In Fig. 5, we see that the model of

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(19) corresponds well with the simulations on 100- and 10-nm devices. Note that (19) is expected to be least accurate in the proximity of source/drain extensions because, as mentioned in Section III, the expression for $n(x)$ in (4) which is in turn used in deriving (19), does not account for the carrier density profile near the source/drain extensions.

In the same way as (4) models the carrier density between the quasi-ballistic and ballistic devices in a continuous manner, (19) models the channel potential between the two. It predicts the flat potential profile in the longer channel ballistic devices. In the fully ballistic case for which $\beta = 1$ in (19), the last term disappears. In addition, the x^2 dependence in $n(x)$ vanishes [according to (4)]. As discussed previously, the ξ_x and ξ_{L-x} terms decay in the channel away from the source and drain proximity. Consequently, $V_D \xi_x$ and $V_S \xi_{L-x}$ terms are negligible, and $(1 - \xi_x - \xi_{L-x}) \approx 1$, a few nanometers away from the drain and source. This leaves only the term $V_G^{'} + (q/\varepsilon_{si})\lambda^2 n_b$, a constant, to shape $\psi_c(x)$ in the middle regions of the channel. On the other hand, the ξ_x and ξ_{L-x} terms are non-negligible even in the middle of the channel of the very short ballistic devices, thereby influencing the shape of $\psi(x)$, which is not flat anymore. The potential profile of the 10 nm fully ballistic device is markedly different from that of the 100-nm device, as can be observed in Fig. 6. In Figs. 5 and 6, the potentials profiles are quite insensitive to the value of β at $V_G = 0.5$ V, because for $V_G < V_T$, the potential shape is largely determined by the first three terms in (19) that are independent of β.

V. Conclusion

In this paper, we presented an analytical description of the channel profile of the carrier density (4) and the center potential (19) in nanoscale DG MOSFETs. The equations so developed can be scaled between the quasi-ballistic and ballistic cases simply by varying the value of a single parameter (β) between 0 and 1. Admittedly, the carrier density equation is semiempirical in nature. However, it corresponds well with the results of the Monte-Carlo simulations. Lundstrom and Antoniadis [31] argue that from a compact-modeling perspective the development of fully physical models that are seamlessly scalable between the long-channel and nanoscale FETs is an interesting intellectual exercise, but not an essential one. In the same spirit, the main goal of this paper was to be able to model the charge and potential profiles of the ballistic and quasi-ballistic MOSFETs, which are evidently different from each other, in a continuous yet compact manner, while retaining the device physics. We believe that the conceptual separation of the channel charge into ballistic and diffusive components, represented by (1), can be used as the starting point for a complete I–V model for circuit simulation.

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References

[1] M. Shur and L. Eastman, “Ballistic transport in semiconductor at low temperatures for low-power high-speed logic,” *IEEE Trans. Electron Devices*, vol. 26, no. 11, pp. 1677–1683, Nov. 1979.

[2] T. Skotnicki *et al.*, “Innovative materials, devices, and CMOS technologies for low-power mobile multimedia,” *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 96–130, Jan. 2008.

[3] M. V. Fischetti *et al.*, “Scaling MOSFETs to 10 nm: Coulomb effects, source starvation, and virtual source model,” *J. Comput. Electron.*, vol. 8, no. 2, pp. 60–77, Jul. 2009.

[4] D. Fleury, G. Bidal, A. Cros, F. Boeuf, T. Skotnicki, and G. Ghibaudo, “New experimental insight into ballisticity of transport in strained bulk MOSFETs,” in *Proc. Symp. VLSI Technol.*, Jun. 2009, pp. 16–17.

[5] D. Csontos and S. E. Ulloa, “Crossover from diffusive to quasi-ballistic transport,” *J. Appl. Phys.*, vol. 101, no. 3, p. 033711, 2007.

[6] K. Natori, “Ballistic/quasi-ballistic transport in nanoscale transistor,” *Appl. Surf. Sci.*, vol. 254, no. 19, pp. 6194–6198, Jul. 2008.

[7] K. Natori, “Ballistic metal-oxide-semiconductor field effect transistor,” *J. Appl. Phys.*, vol. 76, no. 8, p. 4879, 1994.

[8] A. Rahman and M. Lundstrom, “A compact scattering model for the nanoscale double-gate MOSFET,” *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 481–489, Mar. 2002.

[9] S. Martinie, D. Munteanu, G. L. Carval, and J.-L. Autran, “Physics-based analytical modeling of quasi-ballistic transport in double-gate MOSFETs: From device to circuit operation,” *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2692–2702, Nov. 2009.

[10] H. Wang and G. Gildenblat, “Scattering matrix based compact MOSFET model,” in *Proc. IEEE IEDM*, Dec. 2002, pp. 125–128.

[11] G. Mugnaini and G. Iannaccone, “Physics-based compact model of nanoscale MOSFETs—Part I: Transition from drift-diffusion to ballistic transport,” *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1795–1801, Aug. 2005.

[12] G. Mugnaini and G. Iannaccone, “Physics-based compact model of nanoscale MOSFETs—Part II: Effects of degeneracy on transport,” *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1802–1806, Aug. 2005.

[13] A. Khakifirooz, O. M. Nayfeh, and D. A. Antoniadis, “A simple semiempirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters,” *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1674–1680, Aug. 2009.

[14] L. Wei, O. Mysore, and D. Antoniadis, “Virtual-source-based self-consistent current and charge FET models: From ballistic to drift-diffusion velocity-saturation operation,” *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1263–1271, May 2012.

[15] M. Lundstrom, “Elementary scattering theory of the Si MOSFET,” *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 361–363, Jul. 1997.

[16] M. Lundstrom and Z. Ren, “Essential physics of carrier transport in nanoscale MOSFETs,” *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 133–141, Jan. 2002.

[17] M.-J. Chen and L.-F. Lu, “A parabolic potential barrier-oriented compact model for the $k_B T$ layer’s width in nano-MOSFETs,” *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1265–1268, May 2008.

[18] A. Svizhenko and M. Anantram, “Role of scattering in nanotransistors,” *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1459–1466, Jun. 2003.

[19] C. Sampedro *et al.*, “Multi-subband ensemble Monte Carlo simulation of bulk MOSFETs for the 32 nm-node and beyond,” *Solid-State Electron.*, vols. 65–66, pp. 88–93, Nov. 2011.

[20] C. Sampedro, F. Gamiz, A. Godoy, R. Valin, A. Garcia-Loureiro, and F. Ruiz, “Multi-subband Monte Carlo study of device orientation effects in ultra-short channel DGSOI,” *Solid-State Electron.*, vol. 54, no. 2, pp. 131–136, 2010.

[21] C. Sampedro, F. Gamiz, L. Donetti, and A. Godoy, “Reaching sub-32 nm nodes: ET-FDSOI and BOX optimization,” *Solid-State Electron.*, vol. 70, pp. 101–105, Apr. 2012.

[22] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom, and D. Jovanovic, “Simulating quantum transport in nanoscale transistors: Real versus mode-space approaches,” *J. Appl. Phys.*, vol. 92, pp. 3730–3739, Oct. 2002.

[23] M. V. Fischetti and S. E. Laux, “Monte Carlo study of electron transport in silicon inversion layers,” *Phys. Rev. B*, vol. 48, no. 4, pp. 2244–2274, 1993.

[24] E. Fuchs *et al.*, “A new backscattering model giving a description of the quasi-ballistic transport in nano-MOSFET,” *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2280–2289, Oct. 2005.

[25] J. S. Martin, A. Bournel, and P. Dollfus, “On the ballistic transport in nanometer-scaled DG MOSFETs,” *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1148–1155, Jul. 2004.

IEEE Proof

[26] J.-H. Rhew, Z. Ren, and M. S. Lundstrom, “A numerical study of ballistic transport in a nanoscale MOSFET,” *Solid-State Electron.*, vol. 46, no. 11, pp. 1899–1906, Nov. 2002.
[27] C. Sampedro, F. Gamiz, A. Godoy, and S. Cristoloveanu, “Ballisticity at very low drain bias in DG SOI nano-MOSFETs,” in *Proc. Int. Semicond. Device Res. Symp.*, Dec. 2007, pp. 1–2.
[28] N. Sano, “Kinetics of quasiballistic transport in nanoscale semiconductor structures: Is the ballistic limit attainable at room temperature?” *Phys. Rev. Lett.*, vol. 93, no. 24, p. 246803, Dec. 2004.
[29] R.-H. Yan, A. Ourmazd, and K. Lee, “Scaling the Si MOSFET: From bulk to SOI to bulk,” *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.
[30] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, “Scaling theory for double-gate SOI MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 40, no. 12, pp. 2326–2329, Dec. 1993.
[31] M. S. Lundstrom and D. A. Antoniadis, “Compact models and the physics of nanoscale FETs,” *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 225–233, Feb. 2014.

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