Modeling the Effects of Thermal Pad Voiding on Quad Flatpack No-lead (QFN) Components

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ABSTRACT

Finite element modeling was used to evaluate the effects of thermal pad solder voiding on the thermal resistance of Quad Flatpack No Lead components. This included two different approaches for modeling solder voids: many small, distributed voids, the effects of which were averaged across the entire solder contact area or a single discrete void. Two approaches were used for defining the thermal path established in the solder. The effects of other design parameters - thermal boundary conditions, the presence of thermal vias under the package, and the size of the die power dissipation area – were also addressed. Modeling showed that thermal vias and external boundary conditions had the most significant impact on the package thermal resistance. Solder pad voids and concentrated die-level heat dissipation, for the range used in this study, had noticeable but less significant impacts on thermal resistance. The study also compared different approaches for simulating solder voiding and identified ranges in which modeling simulations are most appropriate.

Keywords: Quad flatpack no-lead (QFN), Solder voiding, thermal resistance

Acronyms

FEM	Finite element model (or modeling)
I/O	Input / output
PCB	Printed circuit board
QFN	Quad flatpack no-lead
R	Junction-to-board thermal resistance
REL	Family of lead-free solders
SAC305	Sn/Ag3%/Cu0.5% solder
SnPb	Tin-lead solder

INTRODUCTION

Quad Flatpack No Lead (QFN) components are soldered directly to a circuit board without compliant leads. They typically include a large solder pad, which is directly under the die, that provides a mechanism for holding the part onto the circuit board as well as the primary thermal path and electrical ground for the component. This center pad, referred to in this paper as the thermal pad, is surrounded by one or more rows of input/output (I/O) pads (interconnect pads) that provide electrical connections between the circuit board and the die. Figure 1 shows conceptual views of a representative QFN. Figure 1a) shows the thermal and I/O pads on the bottom of the component while Figure 1b) shows a cross-sectional image of a QFN attached to a circuit board. For reference, the printed circuit board (PCB) is shown with both microvias, which provide a vertical interconnect between outer layers of copper traces, and thru vias that extend completely through the PCB.

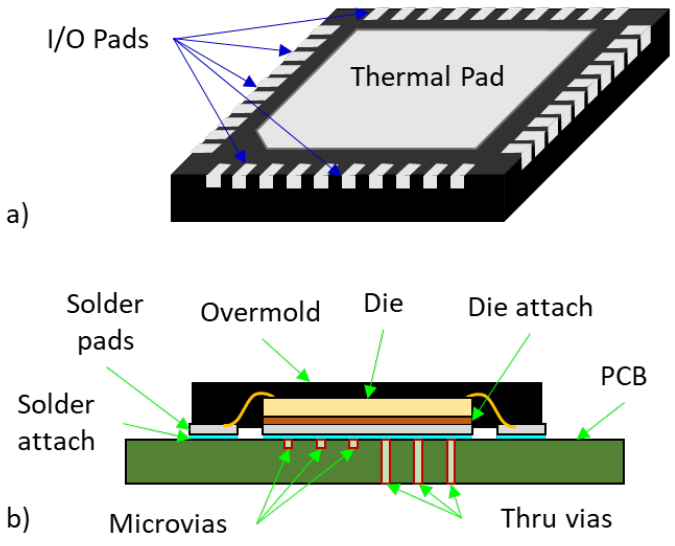

Figure 1: QFN package a) view from the bottom of component, b) cross-section of component assembled to printed circuit board [7]

The increasing availability of X-ray inspection/analysis technologies applied to the printed circuit assembly process has led to greater recognition of the presence of voids in solder joints. Voids can be important in solder joints because they can adversely affect their mechanical reliability. Voids in QFN thermal pads can also affect the component's thermal resistance.

A previously reported study described how QFN thermal pad voiding impacted component reliability under thermal cycling QFN [1, 2]. That work included four different package sizes assembled with four different solder alloys: eutectic tin-lead (SnPb), tin/silver/copper (SAC305), Sn/Ag Sn/Ag3% Bi 2-3% Cu 0.5-0.7% (REL22) and Sn/Ag 0.5-0.7% Bi 1.8-2.2% Cu 0.6-0.8% (REL61). Figure 2 shows an example of X-ray imaging conducted in that study to characterize voiding in each component while Figure 3 plots the measured voiding as a function of cycles to failure for components with all four different solder alloys. This shows that, in the range of values included in those studies, thermal pad voiding did not substantially affect QFN reliability. Measured values of voiding, which are shown in Figure 3, demonstrated that the SnPb components had maximum volumetric voiding of ~15% while the lead-free solders exhibited much higher voiding, with two parts that had more than 40% voiding. Additional information on the failure distributions and voiding for different component sizes, how the presence of microvias may have slightly increased the amount of voiding, etc. can be found in previous publications [1, 2].

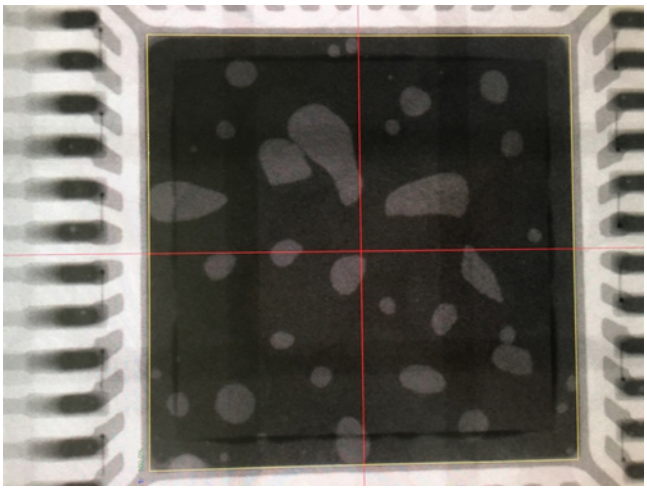

Figure 2: Example of voiding in QFN thermal pad [2]

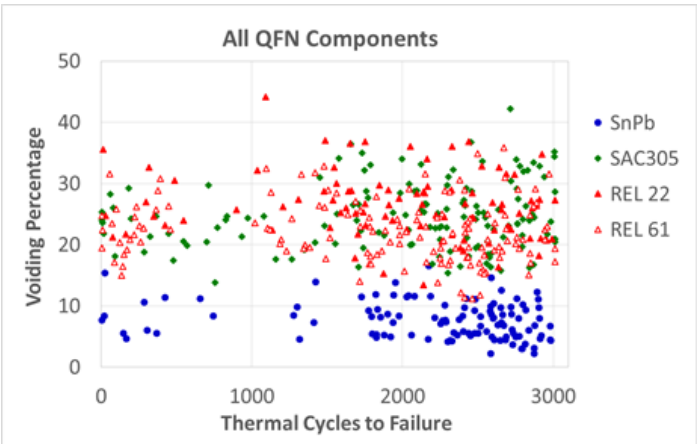

Figure 3: Void results vs. thermal cycles: all samples [2]

While testing indicated that thermal pad voiding did not affect solder joint reliability, it did not address the impact of voids on QFN thermal resistance. Several studies have discussed factors that influence QFN thermal resistance, including voids. Codecasa et al described a calculator for determining compact model parameters for components including QFNs [3]. They showed that, for example, a larger die reduces the QFN thermal resistance. Arzhanaov et al described a method for generating models to determine the thermal resistance of QFNs mounted to circuit boards [4]. This work showed that the number of thermal vias and circuit board copper layers influence the package thermal resistance. Simulations showed that voiding in the thermal pad had a relatively small impact on the QFN's thermal resistance; increasing the voiding to as high as 80% only increased the overall thermal resistance by ~8%. The study also included thermal testing of components, which were purposefully assembled to have substantial voiding. The measured thermal resistance of those components showed good agreement with the values predicted by FEM. Wilcoxon et al used numerical simulations to conclude that, for a specific set of boundary conditions, the impact of thermal pad voiding on QFN thermal resistance was generally small in comparison to, for example, the presence of vias under the part [7].

This paper extends that work to apply a wider range of boundary conditions on the circuit board and die-level heat source to identify conditions under which QFN voiding may be more important to thermal resistance. The paper also describes the impact of using different approaches for simulating voids in the thermal model.

QFN Thermal Resistance Model

A simplified finite element model (FEM) of a 72 I/O, 10mm QFN package style was created in ANSYS Workbench. The model consisted of a quarter of the QFN package with insulated boundary conditions on the symmetry axes of the component. Figure 4 shows the QFN model in which the two front edges are the axes of symmetry, and the two rear edges show the I/O pads. The quarter-silicon die was 3mm x 3mm x 0.35mm.

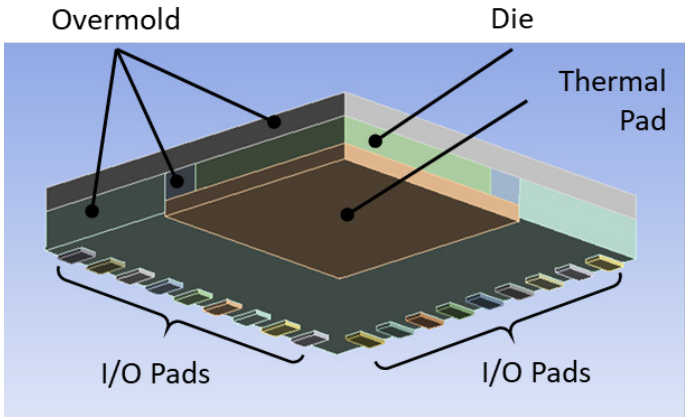

Figure 4: Quarter Model of QFN Package (view from bottom)

The thermal and I/O pads were attached to a quarter model of a 3cm x 3cm x 1.5mm PCB. The PCB included a 10x10 array of 0.3mm diameter vias that each contained two cylindrical bodies of the same diameter. The cylinder nearest the QFN was 0.25mm tall; the other cylinder was 1.25mm long to fill the rest of the volume within the PCB. The small cylinders represented microvias; both cylinders combined represented thru vias.

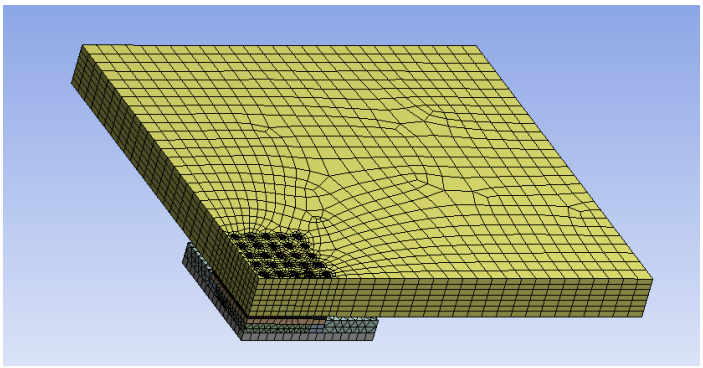

Figure 5: Quarter model of meshed QFN on PCB model (view from bottom): 10x10 array of vias visible in PCB

Table 1 shows the QFN material properties used in the model (these values are shown to two significant digits of values reported in the indicated references). The thermal conductivity of the PCB assumed two copper signal layers and two copper ground planes, but no thermal vias other than the 10x10 array. The nominal die attach between the silicon die and copper was assumed to be a silver-filled epoxy with thermal conductivity of 6W/mK and 30 micron bond line thickness, leading to an interface conductance of 2e5 W/m²K.

Table 1: Material Properties used in Thermal Model

Material	Conductivity (W/mK)
Silicon	150 [5]
Overmold Epoxy	1 [5]
Copper	390
PCB	15 (x-y), 0.5 (z)
SnPb Solder	50 [6]
SAC Solder	~60 [6]

The vias in the model were 0.3mm (11.8 mil) in diameter, which is larger than the vias used in the test boards of Ref. [1]: 0.127mm (5 mil) in diameter. The larger model vias helped to avoid the extremely fine mesh necessary to simulate small vias. The via thermal conductivity in the model was reduced to 35 W/mK to account for the amount of copper in the via and the size of the modeled via. Ref. [7] provides additional information on how the effective via conductivity was determined, as well as investigations on the sensitivity of the final results on the via conductivity, die attach thermal resistance, and PCB thermal conductivity.

Two thermal boundary conditions were included in the model in the work reported in Ref. [7]. Since a quarter model was used, 0.25W of heat flux was applied to the top surface of the die to simulate 1W total power dissipation. A convection coefficient of 10kW/m²K with ambient temperature of 0°C was applied to the two edges of the PCB, which were 1 cm from the outer edges of the QFN. The size of the PCB and convection coefficient applied to its outer edges were selected to create a model that accounted for the effects of thermal spreading without being dominated by the thermal resistance associated with natural convection from the PCB or introducing errors that can result from fixed boundary temperatures.

For this study, an additional boundary condition of 'back-side' cooling was simulated by applying a convection coefficient, h, to the surface of the PCB opposite the side to which the QFN was attached. The convection coefficient had a reference temperature of 0°C and four different values were used: h = 0 W/m²K corresponded to an insulated condition, h = 10 W/m²K represented a PCB cooled with natural convection, h = 100 W/m²K represented a PCB cooled with forced air cooling from a small heat sink, and h = 1000 W/m²K represented cooling to a large heat sink. In addition to this new boundary condition, the heat input boundary condition was modified.

In another boundary condition modification relative to the work reported in [7], the die surface heat input region was divided into four equal areas so that the effects of concentrated power dissipation could be assessed. Figure 6 shows these four areas: in the '25% heat' condition, the entire 0.25W was dissipated in the area adjacent to the two axes of symmetry; in the '50% heat' condition, 0.125W of heat was applied to the two areas nearest the symmetry corner of the model; in the '75% heat' condition, 0.0833W of heat was applied to each of the inner three areas, and in the '100% heat' condition, 0.0625W was applied to each of the four areas.

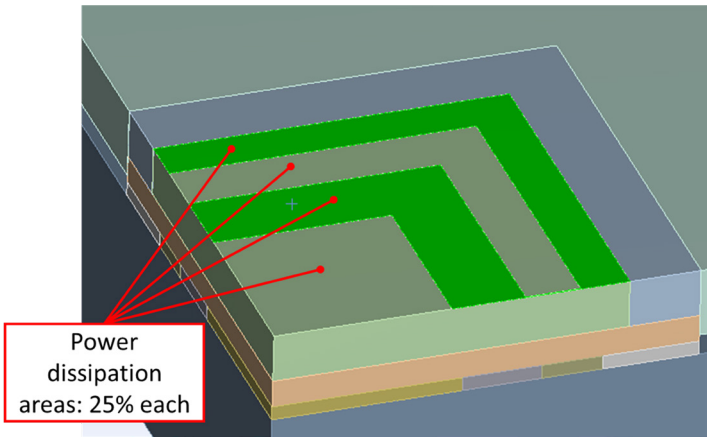

Figure 6: Die heat dissipation areas (top encapsulant hidden)

Ref. [7] accounted for the thermal resistance of solder by assuming that it was 0.1mm (4 mil) thick and therefore its conductance (conductivity/thickness) was 5e5 W/m²K for SnPb solder. Visual inspection of assembled QFNs showed that voids generally extended through the entire solder thickness from the PCB to the QFN thermal pad. Therefore, the effective thermal conductivity of a solder pad with voids would be equal to the solder conductivity multiplied by (1-v), where v is the amount of voiding (between 0 and 100%). This approach assumes that the thermal pad solder layer includes many very small voids with columns of solder between them. In practice, voiding could consist of a few large voids, with the worst-case scenario being a single large void.

To evaluate the impact of how voiding effects are modeled, this study included two approaches to 'bracket' the actual effects of voids. For 'Distributed' voids, the thermal conductivity of the solder was proportional to (1-v), which was the approach used in Ref. [7]. This simulates many small voids. In contrast, for a 'Discrete' void, a portion of the nominal solder contact area, which was equal to the amount of voiding, was removed from the thermal path. This simulates a single large void. Figure 7 illustrates the four areas defined in the model to simulate voiding. For 20% voiding, heat flow was prevented in the area nearest the symmetry corner of the model; for 40% heat flow was prevented in the two areas nearest the symmetry corner, etc.

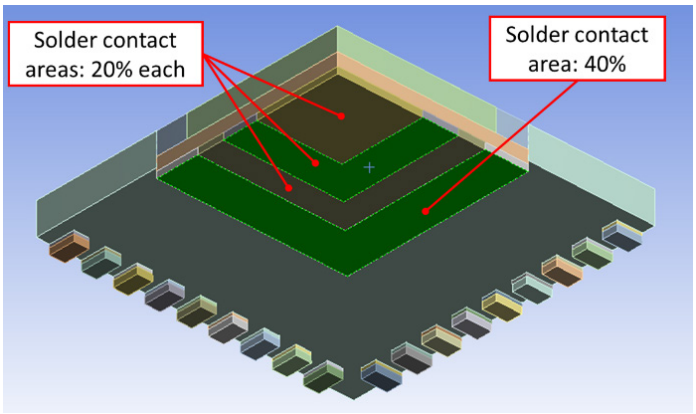

Figure 7: Solder volumes for defining voids

In addition, two different approaches were used to define the thermal resistance of solder. The work in Ref. [7] did not explicitly model the solder but instead defined a thermal conductance of 5e5 W/m²K between adjoining surfaces of the QFN thermal pad and the PCB. Distributed voids were simulated by changing the value of the conductance; for example, 20% voiding was represented with a conductance of 4e5 W/m²K. This study used this 'Conductance' approach in which the solder was not directly modeled, but also included a 'Volume' approach in which the QFN was 0.1mm above the PCB and the soldered areas were occupied by 0.1mm thick volumes that explicitly represented solder. Figure 8 shows both solder simulation approaches that were used in this study: the left-hand image shows soldered surfaces directly bonded together and thermal resistance was defined by a conductance value while the right-hand image shows the model with additional volumes to represent solder; the solder thermal conductivity of these new volumes established the thermal resistance.

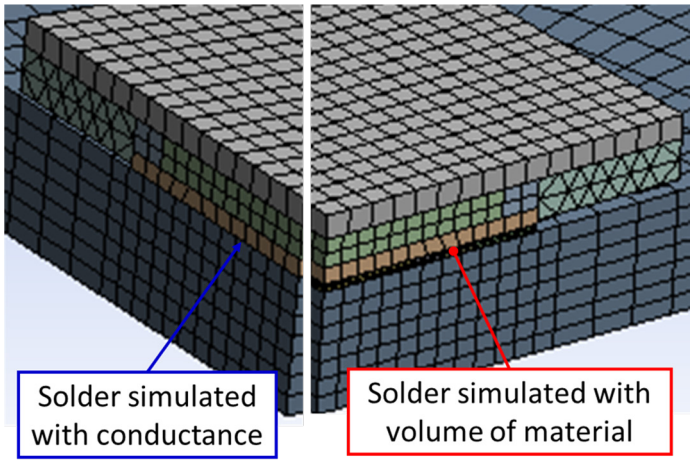

Figure 8: Meshed volumes showing two approaches for simulating solder layer

RESULTS

Figure 9 shows an example of a simulation result for assessing the QFN thermal resistance. Since the power input to the die was 1W (0.25W to the quarter model) and the reference temperature was 0°C, the maximum temperature on the die corresponds to a thermal resistance, R. This resistance provides a relative metric for comparing the thermal characteristics of package configurations, but it is not a standard resistance, such as junction-to-ambient ($\theta_{j\text{-}a}$), or junction-to-board ($\theta_{j\text{-}b}$).

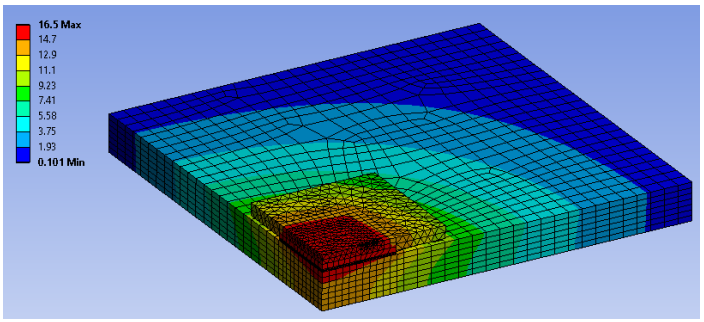

Figure 9: Thermal modeling simulation example

Table 2 summarizes the four approaches that were used to simulate the effects of solder voiding between the QFN and PCB.

Table 2: Summary of approaches for modeling solder voids

Modeling Approach	Thermal constraints applied (v = fraction of voiding)
Discrete void with conductance	Conductance of 5e5 W/m²K to (1-v) of contact area; 1e-5 W/m²K applied to other areas
Discrete void with volume	Conductivity of 50 W/mK to (1-v) portion of solder volume; 1e-5 W/mK to other volumes
Distributed voids with conductance	Conductance of (1-v)*5e5 W/m²K to entire solder contact area
Distributed voids with volume	Thermal conductivity of (1-v)*50 W/mK to entire solder volume
For the Discrete void modeling, areas and volumes were 'turned off' by setting conductance or thermal conductivity to a very low non-zero value. This avoids the numerical errors that would occur in the FEM solution if values of zero were used.	

Figure 10 compares the results for these four different approaches for the four levels of cooling applied to the back surface of the PCB, which are indicated with different colors. These results are for the specific case of '100% heat' in which the power dissipation is uniformly distributed across the entire die surface and for a PCB with a full array of thru vias. In this plot, dashed lines correspond to Distributed voids, i.e., very small voids between columns of solder while solid lines correspond to a single square Discrete void centered on the middle of the QFN. The plot shows the unsurprising results that better back-side cooling reduces the thermal resistance and that thermal resistance increases with more voiding. The plot also that the two modeling approaches (Conductance and Volume) generate similar results. However, the approach used to define voids (Discrete or Distributed) did have a substantial impact when the amount of voiding was ~40-50% or higher).

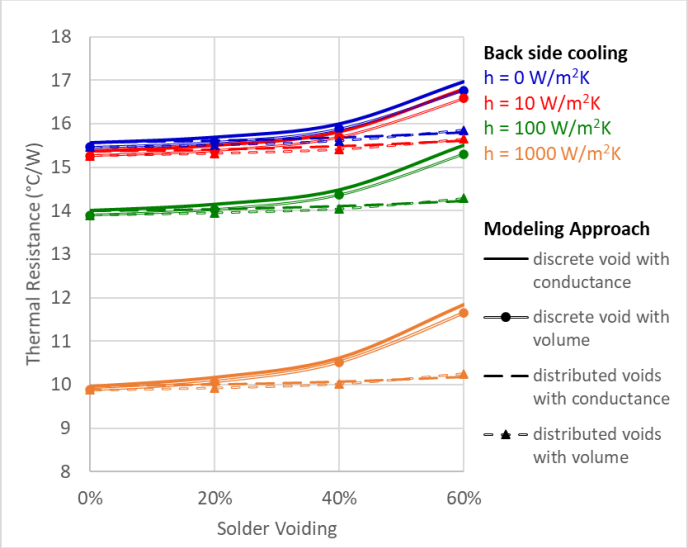

Figure 10: Comparison of solder modeling approaches

Figure 11 compares the effects of solder voiding (4 levels: 0, 20, 40 and 60%), PCB via configuration (3 levels: thru vias, microvias and no vias), back side cooling (4 levels: convection coefficient of 0, 10, 100 and 1000 W/m2K), and die-level heat concentration (4 levels: 25, 50, 75 and 100% heat). These results used the 'Discrete void with volume' approach for simulating the effects of solder voids. The plots in Figure 11 represent 192 individual simulations (4 voiding levels * 3 PCB via levels * 4 backside cooling levels * 4 die-level heat concentration levels).

Once again, many of the results shown in these plots are not terribly surprising. The presence of an array of thru vias substantially reduced the thermal resistance (by ~10°C/W) as compared to no thru vias, with the microvia results falling between. The back-side cooling condition had a significant influence on QFN thermal characteristics, with the best cooling condition used in this study reducing the thermal resistance by 3-5°C/W relative to the insulated condition. The highest level of thermal pad voiding considered (60%) increased the QFN thermal resistance by 1-2°C/W; a similar level of increased thermal resistance was seen when the heat dissipation area on the die was decreased from 100% to 25%.

DISCUSSION

The following observations are made from the simulation results:

• Simulating the thin layer of solder with volumes rather than with a conductance contact condition increased the number of nodes in the finite element model. This increased the typical solution time for a given configuration by 20% from ~100 to ~120 seconds.

• The primary benefit of using the Volume approach instead of the Conductance approach for simulating the solder thermal resistance was that it is very straightforward to parameterize material properties in ANSYS Workbench so that multiple simulations can be run in a batch. Since a large number (192) of simulations were conducted to generate Figure 11, the ability to parameterize inputs was critical. While a script can be used to parameterize a conductance value [9], that approach was not used in this study.

• The Distributed void approach indicated that solder voiding had a small impact on overall thermal resistance. The Discrete void approach showed similar results up to ~30% voiding, but the results increasingly diverged as the voiding increased beyond that level. As long as solder voiding is less than ~30%, it appears reasonable that the Distributed void modeling approach can be safely used if the voiding is relatively discrete.

• Figure 10 indicates that, with the Distributed void approach, voiding of more than ~40% or more causes a small but noticeable increase in QFN thermal resistance. The Discrete void approach indicates that the impact of this level of voiding is much more substantial, but again only when the voiding exceeds ~40%. The distribution of voids in an actual solder layer falls somewhere between the range bracketed by these two extremes. But regardless, it appears that voiding needs to be greater than ~40% before it has a measurable impact on package thermal resistance. This observation agrees with recommendations in IPC specifications for circuit board assembly [8], which indicate that levels of thermal pad voiding of ~50% or less have a negligible impact on QFN thermal resistance.

• For the specific QFN geometry considered in this study, the presence of thermal vias had the most significant impact on the package thermal resistance. The next most significant factor on thermal resistance was the thermal boundary conditions (backside of the circuit board). In the ranges included in this study, solder pad voiding and concentrated power dissipation on the die area had similar, secondary impacts on the package thermal resistance compared to those other two factors.

• While the impact of solder voiding on QFN thermal resistance was not the most significant factor in determining overall package thermal

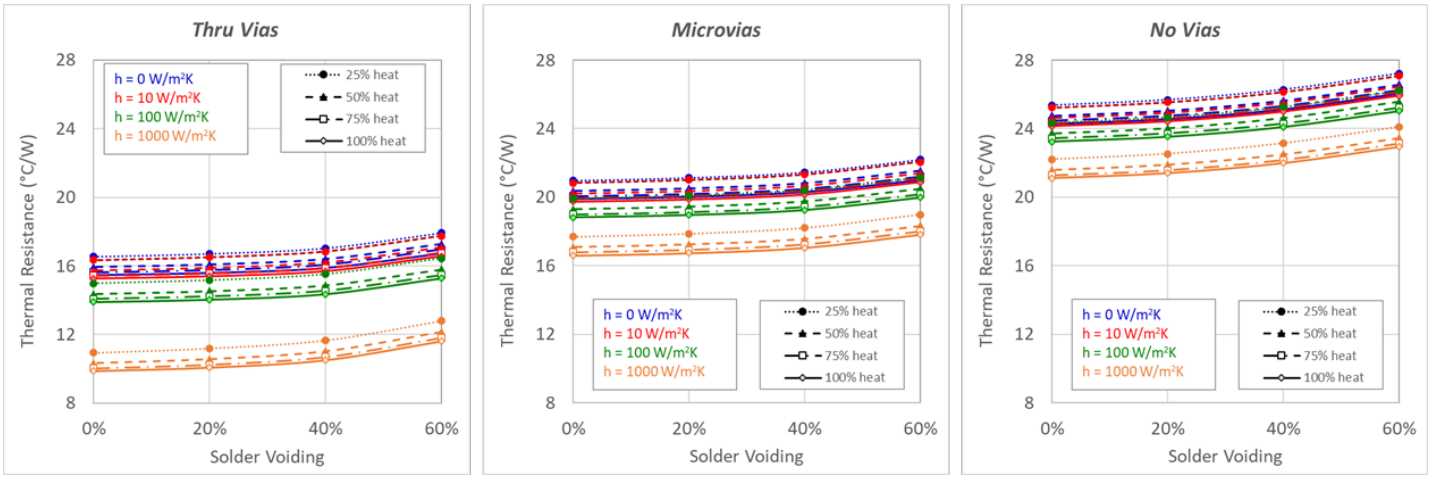

Figure 11: Effects of solder voiding, back-side cooling, and heat dissipation concentration on QFN thermal resistance for different via configurations

resistance, under optimal thermal conditions – namely, when thermal vias are included in a circuit board that has good back-side thermal resistance, a single large void of ~60% would increase the QFN thermal resistance by approximately 20% (from ~10 to 12°C/W).

CONCLUSIONS

Finite element modeling of the QFN component on a circuit board indicated that, even at the maximum levels identified in the test vehicle (>40%), voiding in the thermal solder pad attachment had a very small effect on the component thermal resistance. While Ref. [2] found that the presence of microvias in the thermal pad solder land may slightly increase voiding, the thermal benefits associated with the improved conduction provided by vias far outweigh any increase in thermal resistance caused by that voiding.

For the range of conditions evaluated in this study, the via configuration and back-side cooling conditions had the most significant effects on QFN thermal resistance. Thermal pad solder voiding is only likely to have a substantial impact on component thermal resistance in cases with otherwise excellent thermal conditions (vias under the package and good back-side cooling).

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BIOGRAPHIES

Dr. Ross Wilcoxon is a Senior Technical Fellow in the Collins Aerospace Advanced Technology group in Cedar Rapids, IA. He conducts research and supports product development in the areas of component reliability, electronics packaging and thermal management for airborne communication, processing, displays and radars. He has more than 50 journal and conference publications, is an inventor on over 30 US Patents, and is an editor of Electronics Cooling Magazine. Prior to joining Rockwell Collins (Now Collins Aerospace) in 1998, he was an assistant professor at South Dakota State University.

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David D. Hillman is a Metallurgical Engineer in the Advanced Operations Engineering Department of Rockwell Collins Inc. in Cedar Rapids, Iowa. Mr. Hillman graduated from Iowa State University with a B.S. (1984) and M.S. (2001) in Material Science & Engineering. In his present assignment he serves as a consultant to manufacturing on material and processing problems. He served as a Subject Matter Expert (SME) for the Lead-free Manhattan Project in 2009. He has published 200+ technical papers. Mr. Hillman was named a Rockwell Collins Fellow in 2016. He was named an IPC Raymond E. Prichard Hall of Fame award recipient in 2018. He serves as the Chairman of the IPC JSTD-002 Solderability committee. Mr. Hillman served as a Metallurgical Engineer at the Convair Division of General Dynamics with responsibility in material testing and failure analysis prior to joining Rockwell. He is a member of the American Society for Metals (ASM), the Minerals, Metals & Materials Society (TMS), and Surface Mount Technology Association (SMTA) and the Institute for Interconnecting and Packaging of Electronic Circuits (IPC).