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Modelling and mitigation of single-event upset in CMOS voltage-controlled oscillator

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Abstract. Single-event effects (SEEs) have been the primary concern in study of radiation effects since late 1970s with the discovery of soft errors in terrestrial and space environments. The interaction of a single ionized particle with electronic devices leads to SEEs. In this paper, single-event upset (SEU) on CMOS devices in designing of a voltage-controlled oscillator (VCO) is analysed. Further, mitigation approaches of SEU are also discussed. To observe the impact of radiation, a VCO was designed in Cadence Virtuoso, and GDSII file of one ring oscillator stage was extracted to incorporate the same design in Silvaco MaskViews. With the help of layer map information file, masks were identified and used to design the CMOS inverter structure file for simulation of SEU condition. The input parameters for SEU simulation were evaluated from linear energy transfer (LET) graph of heavy ion under space conditions. The current profile of CMOS inverter was extracted under influence of a high-energy particle with the help of LET graph of that particle. This current profile was applied to different nodes of VCO and upset conditions were identified. Further, the impact of upset conditions on lock stage of phase-locked loop (PLL) is discussed. Results show that the SEU has significant impact on the logic state of inverters used in ring oscillator stage compared with current starving/biasing stage. The current profile of CMOS device has strong dependence on the energy of ion, its track, angle of incidence and the material. When angle of incidence is very less ($7^\circ - 14^\circ$) the channel will be occupied by a funnel of charge and it leads to the maximum degradation of device. This work shows that a device operating at high frequency is more susceptible to SEU. Triple modular redundancy (TMR) and Radiation Hardened By Design (RHBD) can be used to mitigate SEU. TMR consumes more power and is less accurate compared with the RHBD approach.

Keywords. Radiation hardening; SEU; SEE; RHBD; voltage-controlled oscillators.

1. Introduction

Radiation effects on electronic devices exposed to cosmic rays have been the primary concern in study of radiation effects, especially those used in spacecraft avionics [1]. Due to technology scaling, size of these transistors is so small that a single charge induced by cosmic rays can change or upset the information bit in the storage cell of these circuits. Today it takes only 0.1 pC of charge to change the information bit of a memory cell, and 0.1 pC charge can be generated with around 10^6 electrons. Harsh radiation environment may be experienced by an orbiting spacecraft that may affect microelectronics in undesirable ways. Ionizing radiation affects the microelectronic components of spacecraft in a variety of ways. One of these effects is known as single-event effects (SEEs) [2–5].

SEE is the response of a semiconductor device under the influence of a single ionizing particle event. An erroneous change in the state of a semiconductor device is known as single-event upset (SEU) [6, 7]. In space, electrons, protons and other energetic particles are present in solar flare and cosmic rays. Out of these particles, 85% are protons. These particles can interact with the integrated circuit (IC) and degrade the performance. Shielding is applied to prevent the impact of radiation but it cannot stop all protons and heavy ions. Solar cycles also strongly affect the radiation environment. Ordinarily the helium ions in the solar emitted particle fluxes comprise 5–10%, and heavier ion fluxes are less than the galactic background. Radiation affects microelectronic devices either by ionizing or non-ionizing energy loss. Effects on ICs can be transient as well as

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permanent in nature [2–5]. Deposition of charge, SEU and total ionization dose (TID) are three important consequences of particle strike.

SEE has instant effects on the logic states of a voltage-controlled oscillator (VCO). Also, the voltage level at the output of charge-pump or loop filter might be changed and this would lead to erroneous output for a certain period of time or completely throw the phase-locked loop (PLL) out of lock when an SEE hit occurs [8].

In this work, we use a TRIM and Silvaco Atlas tool for radiation transport simulations to evaluate the impact of heavy ions on CMOS technology and its impact on VCO. A 180 nm CMOS inverter is designed by Victory Process and Athena using masks generated by DRC and LVS clean GDS-II file from Cadence Virtuoso. A CMOS inverter is also designed in claver for parasitic estimation. The current profile obtained from CMOS inverter under influence of SEU is applied to VCO at different nodes, and impact of SEU is observed. Later on, radiation hardened VCO design is proposed. The present work is a part of development of Radhard VCO by Semi-Conductor Laboratory, Department of Space (DoS), Government of India. Since low area and wide tuning range of VCO are major demands of application, we explored current-starved-type VCO.

2. Current-starved VCO design

Current-starved design is one of the best approaches to implement VCO when operating frequency range is high. In current-starved VCO, design can be easily tuned to work at high frequency. Here the total inverter stages are always in odd numbered form. Current-starved VCO is used to generate a clock signal inside the PLL. Frequency and phase of a reference signal are locked with the generated local clock signal [8].

VCO is one of the major components of PLL, which is sensitive to heavy ion strike. To find out the frequency of oscillation of VCO, total delay offered by inverters is desired. The total delay offered by inverters can be calculated by finding the capacitance offered by one inverter [8–14].

$$C_{tot} = C_{out} + C_{in}, \tag{1}$$

$$C_{out} = C'_{ox}(w_p l_p + w_n l_n), \tag{2}$$

$$C_{in} = \frac{3}{2} C'_{ox}(w_p l_p + w_n l_n). \tag{3}$$

Hence, total capacitance can be written as

$$C_{tot} = \frac{5}{2} C'_{ox}(w_p l_p + w_n l_n), \tag{4}$$

$$C'_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{T_{ox}}. \tag{5}$$

For $T_{ox} = 7$ nm

$$C'_{ox} = 4.931 \times 10^{-3}$$

where C_{in} is input capacitance of inverter, C_{out} is output capacitance of inverter, C_{tot} is total capacitance offered by one inverter, C'_{ox} is oxide capacitance, W_p is width of PMOS, W_n is width of NMOS, L_p is length of PMOS and L_n is length of NMOS.

Values of W_n, L_n, L_p and W_p used for RO stage are as follows:

$$W_n = L_n = L_p = 0.35\ \mu\text{m},$$
$$W_p = 0.7\ \mu\text{m}.$$

Hence, total capacitance is

$$C_{tot} = 4.53 \times 10^{-12}.$$

The time it takes to charge C_{tot} from 0 to V_{SP} is given by the relation

$$t_1 = C_{tot} \frac{V_{SP}}{I_d}. \tag{6}$$

The time it takes to discharge C_{tot} from V_{DD} to V_{SP} is given as

$$t_2 = C_{tot} \frac{V_{DD} - V_{SP}}{I_d}. \tag{7}$$

The I_d is the current when V_{in} is half of V_{DD}. Adding Eqs. (6) and (7) gives

$$t_1 + t_2 = C_{tot} \frac{V_{DD}}{I_d}. \tag{8}$$

Hence, for N stages, total delay can be given as

$$t_D = N C_{tot} \frac{V_{DD}}{I_d}. \tag{9}$$

The frequency of oscillation for the N stages current-starved VCO can be given as

$$f_{osc} = \frac{I_d}{N V_{DD} C_{tot}}. \tag{10}$$

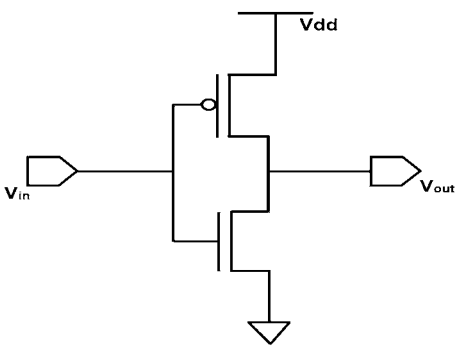

Figure 1. Schematic design of CMOS inverter for ring oscillator.

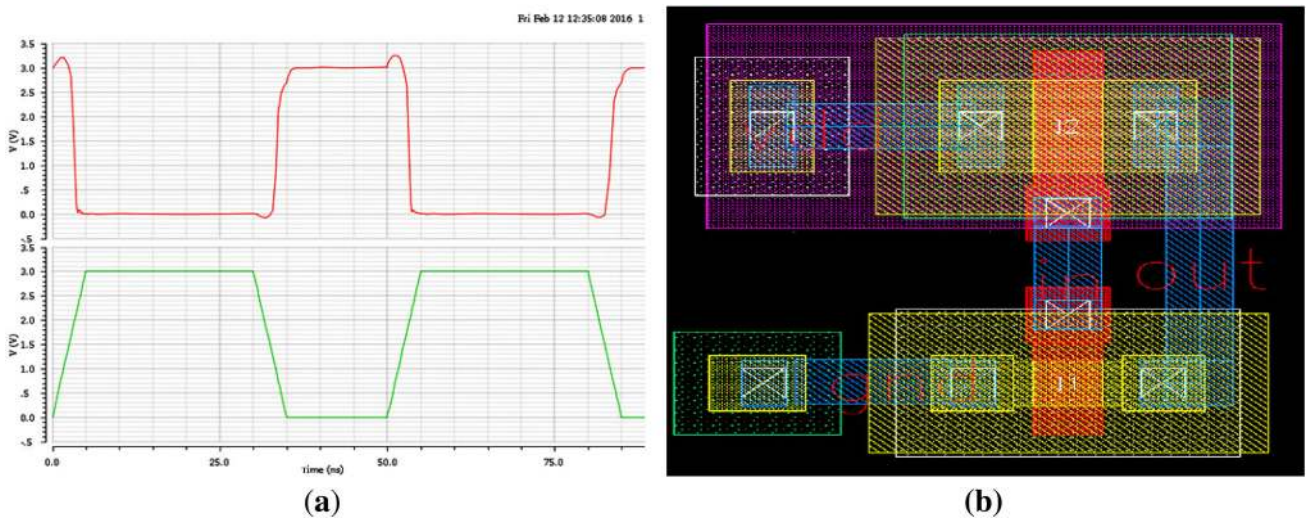

Figure 2. CMOS inverter cell: (**a**) input–output response and (**b**) layout.

This frequency is the centre frequency for the current-starved VCO. For 56.8 μA drain current and 450 MHz centre frequency, Eq. (10) evaluates N as 7.21. Hence, Eq. (10) suggests that for the 450 MHz centre frequency we should take 7 ring oscillator stages. In current-starved VCO, CMOS inverter is designed for ring oscillator stage. Schematics and output response of the designed CMOS inverter are shown in figures 1 and 2a, respectively, and those of the current-starved VCO are shown in figure 3.

3. CMOS process design in Silvaco

MaskViews enables the designer to incorporate the GDS-II file in Silvaco. Using the GDS-II file in Masksviews, masks can be prepared for process development. The masks can be used in Victory Process to develop 3D structures [15]. The CMOS device is shown in figure 4 at different stages in process development.

A cutline from MaskViews provides information to develop a 2D process in Athena as per GDS II file. A 2D CMOS device designed in Athena can also be converted to a 3D device using the Devedit3D tool. The 3D structure achieved from a 2D structure has triangular meshes but Victory Process provides meshes in the form of tetrahedrons. Hence, the method of extending a 2D structure to a 3D structure in Devedit is comparatively less accurate than that of the Victory Process 3D structure [16–19]. Figure 5 shows a 2D structure, extended 3D structure and donor concentration in 3D structure.

4. SEU in CMOS device

To incorporate SEU in a structure, analysis of the impact of a heavy ion in the structure is necessary. When a heavy ion strikes a CMOS device it breaks the covalent bonds and electron–hole pairs are generated. The generation of electron–hole pairs is in the form of a funnel along the ion track. The travelling ion has its kinetic energy, which is transferred to the structure, leading to electron–hole pair generation [19]. Linear energy transfer (LET) is the measure of incident energy that is deposited per unit length along the ion track. Atlas and Victory Device have the capability of incorporating SEU/transient simulation in 2D and 3D structures. It allows designers to specify the radial, length and time dependence of generated charge along tracks [16–18].

4.1 *LET*

As an ion transverses the CMOS device, the charged particle/ion slows down because it loses the kinetic energy

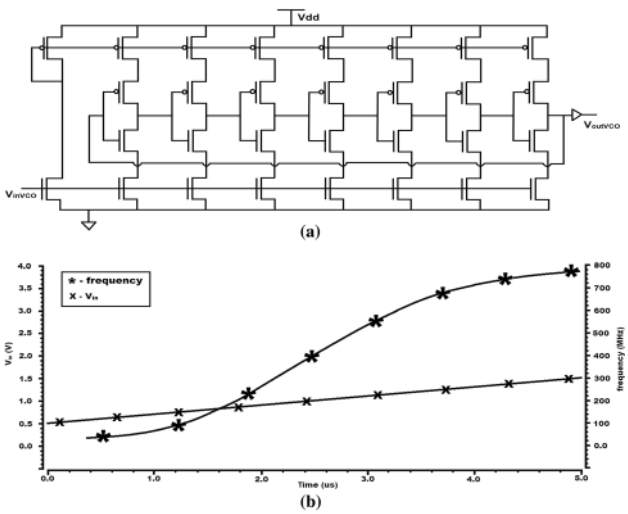

Figure 3. Current-starved VCO: (**a**) schematics design and (**b**) transient response of frequency and input voltage.

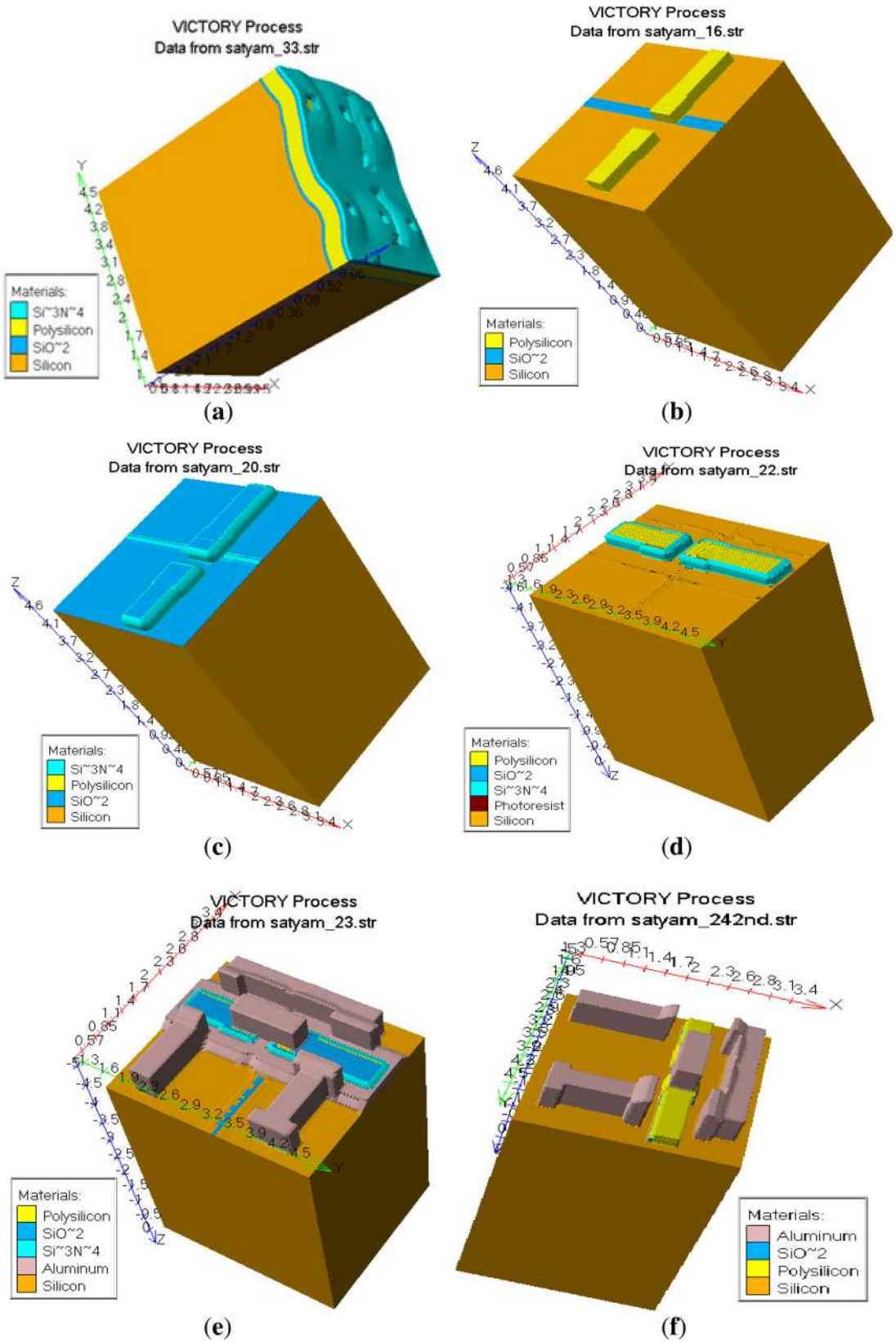

Figure 4. Development of CMOS process in Victory Process: (**a**) impact of negative mask and wrong diffusion time, (**b**) error due to geometrical etching, (**c**) impact of variable implantation dose, (**d**) structure with polysilicon and spacers, (**e**) bad etching methods and (**f**) final structure from Victory Process.

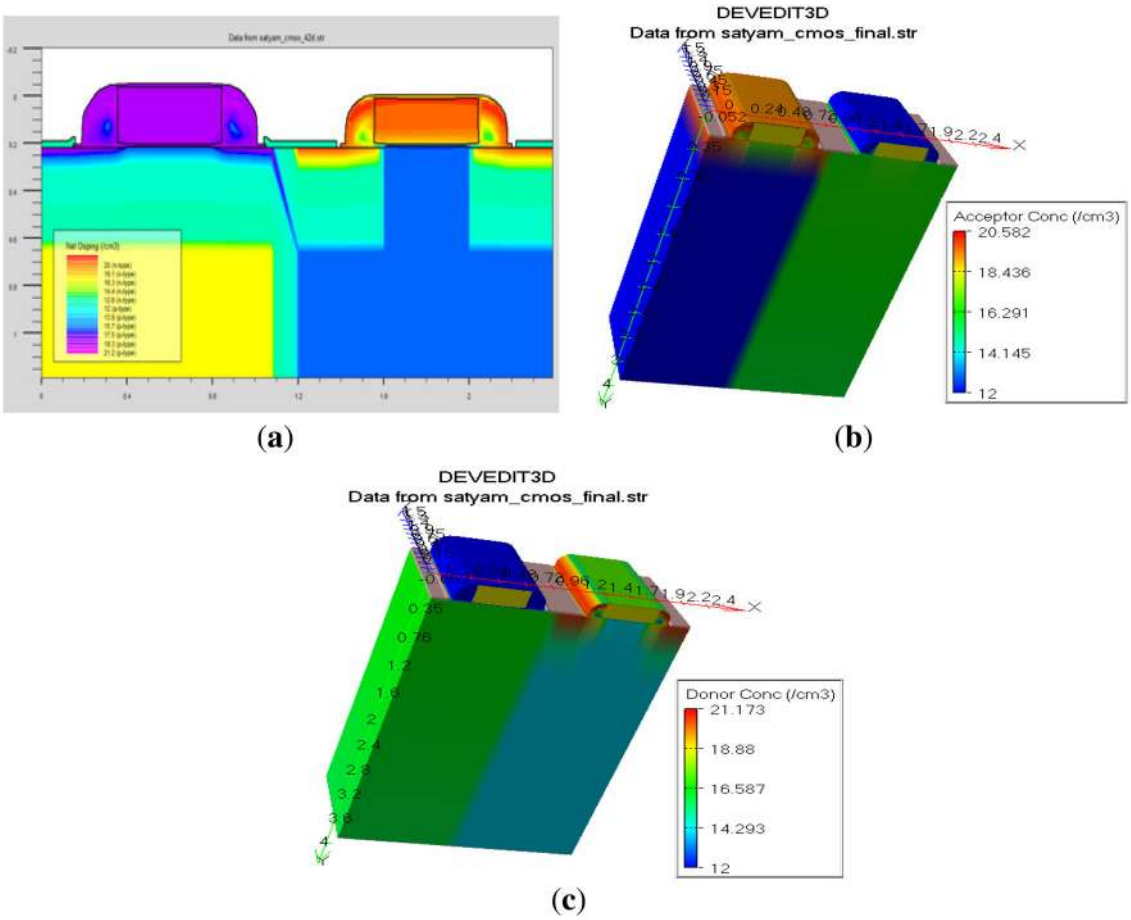

Figure 5. Development of CMOS process in Devedit3D: (**a**) 2D structure, (**b**) acceptor concentration and (**c**) donor concentration.

(figure 6). The energy loss of the ion throughout the ion track is measured in terms of LET. The LET can be called as a stopping power, with some restrictions in a material for a specific particle or species of particles. There is a little difference between stopping power and LET as shown in the following equations [20, 21]:

$$stopping\ power\ S = -\frac{1}{\delta}\frac{dE}{dx} \tag{11}$$

$$LET = \frac{dE}{dx} \tag{12}$$

$$specific\ ionization = \frac{\frac{dE}{dx}\ [\mathrm{eV/cm}]}{w\ [\mathrm{eV/cm}]} \tag{13}$$

where δ is material density, E is energy of incident particle, x is depth of penetration of incident particle in device and w is the energy required to generate one electron–hole pair for a specific material (w is material dependent).

For an 80-MeV hydrogen atom we can get specific ionization with the help of table 1.

$$LET = \frac{1.3}{\text{Å}} \tag{14}$$

$$LET = \frac{1.3 \times 10^8}{\mathrm{cm}} \tag{15}$$

$$specificionization = \frac{1.3 \times 10^8\ \mathrm{eV/cm}}{3.6\ \mathrm{eV}/ip} \tag{16}$$

$$specificionization = 3.61 \times 10^7 ip/\mathrm{eV} \tag{17}$$

This specific ionization can be seen as linear charge density as it comes out to be in *ip*/cm. Further, this linear charge density can be changed into volumetric charge density for funnel/generation rate calculations. For this work the LET is calculated in TRIM software for 80-MeV hydrogen in the target material (Si and SiO_2) [20, 21].

4.2 *Charge generation and current profile extraction*

Atlas and Victory Device have the facility of incorporating SEU/photo-generation transient simulation in 3D and 2D structures. It allows designers to specify the length, radial and time dependence of generated charge along the tracks. It has the capability of specifying single-particle strike and

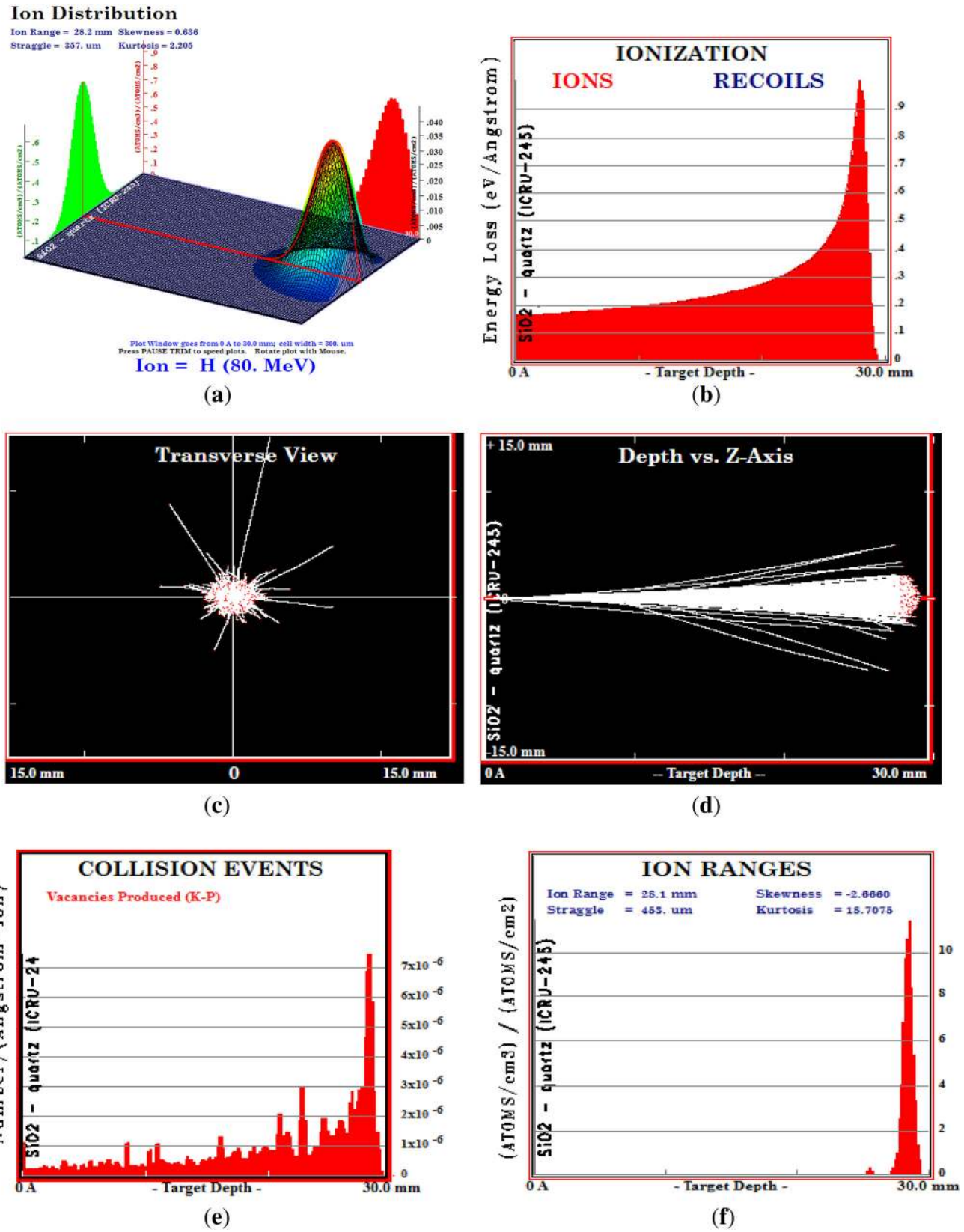

Figure 6. Single-event effect in CMOS device due to 80-MeV hydrogen: (**a**) ion distribution, (**b**) ionization/LET, (**c**) transverse view of incident ion track, (**d**) depth of ion penetration, (**e**) collision event in target material and (**f**) ion range with target depth.

Table 1. Value of required energy (w) to generate e–h pair in different materials.

Sl. no.	Material	w (eV)
1	Air	34.0
2	Si	3.60
3	Ge	2.80
4	GaAs	4.80
5	SiO_2	17.0

multiple strikes. Entry location point (x_0, y_0, z_0) and an exit location point (x_1, y_1, z_1) can be provided for each track. The generated electron–hole pairs at a point are a function of the distance along the track (l), the radial distance (r) from that point to centre of the track, and time t. Atlas provides the facility to define generation rate in the form of number of electron–hole pairs per cm^3 along the track according to Eq. (18):

$$G(r,l,t) = [D_n L_1(l) + SB_{dn} L_2(l)] R(r) T(t) \tag{18}$$

$$S = \frac{1}{2\pi R^2} \tag{19}$$

$$L_1(l) = A_1 + A_2 l + A_3 (e^{A_4 l}) \tag{20}$$

$$L_1(l) = B_1 (B_2 + l B_3)^{B_4} \tag{21}$$

where

S is scaling factor, R is radius, density $= D_n$ is number of generated electron–hole pairs and b.density $= B_{dn}$ is density in pc unit; if pc unit is not initiated then b.density can be taken in cm^{-3}; hence, it is similar to density.

L_1(l) and L_2(l) are variation of charge/carrier generation along the ion track. A_1, A_2, A_3, A_4 and B_1, B_2, B_3, B_4 are constants. To calculate the generation of electron–hole pairs from Eq. (18), the value of density (D_n), b.density, A_1, A_2, A_3, A_4, B_1, B_2, B_3 and B_4 are required. A_1, A_2, A_3, A_4, B_1, B_2, B_3 and B_4 can be calculated from the LET curve of the ion track.

Density can be calculated by extending the line charge density from Eq. (11) to volume charge density using the following equations:

$$\text{density} = \frac{\text{specific ionization}}{\pi r^2}. \tag{22}$$

By default, the value of r is taken to be of order 0.1 on the basis of practical results. Another way to find the value of r is using

$$r = \frac{K q_\alpha Q}{\frac{1}{2} m_\alpha V^2} \tag{23}$$

where Q is atomic charge generated in the target, K is Coulomb's constant, q_α is charge of incident particle, m_α is mass of incident particle and V is velocity of incident particle.

These calculated values are applied to the designed CMOS structure in Silvaco Atlas. Figure 7a shows the impact of SEU in designed CMOS structure.

In radiation ionization, linear charge decomposition (LCD) is the measure of energy transfer. LCD is measured in pc/μm unit and hence can directly be related to b.density parameter of Silvaco. However, b.density is taken in units of cm^{-3} for this work. We can convert LCD to LET value with the conversion factor of 0.01.

4.3 *Impact of SEU on designed VCO*

To incorporate the SEU in VCO, the current extracted from CMOS inverter file was given to one of the RO stage inverters with the help of a PWL current source at the particular node. The output wave frequency was observed during the single-event entry time. The extracted current

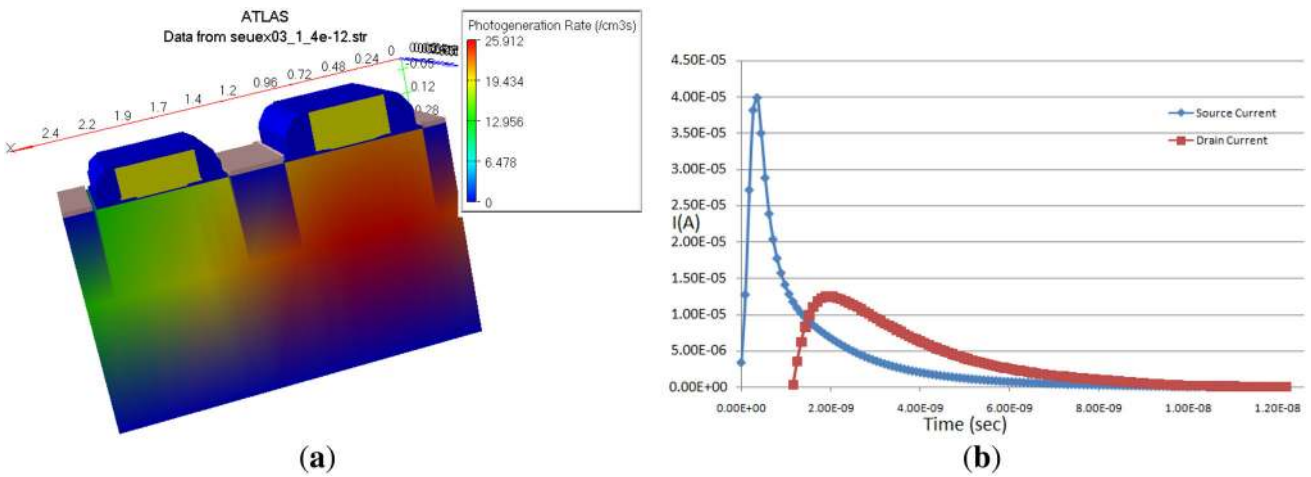

Figure 7. Impact of SEU on designed CMOS device: (**a**) generation rate along the particle track and (**b**) current profile of the CMOS device.

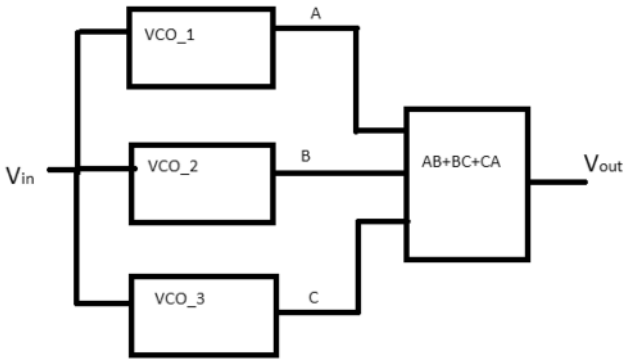

Figure 8. Block diagram of triple modular redundancy VCO.

profile is for an oblique incident angle, which leads to more electron–hole pair generation and hence more current. Hence, the worst case of SEU is analysed in this work; it may happen that the current is less than the current extracted or exists for less time. A schematic of the designed VCO is shown in figure 8 and SEU that can be tolerated by the designed VCO is shown in figure 9a.

The work presented is carried out at the Semi-Conductor Laboratory, which has its own 180-nm fabrication line. The TCAD software is used for enhancement of 180-nm baseline process and it is calibrated using a fab, various test structures and ET parameter report. The parameters/recipe used is from a baseline process and the results are expected to be within 10% tolerance limit. Various space grade products are in test for SEU/SEL at Inter-University Acceleration Center (IUAC), Delhi, and tests for other designs have shown acceptable results (within 10% tolerance limit) for simulated data and measured data.

5. Radiation hardened VCO design

Radiation hardened design is the one that can tolerate radiation effects or reduce it to a considerable value [22]. Radiation hardened design can be achieved by two methods:

(i) RHBP and (ii) RHBD.

Here, we can use the RHBD for radiation hardened design. We can implement two different techniques to reduce the SEU in a CMOS device. The two methods are

(i) triple modular redundancy (TMR) and
(ii) design of VCO by radiation hardened NOT gate circuit.

5.1 *TMR*

In the TMR approach, three different VCOs can be designed. Outputs of all the three VCOs are compared and the output that is the same for more than two VCOs is used. It works under the assumption that an ion will strike on a single VCO at a time and hence the output of other two VCOs will be intact.

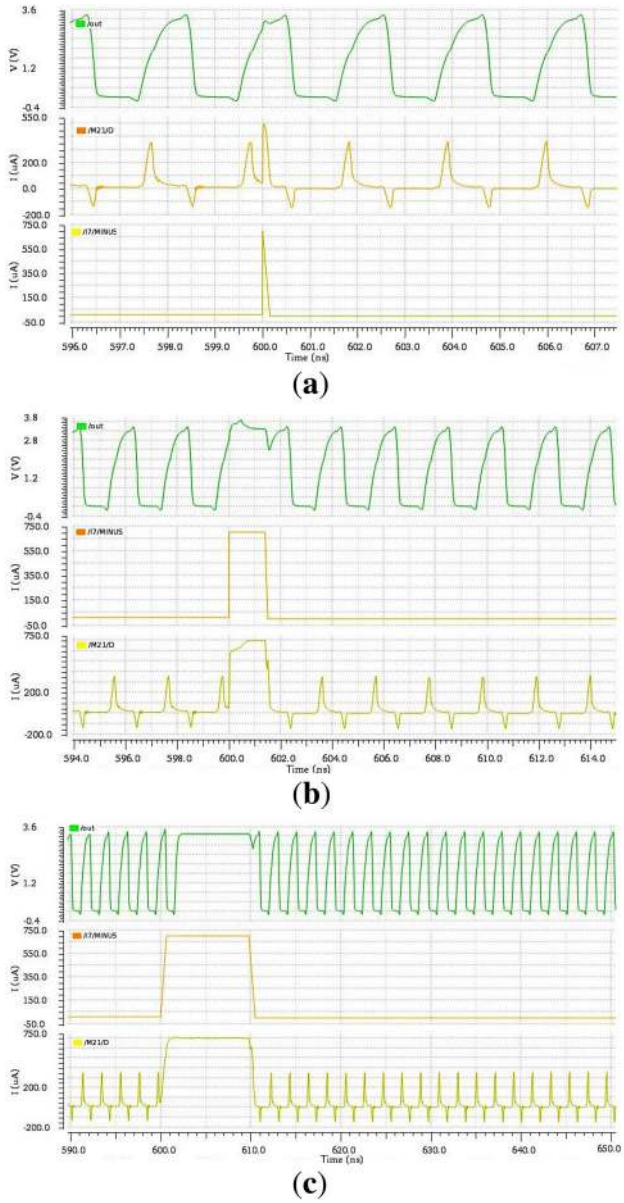

Figure 9. Response of VCO under SEU condition: (**a**) tolerable generated SEU current (100 ps), (**b**) non-tolerable SEU current (2 ns) and (**c**) longer duration SEU current (8 ns).

5.2 *Design of VCO by radiation hardened NOT gate circuits*

A radiation hardened NOT gate can be designed that can reduce the radiation impact to a considerable amount. In this method the NOT gate is designed in such a manner that decreases the impact of any short change in current through the circuit [23–25]. A schematic diagram and layout designed in Cadence Virtuoso for radiation hardened NOT gate is shown in figure 10.

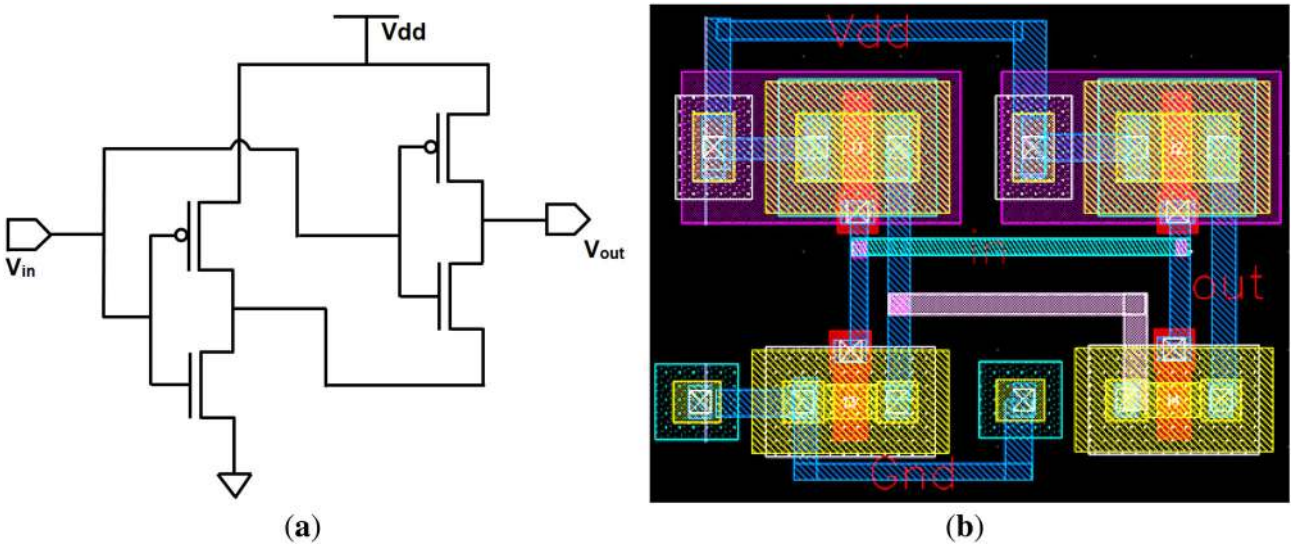

Figure 10. Radiation hardened NOT gate: (**a**) schematic diagram of NOT gate and (**b**) layout of the NOT gate schematic.

6. Power analysis of designed VCO and radiation hardened approach

From the schematic design shown in figure 1 and block diagram in figure 8 it can be stated that the power dissipation of TMR-based RHBD VCO is 200% more than that of designed VCO. Numerous advantages can be gained using the radiation hardened NOT gate approach for VCO design. From the schematic designs shown in figures 1 and 10a it can be stated that the power dissipation of VCO designed by radiation hardened NOT gate approach is almost 60% more than that of conventionally designed VCO. The TMR approach has the limitation that an ion should strike at only one VCO at a time and it also consumes more power than that of the radiation hardened NOT gate approach.

7. Conclusion

The design of radiation-tolerant VCOs that can be employed as an accurate oscillator in PLL for high-frequency clock generators has been analysed for space applications. This work suggests alteration of device width for achieving desired input and output capacitance to match frequency requirements of VCO. By altering device width, linear variation in frequency of VCO can be achieved over a long input voltage range. This experiment shows that the SEU has significant impact on the logic state of ring oscillator stage inverters used in VCO design compared with current starving/ biasing stage. Therefore, special care must be taken in the design of CMOS inverters to achieve radiation-tolerant VCO. The current profile of CMOS device has strong dependence on the energy of incident ion, its track, angle of incidence and the material. When angle of incidence is very less ($7^\circ - 14^\circ$) the device is more prominent for SEU because the channel will be occupied by a funnel of charge and degradation of device will be maximum. As angle of incidence increases ($0^\circ - 90^\circ$) the degradation of device decreases. This work shows that the degradation due to radiation has strong dependence on the operating frequency of the device. High-frequency VCOs are more susceptible to radiation as they go to the upset condition for even very small duration of SEU current. For radiation hardening, we can use TMR and RHBD approaches; the TMR approach consumes more power and is less accurate than the RHBD approach.

Acknowledgements

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