BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES
Vol. 54, No. 1, 2006

Modern micropassives: fabrication and electrical properties

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Abstract. This paper presents the concept and modern technological approach to the fabrication of discrete, integrated and integral micropassives. The role of these components in modern electronic circuits is discussed too. The material, technological and constructional solutions and their relation with electrical and stability properties are analyzed in details for linear and nonlinear microresistors made and characterized at the Faculty of Microsystem Technology, Wrocław University of Technology.

Key words: resistor, varistor, thermistor, thick-film, LTCC, multichip module, geometrical properties, electrical properties, long-term stability, pulse durability, low-frequency noise, trimming.

1. Introduction – general characterization of modern passives

Electronic devices, components, circuits and systems continue to become faster, smaller, lighter and cheaper. In general the progress in microelectronics is understood as an increase of number of transistors and the reduction of characteristic dimension of integrated circuits. But proper functionality of modern electronic circuits demands both active devices and passives (primarily resistors, capacitors and inductors, but also nonlinear resistors – thermistors and varistors, potentiometers, transformers, filters, fuses, mechanical switches and electromechanical relays).

The concept of passive components is very simple and they are inexpensive in a mass production. But about 10^{12} of passives are used by electronic industry every year and the world wide market in this segment is equal to about 25 milliard of US dollars. Similarly as other areas of electronics the passives undergo deep transformations. Around 1980's the through-hole packaging moved towards surface mount technology (SMT). Wirewound components were replaced gradually but rapidly by surface mount ones and about 80% passives is SMT adapted at present. According to the classification of National Electronics Manufacturing Initiative (NEMI) from USA the following generation of passives can be distinguished [1–5]:

— Discretes[1] – traditional single purpose surface mount or through-hole passives.
— Arrays – multiple passive components with identical function in a single SMT case.
— Networks – multiple passive components of more than one function in a single SMT case, usually 4 to 12 elements.
— Integrated – a package containing multiple passive elements of more than one function and possibly a few active elements in a single SMT or Chip Scale Package (CSP).
— Integral – passives either embedded in or incorporated on the surface of an interconnecting substrate.
— On-chip passives – passive components that are fabricated along with the active ICs as a part of semiconductor wafer.

The requirements for passives are dependent on type of circuits. For example, digital circuits include decoupling capacitors (0.01–0.1 μF), timing capacitors (10–100 pF), terminating resistors (20–100 Ω), pull up/down resistors (1–30 kΩ) and filter resistors (1 – 10 MΩ).

The average linear dimension of passives was decreased twice during recent twenty years (Fig. 1). But this is much less than changes of characteristic dimension and complexity of integrated circuits. This is one of the basic reasons why the ratio between passives and active devices is increased almost all the time (Table 1). However further miniaturization of passives reaches the equipment barrier – for example modern pick-and-place machines are not adjusted for accurate placement of 0201 (2.5×1.25 mm^2) and 01005 components. Therefore an old idea of planar arrays and networks was reanimated.

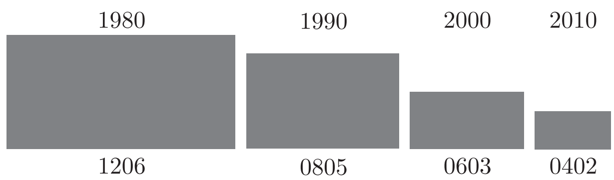

Fig. 1. Dominant package size for SMT passive components

Table 1
Number of passives on PC motherboards (after Ref.1, based on NEMI 2000 Roadmap)

Processor	Number of passives
486	165
Pentium, 120 MHz	369
Pentium, 200 MHz	593
Pentium II, 330 MHz	1473
Pentium III	2195

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[1]The classification and terminology used in this paper is based on classification of National Electronics Manufacturing Initiative (NEMI), USA

It is worth to notice that four 0603 capacitors, together with solder pads and technological margins, need 17.5 mm^2 area. But array of 4 identical capacitors placed in one 1206 ceramic structure needs only 7.75 mm^2 of printed circuit board area. Moreover, considering the necessary technological margins, the contribution of area (volume) of active layer in relation to nominal device dimensions is decreased for smaller packages. For example this is 43% in 1206 multilayer ceramic capacitors and only 19% in 0402 ones. Smaller area is not the only advantage of passive arrays and networks. In comparison with discrete surface mount components they are characterized by smaller serial inductance and better frequency behaviour as well as lower assembly cost and higher circuit reliability.

The integration of passives is the best solution for very high component density with increased electrical performance, improved reliability, reduced size and weight as well as lower cost. This process causes reduction or elimination of discrete SMT components and the same reduction of overall part count, elimination of solder joints, improvement of wireability and frequency behaviour due to elimination of parasitic inductance. The above advantages are possible thanks to multichip module (MCM) technologies [6–8].

Multichip modules (MCM) are an extension of hybrid technology, which permit a higher packaging density than can be assures by other approaches. The signal transmission lines in MCM are placed at many levels and the ratio of bare VLSI circuits‘ area (mounted on MCM surface) to MCM area is greater than 20%. Therefore MCM can transmit signals with frequency higher than 100 MHz. There are three kinds of MCM technology [1,5]:

- MCM-D, where interconnections are formed in a similar manner as in thin-film circuits, i.e. by depositing alternate layers of conductors and dielectrics onto an underlying substrate.
- MCM-L, where multilayer structures are formed by lamination of printed circuit board materials with etched patterns in copper foils and metallized vias.
- MCM-C, where multilayer structures are made by co-firing of ceramic or glass/ceramic tapes, similar to thick-film process. This means that vias are punched in green tapes and then filled with conductive electronic paste. The individual layers are screen-printed to create desired metallization patterns. Several such prepared tapes are laminated at elevated temperature and then co-fired at proper temperature to form a monolithic structure.

Modern MCM substrates consist not only interconnections but also many integral (embedded) passives. In this manner they fulfill the demands for the next generation of packaging needs. For example, surface mount resistors and capacitors have inherent parasitics, due to their geometry. Perhaps the most important is the parasitic inductance, which affects the high frequency behaviour and thus limits transmission speed. But integral passives significantly reduce the parasitics connected with the current discrete passive packages. Much information about current situation in the area of discrete, integrated and integral passives, this is about their fabrication as well as physicochemical, electrical and stability properties one can find in [2–4] and references therein. This paper concentrates on activity of Faculty of Microsystem Electronics and Photonics, Wrocław University of Technology in the area of passives, especially linear and nonlinear resistors.

2. Microresistors

2.1. Fabrication and geometrical properties. Most of resistors made in microelectronic technologies have very simple construction – planar resistive layers are deposited onto substrates used in thin- or thick-film technology or on inner/outer layers applied in the case of MCM-C, MCM-D or MCM-L technologies (Fig. 2). Except of this classical solution we investigated novel configuration of passive components, especially recommended for Low Temperature Cofired Ceramics (LTCC) technology [9]. So far the vias were filled by conductive material and were used as interlayer connections in multilayer circuits. Open vias were also applied for the change of thermal conductivity/insulation. In our solution (Fig. 3) vias were filled by resistor, thermistor or varistor inks and after lamination and firing the microvolume resistors, thermistors or varistors were obtained, respectively. These components were also called three-dimensional (3D) because, contrary to planar topology, all their dimensions limited by via diameter and tape thickness are comparable. One should remember that microresistor means situation where all dimensions (length, width, thickness or diameter) are less than 1 mm.

One part of our activity in the area of microresistors was connected with miniaturization of planar components, both on alumina substrate as well as in/on LTCC substrates. Different attempts were made. For example, the 60×125 μm^2 microresistors were fabricated using photoprintable silver-based Fodel inks as resistor termination [10] whereas 80×300 μm^2 were made, when the distance between electrodes was created by laser cutting of dried conductive films [11]. These microresistors were made on alumina. The distance between electrodes, i.e. proper resistor length, was created by laser cutting of dried conductive films. Next the resistive film was screen-printed (Fig. 4). This means, that the fabrication procedure was very similar to used in LTCC technology. Because of various behaviour of cut films during firing, the real notch width was dependent on conductor metallurgy. The spaces equal to 109, 120 and 96 μm have been received for 80 μm designed distance in the case of PdAg-, Au- or Ag-based films, respectively.

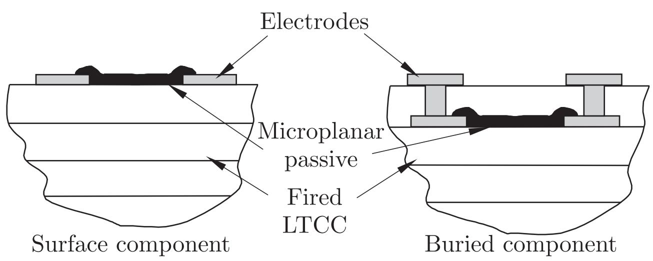

Fig. 2. Schematic cross-section of surface and buried microplanar microelectronic resistor

Table 2
Basic electrical properties of standard resistors and microresistors with laser patterned gap as a function of kind of resistive ink, contact metallurgy and screen density

Resistive ink	Contact metallurgy	Screen density (mesh)	Resistor 1.5×0.3 mm^2		Resistor 0.08×0.3 mm^2	
			$R_\square$ $(\Omega/\square)$	HTCR (ppm/K)	$R_\square$ $(\Omega/\square)$	HTCR (ppm/K)
DP 8019	PdAg	400	238	+12	85	+2
DP 8019	Au	400	303	–21	179	+1
DP 8019	Ag	400	237	–9	121	–52
DP 8039	PdAg	400	25370	+7	5680	–153
DP 8039	Au	400	40230	–58	15760	–23
DP 8039	Ag	400	26280	+5	12810	–407
R 344	PdAg	200	11550	–10	5850	–74
R 344	Au	200	11840	–18	5230	–50
R 344	Ag	200	13110	+13	11810	+71

Conventional screen printing permits to fabricate only 100 μm conductive lines and spaces in volume production. Therefore the photoimageable thick-film technology is used in applications requiring high packaging density. Various photosensitive conductor and dielectric inks are commercially available. But such resistive compositions are only at the research and development stage. The 1 kohm/sq. experimental RuO_2-based Fodel resistive ink from Du Pont and Ag-based DP 6453 Fodel conductor were used for microresistors‘ fabrication on alumina as well as onto LTCC substrate (in this case both postfired and cofired resistors were made) [12–14]. The conductors were made in full Fodel process whereas the resistors were screen-printed or made in Fodel process. Two basic test structures (A and B) were designed (Table 3).

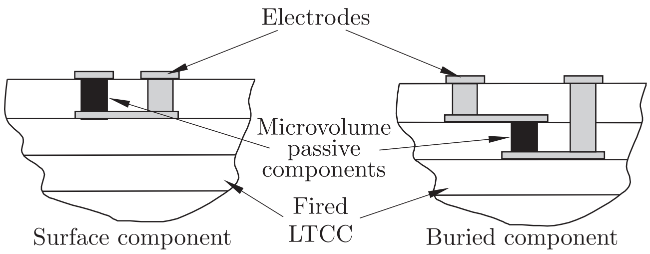

Fig. 3. Schematic cross-section of buried and surface microvolume resistor (especially recommended for LTCC technology)

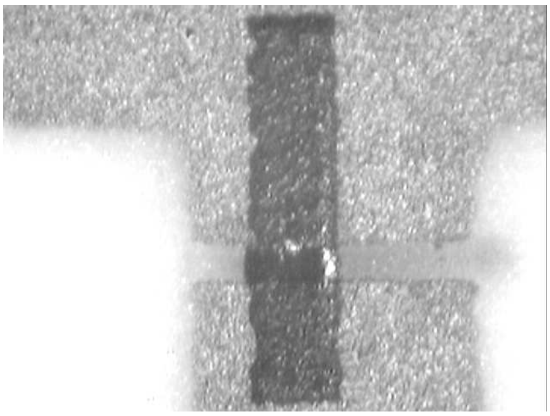

Fig. 4. Microresistor with laser patterned and fired gap in thick-film conductor and screen-printed resistive film

Table 3
Designed length and width of LTCC and thick-film microresistors

	Length (μm)	Width (μm)
Structure A	50	50
	100	100
	200	200
Structure B	50	50/100/200
	100	50/100/200
	200	50/100/200
	400	50/100/200
	800	50/100/200

The microresistors on alumina were made in two different fabrication procedures. In variant I conductor tracks were made at the beginning (based of Fodel process) and next resistive layer were conventionally screen-printed through 325 mesh stainless screen. In variant II resistive film was subjected to the Fodel process and fired at the beginning and then conductor terminations were made in next Fodel process. Surface resistors prepared according to variant I were made onto LTCC substrate. They were fabricated as postfired (resistor is screen-printed onto previously laminated and fired LTCC substrate) or cofired (resistor is screen-printed onto green ceramic tape and then the whole structure is laminated and fired in the single process) components.

The optical backlight microscope served for length and width measurements (Fig. 5) whereas the laser profilometer was used for three-dimensional characterization of investigated components (Fig. 6). The length of resistors is dependent on Fodel conductor behaviour. In general photosensitive conductor materials exhibit shrinkage. Therefore the conductive tracks realized in Fodel technology have smaller widths and larger spaces than designed. This leads to somewhat larger length of microresistors in comparison with design (by about 20 to 40 micrometers). The average width of microresistors made in Fodel process is smaller than design pattern. The same parameter for screen-printed ones exceeds designed one by about 20–50 μm. There are also noticeable differences in width of microresistors in dependence on substrate and firing technology. Moreover the standard deviation for screen-printed structures is larger than for Fodel ones. Therefore the actual aspect ratio (number of squares) does not agree with assumed one and the ratio between maximal and minimal number of squares is increased for smaller design structures. Chosen results are presented in Table 4; more details can be found in [12–14].

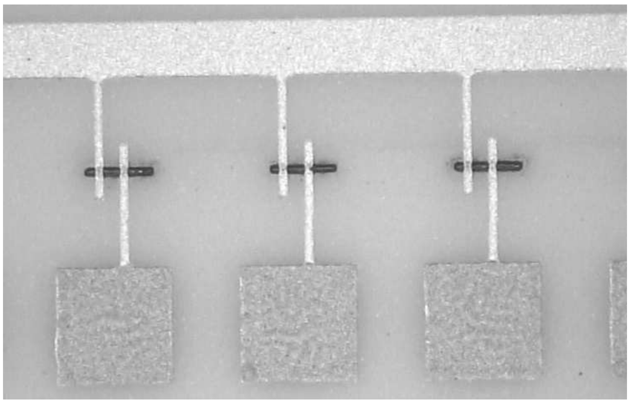

Fig. 5. Microresistors fabricated in full Fodel process (designed width – 100 μm)

Table 4
Mean dimensions and their standard distribution for screen-printed and full Fodel processed microresistors made on Al_2O_3

Structure	Planar dimensions (μm)		Thickness (μm)
	Design	Realized	
Al_2O_3/Fodel	length = 50	86±2	
	100	143±4	
	200	229±12	
	400	405±12	
	800	826±10	
	width = 50	40±4	5.5
	100	74±6	18.0
	200	166±5	18.0
Al_2O_3/screen-printing	length = 50	86±2	
	100	143±4	
	200	229±12	
	400	405±12	
	800	826±10	
	width = 50	79±8	4.5
	100	127±10	7.0
	200	227±10	9.0

Except planar it is also possible to manufacture 3D components, made inside substrate to exploit it in a more efficient way [9]. Passives were made inside alumina as well as in LTCC (DP 951) substrate. The first step of passives' fabrication process in alumina was drilling of vias in a substrate with CO_2 laser. Next vias were filled with paste by injection under 0.3–0.6 MPa pressure. Then filled holes were dried and subjected to high pressure of 20 MPa to improve uniformity and density of the microvolume. Vias were filled up again; after drying the conductive tracks were screen-printed and structures were fired (in general at 850°C). In case of LTCC structures vias were cut in two laminated green tapes and filled by proper ink. Before firing two additional bottom tapes were laminated to structure [15]. Microcomponents of five different diameters: 100, 200, 300, 400 and 500 μm were made. The length was determined by thickness of substrate and for alumina ones was 260 and 640 μm, for LTCC – 300 μm.

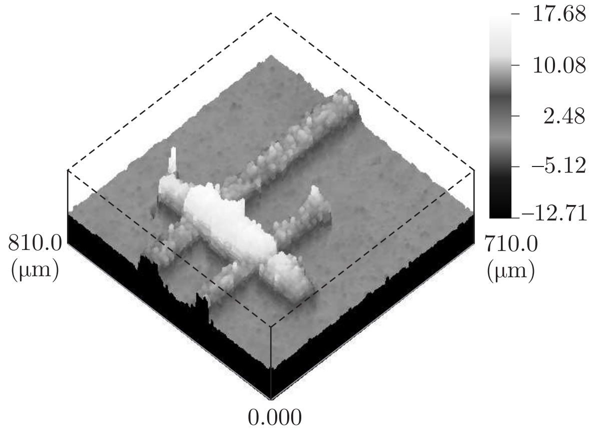

Fig. 6. Three-dimensional profile of 100×100 μm^2 LTCC-cofired resistor

The standard resistors, even with reduced dimensions, have two terminations. When they create resistor arrays the designer has to take into consideration all necessary technological margins. The whole resistor array still has relatively large area. A reduction of total component area is possible as a result of substitution of array consisting of two-terminal resistors by equivalent multicontact resistor [16]. Simple three-contact resistors and more sophisticated six-contact structures were designed based on conformal mapping used for calculation resistance values as well as determination of coordinates of contact edges. Different topologies of three-contact and six-contact test patterns were designed and fabricated – the examples are shown in Fig. 7. The following dimensions were chosen for three-contact resistors: 300×100, 600×200, 900×300 and 1500×500 μm^2 whereas 4×2, 3×1.5 and 2×1 mm^2 structures were made for six-contact ones. All resistors were prepared on standard alumina and DP 951 LTCC tape (Du Pont). For all tested resistors we noted that real planar dimensions were smaller than designed ones; by about 15–25 μm for photopatterned conductive ink and 50–60 μm for screen-printed resistive inks [17].

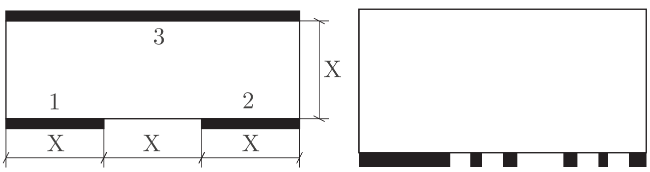

Fig. 7. Examples of three-contact and six-contact resistor topology

Table 5
Critical electrical field and power spectral density as a function of resistor dimensions, applied technological variant and pulse width

Substrate/ deposition method	Designed resistor (μm^2)	t_p = 0.1 ms		t_p = 5 ms	
		E_{CRIT} (V/mm)	$(P_s)_{CRIT}$ (W/mm^2)	E_{CRIT} (V/mm)	$(P_s)_{CRIT}$ (W/mm^2)
Al_2O_3/ Fodel	100×100	389	212	264	102
	200×200	340	175	218	71
Al_2O_3/screen-printing (SP)	100×100	319	115	189	55
	200×200	313	167	179	52
LTCC- cofired/SP	100×100	314	89	208	49
	200×200	321	109	169	27
LTCC-postfired/SP	100×100	274	81	188	53
	200×200	265	160	116	50

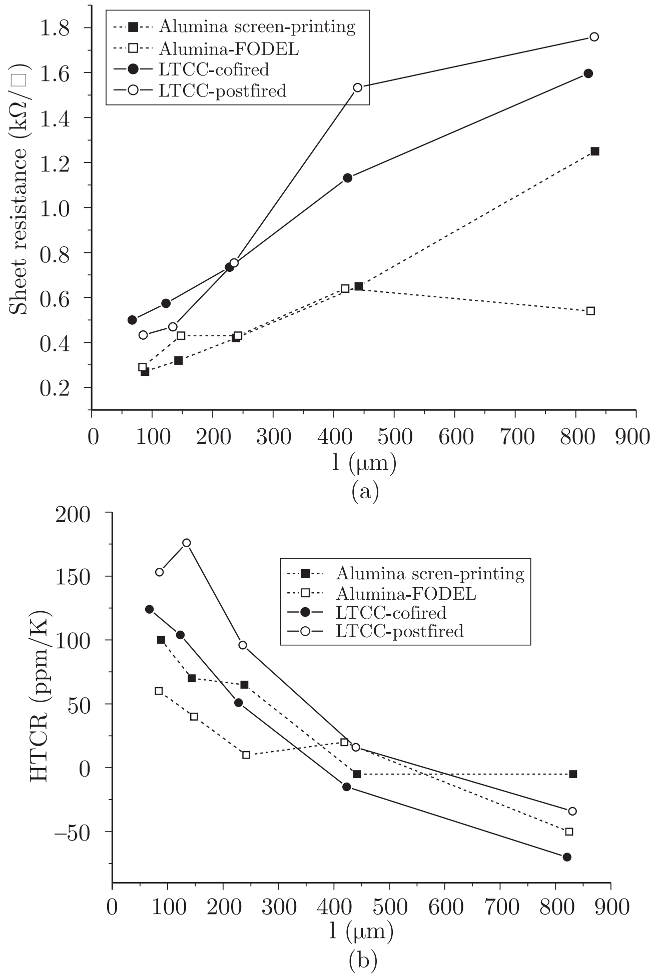

Fig. 8. Influence of kind of substrate and resistive film deposition method on sheet resistance (a) and HTCR versus resistor length dependence (resistor width w = 100 μm) (b)

2.2. Electrical and stability properties. Basic electrical properties include sheet resistance and its distribution as well as hot temperature coefficient of resistance (HTCR) and its distribution. They were related to microresistors' length, width and thickness [10–14,17]. Moreover normalized temperature dependence of resistance in a wide temperature range (between –170°C and 130°C) was measured and analyzed [10,12]. All of these parameters were characterized for as-fired and thermally aged microresistors. Moreover the AC properties in the frequency range from 1 Hz to 3 GHz [18,19], low frequency noise [18–20] and durability of microresistors to various short electrical pulses [13–14,21–23] were investigated.

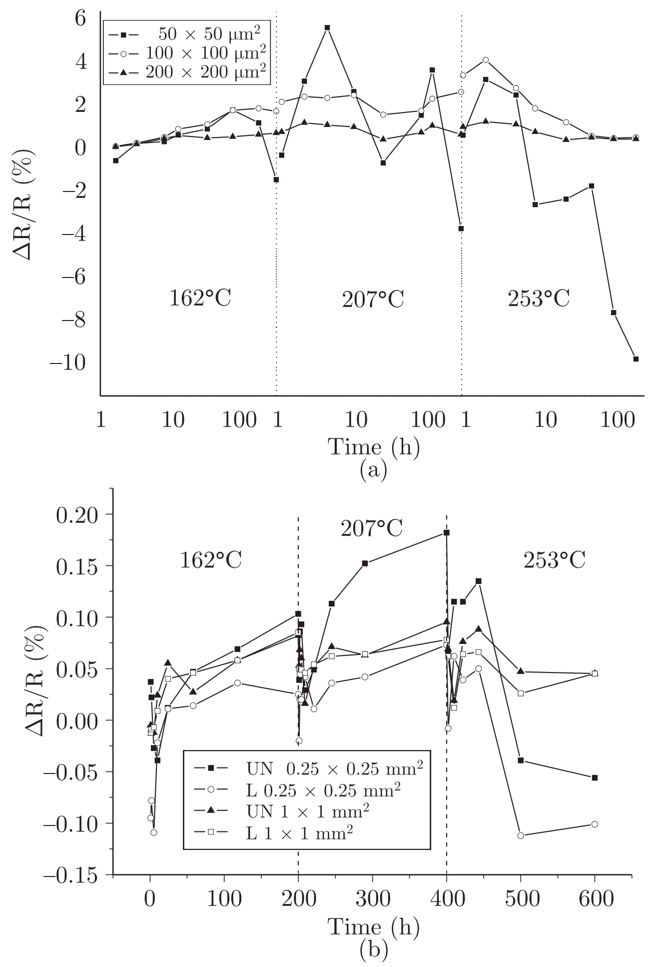

Fig. 9. Long-term thermal stability of LTCC-postfired thick-film microresistors (a) and typical cermet thick-film resistors (DP 6620, 100 ohm/sq) (b)

The basic electrical properties of standard thick-film resistors and microresistors with laser-patterned gap in conductive film are compared in Table 2. There are many technological variants (e.g. those with Au terminations), where rather small geometrical effect is appeared (very similar values of HTCR, insignificant difference in sheet resistance of both tested topology). Therefore the above solution seems to be appropriate even for 01005 (0.25×0.125 mm^2) components.

Microresistors with Ag-based Fodel terminations exhibit much stronger geometrical effect (this means significant dependence of sheet resistance, hot temperature coefficient of resistance and normalized temperature dependence of resistance on resistor length) from those with laser patterned electrodes (Fig. 8). The R(T) characteristics of these components are typical for thick-film resistors. They have resistance minimum at certain temperature. This minimum shifts towards lower temperatures when the resistor aspect ratio is decreased.

The long-term thermal stability of microresistors made from experimental photosensitive ink and typical thick-film resistors was compared (Fig. 9). The samples were kept in turn for about 200 hours at three different temperatures – 162°C, 207°C and 253°C. The behaviour of 200×200 μm^2 microresistors is similar to typical thick-film resistors. The 100×100 μm^2 microresistors also exhibit acceptable results but somewhat worse than larger structures.

Pulse durability test is very promising and efficient characterization method for LTCC and thick-film microsystems [21,22]. For example, by changing the pulse duration it is possible to find so-called load hyperbola (the dependence between electrical load and component life time), i.e. to find an admissible power of electronic devices. Investigations of pulse durability can help to fix the critical electric field and next surface or volume power density for microresistors in dependence on resistor dimensions or pulse duration. The self-made Programmed Pulse Generator [22] was used for investigation of microresistors' pulse durability. During the measurements the rectangular pulse voltage (with duration 0.1 ms – "short" pulse, or 5 ms – "long" pulse and 2 seconds pulse off time between pulses) was changed in linear stair mode. During the pulse the voltage was kept constant whereas the current was measured at the end of every pulse. Several one-square microresistors (structure A with 50×50, 100×100 or 200×200 μm^2 microcomponents) were tested for various pulse durations, substrate kinds and deposition techniques of resistive layer. This permitted to find the current-voltage (*I-V*) characteristics used for calculation of the *R-V* dependencies. The electrical field (*E*) and the surface density of power (P_s) were calculated based on real dimensions of microcomponents. The example of relative changes of resistance as a function of electrical field or surface power density is shown in Fig. 10.

We assumed, that the pulse amplitude is called critical (V_{CRIT}) for chosen pulse width if during 2 identical rectangular pulses the resistance of tested components was changed by more than ±10% or investigated devices were destroyed completely. Values of V_{CRIT} and actual planar dimensions allow calculate E_{CRIT} and $(P_s)_{CRIT}$. They are summarized in Table 5.

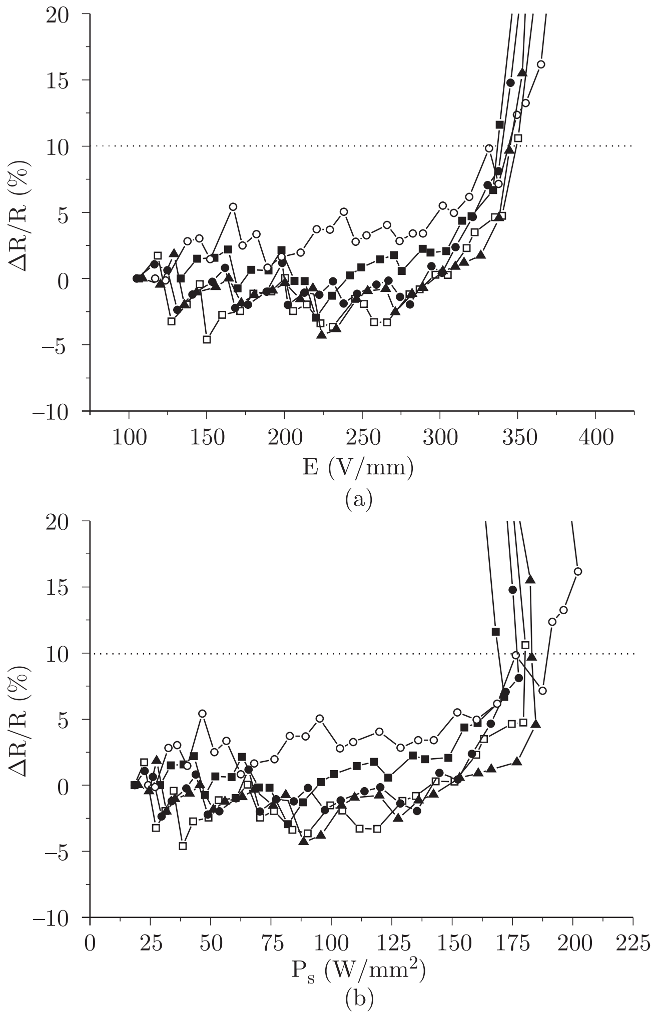

Fig. 10. Relative resistance changes versus electric field and pulse surface power density for 200×200 μm^2 thick-film microresistors screen-printed on alumina (t_p = 0.1 ms)

Microresistors made in full Fodel process show much weaker dimensional effect and exhibit noticeably smaller distribution of basic electrical properties. Much better reproducibility of this technology leads also to their much better pulse behaviour (increase of critical electrical field and surface power density approximately by 20–30% in comparison with screen-printed ones).

It is worth adding that resistors with smaller planar dimension are characterized by better frequency behaviour i.e. wider transmission band (Fig. 11).

2.3. Trimming. Currently laser trimming is the dominant trimming method of thick-film and LTCC resistors. As-fired thick-film resistors have the resistance tolerance within ±20% range and this tolerance is increased for smaller components. It was shown that buried LTCC resistors can be laser trimmed through one thin LTCC tape [11]. But in general the laser trimming is insufficient for thick-film and LTCC microresistors. Therefore the novel trimming methods are necessary for microresistors, especially when they are embedded in LTCC substrate [23,24]. The most advanced research is connected with trimming by energy of high voltage pulses. The electrical (normalized temperature dependence on resistance, low frequency noise) and stability (relative resistance drift, changes of current noise index) characteristics are presented below for untrimmed, pulse voltage trimmed or laser trimmed thick-film resistors subjected to the step-increased long-term thermal ageing at 162°C, 207°C and 253°C.

The untrimmed and laser-trimmed resistors are much more stable than voltage pulsed ones – Figs. 12 and 13. Untrimmed resistors exhibit resistance increase at all temperature levels. This increase is larger at the beginning of every temperature step but even after keeping the samples at 253°C it does not exceed 1%. Very small laser trimmed resistors (0.25×0.25 mm^2) have negative resistance drift after keeping at 207°C and

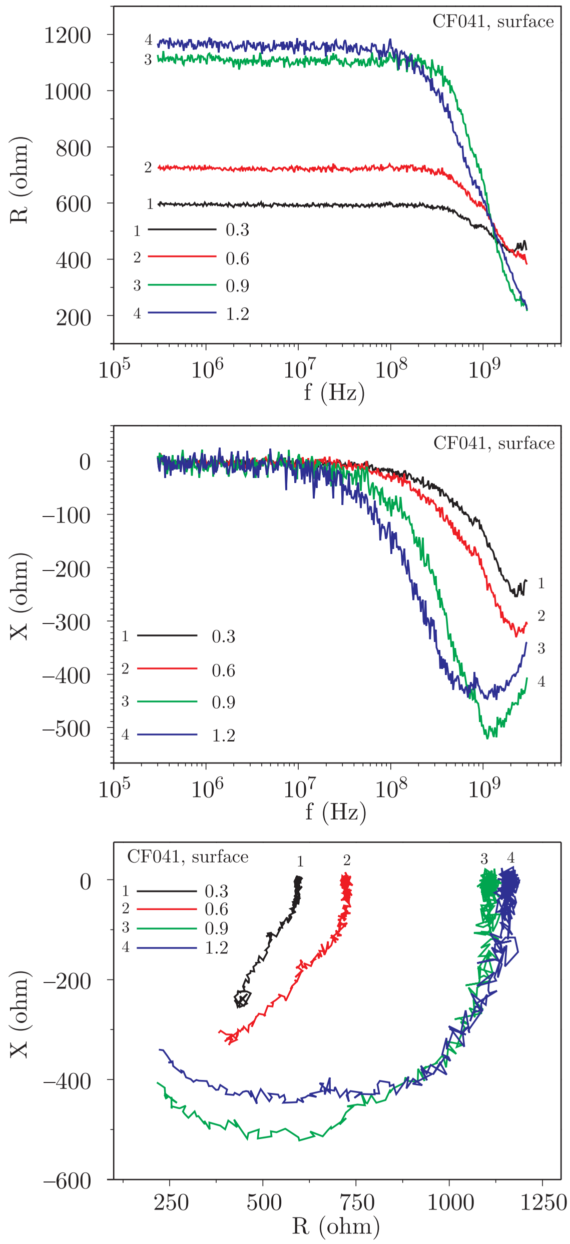

Fig. 11. Bode and Nyquist plots of CF 041 LTCC surface resistors with various unit square

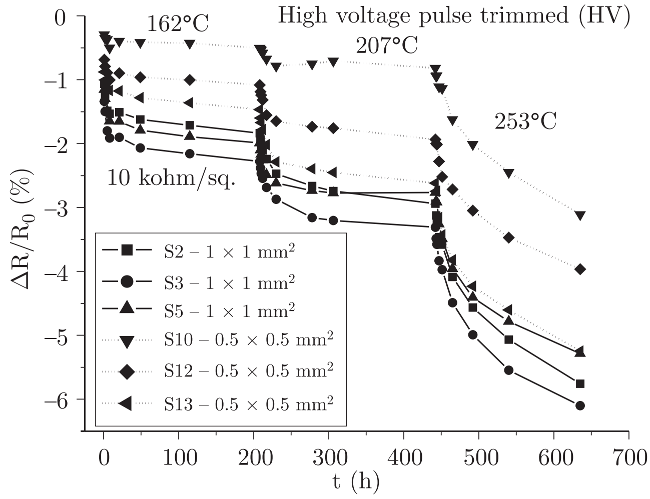

Fig. 12. Long-term stability of high voltage discharge trimmed 10 kohm/sq. thick-film resistors (changes of resistance in trimming process: S2; –13.0%, S3; –10.3%, S5; –5.4%, S10; –3.8%, S12; –10.5%, S13; –13.6%)

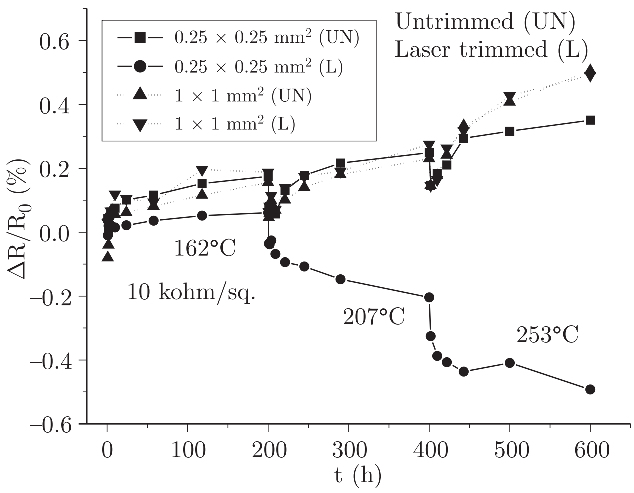

Fig. 13. Long-term stability of untrimmed and laser-trimmed 10 kohm/sq. thick-film resistors

253°C but still within ±1% range. Resistors trimmed by energy of high voltage pulses show decidedly larger negative drift of resistance. It depends on trimming level. Resistors with higher trim level are much less stable at every investigated temperature.

Current Noise Index (*CNI*) is one of the most important parameters of resistors. The noise with a typical $1/f$ shape (caused by equilibrium resistance fluctuations) is dominant in the low frequency range independently of the trimming method. The initial (i.e. before ageing) noise intensity is comparable for all resistors made of the same ink and of identical planar dimensions. After long-term thermal ageing the *CNI* of high voltage-trimmed resistors increases noticeably in spite of simultaneous slight decrease of resistance. The CNI increase is larger in case of strongly trimmed structures – Fig. 14. On the other hand the noise level of untrimmed and laser trimmed resistors does not change after ageing process (similarly as resistance).

Only a few papers discuss trimmed resistor design problem. Trim resolution is inversely proportional to sensitivity (which is the first derivative of trim characteristics). Therefore this characteristic is very important to calculate the resistor layout dimensions. Very recently a new resistor configuration was proposed for laser trimming – two-contact resistors were replaced by three-contact distributed structures (Fig. 15) trimmed by narrow cuts just around additional contacts of different shapes [25]. An additional contact lowers the resistance value between the other contacts, this widens resistance trimming range and due to this there is no need to design resistors with lower resistance values than the required nominal value. What is more, this enables us to achieve correction with smaller cut length so it can lead to a faster and cheaper hybrid IC fabrication process.

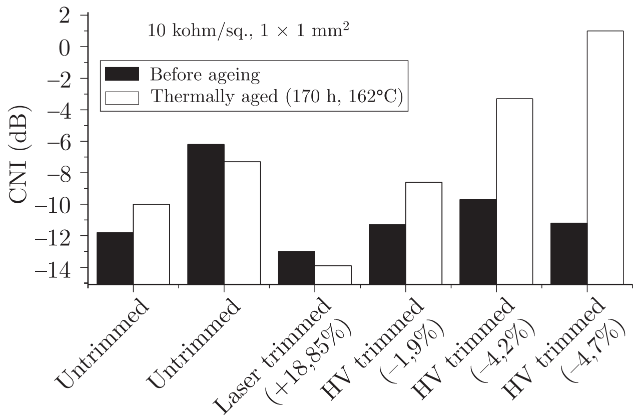

Fig. 14. Changes of current noise index of 10 kohm/sq. as a function of trimming method and ageing process

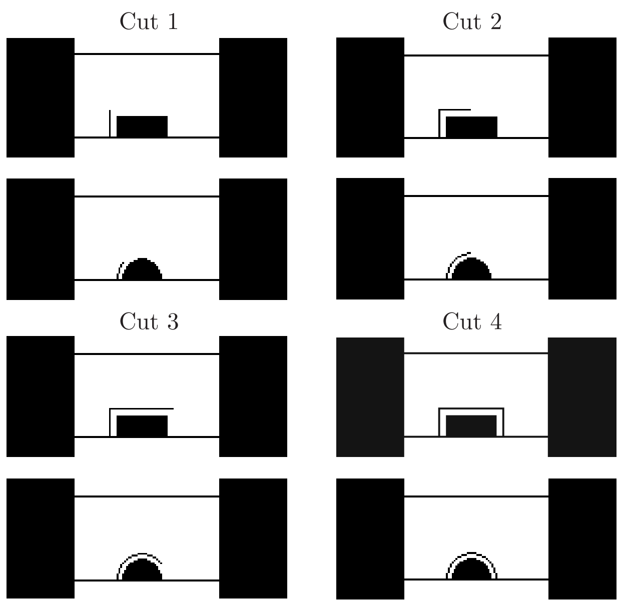

Fig. 15. Illustration of laser cut length used in three-contact resistors with rectangular and semicircular additional contact

It was proved [26] that:

- Three-contact resistors assure larger range of resistance increase than two-contact ones for the same length of trim cut.
- The shape of additional contact as well as the shape of laser trimming pathway affect the trim range and the trim sensitivity characteristics versus trim pathway length.
- Long-term thermal stability of tested resistors does not depend on resistor configuration, shape of additional contact and cut length.
- Trimmed resistors have larger noise level and worse pulse durability independently on resistor configuration.
- Cut 1, which can be treated as typical single P-cut, causes the strongest deterioration of noise level and pulse voltage durability.

The three-contact structure with semicircular additional contact seems to be the most appropriate for proper pulse durability, even when long trimming kerf is necessary.

3. Nonlinear resistors

3.1. Thermistors. Typical commercial NTC and PTC thermistors are realized in ceramic technology. Because of many similarities between ceramic and thick-film technologies these devices were adapted very quickly for realization in thick-film technology. Thick-film NTC thermistor pastes consist of the powder of spinel-type semiconductor metal oxides (or spinel-type semiconductor is formed during firing process from powders of various metal oxides) blended with the powder of precious metal or conducting oxide, the glass binder and the organic vehicle – please see [27] and references herein.

We investigated both planar [22,28,29] and 3D thermistors [9,15] made on alumina or on/in LTCC substrate from self-made composition consisted of $Mn_{1.6}Co_{0.8}Ni_{0.35}Ru_{0.25}O_4$ (44 wt %), RuO_2 (16 wt %) and glass (40 wt %) or from NT40 ink (10 kohm/sq.) from Du Pont [9,15,22,28,29] or based on Si:B, stoichiometric SiC and SiC:B magnetron sputtered thin films deposited process through metal mask onto alumina (A) or fired LTCC substrate (S) with previously screen-printed and fired electrodes.

The following formula was used for description of $R(T)$ characteristics of thermistors:

$$R(T) = R_\infty \exp(B/T) \tag{1}$$

where coefficients R_∞, and B were calculated based on experimental curves – chosen examples of these characteristics are shown in Fig. 16.

Standard thermistor inks can be applied in LTCC circuits. Metallurgy of electrodes, i.e. the interface conductor/thermistor, affects the electrical properties of thick-film and LTCC thermistors much stronger than configuration. The resistivity of 3D thermistors is lower than for planar ones in the case of Ag contacts. Moreover, silver electrodes strongly influence the $R(T)$ characteristics both for planar and 3D components, decreasing thermistor constant B 2÷2.5 times in comparison with thermistors possessing PdAg contacts. Basic electrical parameters of thermistors (resistivity, thermistor constant B) are dependent on the kind of substrate as well as device configuration and placement in/on the substrate. All microvolume thermistors show smaller B values in comparison with planar one.

Magnetron sputtered thermistors exhibit rather small influence of thermistor geometry on sheet resistance and negligible on B. All magnetron sputtered layers (Si:B, SiC, SiC:B) are compatible with DP 951 ceramic substrate. The interaction between boron and substrate affects very strongly basic electrical properties of these films.

NT 40 thermistors possess stronger dimensional effect than magnetron sputtered ones. Also their stability is strongly dependent on substrate kind as well as thickness and position of thermistor layer. NT 40 thermistors embedded in DP 951 ceramics have much better long term stability than typical NTC ceramic thermistors.

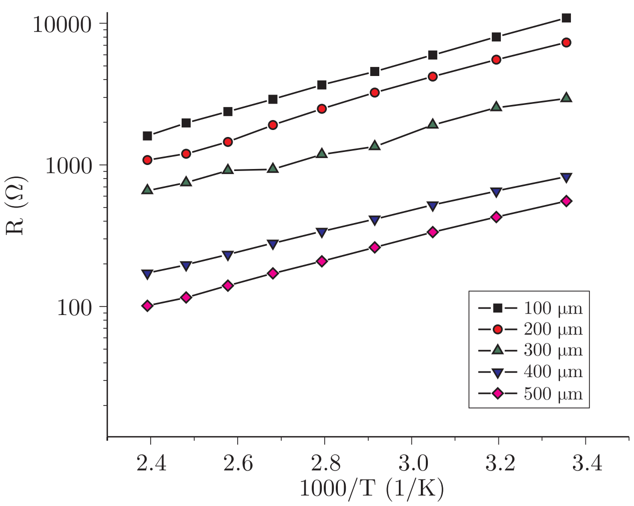

Fig. 16. *R-T* characteristics of microvolume thermistors made in 640 μm thick alumina substrate

3.2. Varistors. Traditional ZnO-based varistor ceramics are sintered at about 1250–1300°C. Thick-film varistors are also familiar – they can be discrete or prepared as a part of integrated single component comprising of inductor-capacitor-varistor (LCV) cells, or cofired multilayer varistor and capacitor. They can be applied in protection of electrical circuits against low energetic electrostatic discharges. Usually they are fired at temperatures in the range 1060–1100°C. This is about 200°C higher than typical firing profile used in thick-film or LTCC technologies. It is interesting to investigate the possibility of significant reduction of varistor sintering temperature to the range 850–900°C. At that time it would be possible to include varistors in the group of integral passives, i.e. passives either embedded in or incorporated on the surface of an interconnecting substrates, made for example in LTCC technology.

A mixture of ZnO with small amount of additives (Bi_2O_3, Sb_2O_3, Co_2O_3, Cr_2O_3, MnO_2, NiO) was applied for fabrication of three-dimensional and planar varistors made on alumina or on/in LTCC substrate. The DC current-voltage (I-V) characteristics were measured for all as-fired and voltage pulse subjected thick-film and LTCC varistors. The varistor voltages were determined at 0.01, 0.05, 0.1 and 1 mA DC current. Next the I-V characteristic was fixed by the equation

$$I = CV^{\alpha} \tag{2}$$

where C is a constant and the exponent α defines the degree of nonlinearity. The 3D varistor nonlinearity exponent is dependent on ceramic tape – for Ferro A6-M tapes it was between 10 and 15 and breakdown voltage of about 30–40 V [9]. But the same composition deposited into Du Pont 951 tape leads to α from the range between 5 and 11 for planar structures [30] and 6 to 8 for 3D ones [15] (identical 3D varistors in alumina substrate give nonlinearity degree only from the range $3.5 \div 5$). Probably these results are caused by much lower firing temperature. But as was recently reported in [32] printing sequence for varistor and conductor layer, kind of electrode paste and additional densification process affect varistor nonlinearity – for example since this component properties occur at the grain boundaries the smaller porosity and suppression of additives improve significantly the I-V characteristic (α can be equal to about 20) [31]. Similar results – α anywhere from ten to twenty – were obtained for LTCC varistor tape made by tape casting method. Next the several varistor green tapes with thick film PdAg electrodes on each tape were laminated together and cofired in the profile typical for Du Pont green tape system [32].

4. Conclusions

This paper presents current situation in the area of discrete, integrated and integral micropassives. Integration of passive components into MCM substrates improves electrical properties and reliability and reduces cost, size and weight of electronic systems in a such manner that this solution should fulfill the demands of current and next electronic packaging generations.

Probably thick film and LTCC technologies are the most popular in fabrication of modern microresistors, even for 0201 and 01005 package size. Of course size reduction causes that geometrical errors connected with technological margins and physicochemical processes at the interfaces, for example between resistive film and terminations or substrates, affect more and more significantly electrical and stability properties of LTCC and thick-film microresistors. Therefore some examples of relation between geometrical, electrical and stability properties were presented both for microplanar and microvolume resistors. Moreover various methods of trimming process were characterized and discussed from the stability and trim sensitivity point of view.

Acknowledgements. This work was supported by Wroclaw University of Technology, grant no 343 189 W12. The Author would like to express his gratitude to Prof. Leszek Golonka and Mr Edward Miś from Wrocław University of Technology, Dr. Jarosław Kita (at present from University of Bayreuth), Prof. Andrzej Kolek from Rzeszów University of Technology, Prof. Klaus-Juergen Wolter and Dr. Lars Rebenklau from Dresden University of Technology and Dr. Witold Mielcarek from Electrotechnical Institute – Wrocław Branch for long-term and fruitful collaboration in the area presented in this paper.

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