Modification of textured silicon wafer surface morphology for fabrication of heterojunction solar cell with open circuit voltage over 700 mV

L. Fesquet[1], S. Olibet[1], J. Damon-Lacoste[1], S. De Wolf[1], A. Hessler-Wyser[2], C. Monachon[2], C. Ballif[1]

[1]Ecole Polytechnique Fédérale de Lausanne (EPFL), Institute of Microengineering, Photovoltaics and thin film electronics laboratory, Breguet 2, 2000 Neuchâtel, Switzerland
[2]Ecole Polytechnique Fédérale de Lausanne (EPFL), Interdisciplinary Centre for Electron Microscopy CIME, 1015 Lausanne, Switzerland

luc.fesquet@epfl.ch +41 (0) 32 718 33 21

ABSTRACT

Crystalline silicon wafer (c-Si) can be extremely well passivated by plasma enhanced chemical vapor deposited (PECVD) amorphous silicon (a-Si:H) films. As a result, on flat substrates, solar cells with very high open circuit voltage are readily obtained. On textured substrates however the passivation is more cumbersome, likely due to the presence of localized recombinative paths situated at the pyramid valleys. Here, we show that this issue may be resolved by selecting a silicon substrate morphology featuring large pyramids. Chemical post-texturization treatments can further reduce the surface recombination velocity. This sequence has allowed us to fabricate solar cells with open circuit voltage over 700 mV, demonstrating also on device level the effect of pyramid density and surface micro-roughness on the surface passivation quality.

INTRODUCTION

By depositing intrinsic amorphous silicon (a-Si:H) on crystalline silicon wafer (c-Si) surfaces, very good electronic passivation can be obtained. Depositing subsequently doped layers on these intrinsic films can then lead to the fabrication of a heterojunction solar cell (HJ) with very high open circuit voltage (V_{oc}). As a result, efficiencies up to 22% have been demonstrated [**1**]. The thin a-Si:H layers creating the emitter and back surface collector of the cells are typically deposited by plasma enhanced physical vapor deposition system (PECVD) at low temperature (<250°C). This particularity makes this process suitable for fabrication of solar cells on thin wafers. Using this deposition technique, good passivation [**2**] and solar cell results (19.1% conversion efficiency) were previously obtained, using n-type doped flat wafers [**3**]. To further improve the efficiency, the use of textured wafers is necessary. For (100) oriented wafers, this texturization consists in etching anisotropically the wafer to reveal pyramidal structure defined by the {111} planes [**4**]. These randomly distributed pyramids greatly improve light trapping, and therefore increase the short circuit current density of the solar cells. However, a decrease of the open circuit voltage is sometimes observed. The major difference between film deposition on flat and textured wafers comes from the multiple deposition conditions that pyramidal texturization engenders. Especially epitaxial growth and/or mixed phase, that can be detrimental for solar cell fabrication, is likely occurring on the nanoscopically uneven surfaces [**5**]. Therefore, substrate morphology appears to be a key issue. Fortunately, this morphology can be accurately controlled: by varying anisotropic etching process, different textures can be achieved with different pyramid sizes and thus densities. Moreover, by applying a post isotropic etching, a modification of the surface morphology, rounding the top and the valleys of pyramids, is achieved [**6,7**]. All these parameters appear to be crucial when amorphous silicon passivating layer is deposited on top of the textured wafer. In this article, by varying the morphology, and analyzing results by transmission electron microscopy (TEM) and relating them to passivation quality, optimization of surface morphology is performed.

EXPERIMENTAL

Wafer preparation

The wafers used are (100) n-type doped, obtained by CZ growth method with a resistivity of 1.25 Ω.cm.

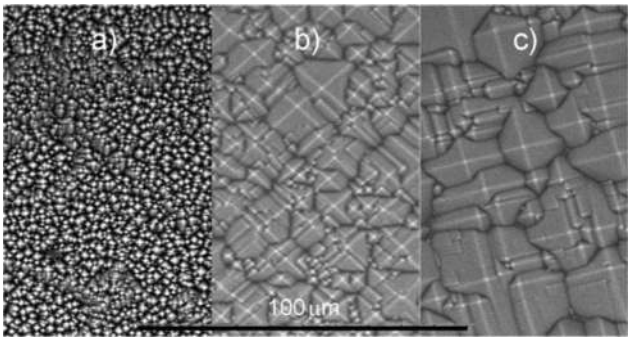

Fig. 1. SEM pictures of textured wafers with different average pyramid sizes. a) 1-3 µm height pyramids, b) 5-15 µm height pyramids, c) 10-25 µm height pyramids

Texturization of wafers is performed using solution of KOH diluted in IPA.
The IPA concentration is varied to obtain three different sizes of pyramids, as shown by the scanning electron microscopy (SEM) micrographs in Figure 1, from small (1-3 μm), medium (5-15 μm), to large (15-25 μm) ones. In all the case, pyramid distribution includes some sub-micronic pyramids, which formation cannot be easily controlled.
Roughly, the pyramid density is inversely proportional to the square of the pyramid size, and as a consequence, the pyramid density quickly decreases from small to large pyramids.
After pyramid formation, isotropic etching can be used to reduce the sharpness of the pyramids, as well as to reduce the sub-micron pyramids density, as seen in Figure 2. It results in a pyramid rounding, with no roughness.

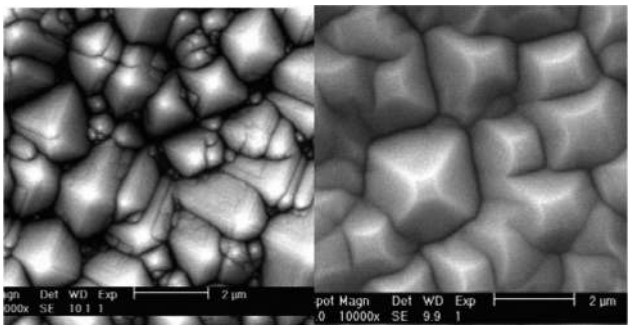

Fig. 2. SEM pictures of 1-3 μm textured wafer a) before and b) after isotropic chemical etching of pyramids. Sub-micron pyramids are etched away during the treatment, and surface is smoothed.

In all cases, the final wafer preparation step consists in a RCA-clean, to remove organic and metallic contaminants from the c-Si surface, and oxide removal in HF is performed before amorphous layer deposition.

Layer depositions

On top of textured wafers, thin film silicon layers are deposited using very high frequency PECVD (70 MHz). In order to understand the effect of morphology on surface passivation, first experiments deal with symmetrical passivating stacks made only of thin film silicon layers. 50 nm i a-Si:H layers are in a first time deposited on the 3 differently textured wafers, and with or without post texturization chemical polishing. After result analysis, i-p and i-n stack are considered as passivation layers on the different wafers as well. 5 nm of intrinsic a-Si:H is used on both sides to reduce a-Si:H/c-Si interface defect density. Then the doped layers are grown on top of them. Doped layers are grown using phosphine for n-type doping, and thrimethylboron for p-type doping. These layers are microcrystalline, in order to ensure a good electrical contact with the outer part of the prospect cell, and have a thickness each of about 15 nm.
Final solar cell outer part consists in ITO deposited by reactive sputtering, and sputtered aluminum at the back, in order to further increase the back stack conductivity and reflectivity. The structure is: ITO /μc-Si:H (p)/ a-Si:H (i)/c-Si (n)/ a-Si:H (i)/ /μc-Si:H (n)/ITO/Al. After deposition is complete, the device is annealed at 180°C for 180 min, under nitrogen flow.
To characterize passivation quality, different techniques are used.

Characterization

The passivation stacks are characterized with two methods. Lifetime measurements are made using a contactless Sinton WCT-100 tool [8], either in quasi steady state (QSS), or transient mode. Thanks to this instrument, lifetime as a function of excess carrier density can be measured. Effective lifetime curves obtained are then compared to wafer bulk intrinsic lifetime, using Kerr parameterization [9]. Microstructure characterization is performed using a TEM Philips CM300 aligned at 200 kV [10]. Cross-sectional TEM lamellae of microstructured cells is obtained by mechanical polishing followed by 3 keV Ar ion milling using a Gatan PIPS ion miller. Observations in high resolution (HRTEM) allow identifying clearly local epitaxial growth in the amorphous Si layer.
Pyramid size and density is determined by using a SEM FEI XL30f.

RESULTS

50 nm i layer passivation

Passivation of the different silicon wafers by the 50 nm i a-Si:H layer is quantified first by lifetime measurement. It shows (Fig. 3) that lifetime as a function of excess carrier density is low in the case of a-Si:H layer deposited on small pyramids, whereas on medium and large pyramids, the lifetime is higher, and actually almost equal in both cases.
For the 50 nm passivation it is observed that it makes no differences to apply a post texturization chemical polishing on the pyramidal texture.

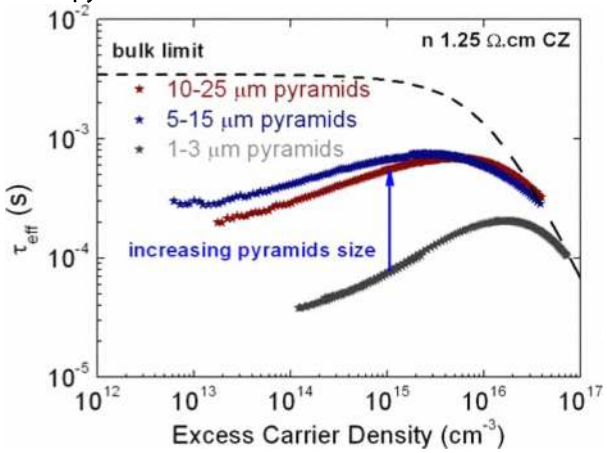

Fig. 3. Effective carrier lifetime as a function of excess carrier density for 3 different texturization structures, using symmetrical 50 nm i a-Si:H layers: small pyramids (1-3 μm), medium (5-15 μm) and large pyramids (10-25 μm).

50 nm i a-Si:H passivation layer is a much more tolerant stack than i-p and i-n stack. Therefore, wafers with small pyramids are not considered to be suitable for solar cell fabrication and will not be used for the following tests.

i-p stack passivation

Passivation of wafers with medium and large pyramids by i-p stack gives useful information about passivation by the thin 5 nm intrinsic and 15 nm doped layer. High lifetime is reached with this stack, as shown in Figure 4, and implied V_{oc} of more than 700 mV is attained in all the case. It can be pointed out that the by applying a final isotropic etching of the wafer surface, an even higher lifetime is obtained.

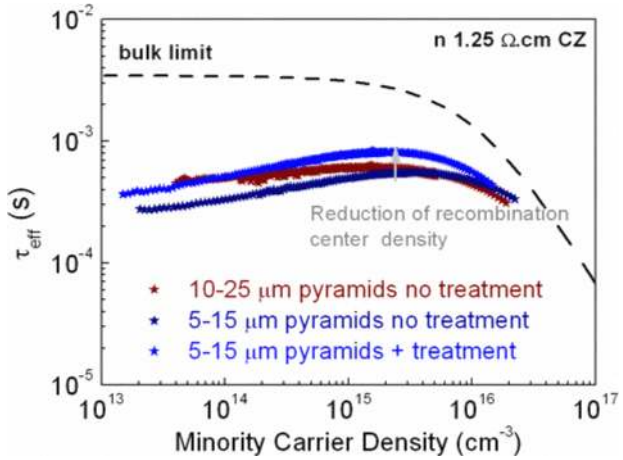

Fig. 4. Effective carrier lifetime as a function of excess carrier density measured in 3 cases: large pyramids without post chemical polishing, and medium sized pyramids with and without chemical polishing.

This latest point is highlighted by TEM micrographs (Fig. 5), showing local epitaxial growth at the bottom of the pyramids. The contact between crystalline silicon and microcrystalline doped layer is harmful for the passivation, and will increase the a-Si:H/c-Si interface recombination. The micrograph taken from rounded pyramid valley shows that the a-Si:H is by far more conformal, leading to reduced density of defects.

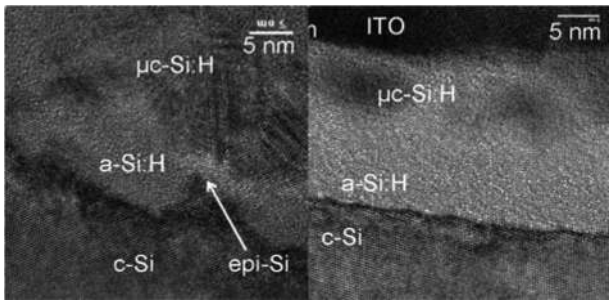

Fig. 5. TEM picture of textured c-Si wafer (10-25 μm pyramids) before (left), and after (right) post texturization chemical polishing.

Furthermore, the SEM pictures (Fig. 6) before and after isotropic etching show a clear reduction of the density of small pyramids, which will result in a reduced proportion of pyramid valleys.

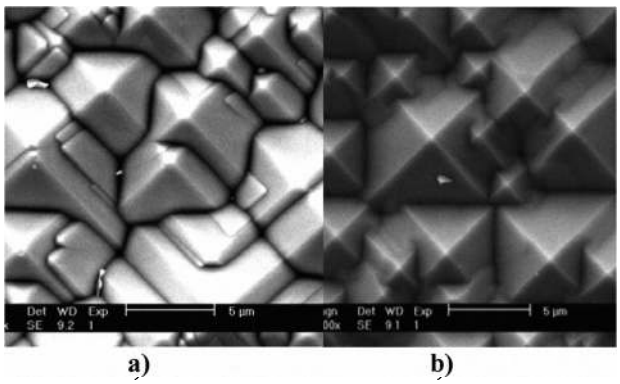

Fig. 6. SEM picture of textured c-Si wafer (5-15 μm pyramids) a) before, and b) after post texturization chemical polishing.

By moderating influence of problematic zones, wet chemical polishing promotes a proper a-Si:H deposition and a better surface passivation.

i-n stack passivation

Passivation results obtained using this stack is rather similar to the passivation using i-p stack. Indeed, the i layer thickness is the same in both cases, and the n layer is also microcrystalline. Therefore, the same influence of isotropic etching is seen in this case.

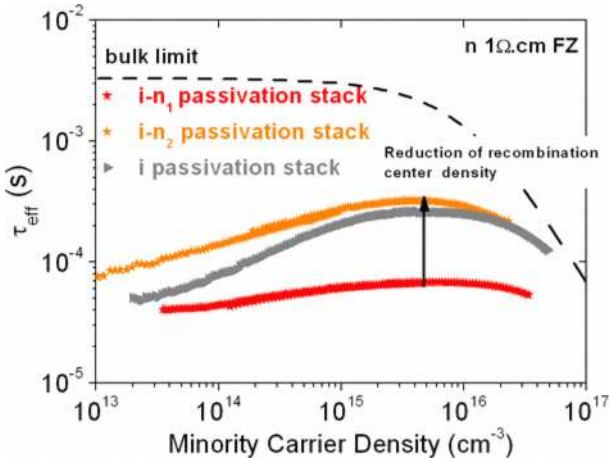

Fig. 7. Effective carrier lifetime as a function of excess carrier density measured in 3 cases: wafer passivated by i layer, and 2 other i-n stacks: optimized i-n_2 stack engenders less damages to the i-layer passivation than the former i-n_1 stack.

Nevertheless, in a first time, the n-type microcrystalline layer had to be developed, to reduce damages to the underlayer (Fig. 7), because of the too aggressive plasma deposition.
Thanks to that improvement, passivation results as good as with only 50 nm i a-Si:H layers are obtained.

Solar cell final stacks

Final solar cell is made using previous stacks of intrinsic a-Si:H and doped μc-Si:H. By using wafer with large, rounded pyramids, an outstanding increase of open circuit voltage from 660 mV to 704 mV is observed (Fig. 8). Moreover a slight increase in short circuit current can be seen. With these different improvements, solar cell up to 17% conversion efficiency can be achieved.

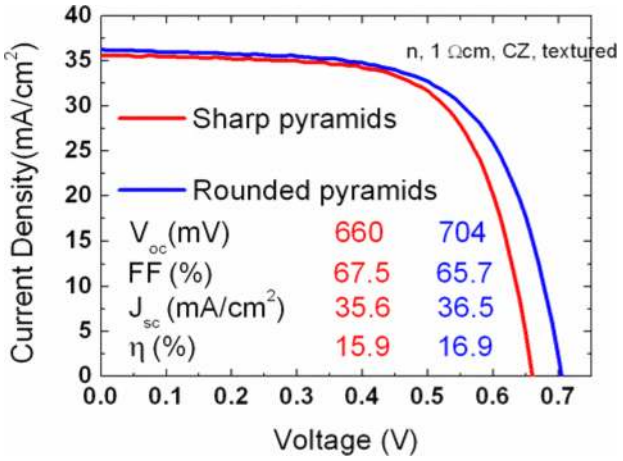

Fig. 8. IV curves of final solar cells on large pyramids, with or without post texturization chemical polishing.

DISCUSSION

It has been seen that one of the main parameters to be aware of is the density of pyramid valleys, which plays a role in the degradation of the quality of c-Si surface passivation. The increased recombination rate in these valleys can be explained by local epitaxial growth and/or mixed phase, making a non abrupt interface between the c-Si and the a-Si:H phases **[11, 12]**, potentially more probable than on the {111} facets **[13]**, and capture of contaminants from the texturization process, on this rougher zone. From figure 4, applying a simple recombination model **[5]**, shows that the lifetime increase correspond to a 4 times reduction of the recombination center density. This value is slightly lower than the reduction of the theoretical pyramid valleys density. Moreover, no change is visible while increasing the size of pyramids from medium to large. Therefore, it can be supposed that the recombination is governed by the pyramid valleys density up to the critical size for which the recombination on the overall pyramid valleys is equivalent to the recombination on the pyramids facets.

The effect of the post-texturization chemical polishing, as seen by different groups, is efficient in the case of i-p or i-n stack. This chemical polishing has no effect while passivating the wafer using a simple 50 nm i layer. TEM observations showed that local epitaxy occurs on the pyramid valleys if they are sharp and not rounded. It can then be supposed that the local epitaxy is not a problem in the case of the i layer passivation, since it will not propagate through the entire i layer, but will be probably covered by a-Si:H. In the case of the i-p or i-n stacks. However, this local epitaxy is very detrimental, as it will directly contact the defective doped layers. Moreover, the thinner i a-Si:H layer in this case increases the probability to have mixed phases reaching the doped regions.
By changing the n layer, as shown in figure 7, a large increase in lifetime is observed. However, this new n layer also reduces the field effect, as shown by the decrease of effective lifetime at low injection. Consequently, a reduction of fill factor has to be expected, as seen in figure 8. By improving further the n layer doping, a clear increase in fill factor can be expected, and even better conversion efficiency reached.

CONCLUSION

By playing on KOH/IPA concentration, textured c-Si wafers with randomly distributed pyramids were produced having different sizes. Post-texturization chemical polishing was also performed to detect possible changes.
By passivating these different samples with 50 nm i layer, and i-p and i-n stacks, best texture morphology has been selected. It has been pointed out that wafer with small pyramids, due to their increasing density of pyramids valley, are not suitable for heterojunction solar cells. Main problem arising from these pyramid valleys are local epitaxial growth and possible capture of wet processes contaminants.
Therefore, passivation of medium and large pyramid wafers, with additional chemical polishing, leads to optimal surface passivation. Finally, after having selected this optimized substrate morphology, 704 mV open circuit voltage cell was built and efficiency up to 16.9% was obtained.

AKNOWLEDGMENTS

The authors gratefully acknowledge Adolf Münzer from Solarworld München for preparing wafers with a high quality of surface texturization. This work is supported by the Swiss National Science Foundation (Grant SNSF 200020-116630) and by the Axpo Holding AG, Switzerland in the frame of the Axpo Naturstrom Fond.

REFERENCES

[1] Y. Tsunomura et al. "Twenty-two percent efficiency HIT solar cell" *Sol. Energy Mater. Sol. Cells*, **93**, 2009, 670–673

[2] S. Olibet, et al. "Model for a-Si:H/c-Si interface recombination based on the amphoteric nature of silicon dangling bonds" *PhysicalReview B*, **76,** 2007, 035326

[3] L. Fesquet et al. *Proceedings 22nd European Photovoltaic Solar Energy Conference*, 2007, 1678-1673

[4] D. Muñoz et al. "Optimization of KOH etching process to obtain textured substrates suitable for heterojunction solar cells fabricated by HWCVD" *Thin Solid films,* **517**, 2009, 3578–3580

[5] S. Olibet et al. "Textured silicon heterojunction solar cells with over 700 mV open circuit voltage studied by TEM" *Proceedings 23nd European Photovoltaic Solar Energy Conference*, 2008, 1678-1673

[6] M. Edwards et al. "Effect of texturing and surface preparation on lifetime and cell performance in heterojunction silicon solar cells" *Sol. Energy Mater. Sol. Cells*, **92**, 2008, 1373–1377

[7] H. Angermann et al. "Optimization of electronic interface properties of a-Si:H/c-Si hetero-junction solar cells by wet-chemical surface pre-treatment" *Thin Solid films,* **516**, 2008, 6775–6781

[8] R.A. Sinton et al. "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data" *Applied Physics Letters*, **69**, 1996, 2510

[9] M.J. Kerr et al. "General parameterization of Auger recombination in crystalline silicon" *Journal of Applied Physics*, **91,** 2002, 2473.

[10] A. Hessler-Wyser et al. "TEM characterization of textured silicon heterojunction solar cells" *14th European Microscopy Congress,* ***2,*** 2008, 335-338

[11] S. De Wolf et al. "Abruptness of a-Si:H/c-Si interface revealed by carrier lifetime measurements" *Applied Physics Letters*, **90**, 2007, 042111

[12] J. Damon-Lacoste et al. "Toward a better physical understanding of a-Si:H/c-Si heterojunction solar cells" *Journal of Applied Physics*, **105,** 2009, 063712

[13] U.K. Das et al. "Surface passivation and heterojunction cells on Si (100) and (111) wafers using dc and rf plasma deposited Si:H thin films" *Applied Physics Letters*, **92**, 2008, 063504