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Modified Discontinuous PWM for Size Reduction of the Circulating Current Filter in Parallel Interleaved Converters

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Abstract—Parallel Voltage Source Converters (VSCs) require an inductive filter to suppress the circulating current. The size of this filter can be minimized by reducing either the maximum value of the flux linkage or the core losses. This paper presents a modified Discontinuous Pulsewidth Modulation (DPWM) scheme to reduce the maximum value of the flux linkage and the core losses in the circulating current filter. In the proposed PWM scheme, the dwell time of an active vector is divided within a half-carrier cycle to ensure simultaneous occurrence of the same zero vectors in both VSCs. A function to decide the ratio of the dwell time of the divided active vector is also presented. The effect of the proposed PWM scheme on the maximum value of the flux linkage and the core losses is analyzed and compared with that of the space vector modulation and 60° clamped DPWM schemes. The analytical expressions for the maximum value of the flux linkage are derived for each of these PWM schemes. In addition, the effect of the proposed PWM scheme on the line current ripple and the switching losses is also analyzed and compared. To verify the analysis, experimental results are presented, which prove the effectiveness of the proposed PWM scheme.

I. INTRODUCTION

Three-phase voltage source converter (VSC) is widely used as a dc/ac converter in power electronics applications and often connected in parallel to meet the ever increasing demand for higher power rating converter [1], [2]. In grid-connected application, the total harmonic distortion (THD) in the line current should be low [3]. Due to limited switching frequency in the high power converters, large filters are required [4]. This leads to the increase in the size, weight, and cost of the overall converter system. For VSC fed variable speed machines, the harmonic distortion in the line current must be low for satisfactory operation of the drive [5]. The harmonic distortion depends primarily on the switching sequence, modulation index, and the switching frequency [5]. Several efforts have been made to improve the performance of the VSC in terms of the harmonic distortion and switching losses by using optimal switching sequences for modulation of the VSC legs [6]–[8].

The harmonic distortion in the line current can be reduced by increasing the switching frequency. However, the switching frequency of the semiconductor devices for high power applications is often limited. The effective switching frequency can be increased by using interleaved carriers in parallel-connected VSCs, and the line current quality can be improved [9]. The selection of the proper interleaving angle leads to the reduction

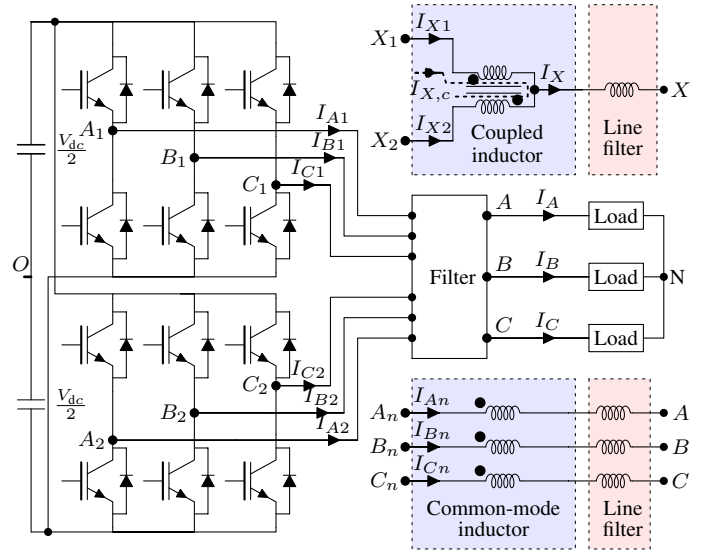


Fig. 1. Two parallel interleaved VSCs with a common dc-link. The filter arrangement for circulating current suppression using the CI and the CM inductor is depicted, where $X = \{A, B, C\}$ and $n = \{1, 2\}$.

in the line current ripple [9]–[15]. This implies that with interleaved parallel VSCs, the size of the line filter can be reduced, or the switching frequency can be reduced for a given set of filter components without violating the THD constraints.

The circulating current is generated in the parallel VSCs due to hardware and control asymmetries [2]. When carrier interleaving is used, the pole voltages (measured with respect to the fictitious mid-point of the dc-link O , as shown in Fig. 1) of the interleaved parallel legs are phase shifted. Therefore, there exists a potential difference that further increases the circulating current [16]. This is a high frequency circulating current with harmonic components concentrated around the odd multiples of the switching frequency [12]. This unwanted current increases stress on the semiconductor switches and causes additional losses. Therefore, it should be suppressed.

The circulating current is strongly influenced by the Pulsewidth Modulation (PWM) scheme. The conventional Space Vector Modulation (SVM) uses two adjacent active vectors and both of the zero vectors to synthesize a reference space vector. The zero vectors are applied at the beginning and at the end of a half-carrier cycle. Various other variants of the

SVM scheme can be obtained by merely dividing the dwell time of the zero vectors unequally [17]. The Discontinuous PWM (DPWM) schemes use only one zero vector in each half-carrier cycle. The commutation of each phase leg is ceased for the one third period of the fundamental cycle [18], [19]. The PWM schemes, which modify the DPWM schemes by dividing one of the active vectors into two equal halves, are proposed in [20], [21]. These PWM schemes affect the line current ripple. A hybrid PWM scheme, which is a combination of the conventional SVM and different DPWM schemes, is proposed in [14] to minimize the line current ripple for the parallel VSCs. However, separate dc-links are used and thus the circulating current filter is not present.

To avoid the circulating current, galvanic isolated transformer can be used for each VSC [22]. However, the use of the bulky transformer adds to the cost and increases the size. Therefore, it should be avoided. Instead of this, a coupled inductor (CI) [23]–[26] for each phase or a common-mode (CM) [27] inductor for each VSC can be used as a circulating current filter (Fig. 1). Assuming strong magnetic coupling in the circulating current filter, the flux linkage in the core due to the line current can be neglected. Therefore, the flux linkage has only the high frequency components determined by the switching frequency. These high frequency components result in high core losses, and the circulating current filter requires larger surface area to dissipate the heat. Ewanchuk *et al.* [28] proposed a modified DPWM scheme that can make the CM voltage zero. This permits the use of a three limb inductor only. However, the number of commutations are increased. Therefore, it may not be feasible for medium/high power applications. Another PWM scheme is proposed in [29] to change the zero vector pattern by introducing an additional switching. This avoids the coexistence of the different zero vectors at a sector transition, and thus the jumping of the circulating current can be avoided.

The CI is used to provide magnetic coupling between the parallel interleaved legs [23]–[26]. A modified CI, which is proposed in [30], combines the functionality of both the line filter inductor and the circulating current filter. To reduce the flux linkage in the CI, a PWM scheme is proposed in [25]. This PWM scheme adds an optimal common-mode offset to the reference signals based on the modulation index. This can lead to the reduction of the maximum value of the flux linkage, but the discussion on the core losses is not given. However, the core losses are an important parameter to consider in the design of the circulating current filter. As discussed before, the high frequency components of the flux linkage increase the core losses. This may lead to a thermally limited design of the circulating current filter, where the maximum flux density in the core is limited by the heat dissipation capability and not by the magnetic saturation. In this case, the core losses can be reduced by reducing the peak flux density for a given switching frequency and core dimensions.

An active method to reduce the peak flux linkage as well as the core losses for the circulating current filter is proposed in this paper. The method divides the dwell time of an active vector within a half-carrier cycle to ensure simultaneous occurrence of the same zero vectors in both VSCs. A function

to calculate the division of the dwell time are also proposed. This reduces both the maximum value of the flux linkage and the core losses in the circulating current filter.

The paper is organized as follows. Section II presents the basic theory of the circulating current. In addition, the relationship between the flux linkage in the circulating current filter and the pole voltages is discussed for the interleaved VSCs. The effect of the different switching sequences on the flux linkage in the core is analyzed in Section III. Section IV presents the proposed DPWM scheme. The effect of the proposed PWM on the flux linkage in the CI and the CM inductor, the harmonic distortion in the line current, and the switching losses are also discussed and compared with that of the SVM and the 60° clamped DPWM. The experimental results are presented in Section V.

II. PARALLEL INTERLEAVED VSCS

A. Circulating Current

The parallel-connected VSCs are operated with interleaved carrier signals. The circulating current ($I_{X,c}$) flows through the VSC legs in addition to the line current component $I_{X1,l}$, as shown in Fig. 1. Therefore, the phase currents can be given by

$$\begin{aligned} I_{X1} &= I_{X1,l} + I_{X,c} \\ I_{X2} &= I_{X2,l} - I_{X,c} \end{aligned} \quad (1)$$

where $I_{X1,l}$ and $I_{X2,l}$ are the components of the phase currents contributing to the resultant line current I_X . $I_{X,c}$ is the circulating current, where $X = \{A, B, C\}$. Assuming ideal VSCs and neglecting the effect of the hardware/control asymmetries, the current component of each VSC, contributing to the grid current, are considered to be equal ($I_{X1,l} = I_{X2,l}$). Therefore,

$$I_{X,c} = \frac{I_{X1} - I_{X2}}{2} \quad (2)$$

The differential equation describing phase X circulating current can be given as

$$\frac{dI_{X,c}}{dt} = \frac{V_{X1O} - V_{X2O}}{L_c} \quad (3)$$

where L_c is the inductance offered to the circulating current. V_{X1O} and V_{X2O} are the pole voltages measured with respect to the fictitious dc-link mid point O .

B. Flux Linkage in Circulating Current Filter

To offer the desired inductance L_c to the circulating current, a CI and a CM inductor based solution is proposed in literature. To design the inductor, the maximum value of the flux linkage should be known. Therefore, the flux linkage analysis for both the CI and the CM inductors is presented in this subsection.

1) *Coupled Inductor*: In case of the CI, the flux density in the core is given by

$$B_X(t) = \frac{1}{2NA_c} \int (V_{X1O} - V_{X2O}) dt \quad (4)$$

and the flux linkage is

$$\lambda_X(t) = \lambda_{X1}(t) + \lambda_{X2}(t) = \int (V_{X1O} - V_{X2O}) dt \quad (5)$$

where N is the number of turns, and A_c is the core cross-sectional area. The differential voltage across the filter ($V_{X1O} - V_{X2O}$) is responsible for the flux linkage, and in order to reduce the flux linkage, the time integral of this differential voltage should be reduced [26], [31].

Let L be the self inductance, and M be the mutual inductance of the CI. The pole voltage difference is given by

$$V_{X1O} - V_{X2O} = (L + M) \frac{dI_{X1}}{dt} - (L + M) \frac{dI_{X2}}{dt} \quad (6)$$

Using (2) and (6), the dynamic equation of the circulating current is given as

$$\frac{dI_{X,c}}{dt} = \frac{V_{X1O} - V_{X2O}}{2(L + M)} \quad (7)$$

If strong coupling is ensured ($L \approx M$), the inductance offered to the circulating current is $L_c = 4L$. From (5) and (7), the flux linkage in the CI is proportional to the circulating current $I_{X,c}$, which is half of the difference of the phase currents.

2) *Common-mode Inductor*: In the CM inductor, the magnetic coupling between the phases is used to suppress the circulating current. Since all three phases are wound on the same core, the flux linkage is proportional to the average of the phase currents, and the flux linkage is three times the CM flux linkage, where the CM flux linkage is given as

$$\lambda_{CM}(t) = \frac{\lambda_A(t) + \lambda_B(t) + \lambda_C(t)}{3} = \int (V_{CM1} - V_{CM2}) dt \quad (8)$$

where V_{CMn} is the CM voltage of the n th VSC, and it is given by

$$V_{CMn} = \frac{V_{AnO} + V_{BnO} + V_{CnO}}{3} \quad (9)$$

where $n = \{1, 2\}$.

The size of the CM inductor can be made smaller by reducing the peak flux linkage, which can be achieved by minimizing the time integral of the difference of the CM voltages. The difference depends on the interleaving angle, modulation index, and the PWM scheme used, and it is described in the following section.

III. SWITCHING SEQUENCES AND THEIR EFFECT ON THE FLUX LINKAGE

The two-level VSC has eight voltage vectors defined by the combination of the switch states. These states generate six active vectors ($\vec{V}_1 - \vec{V}_6$) and two zero vectors (\vec{V}_0, \vec{V}_7), as shown in Fig. 2. The three-phase reference signals can be represented by a complex reference vector \vec{V}_{ref} . Based on the magnitude ($|\vec{V}_{ref}|$) and angle (ψ) of the sampled

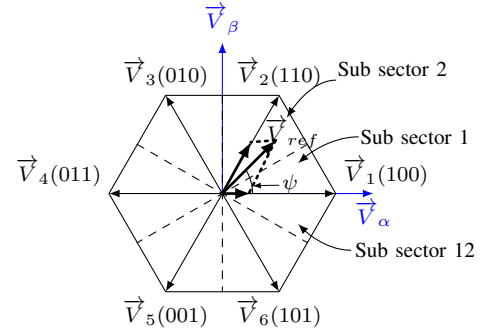


Fig. 2. Basic space vector sectors and states in complex $\alpha\beta$ plane.

\vec{V}_{ref} , two adjacent active voltage vectors and zero vectors are commonly applied to synthesize the reference vector [19], [32], [33]. The respective dwell time of the active vectors is chosen to maintain the volt-sec balance. Let T_1 , T_2 , and T_z be the dwell time of \vec{V}_1 , \vec{V}_2 , and \vec{V}_0/\vec{V}_7 , respectively, and they are given by

$$T_1 = \frac{2}{\sqrt{3}} \frac{|\vec{V}_{ref}|}{V_{dc}} T_s \sin(60^\circ - \psi) \quad (10a)$$

$$T_2 = \frac{2}{\sqrt{3}} \frac{|\vec{V}_{ref}|}{V_{dc}} T_s \sin(\psi) \quad (10b)$$

$$T_z = T_s - T_1 - T_2 \quad (10c)$$

where T_s is the carrier interval. The dwell time of the zero voltage vectors \vec{V}_0 and \vec{V}_7 are given by $K_z T_z$ and $(1 - K_z) T_z$, respectively, where $0 \leq K_z \leq 1$. Different modulation possibilities exist with variation in the parameter K_z [32]. For example, $K_z = 0.5$ results in the conventional SVM. By changing the value of K_z between zero and one with a frequency three times higher than the frequency of the reference signal, several DPWM schemes can be realized [32]. If the value of K_z is changed from zero to one in the middle of the sector 1, the reference signals for 60° clamped DPWM (DPWM1) is generated. Although the number of commutations is two-third of that of the SVM, the switching losses can be reduced up to 50% for unity power factor applications. However, the reduction in the switching losses strongly depend on the displacement power factor angle. For equal switching losses, the carrier frequency of the DPWM1 can be increased by a factor of K_f times than that of the SVM. The value of K_f varies in a wide range with the displacement power factor angle [19]. Therefore, the carrier frequency is taken to be the same in all of the cases for comparing the effect of the PWM schemes on the design of the circulating current filter. In addition, the switching losses are also compared for a fair evaluation. The effect of the switching sequences of the SVM and the DPWM1 on the CM flux linkage is analyzed. The interleaving angle is considered to be 180° .

A. Conventional Space Vector Modulation

In SVM, the opposite polarity zero vectors are applied at the same time and result in a maximum value of the CM voltage difference, as depicted in Fig. 3. The simultaneous occurrence of \vec{V}_7 in VSC1 and \vec{V}_0 in VSC2 results in more flux linkage since the polarity of the CM voltage is opposite in

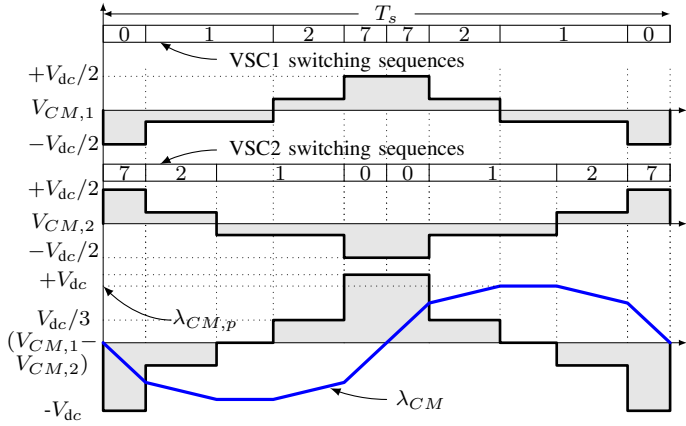


Fig. 3. SVM: Common mode voltages of individual VSCs and their voltage difference when the carriers are interleaved by an angle of 180° .

this case. The same argument applies when both \vec{V}_0 in VSC1 and \vec{V}_7 in VSC2 coexist. Both of these undesirable voltage vectors appear when SVM is used with the interleaving angle of 180° . For low modulation indices, the dwell time of the zero vectors is dominant. This results in high flux linkage at lower modulation indices.

B. 60° Clamped Discontinuous PWM (DPWM1)

The DPWM1 uses two different switching sequences in each sector. For $0^\circ \leq \psi < 30^\circ$ (sub-sector 1), the voltage vectors \vec{V}_1 , \vec{V}_2 , and \vec{V}_7 (127) are applied sequentially and vice-versa, as shown in Fig. 4(a). Accordingly, \vec{V}_0 , \vec{V}_1 , and \vec{V}_2 (012) are applied for $30^\circ \leq \psi < 60^\circ$ (sub-sector 2), as shown in Fig. 4(b). The CM voltages, their difference, and the CM flux linkage in both of the sub-sectors are depicted in Fig. 4. The use of \vec{V}_1 and \vec{V}_7 results in opposite polarity CM voltages. Similarly, the polarities of the CM voltages are different when the voltage vectors \vec{V}_0 and \vec{V}_2 are used. The CM voltage difference increases if the polarities of the CM voltages are different in both VSCs. These undesirable vectors appear in both sub-sectors, when DPWM1 is used, as shown in Fig. 4.

IV. MODIFIED DPWM FOR CIRCULATING CURRENT REDUCTION

It is evident that the PWM sequences determine the flux linkage pattern. Therefore, the design of the circulating current filter is strongly influenced by the PWM scheme used. Some vectors in a PWM scheme which may lead to high flux linkage are summarized below.

- The simultaneous application of \vec{V}_7 in VSC1 and \vec{V}_0 in VSC2 and vice-versa.
- The simultaneous occurrence of a zero vector in VSC1 and an active vector in VSC2 and vice-versa. For example, the simultaneous occurrence of \vec{V}_7 and \vec{V}_1 (vectors with opposite polarity CM voltage).

Since these vectors cause high flux linkage in the circulating current filter, they should be avoided. However, if the same

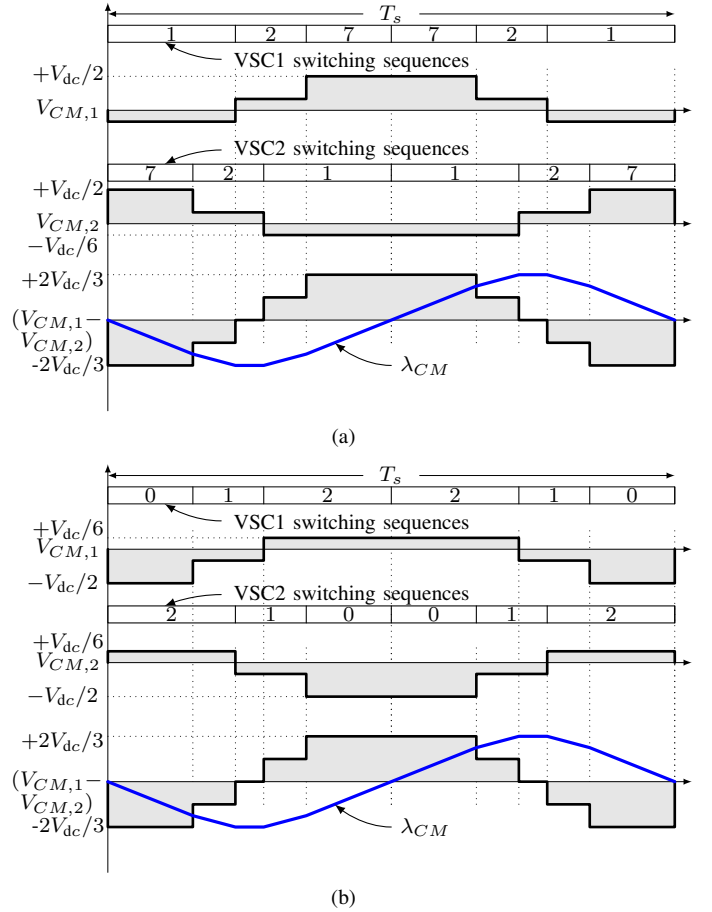


Fig. 4. DPWM1: Switching sequences and common-mode voltages of both the VSCs. (a) sub-sector: 1, $0^\circ \leq \psi < 30^\circ$, (b) sub-sector: 2, $30^\circ \leq \psi < 60^\circ$.

zero vectors in both VSCs (e.g. \vec{V}_7 in both VSCs) are applied simultaneously, a significant reduction in the flux linkage can be achieved. Based on these observations, a PWM scheme is presented where the division of an active vector within a half-carrier cycle is used to align the same zero vector in both VSCs.

The PWM schemes where the dwell time of the active vector are divided into two equal intervals in each half-carrier cycle is proposed in [5], [20], [21], [34], [35]. However, the dwell time of an active vector is not divided equally in this paper. It is divided in a manner to align the same zero vectors of both VSCs. The ratio, in which the dwell time is divided, varies with the reference space vector angle, and it is updated in each half-carrier cycle.

The sequences used in the proposed PWM scheme are depicted in Fig. 5. The numbers shown in Fig. 5 represent the sequence in which the voltage vectors are applied, e.g. 1012 represents that \vec{V}_1 , \vec{V}_0 , \vec{V}_1 , and \vec{V}_2 are applied in sequence. The discussion is restricted to the first sector of the space vector diagram. The same discussion applies to other sectors due to the symmetry. From Fig. 5, it is evident that each phase discontinues switching for one third period of the fundamental cycle. For example, phase A is clamped twice to the positive dc-link for $30^\circ \leq \psi < 60^\circ$ and $300^\circ \leq \psi < 330^\circ$

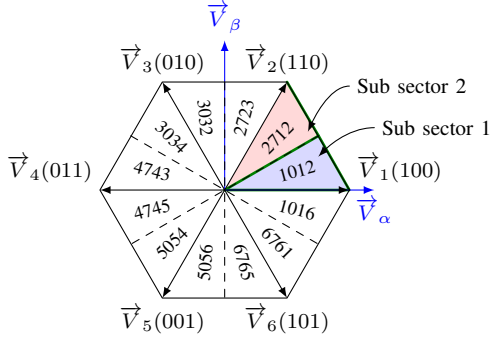


Fig. 5. Switching sequences of the proposed scheme in each sub-sector.

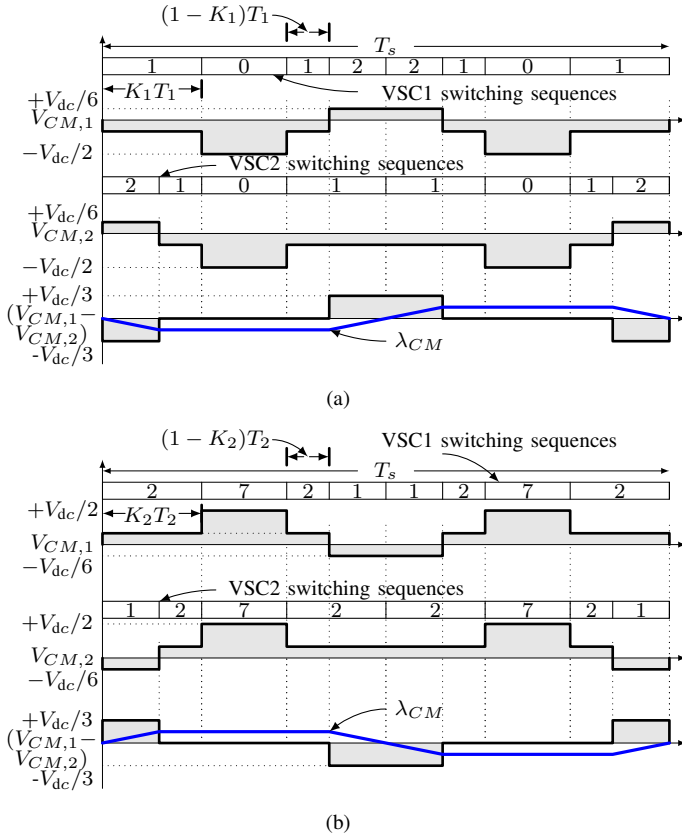


Fig. 6. Proposed modulation scheme: Switching sequences and CM voltages of both the VSCs with an interleaving angle of 180° . (a) sub-sector 1: $0^\circ \leq \psi < 30^\circ$, (b) sub-sector 2: $30^\circ \leq \psi < 60^\circ$.

and clamped twice to the negative dc-link for $120^\circ \leq \psi < 150^\circ$ and $210^\circ \leq \psi < 240^\circ$ in a fundamental period. The active voltage vector with the maximum dwell time is divided into two intervals and applied twice in a half-carrier cycle. Therefore, one of the phase legs is switched twice. In the proposed PWM scheme, one phase does not switch, whereas one of the phases is switched twice in a half-carrier cycle. Hence, it is referred to as the modified DPWM in this paper.

If the reference vector is in sub-sector 1, as shown in Fig. 5, the dwell time of \vec{V}_1 is more than the dwell time of \vec{V}_2 . Thus, the dwell time of \vec{V}_1 is divided, and \vec{V}_0 is applied in between to ensure simultaneous occurrence of the same zero vector in both VSCs. The reverse is true for sub-sector

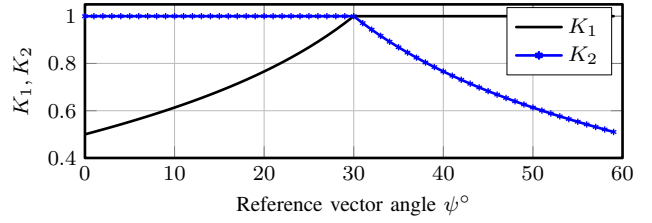


Fig. 7. Variation in parameter K_1, K_2 with reference vector angle ψ . Due to the symmetry the plot is restricted to the first sector.

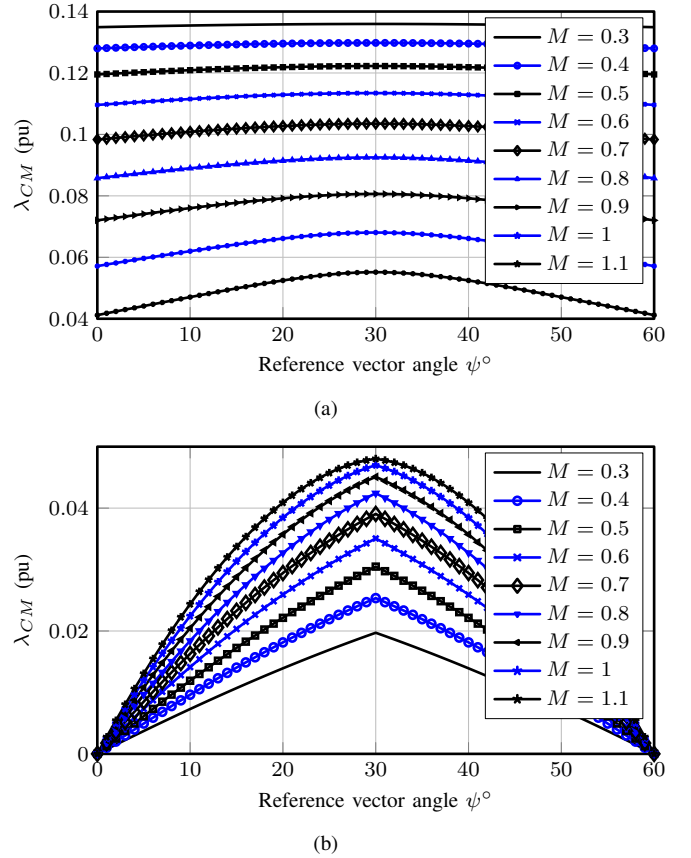


Fig. 8. RMS value of the CM flux linkage λ_{CM} vs. reference space vector angle ψ in a switching cycle for (a) SVM and (b) the proposed PWM scheme. The flux linkage is normalized with respect to the $V_{dc}T_s$.

2. Therefore, in sub-sector 1 ($0^\circ \leq \psi < 30^\circ$), T_1 is divided into two intervals and can be given as

$$T_1 = K_1 T_1 + (1 - K_1) T_1 \quad (11)$$

where $0 \leq K_1 \leq 1$. Similarly, in sub-sector 2 ($30^\circ \leq \psi < 60^\circ$), T_2 is divided into two intervals;

$$T_2 = K_2 T_2 + (1 - K_2) T_2 \quad (12)$$

where $0 \leq K_2 \leq 1$. The flexibility offered by the division of the active vectors is used to ensure simultaneous occurrence of the same zero vectors in both VSCs.

The switching sequences and the CM voltages in sub-sector 1 and sub-sector 2 for the proposed scheme are shown in Fig. 6(a) and Fig. 6(b), respectively for one switching cycle. In sub-sector 1, the value of K_1 is updated in each half-carrier cycle,

while K_2 is equal to one. In sub-sector 2, K_2 is varied, and K_1 is equal to one. The careful observation of the switching sequence depicted in Fig. 6 reveals that the same zero vector of both VSCs can coexist if

$$K_1 = \frac{T_1 + T_2}{2T_1}, K_2 = 1 \quad (13)$$

in sub-sector 1 and

$$K_1 = 1, K_2 = \frac{T_1 + T_2}{2T_2} \quad (14)$$

in sub-sector 2. The variation of K_1 and K_2 over a sector is depicted in Fig. 7. The rms value of the CM flux linkage λ_{CM} in a switching cycle for the proposed scheme is shown in Fig. 8 and compared with that of the SVM. A substantial reduction in λ_{CM} is achieved, especially at low values of the modulation indices.

As discussed in Section II, the PWM schemes strongly influence the flux linkage and the core losses in the circulating current filter. Therefore, the effects of the proposed PWM scheme on the filter design along with the line ripple current and the switching losses are discussed and compared with that of the SVM and the DPWM1 in the following subsections.

A. Effect of the Switching Sequences on the Circulating Current Filter Design

The circulating current is suppressed by introducing an impedance in the circulating current path. Typically, this impedance can be introduced by inserting CM inductor in series with the line filter inductors [27] or using CI for each phase group [23]–[25], [30]. Assuming a strong coupling between the windings, the effect of the leakage flux is neglected in the analysis. Therefore, the flux linkage in the core has only high frequency components, which result in more core losses. In addition to this, the maximum value of the flux linkage in the core also influences the core size. Therefore, both maximum value of the flux linkage and the core losses should be considered while designing both the CI and the CM inductor, and they are discussed below.

1) *Coupled Inductor*: The CI provides magnetic coupling between the interleaved legs, and the schematic is shown in Fig. 1. The flux linkage in the coupled inductor of phase A is evaluated using (5). Since the dwell time is updated in each half carrier cycle, the peak flux linkage is also different for each half-carrier cycle. The formulas describing the maximum value of the peak flux linkage as a function of the modulation index is given in Table I, and plotted in Fig. 9. The maximum value of the peak flux linkage is the same in all cases. However, the flux linkage pattern is different, which affects the core losses, and thus the design of the CI.

Due to the quarter wave symmetry of the reference signal, the flux density pattern is the same in each quarter period of the fundamental cycle. Thus, it is sufficient to evaluate the core losses for that period (e.g. $0^\circ \leq \psi \leq 90^\circ$). The flux density behavior in a half-carrier cycle for the proposed PWM scheme is described by the piecewise linear equations given in Table IV and depicted in Fig. 10(c). The piecewise linear equations, describing the flux density behavior in the CI, for the SVM and

TABLE I
MAXIMUM VALUE OF THE PEAK FLUX LINKAGE IN A CI FOR DIFFERENT MODULATION SCHEMES

Scheme	Max. value of peak flux linkage ($\lambda_{A,pmax}$)
SVM	$\lambda_{A,pmax} = \frac{1}{4}V_{dc}T_s$
DPWM1	$\lambda_{A,pmax} = \begin{cases} V_{dc}T_s(\frac{1}{\sqrt{3}}\frac{ \vec{V}_{ref} }{V_{dc}}), & 0 \leq M < 1/\sqrt{3} \\ \frac{1}{4}V_{dc}T_s, & 1/\sqrt{3} \leq M < 2/\sqrt{3} \end{cases}$
Proposed	$\lambda_{A,pmax} = V_{dc}T_s(\frac{1}{2\sqrt{3}}\frac{ \vec{V}_{ref} }{V_{dc}})$

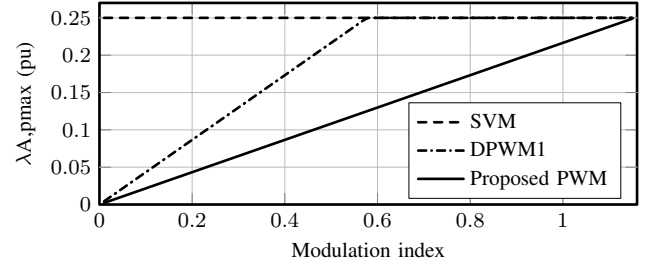


Fig. 9. Comparison of the maximum value of the peak flux linkage as a function of the modulation index. The flux linkage is normalized with respect to the $V_{dc}T_s$.

the DPWM1 are given in Table II and Table III, respectively. The term T_3 in those tables is the dwell time of the voltage vector \vec{V}_3 .

In case of SVM, the core is excited over an entire fundamental cycle. However, for the DPWM1, the core is excited for two third of the fundamental cycle, as shown in Fig. 10. On the other hand, in the proposed PWM scheme, the core is excited only for one third of the fundamental cycle, as depicted in Fig. 10(c).

The core losses with the proposed PWM scheme are expected to reduce due to the reduction in both the peak flux linkage and the duration of the core excitation, and it is evaluated using the Improved Generalized Steinmetz Equation (IGSE) [36], [37] given as

$$P_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB(t)}{dt} \right|^\alpha (\Delta B)^{\beta-\alpha} dt \quad (15)$$

where α , β , and k_i are the constants determined by the material characteristics, and P_v is the core loss per unit volume. Using (15), the core losses averaged over a quarter of the fundamental cycle is given as

$$P_{v,avg} = \frac{2}{(f_{sw}/f_0)} \sum_{k=1}^{(f_{sw}/2f_0)} \frac{2}{T_s} \int_0^{T_s/2} k_i \left| \frac{dB_k(t)}{dt} \right|^\alpha (\Delta B_k)^{\beta-\alpha} dt \quad (16)$$

where f_0 is the fundamental frequency, and f_{sw} is the switching frequency. In order to make the core loss analysis more general (independent of the core dimensions), the loss behavior

TABLE II
FLUX DENSITY DESCRIPTION IN A HALF-CARRIER CYCLE USING PIECEWISE LINEAR EQUATIONS FOR SVM

PWM scheme	Sub-sector	Peak flux density B_p	Flux density $B(t)$
SVM	$0^\circ \leq \psi \leq 90^\circ$	$B_p = \frac{V_{dc}(T_z)}{8NA_c}$	$B(t) = \frac{4B_p}{T_z}t$ for $0 \leq t \leq \frac{T_z}{4}$ $B(t) = B_p$ for $\frac{T_z}{2} \leq t \leq (\frac{T_z}{2} - \frac{T_z}{4})$ $B(t) = B_p - \frac{4B_p}{T_z}[t - (\frac{T_z}{2} - \frac{T_z}{4})]$ for $(\frac{T_z}{2} - \frac{T_z}{4}) \leq t \leq \frac{T_z}{2}$

TABLE III
DPWM1: FLUX DENSITY DESCRIPTION IN A HALF SWITCHING CYCLE USING PIECEWISE LINEAR EQUATIONS

Sub-sector	\vec{V}_{ref} position	Peak flux density B_p	Flux density $B(t)$
$0^\circ \leq \psi \leq 30^\circ$	-	$B_p = 0$	$B(t) = 0$
$30^\circ \leq \psi \leq 60^\circ$	$M \cos(30 - \psi) \geq \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}T_z}{4NA_c}$	$B(t) = \frac{-2B_p}{T_z}t$, for $0 \leq t \leq \frac{T_z}{2}$ $B(t) = -B_p$, for $\frac{T_z}{2} \leq t \leq \frac{T_s - T_z}{2}$ $B(t) = -B_p + \frac{2B_p}{T_z}[t - (\frac{T_s - T_z}{2})]$, for $\frac{T_s - T_z}{2} \leq t \leq \frac{T_s}{2}$
	$M \cos(30 - \psi) < \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}(T_1 + T_2)}{4NA_c}$	$B(t) = \frac{-2B_p}{T_1 + T_2}t$, for $0 \leq t \leq \frac{T_1 + T_2}{2}$ $B(t) = -B_p$, for $\frac{T_1 + T_2}{2} \leq t \leq \frac{T_s - T_1 + T_2}{2}$ $B(t) = -B_p + \frac{2B_p}{T_1 + T_2}[t - (\frac{T_s - T_1 - T_2}{2})]$, for $\frac{T_s - T_1 - T_2}{2} \leq t \leq \frac{T_s}{2}$
$60^\circ \leq \psi \leq 90^\circ$	$M \sin(60 - \psi_s) \geq \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}(T_2 + T_3)}{4NA_c}$	$B(t) = \frac{-2B_p}{T_2 + T_3}t$, for $0 \leq t \leq \frac{T_2 + T_3}{2}$ $B(t) = -B_p$, for $\frac{T_2 + T_3}{2} \leq t \leq \frac{T_s - T_2 - T_3}{2}$ $B(t) = -B_p + \frac{2B_p}{T_2 + T_3}[t - (\frac{T_s - T_2 - T_3}{2})]$, for $\frac{T_s - T_2 - T_3}{2} \leq t \leq \frac{T_s}{2}$
	$M \sin(60 - \psi_s) < \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}T_2}{4NA_c}$	$B(t) = \frac{-2B_p}{T_2}t$, for $0 \leq t \leq \frac{T_2}{2}$ $B(t) = -B_p$, for $\frac{T_2}{2} \leq t \leq \frac{T_s - T_2}{2}$ $B(t) = -B_p + \frac{2B_p}{T_2}[t - (\frac{T_s - T_2}{2})]$, for $\frac{T_s - T_2}{2} \leq t \leq \frac{T_s}{2}$

TABLE IV
FLUX DENSITY DESCRIPTION IN CI FOR THE PROPOSED PWM SCHEME USING PIECEWISE LINEAR EQUATIONS

Sub-sector	Peak flux density B_p	Flux density $B(t)$
$0^\circ \leq \psi \leq 60^\circ$	$B_p = 0$	$B(t) = 0$
$60^\circ \leq \psi \leq 90^\circ$	$B_p = \frac{V_{dc}(T_3)}{4NA_c}$	$B(t) = \frac{2B_p}{T_3}t$ for $0 \leq t \leq \frac{T_3}{2}$ $B(t) = B_p$ for $\frac{T_3}{2} \leq t \leq \frac{T_s - T_3}{2}$ $B(t) = B_p - \frac{2B_p}{T_3}[t - (\frac{T_s - T_3}{2})]$ for $\frac{T_s - T_3}{2} \leq t \leq \frac{T_s}{2}$

is described in terms of B_{max} and T_s , as

$$P_{v,avg} = \frac{2}{(\frac{f_{sw}}{f_0})} \sum_{k=1}^{(\frac{f_{sw}}{2f_0})} \frac{2}{T_s} \int_0^{\frac{T_s}{2}} k_i (4B_{max} f_{sw})^\alpha (\Delta B_k)^{\beta - \alpha} dt \quad (17)$$

To make the core losses comparison independent of the design parameters, the analysis is presented in terms of the Core Loss Function (CLF), where CLF is given as the ratio of the average volumetric core loss for a PWM scheme to the average volumetric core loss for the SVM at a given modulation index M .

$$CLF = \frac{P_{v,avg}(M)}{P_{v,avg}(SVM)(M)} \quad (18)$$

The CLFs for all considered PWM schemes are depicted in Fig. 11. Amorphous metal core is considered, where $\alpha = 1.51$, $\beta = 1.74$, and $k_i = 0.622$. Lower core losses over the entire modulation range are observed for the proposed method compared to the other considered schemes. The use of the SVM results in highest core losses in the CI for low modulation indices ($M < 0.6$), whereas the core losses are the highest in case of DPWM1 at high modulation indices.

The volume optimized design of the inductor often results in non-saturated thermally limited design, and the core losses primarily determine the size of the CI [38]. Due to the substantial reduction in the core losses with the proposed scheme, small size of the CI with minimal thermal management can be achieved with the proposed PWM scheme.

2) *Common-mode Inductor*: Asiminoaei *et al.* [27] proposed the use of a CM inductor to reduce the circulating current. This solution permits un-equal load sharing between the parallel interleaved VSCs and scalability, and may be a preferred solution when the modularity is the main design objective. The volume of the CM inductor can be minimized by reducing either the maximum value of the peak CM flux linkage or the core losses. The maximum value of the peak CM flux linkage as a function of the modulation index is given in Table V and plotted in Fig. 12 for the proposed PWM scheme along with that of the SVM and the DPWM1.

For SVM, the maximum value of the peak flux linkage increases as the modulation index decreases. Therefore, for applications demanding operation over the full modulation range, the CM inductor has to be designed for the maximum flux linkage, which occurs at low modulation indices. On the

TABLE V
MAXIMUM VALUE OF THE PEAK CM FLUX LINKAGE

PWM scheme	Max of the peak CM flux linkage ($\lambda_{CM,max}$)
SVM	$\lambda_{CM,max} = V_{dc}T_s(\frac{1}{4} - \frac{1}{3\sqrt{3}}\frac{ \vec{V}_{ref} }{V_{dc}})$
DPWM1	$\lambda_{CM,max} = V_{dc}T_s(\frac{1}{3}\frac{ \vec{V}_{ref} }{V_{dc}})$ for $(0 \leq M \leq \frac{2}{3})$ $\lambda_{CM,max} = V_{dc}T_s(\frac{1}{3} - \frac{1}{3}\frac{ \vec{V}_{ref} }{V_{dc}} \cos(60 - \arcsin \frac{\sqrt{3}V_{dc}}{4 \vec{V}_{ref} }))$ for $(\frac{2}{3} \leq M \leq \frac{2}{\sqrt{3}})$
Proposed PWM scheme	$\lambda_{CM,max} = V_{dc}T_s(\frac{1}{6\sqrt{3}}\frac{ \vec{V}_{ref} }{V_{dc}})$

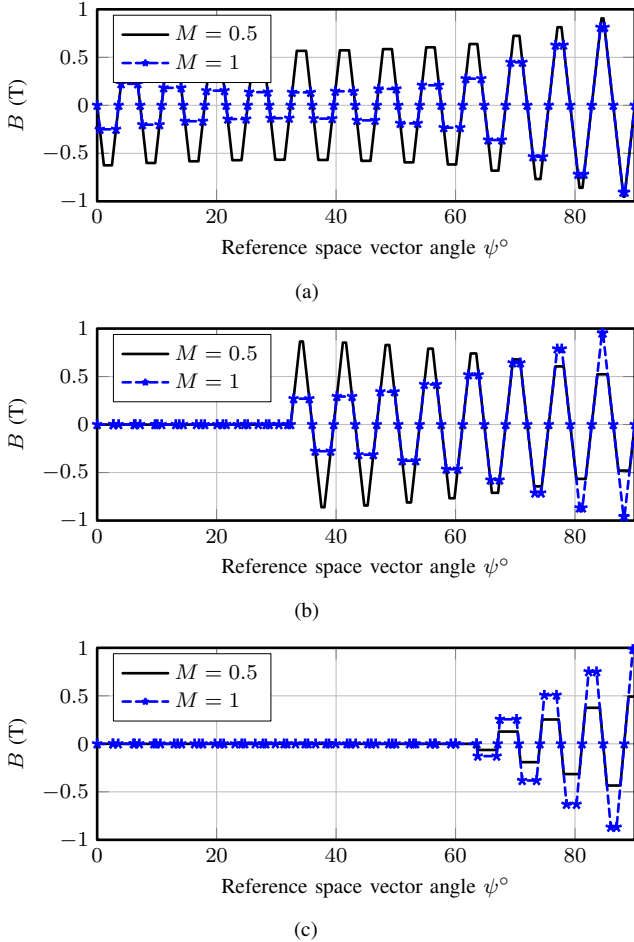


Fig. 10. The flux density pattern in the CI core for modulation indices of 0.5 and 1. (a) SVM, (b) DPWM1, (c) Proposed scheme.

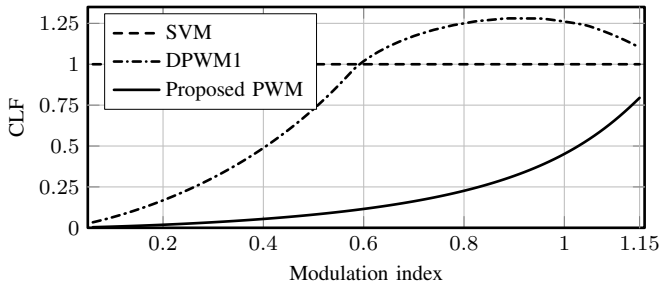


Fig. 11. CLF as a function of the modulation index.

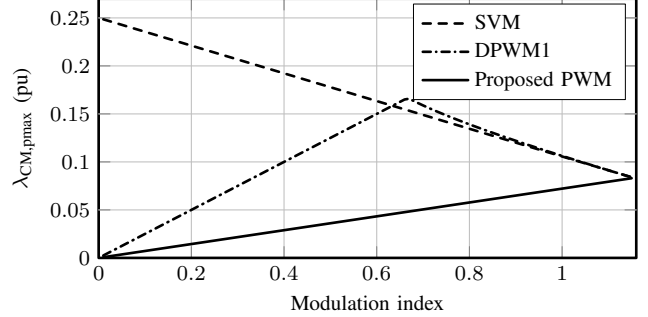


Fig. 12. Comparison of the maximum values of the peak CM flux linkage as a function of the modulation index. The flux linkage is normalized with respect to $V_{dc}T_s$.

other hand, the CM is subjected to maximum flux linkage for a modulation index $M = 2/3$ if DPWM1 is employed. The proposed PWM scheme has the lowest peak flux linkage, compared to other PWM schemes, for the entire modulation range. The reduction in the maximum flux linkage in case of the CM filter is achieved by using the proposed DPWM1 scheme. As a result, small CM inductor can be realized.

B. Ripple Current Analysis

The line current ripple of the proposed PWM scheme is analyzed and compared with that of the SVM and the DPWM1. The reference vector is synthesized using the discrete vectors. Thus, at any given instant, an error between the applied voltage vector and the reference vector exists. The error voltage vectors for a given sampling instance are shown in Fig. 13(a). The time integral of the error vectors gives the harmonic flux vector, which is proportional to the ripple current [5], [20], [21].

In the synchronously rotating reference frame, the instantaneous error voltage vectors depicted in Fig. 13(a) are given as

$$\vec{V}_{err,1} = [\cos \psi - V_{ref}] - j \sin \psi \quad (19a)$$

$$\vec{V}_{err,2} = [\cos(60^\circ - \psi) - V_{ref}] + j \sin(60^\circ - \psi) \quad (19b)$$

$$\vec{V}_{err,z} = -V_{ref} \quad (19c)$$

In the proposed scheme, the time duration, for which an active vector is applied, is divided unequally, and the division of the active vector follows the rule given by (13) and (14). For the

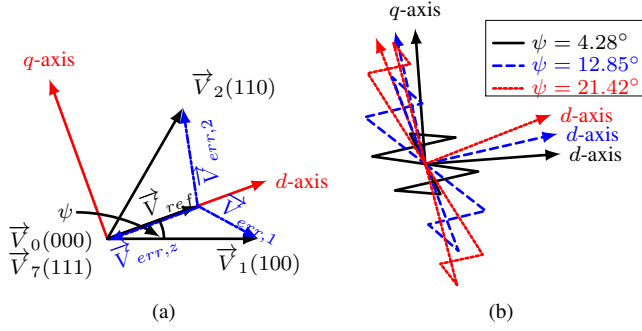


Fig. 13. (a) The active and zero vectors to synthesize given reference vector and corresponding error voltage vectors, (b) Harmonic flux vector trajectory for different values of reference vector angle ψ for 1012 sequence in sub-sector 1.

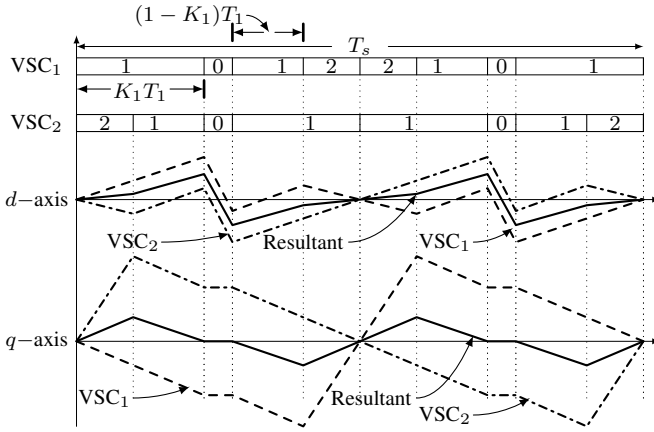


Fig. 14. d -axis and q -axis ripple components of a harmonic flux vector over a switching cycle for two parallel VSCs and their resultant with an interleaving angle of 180° and reference vector angle $\psi = 12.8^\circ$.

proposed PWM scheme, the harmonic flux vector is given as

$$\vec{V}_{err,1}K_1T_1 = [\cos\psi - V_{ref}]K_1T_1 - jK_1T_1 \sin\psi \quad (20a)$$

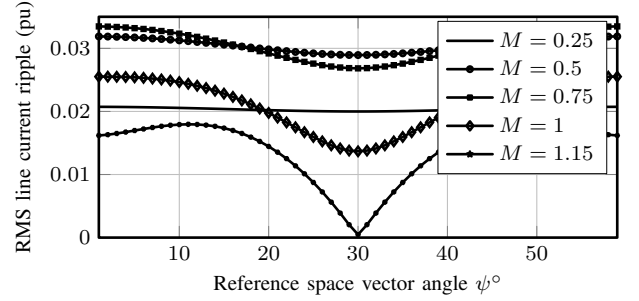
$$\vec{V}_{err,1}(1-K_1)T_1 = [\cos\psi - V_{ref}](1-K_1)T_1 - j(1-K_1)T_1 \sin\psi \quad (20b)$$

$$\vec{V}_{err,2}T_2 = [\cos(60^\circ - \psi) - V_{ref}]T_2 + jT_2 \sin(60^\circ - \psi) \quad (20c)$$

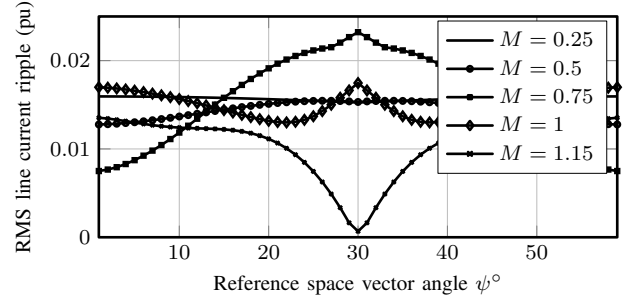
$$\vec{V}_{err,z}T_z = -V_{ref}T_z \quad (20d)$$

and it is plotted in Fig. 13(b) for different values of the reference space vector angles. The harmonic flux vector is decomposed into d -axis and q -axis components, as shown in Fig. 14. The resultant vector for an interleaving angle of 180° is also shown, and it is used to evaluate the ripple current/harmonic content in the line current.

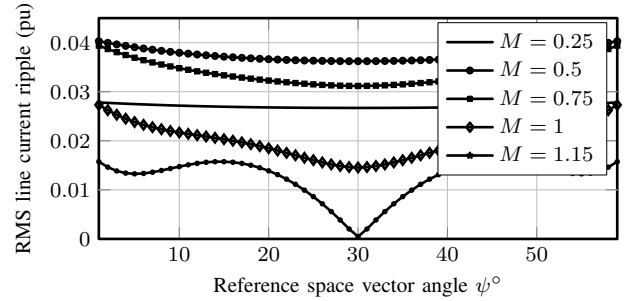
The normalized rms value of the line current ripple over a half-carrier cycle [14] for different modulation indices for the proposed PWM scheme is plotted in Fig. 15(c) as a function of the ψ . The variation in the rms value of the line current ripple for SVM and DPWM1 are also shown in Fig. 15(a) and 15(b), respectively. The variation of the total rms value of the line current ripple over the entire modulation range is also shown in Fig. 16. DPWM1 demonstrates better line current quality



(a)



(b)



(c)

Fig. 15. Space dependency of the rms value of the line current ripple (normalized) for different modulation indices. (a) SVM, (b) DPWM1, (c) Proposed scheme.

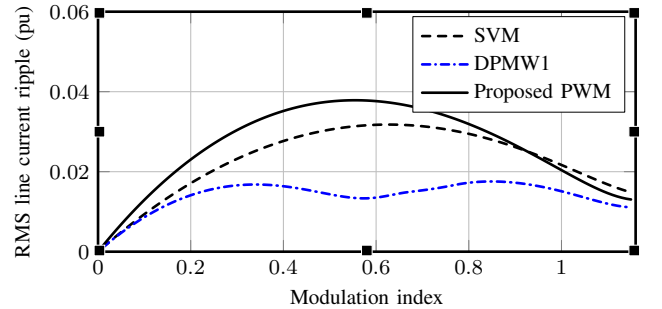


Fig. 16. Total rms value of the line current ripple (normalized) as a function of modulation index.

over an entire modulation range. The total rms value of the line current ripple for the proposed PWM scheme closely matches that of the SVM. For SVM, the harmonic content for low modulation indices is slightly less compared to the proposed PWM scheme. On the other hand, the line current quality in the case of the proposed PWM scheme is marginally better

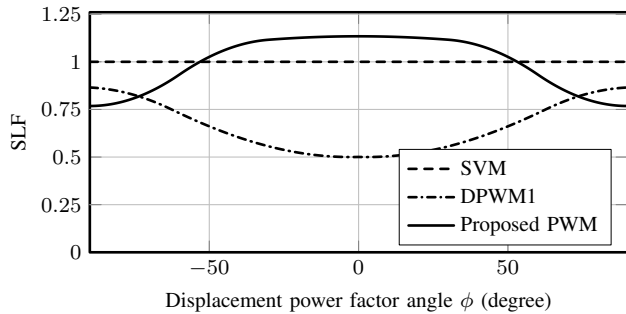


Fig. 17. Comparison of the switching losses.

than that of the SVM at higher modulation indices ($M > 0.9$).

C. Semiconductor losses

Although one of the phase legs is clamped to dc-link for one third period of the fundamental cycle in the proposed scheme, an additional commutation is introduced in another leg as explained in the previous section. Thus, the switching losses are also evaluated in this paper. The switching loss function (SLF) [18] is used to compare the switching losses of the proposed PWM with other PWM schemes. The turn-on and turn-off characteristics of the semiconductor devices are assumed to be linear with respect to time. The contribution of the ripple current towards the switching losses is also neglected. Since the SLF normalizes the switching loss of the proposed method with respect to the switching loss of SVM, the relative error is small despite the simplified loss model [18] used. The SLF for the proposed method is given as

$$\text{SLF} = \begin{cases} 1 + \frac{(2-\sqrt{3})}{2} \cos \phi, & 0 \leq |\phi| < \frac{\pi}{6} \\ \cos \phi + \frac{1}{2} \sin \phi, & \frac{\pi}{6} \leq |\phi| < \frac{\pi}{3} \\ 2 - \frac{(2\sqrt{3}-1)}{2} \sin \phi, & \frac{\pi}{3} \leq |\phi| \leq \frac{\pi}{2} \end{cases} \quad (21)$$

where ϕ is the displacement power factor angle. The SLFs for the proposed PWM scheme along with that of the SVM and DPWM1 are plotted in Fig. 17. For the unity power factor applications, the switching losses are minimum if DPWM1 is used. For a displacement power factor angle higher than 53° , the proposed method has lower switching losses compared to that of the SVM. However, for a displacement power factor angle in the vicinity of zero, the proposed method has high switching losses. For the reactive power compensation applications, the use of the proposed PWM scheme results in the lowest switching losses, as shown in Fig. 17.

V. EXPERIMENTAL RESULTS

The experiments have been performed using single-phase inductors, which act as both line filter inductor and the circulating current filter. This arrangement is used to simplify the measurement [39]. The results for $I_{A1} - I_{A2}$ are obtained, which is equal to $2 \times I_{A,c}$. As explained in Section II, the $I_{A,c}$ is proportional to the flux linkage in CI. Similarly, the sum of three-phase currents of each VSC is obtained. This current is equal to $3 \times I_{CM}$, and it is proportional to the CM flux linkage. The dc-link voltage of 600 V is used. The carrier frequency is

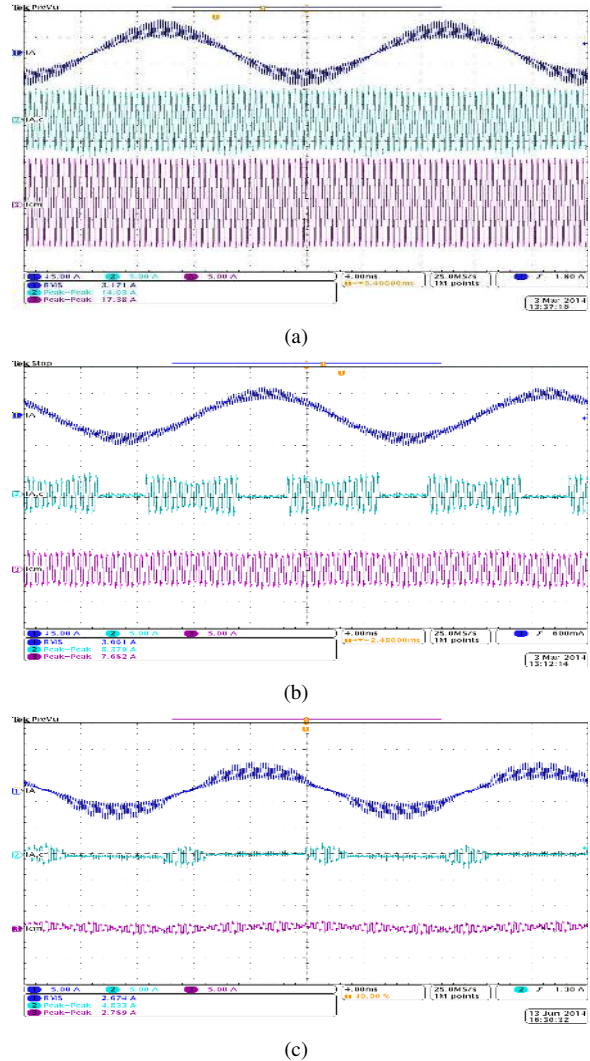


Fig. 18. The performance comparison of the proposed PWM scheme. The modulation index $M=0.3$. Ch1: Phase A line current (5 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (5 A/div), Ch3: CM circulating current ($3 \times I_{CM}$) (5 A/div). (a) SVM, (b) DPWM1, (c) Proposed scheme.

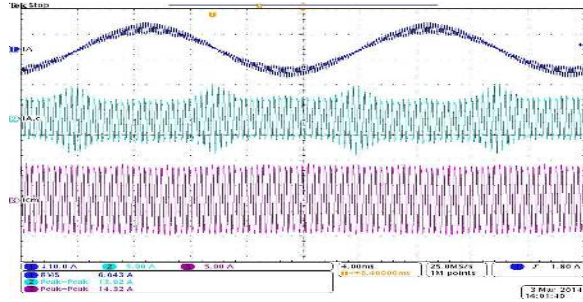
taken to be 2.5 kHz and interleaving angle of 180° is chosen. The line filter inductor of 6.8 mH is used, and a resistive load is set to 20 Ω . The inductance in the circulating current path is $L_c = 2 \times 6.8$ mH.

The line current of phase A (I_A), the circulating current of Phase A ($2 \times I_{A,c}$), and the CM current ($3 \times I_{CM}$) for modulation index of 0.3, 0.6, and 1 for SVM, DPWM1, and the proposed PWM scheme is depicted in Fig. 18, 19, and 20, respectively. The experiments have been performed for the entire linear range of the modulation index and the results are given in Table VI. The line current THD, the maximum value of the peak circulating current of phase A, and the maximum value of the peak CM circulating current of the proposed method are compared with that of the SVM and the DPWM1. The THD is calculated by performing discrete Fourier transform of the measured line current.

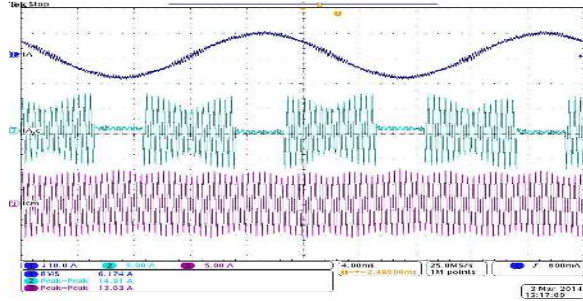
For the SVM, the maximum value of the peak circulating current of phase A remains almost constant over the entire modulation range. Since, the phase A circulating current is

TABLE VI
PERFORMANCE COMPARISON OF THE PROPOSED METHOD

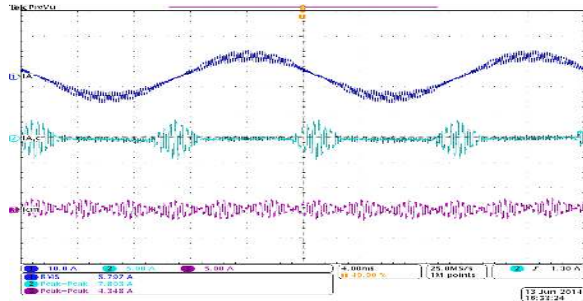
M	Max. of $I_{A,c}$ (A)			Max. of I_{CM} (A)			Line current THD (%)		
	SVM	DPWMI	Proposed	SVM	DPWMI	Proposed	SVM	DPWMI	Proposed
0.1	3.55	0.79	0.59	3.98	0.52	0.32	24.15	26.14	28.62
0.2	3.52	1.46	0.85	3.12	0.93	0.33	22.30	19.29	25.31
0.3	3.50	2.09	1.15	2.89	1.28	0.46	19.60	15.21	22.06
0.4	3.55	2.68	1.42	2.71	1.62	0.52	17.63	11.56	19.68
0.5	3.50	3.23	1.76	2.57	1.94	0.61	15.86	7.95	16.49
0.6	3.48	3.72	2.03	2.38	2.27	0.73	13.85	6.03	14.38
0.7	3.48	3.63	2.28	2.20	2.39	0.82	11.88	5.92	12.38
0.8	3.42	3.55	2.53	2.03	2.10	0.91	10.03	5.85	10.26
0.9	3.40	3.50	2.81	1.85	1.86	0.98	8.25	5.28	8.09
1.0	3.40	3.48	3.03	1.64	1.64	1.14	6.37	4.49	6.17
1.1	3.36	3.48	3.19	1.46	1.49	1.27	4.71	3.66	4.47
1.15	3.38	3.39	3.37	1.39	1.28	1.29	4.05	3.31	3.87



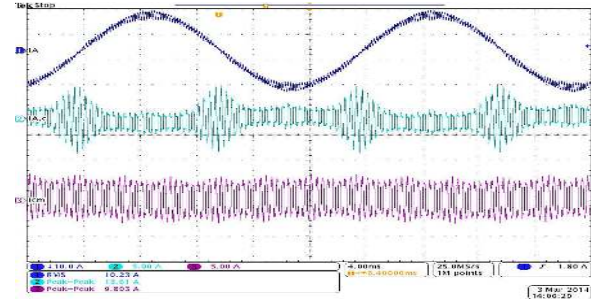
(a)



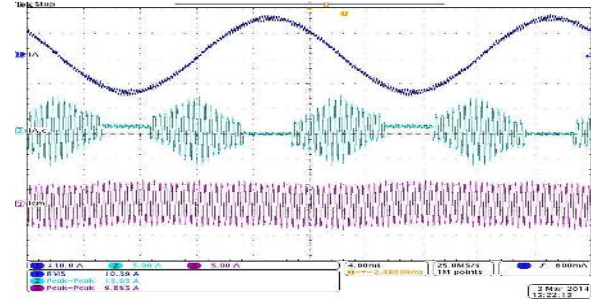
(b)



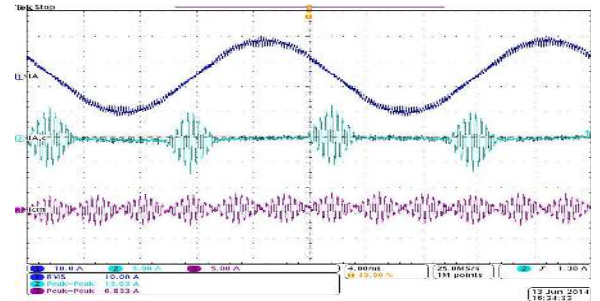
(c)



(a)



(b)



(c)

Fig. 19. The performance comparison of the proposed PWM scheme. The modulation index $M=0.6$. Ch1: Phase A line current (10 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (5 A/div), Ch3: CM circulating current ($3 \times I_{CM}$) (5 A/div). (a) SVM, (b) DPWMI, (c) Proposed scheme.

Fig. 20. The performance comparison of the proposed PWM scheme. The modulation index $M=1$. (a) SVM: Ch1: Phase A line current (10 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (5 A/div), Ch3: CM circulating current ($3 \times I_{CM}$) (5 A/div), (b) DPWMI, (c) Proposed scheme.

proportional to the flux linkage in the CI, it can be concluded that the maximum value of peak flux linkage in the CI over the full modulation range also remains constant. The use of SVM also results in more core losses in case of CI compared to the proposed PWM scheme, as the core is excited over the entire

fundamental cycle. The I_{CM} is proportional to the flux linkage in the CM inductor and the experimental results of I_{CM} are also obtained. For the SVM, the maximum value of the peak CM circulating current decreases with the increase in the modulation index, which is in agreement with the analytical

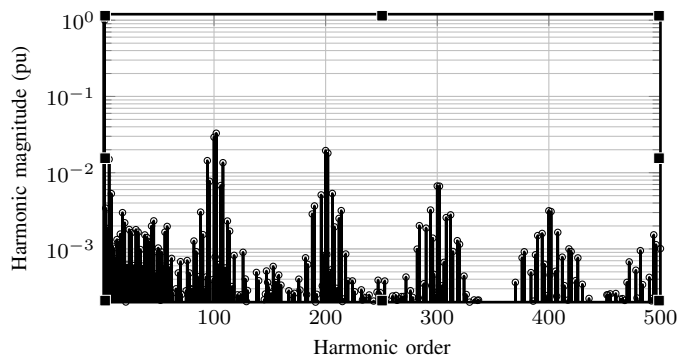


Fig. 21. Proposed scheme: Experimental line current harmonic spectrum for a modulation index of 1. The harmonic magnitude is normalized to the magnitude of the fundamental component.

result presented in Section IV and illustrated in Fig. 12. In the proposed scheme, the maximum value of the I_{CM} occurs at full modulation index, and it decreases with decrease in the modulation index. The maximum value of the peak CM current is 1.29 A at a modulation index of one in the proposed scheme, compared to 3.98 A at modulation index of 0.1 in case of the SVM and 2.39 A at a modulation index of 0.7 for DPWM1. Thus, for applications demanding the operation over the full modulation range, the use of the proposed PWM scheme results in size reduction of CM inductor.

The undesirable effect of larger duration of T_z at lower modulation indices can be reduced by the same zero vector alignment in the proposed scheme. In case of CI, the core is excited only for the one third period of the fundamental cycle, as evident from the waveform of the $I_{A,c}$ in experimental results. If the design of CI is thermally limited, the reduced core losses result in more compact design. The harmonic analysis of the line current is shown in Fig. 21. The major harmonic components are pushed close to the double of the switching frequency by the interleaving effect.

VI. CONCLUSION

A PWM scheme to reduce the maximum value of the flux linkage and the core losses in the circulating current filter is presented in this paper. This PWM scheme uses the division of the active vectors within a half-carrier cycle to ensure simultaneous occurrence of the same zero vector in both of the VSCs. The effect of the proposed PWM scheme on the flux linkage and the core losses in the circulating current filter is analyzed. Both the maximum value of the flux linkage and the core losses are reduced substantially by the same zero vector alignment in the proposed PWM scheme. Thus, the size of the circulating current filter can be reduced. The switching losses are also analyzed for the proposed PWM scheme and compared with that of the SVM and 60° clamped DPWM. The proposed PWM scheme demonstrates superior efficiency for the reactive power compensation applications, as it is evident from the core losses and switching losses comparisons presented in this paper. However, for the applications, where the displacement power factor angle is in the vicinity of zero, the use of proposed method results in high switching

losses. The line current ripple for the proposed scheme is also analyzed, which shows that the THD of the line current closely matches that of the SVM. The line current quality is superior in the case of the DPWM1, however the improvement is marginal at the higher modulation indices. The PWM scheme and the analysis presented in this paper are also supported by the experimental results.

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