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Modified High-power Nanosecond Marx Generator Prevents Destructive Current Filamentation

Guoyong Duan, Sergey N. Vainshtein, and Juha T. Kostamovaara, *Senior Member, IEEE*

***Abstract*—A *traditional Marx circuit* (TMC) based on avalanche transistors with a shortened emitter and base was investigated numerically using a 2-D physics-based approach and experimentally, and compared with a *special Marx circuit* (SMC) suggested here, in which an intrinsic base triggering of all the stages protects the transistors, especially the second one, from thermal destruction due to current filamentation. This is because the entire emitter-base perimeter in the SMC participates in switching, whereas in a TMC the switching is initiated across the entire area of the emitter but then changes to current filamentation due to certain 3-D transient effects reported earlier. Very significant difference in local transient overheating in the transistors operating in TMC and SMC determines the difference in reliability of those two pulse generators. The results suggest a new circuit design for improving reliability and explains the difference in the operating mode of different transistors in the chain which makes the second transistor most prone to destructive thermal filamentation. This new understanding points additionally to ways of optimizing the design of the transistors to be used in a Marx circuit.**

***Index Terms*—High-speed electronics, switching transients, avalanche breakdown, semiconductor device modeling, power generation reliability.**

I. Introduction

MARX circuits (MC) utilizing avalanche transistors to generate superfast (nanosecond or sub-nanosecond) high-voltage pulses are attracting more and more research interest [1, 2] as a simple, compact and low-cost solution [3] for multiple applications such as ultra-wideband radars and high-power microwave sources [4], the chemical analysis of minute material [5], ground-penetrating radar [6] and other applications, particularly when replacing air-gap switches.

A typical MC has one or more serial cascade transistors in each stage, and all the transistors except the first one (utilizing base triggering) have a short-connected emitter and base (e-b). Nearly all publications devoted to circuits of this kind have concentrated on better means of selecting commercial components, the reduction of parasitic inductance and other forms of routine optimization of the circuitry. The main trouble with this circuit is that a transistor in the chain can suddenly shorten, which will not damage the circuit immediately but will cause its degradation, thus drastically reducing practical interest in the Marx generator. In our experience, the transistor in the second stage is typically liable to damage, although this has not been reported so far, and generally no interpretation of this circuit degradation has been suggested. In this paper we investigate the operation of the circuit using 2-D physics-based transient device simulations, compare the numerical data with an experiment, and suggest the reason for the catastrophic degradation of the second transistor and a new circuit design for overcoming the drawback.

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II. Experiments and Simulations

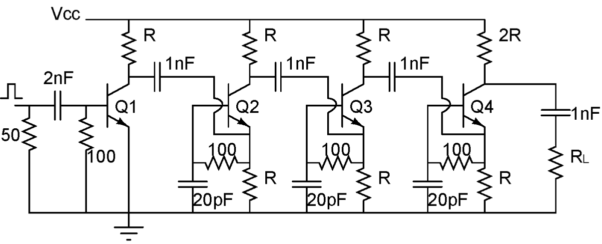

Fig. 1. The special design of the SMC circuit used in the experiment and simulations (unavoidable parasitic inductances are not shown in the figure, but they were used in the simulations, and a value of ~4 nH per stage provided the best fit between the simulated and measured load current waveforms). A 50Ω load was used and resistor R values in the kΩ range were selected in certain experiments as a tradeoff between high repetition rate and circuit reliability (see section IV.3).

Two circuits were used in the experiments and simulations. The specially designed one (SMC), shown in Fig. 1, had a special capacitor of 20 pF in each stage but the first one, aiming at base triggering of each transistor in the chain at the beginning of the switching transient, when the emitter voltage in each of the transistors Q2-Q4 becomes negative. Accordingly, the emitter and base of the transistors should not be shortened in this case, but their shunting using a ~100 Ω resistor should be implemented instead. The other circuit that was simulated and measured was the traditional one (TMC), which can be obtained by removing the three 20pF capacitors and replacing all the 100 Ω resistors (except the one in the first stage) with short connections. Commercial FMMT415 avalanche transistors and capacitors with high-frequency NPO ceramics were used in the circuit, and 20dB/18GHz attenuators and a 30 GHz real-time oscilloscope with a 50 Ω input were used to measure the load current.

Let us discuss briefly the principle of operation of TMC and SMC. The base-triggered transistor Q1 starts avalanche switching, which causes a negative voltage ramp to be applied to the emitter of Q2 across the 1 nF capacitor. In the case of

the TMC transistor Q2 is triggered by the voltage ramp applied between the shortened base-emitter and collector electrodes, while in SMC the negative voltage at the emitter causes additionally the triggering current to be supplied to the base of Q2 thanks to the 20pF capacitor. Now an even steeper voltage ramp produced by switching of both Q1 and Q2 will be applied to the emitter of Q3, and accordingly even more powerful base triggering of Q3, and also of Q4, will take place. Finally, four transistors in both the TMC and SMC will be switched on, with a residual voltage of ~100 V across each of the transistors, and all four 1nF capacitors, connected in series, will be charged each to ~300 V. This results in a voltage of ~ 300V×4 – 100V × 4 ~800 V being applied to the serial connection of the load resistor, the differential resistors of the switched-on transistors and the entire parasitic inductance of the circuit. The parameters of all these elements then determine the amplitude and duration of the current pulse that is generated across the load.

The important difference between the transistor switching initiated by the emitter-collector voltage ramp (in the TMC) and that initiated by the high-current base-triggering pulse (in the SMC) thanks to the added 20pF capacitors will be seen below. The emitter-collector voltage-ramp triggering initially causes switching of the entire emitter area [2], but then current filamentation occurs, with the more powerful filamentation corresponding to the lower voltage ramp (dV/dt) values. In the case of base triggering the emitter-base (e-b) perimeter only participates in the switching, and this regime for an FMMT415 transistor is softer from the point of view of thermal shock: the point to be illustrated and augmented below in the simulation and discussion sections. (Only a very small e-b perimeter, smaller than any currently used in commercial avalanche transistors, might change the situation).

Simulations of the above two circuits were carried out using the 2D MixedMode of Atlas (Silvaco Co.) which has given reasonable results in previous avalanche transistor simulations [2, 7-11]. The cross-sections of the 2-D simulated device shown below correspond to an X-Y plane perpendicular to the e-b interface, while the width of the structure in the direction Z, 0.8 mm, corresponds to 1.6 mm, the entire length of the e-b interface. This selection of the simulated transistor geometry provides the same overall e-b perimeter and the same emitter contact area as in the actual transistor chip used in the experiment (see the chip description in Ref. [8]). As shown in Fig. 3(a), 3(b), the current confinement corresponds to switching of the entire e-b perimeter in the SMC. In the case of the TMC the switching is initiated by the dV/dt ramp applied between the emitter and the collector. This ramp causes a displacement current to pass across the collector-base capacitance and electron injection to occur from the emitter, which triggers homogeneous avalanche switching across the entire emitter area [2], which changed later to filamentary behavior [2, 10, 11], as shown in Fig. 3(c), 3(d).

III. MEASUREMENT AND SIMULATION

The measured and simulated load currents are shown in Fig. 2. Despite a moderate difference in switching time and current amplitudes between the experiment and the simulations (within ~30%), the fit is much poorer than that obtained earlier for a transient in a single transistor [7-9]. It is no surprise on account of complicated interaction between the 4 transistors in the Marx circuit and 3-D effects (i.e. fairly complicated temporal evolution of the size of the switched-on area [10, 11] during the switching of each transistor. In addition, a 3-D filamentation scenario can differ from that predicted by our 2-D simulations, in the sense that more powerful current confinement can be expected in reality).

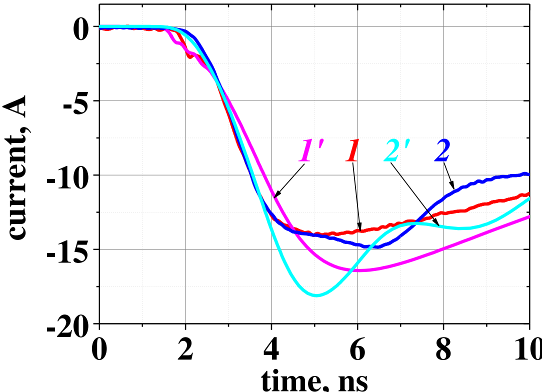

Fig. 2. Measured (curves 1 and 2) and simulated (curves 1'and 2') load currents for traditional (TMC, curves 1 and 1') and specially designed (SMC, curves 2 and 2') circuits.

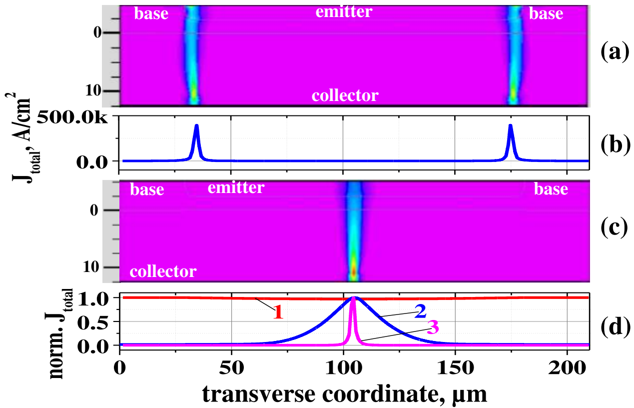

Fig. 3. Simulated total current density for transistor number 4 (Q4) at the instant approximately corresponding to the peak in the load current. (a)-contour cross-section at transient time 4.82 ns (compare with Fig. 2) for SMC. (b)-current density profile along the horizontal (X) cutline at longitudinal coordinate Y=10 µm in (a). (c)-contour cross-section at transient time 5.11 ns for TMC. (d)-horizontal cutline at longitudinal coordinate Y= 10 µm in (c). The absolute values of the peak current density for (d) are 40, 1888 A/cm^2, and 736 kA/cm^2 for curves 1, 2, and 3, respectively. In the SMC the current is confined near the emitter-base perimeter (which intersects the image cross-section in two places), while in the TMC the filamentary zone is located in the middle of the emitter area at equal distances from the e-b interfaces (with externally shortened e-b contacts) [2].

The most instructive results are those shown in Figs. 3 and 4. In the SMC the entire e-b perimeter is in operation (see Fig. 3(a), 3(b)), since all 4 transistors are base-triggered, thanks to the effect of the 20pF capacitors in stages 2-4. In the TMC (Fig. 3(c), 3(d)) switching in the transistors Q2T-Q4T is initiated by application of a collector voltage ramp from one stage to the next [2] and then, during the switching transient,

the profile of the normalized current density changes from the initially homogeneous one represented by curve 1 in Fig. 3(d) (instant 0.83ns) to filamentary ones (curves 2, 3 corresponding to instants 1.46, 5.12 ns respectively). This powerful filamentation (see the physical description in [10, 11]) causes dangerous local heating in the TMC (see Fig. 4 curves Q2T-Q4T), which can be prevented by using our modification of the MC (see Fig. 4 curves Q1S-Q4S).

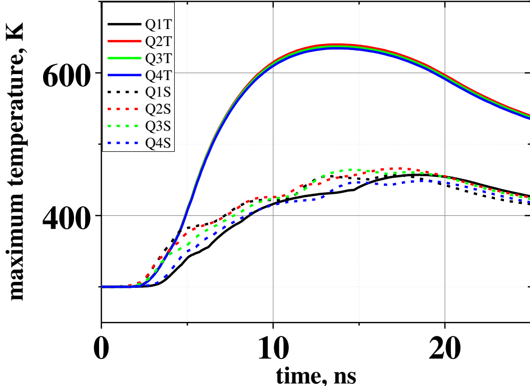

Fig. 4. Temporal profiles of maximum temperature at the hottest points of each of the four transistors (Q1-Q4) in the TMC (Q1T-Q4T) and SMC (Q1S-Q4S). Although the difference in peak temperature between transistors Q2T-Q4T is not large, the hottest one is transistor Q2T, which correlates with our previous empirical statistics for transistor failures in TMCs. The difference in peak temperatures was originally caused by the difference in the voltage ramps applied to the various stages, a point to be explained in detail elsewhere. The reason why the very small difference of ~3K observed in the modeling for second and third transistor can be so important is discussed in Section IV.

IV. Discussion

An imprecise but reasonable agreement was achieved between the measured and simulated current pulses when unavoidably applying a 2-D simulator to a 3-D problem. This does not, however, provide an experimental verification for the main result, namely the essential difference between local transient overheating in the transistors of the TMC and SMC versions.

Three principal questions arise: (i) are there propositions used in the simulations correct, (ii) is the fairly small difference of ~3 K in the overheating of the second transistor relative to the third one sufficient, and (iii) is there any experimental evidence available to confirms this main result at least qualitatively? These problems will be given in the three corresponding sections below.

IV.1 Operation of the entire emitter-base perimeter in the SMC

The peak temperatures shown for transistors 2-4 of the TMC in Fig. 4 should be regarded as optimistic values, as filamentation in a 3-D situation should provide stronger current confinement and more powerful heating than in the 2-D scenario used in our modeling. The significantly lower peak temperatures obtained for the transistors in the SMC are the result of the proposition that the entire e-b perimeter (1.6mm) participates in the switching: a point to be proved. Unfortunately, direct optical visualization of the operating perimeter, as reported in Ref. [8], was impossible due to the much lower permitted pulse repetition rate. We put forward the following arguments to support our approach.

(1) As shown in Ref. [8], given a large (~1 nF) capacitance, even a moderate triggering current density of ~0.3 kA/cm^2 caused operation of the entire perimeter in pulses of duration ~7 ns, unlike current confinement down to as small a fraction of the perimeter as ~0.1 mm, whereupon shorter pulses of ~2 ns are generated at a smaller capacitance (80 pF).

(2) According to the simulation data, the peak base triggering current (caused by base capacitor specially incorporated into the SMC) exceeds 1 A in second stage (that which is most "prone" to destruction according to our own experimental data), implying a triggering current density of j~3 kA/cm^2. (The current in the subsequent stages is even higher by a factor of 2 or 3, so that they are accordingly safer). Thus the triggering current density exceeds the critical value j_c= electron charge × donor density in n_0-collector × saturated electron velocity ~1 kA/cm^2. In this case only homogeneous switching of the entire perimeter can be expected. Indeed, the dynamic current localization in accordance with "the winner takes all" principle that is already well known in thyristors [12] and avalanche transistors [8-11] is caused by the fact that the current density exceeds the critical value earlier in some parts of the structure than in others, so that those parts raise the switching speed. (This occurs due to electric field reconstruction in the n_0-layer both in thyristors and avalanche transistors). Such effects are typical of a situation in which the minimal possible triggering current is used and "slow" switching of different parts of the perimeter causes competition between them for reaching the critical current density: i.e. eventually only one, the most "successful" filament, accelerates and wins out over the others. In stages 2-4 of the SMC the critical current density is already exceeded at the triggering stage everywhere across e-b interface, and thus homogeneous switching of the entire e-b perimeter will inevitably take place.

IV.2 Destruction of the second transistor

We are not familiar with any *direct* discussion of the problem of second transistor destruction in a TMC in the literature, but certain facts certainly deserve mentioning. (i) With reference to a private communication with a user of a commercial sub-picosecond (sub-ps) TMC-type generator, we know that slow degradation of the generator's parameters takes place during long-term (months/year) operation, caused by shortening transistors in the long TMC-like chain one by one. (ii) We have to refer to our own experience gained while developing a high-current (~150 A) TMC-like generator (see Ref. [13]) with both serial and parallel transistor connections and automatic switching synchronization. What is important is that we occasionally (but not frequently) observed in various modifications of this generator that one of the transistors *in the second stage* became shortened. (The problem was not mentioned in Letter-size paper [13]). Once we had developed the SMC idea (used for the first time in that work but not mentioned in Ref. [13]), the problem was solved: at least we did not have any further reliability problems with the SMC

generator in our laboratory tests. (iii) An additional fact will be described in the next section: that while performing the high-repetition rate experiments we figured out that it was *always* the second transistor that reached the thermal filamentation (pre-destruction) mode in both the TMC and SMC devices.

We propose the following arguments as interpretations of this second transistor destruction (or at least of the pre-destructive thermal current filamentation).

In the TMC case the second stage differs from the first one in that it lacks any base triggering and from the third and fourth stages in that it has reduced emitter-collector dV/dt voltage ramps, which should facilitate more powerful filamentation in the second stage than elsewhere (the point following from the interpretation of collector-emitter dV/dt - ramp switching in Ref. [2]). In the SMC case this factor is softened by the base triggering of stages 2-4, but this triggering is weaker in stage 2 than in stages 3 or, more especially, stage 4. Thus again stage 2 is most prone to destructive thermal filamentation.

(1) The peak temperature increment of 3K in stage 2 relative to stage 3 *after a one nanosecond-range switching cycle*, as shown in Fig. 4 is not impressive, but it has to be borne in mind that (i) the thermal accumulation should grow after a large number of cycles, and (ii) *elevated current (and carrier) density can provoke more significant heating at the voltage recovery stage* (see section IV. 3).

(2) In the case of virtually “equal” transistors being used in the circuit even a small variation in the overheating of one transistor can be sufficient for generator destruction due to thermal filamentation in one transistor at the “most susceptible” stage 2.

(3) We used a 2-D simulator to solve a 3-D problem, which was unavoidable given the existing state of the art. 3-D filamentation may provide more significant differences in the switching transients triggered by different dV/dt voltage ramps for the second and third transistors in TMC devices.

In any case this is the only evidence so far which gives an interpretation of the clearly established experimental fact that the second transistor is more prone to destructive thermal filamentation than the others.

IV.3 High-repetition-rate tests.

Rigorously speaking, direct proof of the better reliability of SMC than of TMC requires a number of generators, sufficient time and convincing statistical results. This is apparently not the way, however, to implement this time- and effort-consuming approach in the research that is not directly oriented to the production development.

The main argument arising from our previous experience (see section IV.2) is that destruction of the second transistor in high-current-circuit laboratory tests was effectively prevented by using our SMC design (a result not mentioned or published earlier).

Described below is fairly logical attempt to prove the advantages of the SMC construct by means of high-repetition-rate tests with counts of the pulses required for reaching thermal filamentation in the "most susceptible" transistor (see upper panel in Fig. 5). We were planning to apply triggering pulses at a high repetition rate (1/T1), at a sufficiently low T1 (down to ~10 µs) and in sufficiently large numbers N (~1000) to reach the level required for destruction of the second transistor in the TMC, and then, in the next experiment, to show that at the same T1 we had to use a larger number N of pulses for SMC destruction. The logic of this experiment is explained in Fig. 5, lower panel.

After a single nanosecond-range switching the temperature in the "hot" zone of the transistor structure reached a peak value of ~650 K for TMC or ~450 K for SMC (see Figs. 4 and 5). (The hot zone is determined by the intersection of the high-field domain situated at the n_0-n^+ collector interface with the peak current density zone situated under the e-b interface: see Refs. [7, 8]).

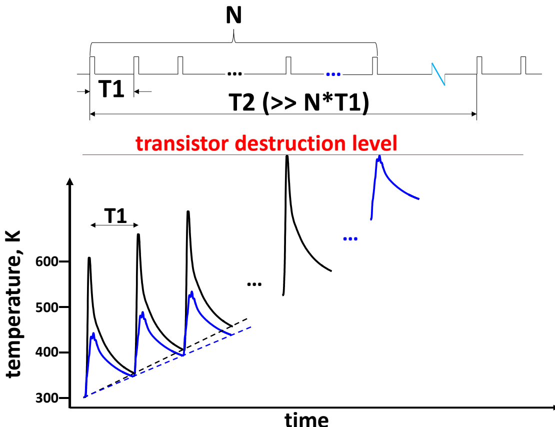

Fig. 5. The idea of the high-repetition-rate experiment to obtain direct experimental proof of the advantage of the SMC approach over TMC. The burst of N pulses arriving with a period T1 and triggering the Marx circuit is shown in the upper panel. T2 is the (sufficiently large) repetition period of the bursts. The temporal profile of the local temperature in the hottest point of the ("most susceptible") second transistor is shown by the black line for TMC and the blue line for SMC.

This hot zone can roughly be conceived of as a cylinder of diameter ~10 µm and length 1.6 mm for SMC or 800µm for TMC. The axis of this cylinder lies at a depth of 15µm below the emitter contact at the n_0-n^+ collector interface. A characteristic time for the reduction of the peak temperature by an order of magnitude in the adiabatic regime can then be estimated in terms of the time required for thermal diffusion *to increase the cylinder volume by an order of magnitude*: $\tau \sim (r_2 - r_1)^2/D_T \sim 1$ µs (where $r_1 \sim 5$µm is initial radius of the cylinder, $r_2 \sim 15$µm is the final radius, and $D_T \sim 1 cm^2/s$ is the thermal diffusion coefficient for Si). At the same time the thermal front reaches the emitter contact and an additional cooling mechanism depending on heat-sink parameters will be added to the process. Thus we can expect that after several microseconds the hot zone will cool down practically to room temperature, but the reduction in T1 will cause a gradual temperature rise from one switching circle to the other: see Fig. 5. It is obvious that a smaller number N of pulses will be required to reach a certain thermal destruction threshold in a TMC device than in an SMC one, and we were planning to make use of this idea in order to obtain experimental proof of the advantages of SMC.

The first problem in the practical realization of this approach was detected when T1 was selected to be just a few µs. In practice T1 it must obviously be larger than 2R×(1nF), but we found that R=1kΩ already causes thermal filamentation of the second transistor after the first switching, a form of behavior to be discussed below. At too high an R (5kΩ) and with a correspondingly large T1 we did not observe any thermal filamentation even without the burst mode when the operation frequency was below 30 kHz.

The targeted burst regime was found at R=2.5kΩ, T1=20µs, N~1000 pulses, provided that the burst period T2 was sufficiently large (>>20ms). Using TMC we gradually increased the number of pulses N, until at N≈950 thermal filamentation was observed in the second transistor. (By thermal filamentation we mean a non-controllable reduction in the voltage across the transistor to about a dozen volts and burning resistors R, connected to this transistor. If the resistors fail to withstand the high power the transistor will survive, otherwise it will be destroyed before the resistors begin to burn).

The same experiment repeated for SMC resulted in thermal filamentation in the second transistor at N≈1050 pulses. In principle this tendency is correct, but the values are not at all convincing, on account of the very large difference in peak temperature (see Fig. 4).

We suggest the following interpretation for these experimental observations. The excess carrier lifetime in the n_0-collector region should be ~1 µs, and let RC value be comparable to this value. *At the voltage recovery stage* not all the carriers will recombine and they may initiate a weak but important avalanche multiplication once the growing voltage across the emitter-collector exceeds ~100V. This multiplication, even at a current of ~several mA and a voltage of ~100 -300V, will correspond to 1W heating power and thus within a time interval of ~ microsecond more thermal energy will be generated during voltage recovery stage than that earlier accumulated during high-current nanosecond-range switching.

This explains why too small resistor R (1kΩ) will in itself not allow even a second switching event, and why the observed favorable difference in behavior between TMC and SMC was not that convincing: the thermal accumulation at the recovery stage predominates and masks the effect of the higher peak temperature at the end of nanosecond switching in TMC.

Any attempt to increase R (and accordingly T1) will not allow thermal filamentation to be observed at all. Thus the high-repetition-rate test does not provide very convincing proof of the advantages of SMC. These advantages can be seen only in moderate frequency/long term operation, when this or some other type of "tiredness" in the device brought about by powerful local thermal shocks causes gradual device degradation. Apparently the most convincing observations so far are those made by us while developing the high-current driver [13], as explained in section IV.2 above.

V. Conclusions

Powerful current filamentation in all the transistors with a shortened emitter base (except the first) that are triggered by the collector voltage ramp [2] will cause local overheating by the end of the current pulse generated by a traditional Marx circuit, and this can be dangerous for the device. A difference in the triggering voltage ramp between the stages (to be discussed elsewhere) makes the second stage most prone to thermal damage, which is in agreement with our long-term empirical observations. The special design suggested here for a Marx circuit, with capacitors added for automatic base triggering of all the stages, reduces overheating drastically and provides a means for resolving the reliability and durability problems experienced in Marx circuits.

Acknowledgements

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