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Article Info	ABSTRACT
	Connecting a single-phase or three-phase inverter to the grid in distributed generation applications requires synchronization with the grid. Synchronization of an inverter-connected distributed generation units in its basic form necessitates accurate information about the frequency and phase angle of the utility grid. Phase Locked Loop (PLL) circuit is usually used for the purpose of synchronization. However, deviation in the grid frequency from nominal value will cause errors in the PLL estimated outputs, and that's a major drawback. Moreover, if the grid is heavily distorted with low order harmonics the estimation of the grid phase angle deteriorates resulting in higher oscillations (errors) appearing in the synchronization voltage signals. This paper proposes a modified time delay PLL (MTDPLL) technique that continuously updates a variable time delay unit to keep track of the variation in the grid frequency. The MTDPLL is implemented along a Multi-Harmonic Decoupling Cell (MHDC) to overcome the effects of distortion caused by gird lower order harmonics. The performance of the proposed MTDPLL is verified by simulation and compared in terms of performance and accuracy with recent PLL techniques.

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1. INTRODUCTION

Distributed generation systems allow customers to power homes with renewable energy during periods when the sun is shining, and any excess electricity produced is fed back into the grid. This will allow the grid to operate at enhanced capacity and more economical levels. Therefore, the integration of DG systems (wind, solar, etc.) in distribution networks has increased rapidly, since the possibility of generating power close to consumers, reduces power losses, increases voltage levels, improves reliability, and others [1, 2]. Single-phase grid-tied inverter is one of the preferable methods of integrating small ratings DG units (power output under 10kW) into the grid [3].

One of the major problems encountered when connecting or synchronizing a DG system with the grid, is to obtain fast and accurate estimations of phase and frequency of the grid. The problem becomes even more challenging with more and more non-linear loads are being connected to the electrical networks; since distortions and transients such as harmonics and phase shift often occur to the grid [4].

Reference [5] presents a detailed review of several algorithms and techniques that are widely used to synchronize single-phase inverters with the grid. Recently, research topics such as; Discrete Fourier Transform [6, 7], Kalman filtering [8, 9], least-squares estimation [10], Artificial Neural Networks [11], the Enhanced PLL technique [12], Second Order Generalized Integrator (SOGI) [13], and Inverse Park Transform (IPT) based PLL methods [14], have been implemented to estimate the phase and frequency of the

grid. As reported in [15-18] one of the major challenges faced by various PLL schemes is to present immunity against the high frequency disturbances and low order harmonics, while at the same time to maintain a reasonable dynamic response in case of frequency and phase jumps. Various modifications and enhancements have been made to improve PLL performance under various grid conditions. Methods presented in [12-14] offer well-established synchronization techniques and can filter high frequency harmonics; however, they suffer from immunity against low order harmonics according to [15-18]. In [18] a comparative time domain performance evaluation of adaptive techniques; such as Pseudo Linear - enhanced PLL (PL-EPLL), SOGI - Frequency Locked Loop (SOGI-FLL) and Adaptive sliding mode Observer (AO) for various grid condition is presented. However, the effects of lower order harmonics on estimating the phase and frequency of the grid using these techniques were not reported.

This paper presents a novel synchronization algorithm that basically relies on the fact that a PLL in synchronized state has a phase error that's either zero or constant between the system output signal and the reference signal [19]. Thus, the proposed algorithm, as shown in Figure 1, implements a feedback that uses the estimated phase output obtained from a PLL over the duration of one cycle of the nominal frequency of the grid voltage. The slop (estimated phase over one cycle) is directly employed to calculate the deviation in the frequency from the nominal (or initial) value of the grid frequency. The amount of deviation in the frequency is then used to update a variable transport delay unit used by the Quadrature Signal Generator (QSG) to generate orthogonal stationary reference frame signals of the grid voltage ($v_{\alpha\beta}$).
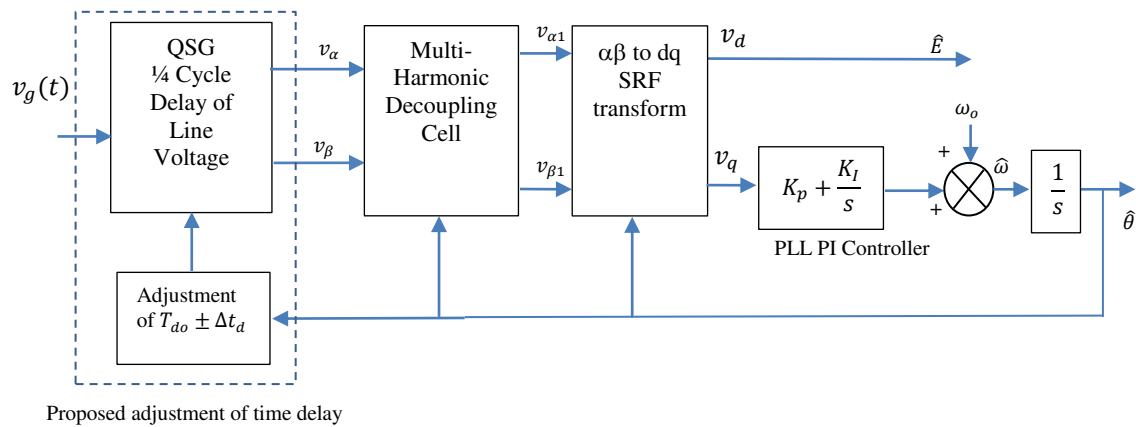

Figure 1. Modified time delay Phase Locked Loop using MHDC
with proposed time delay adjustment at the two-phase generator

The proposed method showed good performance that's accurate and fast in estimating the phase and frequency of the grid voltage signal. However, the performance of the proposed algorithm deteriorates in the presence of the low order harmonics due to the limited bandwidth PI controller (voltage-controlled oscillator) in the PLL. In order to eliminate the effect of low order harmonics, a Multi Harmonic Decoupling Cell (MHDC) as proposed in [17], is implemented to filter the grid fundamental signals.

2.   QUADRATURE SIGNAL GENERATOR

Clarke transform is a well-known method used in three phase applications to generate the two orthogonal stationary reference frame voltages ($v_{\alpha\beta}$). However, in single phase applications, several possibilities exist for the phase generator, such as a method using a look-up table, methods using a first-order and a second-order filters [20] and methods using transport delay of T/4 (delay of quarter cycle of fundamental voltage) [17, 21]. The method using the first-order filter shows the shortest estimation time and the method using the second-order filter shows less oscillation [20].

As depicted in Figure 1, the grid voltage (v_g) is sensed and then fed to the QSG unit to create orthogonal stationary voltage components ($v_{\alpha\beta}$) in a manner equivalent to that of Clarke transformation in three-phase systems. Figure 2(a) and 2(b) show the basic structure of QSG using first order filter, and Quarter cycle (T/4) transport delay methods, respectively. The method that uses the Quarter cycle delay is implemented in this paper.
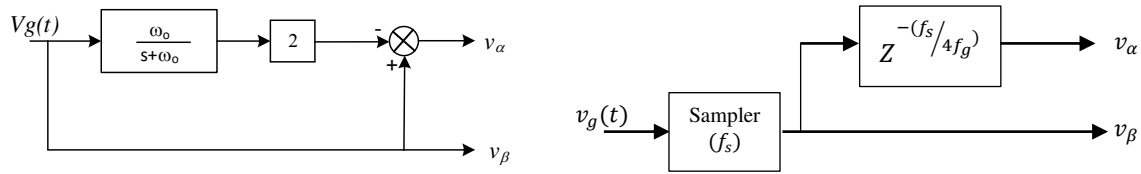
Figure 2. Two-phase generation method (a) using first order filter, (b) using basic quarter cycle delay

Given that the sampling frequency (f_s) is fixed by design, and the grid frequency (f_g) is constant as in an ideal scenario, then the quadrature component of the grid can be generated by a quarter cycle delay (i.e. $z^{-f_s/4f_g}$, where f_s is the sampling frequency and f_g is the grid frequency).

As shown in Figure 1, the output of the two-phase generator is transformed into the synchronously rotating reference frame (SRF) voltages V_{dq} as:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{1}$$

where $\hat{\theta}$ is the estimated phase angle of the grid obtained by the PLL, V_d, and V_q are the normalized direct and quadrature components of the grid voltage, respectively. The input error signal to the PLL PI controller as shown in Figure 1 is given as [20, 21]:

$$V_q = \sin\theta\cos\hat{\theta} - \cos\theta\sin\hat{\theta} \tag{2}$$

where , is the actual grid phase. In eq. (2) the error signal V_q=0 and V_d=1 (grid normalized magnitude), if the estimated phase angle of the grid voltage is an exact match with the actual value, i.e.

$$\left.\begin{array}{l} V_d = 1 \\ V_q = \sin(\theta - \hat{\theta}) = 0 \end{array}\right\} for\ \theta = \hat{\theta} \tag{3}$$

However, for a small deviation in $\hat{\theta}$ from actual value of the grid phase angle θ, the error signal input of the PI controller is:

$$V_q = \sin(\theta - \hat{\theta}) \approx \Delta\theta \tag{4}$$

This initial error will be regulated by the PLL PI controller (low pass filter) and integrated further to produce $\hat{\theta}$ that will eventually match the actual grid phase (θ) and the PLL will enter the synchronized state and will be locked.

Unfortunately, due to deviation in the grid frequency from nominal value, and the distortion in the grid voltage, the two voltage signals (v_α and v_β) produced by the two-phase generator will not be orthogonal. For example, if QSG is set to produce v_α and v_β based on $f_g = 50Hz$ and $f_s = 20kHz$, then an amount of time delay, T_{do}, required (to produce the voltage v_α to be in quadrature with v_β, the sampled grid voltage) will be 5ms or 100 samples. On the other hand, if there is a deviation in the grid frequency from the nominal value where $f_g = 51Hz$, then $T_{do} = 4.902$ms or 98 sample delay is required to produce voltage v_α to be in quadrature with v_β. The effect of such deviation in the grid frequency from the nominal value, will then result in an error in the two voltages in quadrature as,

$$\left.\begin{array}{ll} v_\alpha = \cos(\theta \pm \Delta\varepsilon) & when\ \omega_g \neq \omega_o \\ & or\ f_g \neq 50Hz \\ v_\beta = \sin\theta & true\ grid\ signal \end{array}\right\} \tag{5}$$

where $\pm\Delta\varepsilon$ is the phase error in the phase v_α. Equation (2) is then modified based on (5) and the actual error signal of the PI regulator V_q becomes:

$$\begin{aligned} V_q &= \sin\theta\cos\hat{\theta} - \cos(\theta \pm \Delta\varepsilon)\sin\hat{\theta} \\ &\approx (\theta - \hat{\theta}) \pm \tfrac{1}{2}\Delta\varepsilon \mp \tfrac{1}{2}\Delta\varepsilon\cos(\theta + \hat{\theta}) \end{aligned} \tag{6}$$

Equation (6) has three terms: the first is similar to the error terms as in (4), the second term is a constant term that will result in an error in the estimated phase angle by the PLL, and the third term is an oscillatory term at twice the grid frequency. The PI controller will regulate the first two terms to zero, however, the third term will still present oscillatory component in the estimated variables. A low bandwidth PI controller in the PLL will reduce this component, however this is not an option since a PI controller with lower bandwidth will have a slower dynamic response. The design constraints on the PLL PI controller as addressed in the next section.

3.   DESIGN OF PLL PI CONTROLLER

The transfer function relating the input and estimated phase of PLL is expressed as, [20]:

$$\frac{\hat{\theta}(s)}{\theta(s)} = \frac{K_p s + K_i}{s^2 + K_p s + K_i} \tag{7}$$

Designing the PI controller for PLL is a trade-off process between filtering capability (attenuating the fundamental frequency of negative sequence) and the dynamic performance in terms of the transient time (fast tracking) of fundamental frequency positive sequence. Both requirements can't be met simultaneously. In [22] it is shown that the reduction of the bandwidth has a significant effect on the settling time (2% criteria) of the PLL. On the other hand, increasing the bandwidth will result in faster response but at the expense of filtering (the attenuation) of the fundamental frequency negative sequence component.

Therefore, in this paper the parameters of the PI controller are set to $K_p = 92, K_i = 4255$ as recommended by [17]. Figure 3 shows the Bode plot of the PI controller using the recommended values above. The PI controller has a phase margin of 65.4° and crossover frequency of 101 rad/s which meets the requirements of the PLL system.
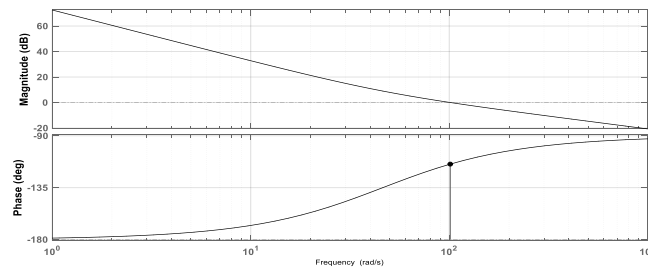

Figure 3. Frequency response of the PI controller PLL

4.   MULTI HARMONIC DECOUPLING CELL (MHDC)

To remove the oscillation in the estimated variables (magnitude and phase of the grid) caused by the grid lower order harmonics, the MHDC presented in [15, 17] is implemented as in Figure 1. The implementation of the MHDC is based on constructing n parallel stages to be equal to the number of the lower order harmonics to be filtered ($n=5$ for filtering 1st, 3rd, 5th, 7th, and 9th harmonics). The n stages will estimate and segregate each of the harmonic components that exist in the grid stationary voltage (v_α, v_β) components. This is done by the means of first transforming the grid signal into the SRF (converting it into DC equivalent, thus the filtering requirements are similar for all the harmonic components of the signal). The signals are then filtered using a low pass filter with cut-off frequency ($\omega_f = 2\pi 50/3$). The n signals resulting out from the low pass filter stage are then converted back to stationary reference frame (they become at common frequency, i.e. fundamental frequency). The $m=n-1$ outputs from all stages, excluding for $n=m$, are used in a feedback to stage n input to cancel out the all the harmonic component in each stage, thus leaving out the estimated n harmonic component as an input to each corresponding n stage. The estimated harmonic components in the input signal is given by (8).

$$\widehat{v_{\alpha\beta}^n} = v_{\alpha\beta} - \sum_{n \neq m} \left[T_{dq^{-sgn(m)m}} \right] [F(s)] \left[T_{dq^{sgn(m)m}} \right] \widehat{v_{\alpha\beta}^m} \tag{8}$$

where $\widehat{v_{\alpha\beta}^n}$ is the estimated n harmonic component (for $n=1,3,5…$etc), $v_{\alpha\beta}$ is QSG output obtained from the grid signal, $T_{dq^{sgn(m)m}}$ Park's transformation rotating with speed $sgn(m)m\omega$ and $sgn(m) = \sin\left(\frac{m\pi}{2}\right)$, $F(s)$ is a low pass filter $=F(s) = \frac{\omega_f}{s+\omega_f}$, and $\widehat{v_{\alpha\beta}^m}$ is the estimated m harmonic component.

The implementation of (8) is shown in Figure 4 for n= 1,3 and 5 for illustration. However, in this paper MHDC is built to filter or process up to the 9th harmonic, Fig. 4 can be extended to any higher order of harmonics extraction. The detailed design and analysis of MHDC is given in references [15, 17].
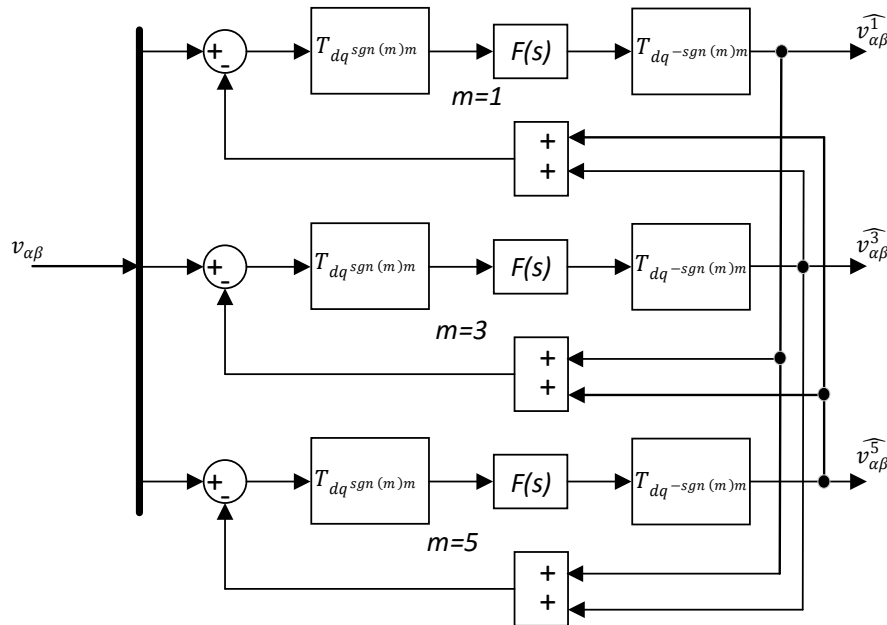

Figure 4. Block diagram of MHDC for n=1,3, and 5

5. PROPOSED MODIFIED TIME DELAY PLL (MTDPLL)

The constraints on the PI controller set a good recommendation for the bandwidth to tackle the tradeoff between speed of response and filtering distortion due to high order harmonics in the grid voltage. However, a slow drift or variation in the supply frequency from nominal value, and the presence of lower order harmonics in the grid will result unfortunately in oscillatory terms at twice the supply frequency, and the harmonic content will still be observed in the estimated variables. This will have significant deteriorating effects on the instantaneous value of the estimated angular frequency and amplitude of the grid and consequently on the power quality of grid-tied inverter as discussed in [17].

A modified time delay algorithm is proposed in this paper to adjust the initial time delay (1/4 cycle of the grid $T_{do} = 0.005s$) periodically, every one cycle of the grid. The adjustment proposed as in Figure 3 depends on the sampling frequency of the processor and an initial value of the grid frequency. The modified time delay ($T_{do} \pm \Delta t_d$) is allowed to either a single increment or decrement every single cycle of the grid to adjust the time delay used by the two-phase generator to produce (v_α and v_β).

For example, a system (e.g. inverter) that operates at PWM of 20kHz switching frequency would require a minimum of 20kHz sampling frequency, i.e. a grid operating at 50Hz would be sampled 400 times in one cycle. Thus, a quarter cycle time delay (5ms) will translate into a delay of 100 samples.

Immediately after the first cycle (400 samples) of the grid voltage the estimated phase $\widehat{\theta_1}$ is loaded (stored) and then another 400 samples later another value is sampled ($\widehat{\theta_2}$). Dividing $\Delta\widehat{\theta}$ is by a constant $2\pi\Delta T$ ($\Delta T=0.02$ s), will give the estimated frequency $\hat{f} = \frac{\Delta\widehat{\theta}}{2\pi\Delta T}$ by the PLL. The deviation or error in the frequency $\Delta\varepsilon_f = \frac{\hat{f}-f_g}{f_g}$ can be used to adjust the quarter time delay (number of samples) $N_{do} \pm \Delta N_d$ where $N_{do} = \frac{f_s}{4f_g}$ and $\Delta N_d = \Delta\varepsilon_f N_{do}$. The adjustment ΔN_d is rounded to an integer value which will be used to adjust the initial time delay that corresponds to nominal grid frequency.

The accuracy of the above proposed adjustment is dependent on N_{do}. For example, a sampling frequency of 20KHz, gives $N_{do} = 100$ thus the smallest error that can be detected in the frequency ($\Delta\varepsilon_f$) is $\pm1\%$, which corresponds to ±0.5 Hz. The accuracy can be improved if the sampling frequency can be increased to higher values. The implementation of the time delay using Simulink is shown in Figure 5.
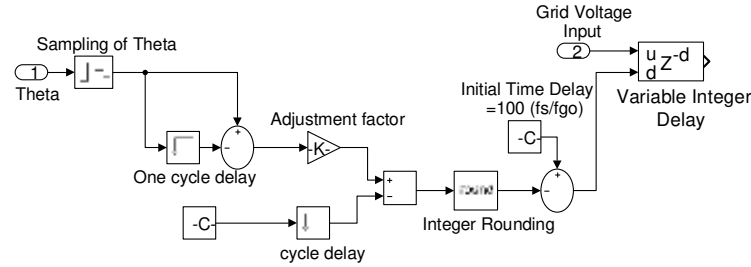

Figure 5. Simulink block diagram of time delay adjustment

6.   RESULTS AND ANALYSIS

The simulation results for conventional PLL and the MTDPLL systems are given in this section. SIMULINK/MATLAB is used in this study with following simulation Model Configuration parameters: Solver: Fixed step automatic solver with fixed step size of 50×10^{-6} (i.e. sampling frequency $f_s = 20kHz$). Initial simulation is carried out to investigate the ability of the proposed MTDPLL to adjust its time delay when the supply is initially at 49Hz and 51Hz. Results in Figure 6(a), 6(b) and 6(c) respectively, show the time delay adjustment, the time delay that corresponds to 49Hz, and phase angle of the grid. Results in Figure 7 show MTDPLL operation for grid initial frequency 51Hz. The results show that the MTDPLL was able to track and detect the grid phase angle after 4 cycles (0.08 sec) in case of 49Hz, and one cycle (0.02 sec) when the grid at 51Hz. The oscillation in the estimated variable were eliminated in the case of the MTDPLL when compared with the conventional PLL (implemented with a low pass filter that has a cutoff frequency fixed at $\omega_o = 2\pi50$ which corresponds to nominal grid frequency $f_g = 50HZ$).
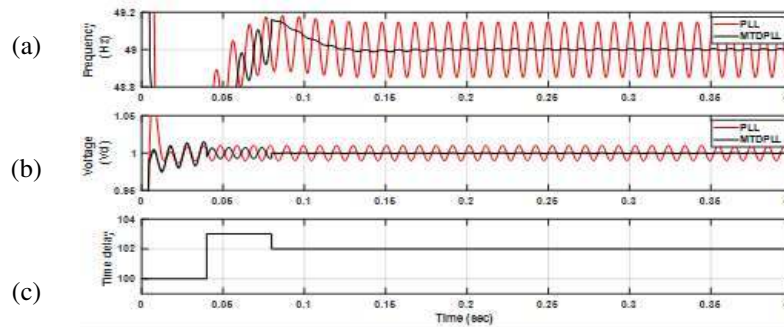

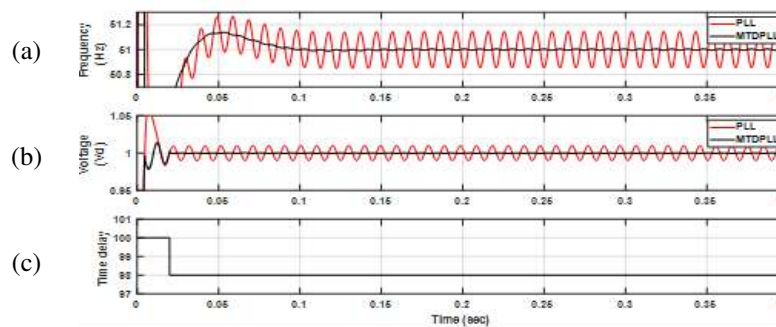Figure 6. Response of conventional PLL and MTDPLL when grid is initially at 49Hz

Figure 7. Response of conventional PLL and MTDPLL when grid is initially at 51Hz

The outputs from the MTDPLL and conventional PLL are next examined under three different conditions: Test I: when frequency of grid is step changed by +2Hz (from (50Hz to 52 Hz), Test II: when phase is jumped by +20°, and Test III: when grid is subjected to voltage sag of -20%. Figures 8, 9 and 10, respectively show the results obtained from the three tests. The results showed that frequency deviation mainly affected the estimated variables in case of the conventional PLL (oscillatory results in the estimated frequency and magnitude of the grid voltage) as in Figure 8. The MTDPLL was able to adjust the variable time delay in 4 cycles in case of frequency jump (Figure 8), and took 5 cycles to adjust in case of phase jump (Figure 9). The voltage sag effect didn't show any change in the time delay adjustment as the deviation in frequency settled to less 0.5Hz in less than one cycle (0.02 sec).
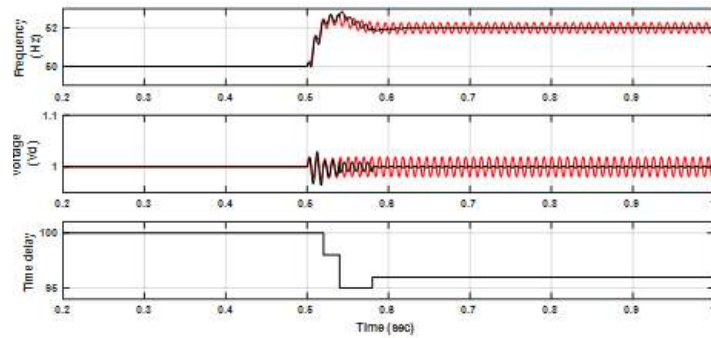

Figure 8. Response MTDPLL when step change in grid frequency from 50Hz to 52Hz
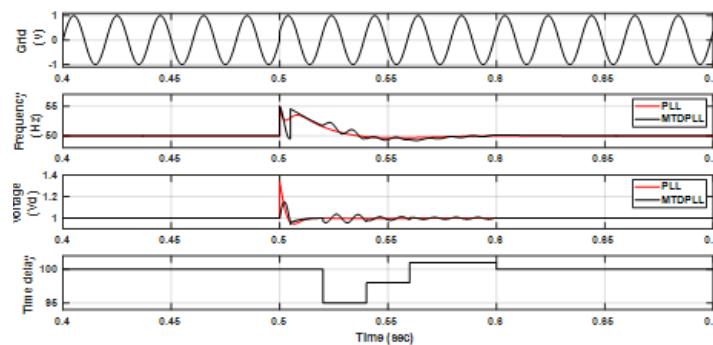

Figure 9. Response of MTDPLL with Phase jump of 20° in grid voltage
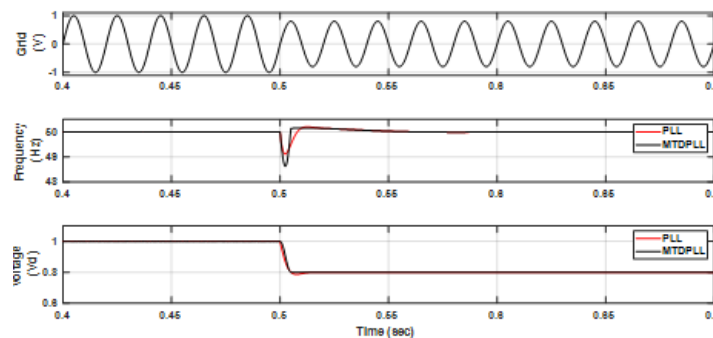
Figure 10. Response of MTDPLL with grid voltage sag 20%

The results were also benchmarked against results obtained in [18] to verify the efficiency and accuracy of the proposed technique. Table 1 summaries the steady state performance as obtained from the proposed MTDPLL and from SOGI-FLL and AO methods. The results in Table 1 showed that the proposed MTDPLL produced a comparable performance in terms of steady state error and settling time given the simplicity of the proposed technique.

Table 1. Summary of time domain performance results of selected well established PLL techniques

| | Test I (Step 2Hz) | | | Test II (Phase Jump 20°) | | | Test III (Voltage Sag 20%) | | |
	AO*	SOGI-FLL*	MTDPLL	AO*	SOGI-FLL*	MTDPLL	AO*	SOGI-FLL*	MTDPLL
Frequency Settling Time (±2% *in Cycles*)	1	3.3	4.5	3	3.9	4.3	1.44	2.82	2.5
Max. Peak Freq. Error (Hz)	2	2.5	2.7	5.87	6.26	5	0.85	2.3	1.3

As obtained from reference [18]

Finally, the effect of low order harmonic distortion is examined. Figure 11 shows the harmonic content in the grid signal that has been used in this part of the simulation. The MHDC in Figure 4 is implemented to decouple the effects of the lower order harmonics up to the 9th harmonic.
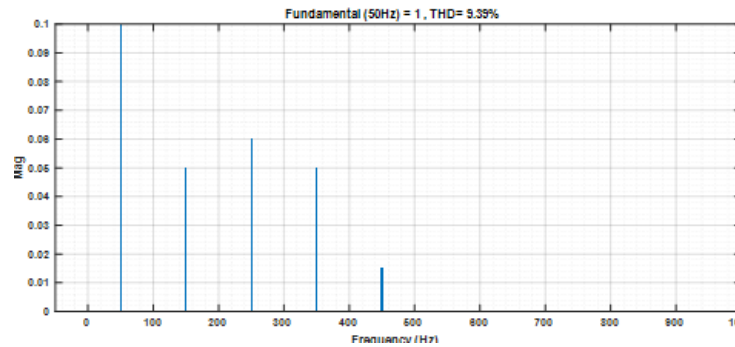

Figure 11. Lower order harmonic content (3rd, 5th, 7th, and 9th) in the grid signal with a THD of 9.39%

Initially, in Test I: from 0-0.5sec, the grid frequency is set at 50Hz with THD at 9.39%. The results in Figure 12 showed that the MTDPLL was capable of detecting the frequency and the magnitude of the grid voltage (V_d). However, the time delay adjustment took slightly longer time to settle due to the insertion of the MHDC block when compared with no harmonics case as shown in Figures 6 and 7. However, the MHDC showed efficient performance in decoupling the harmonics effect from the fundamental signal.
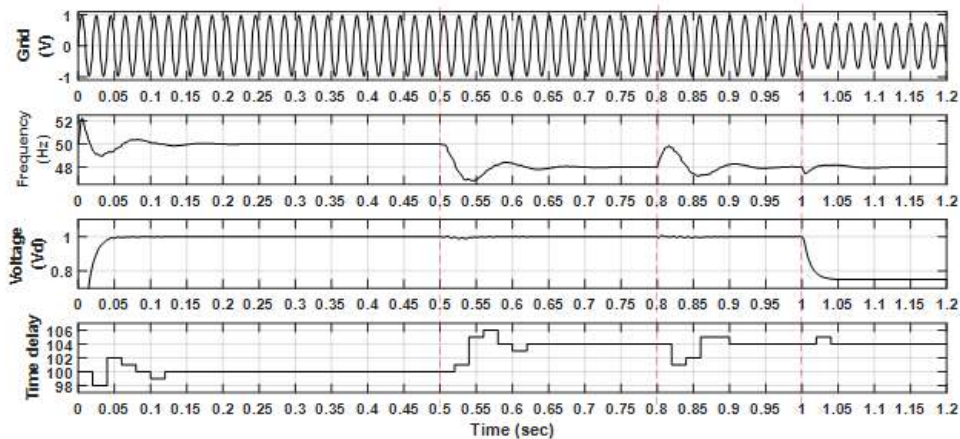

Figure 12. Simulation results of the MTDPLL and MHDC response under sever grid conditions: harmonic distortion, frequency jump, phase jump and voltage sag

In Test II: from 0.5-0.8sec, the frequency of the grid is stepped down to 48Hz with THD of 9.39% in the grid signal. The time delay adjustment settled to the final value in 6 cycles (1.2 secs). It can be observed that accurate synchronization can be obtained even under the sever testing condition. In Test III: from 0.8-1.0 sec, together with conditions in tests I and II, a phase jump of 10° is applied. The MTDPLL was

able to respond accurately and adjust the time delay within 5 cycles to the correct value. Finally, in Test IV: from 1.0-1.2 sec, under all the pervious conditions a voltage sag of 25% is included. The voltage sag effect appeared accurately in the estimated voltage magnitude of the grid (V_d) and the grid estimated frequency sustained at 48 Hz with no change.

7. CONCLUSION

A simple, yet accurate time delay modification technique is presented in this paper for the purpose of accurately generating two orthogonal signals to be used in the application of PLL in synchronization of single-phase grid-tied inverter. The proposed technique uses the slop of the phase angle (generated by conventional PLL) to modify a transport delay time in a Quadrature Signal Generator unit. The accuracy in estimating the phase of the grid voltage resulted in cancelling the oscillation and any steady state errors in the estimated SRF voltages. This will in turn enhance the efficiency of a grid tied-inverter. The proposed technique when combined with Multi Harmonic Decoupling Cells provides excellent accuracy and fast convergence even in the presence of sever grid disturbances (lower order harmonics, frequency jump, phase jump and voltage sag).

REFERENCES

[1]   K. Cabana, et al., "Voltage sensitivity analysis to determine the optimal integration of distributed generation in distribution systems," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 9, pp. 55-65, 2019.

[2]   R. S. R. Sankar, et al., "Adaptive Fuzzy PI Current Control of Grid Interact PV Inverter," *International Journal of Electrical and Computer Engineering (IJECE)*, vol. 8, pp. 472-482, 2018.

[3]   J. R. Didat, et al., "Modeling and experimental testing of a grid-connected small Wind Energy Conversion System," *EWEC 2006*, Athens, Greece, 2006.

[4]   Y. Long, and Y. Sun, "A New PLL Simulation Validation for Three-phase Grid under Heavy Distorted Conditions," *International Journal of Online and Biomedical Engineering (iJOE)*, "MESI 2014," vol. 11, 2015.

[5]   N. Jaalam, et al., "A comprehensive review of synchronization methods for grid-connected converters of renewable energy source," *Renewable and Sustainable Energy Reviews*, vol. 59, pp. 1471-1481, Jun 2016.

[6]   B. P. McGrath, et al., "Power converter line synchronization using a discrete fourier transform (DFT) based on a variable sample rate," *IEEE Trans Power Electron.*, vol. 20, pp. 877-884., 2005.

[7]   M. S. Reza, et al., "Accurate estimation of single-phase grid voltage parameters under distorted conditions," *IEEE Trans. Power Del.*, vol. 29, pp. 74-80, Feb 2014.

[8]   K. De Brabandere, et al., "Design and operation of a phase-locked loop with Kalman estimator-based filter for single-phase applications," *Proc. IEEE IECON/IECON*, pp. 525-530, Nov 2006.

[9]   Y. Liu, et al., "Signal Frequency Estimation Based on Kalman Filtering Method," *Web of Conferences, International Conference on Computer and Automation Engineering (ICCAE 2016)*, vol. 56, 2016.

[10] S. Golestan, et al., "An adaptive least-error squares filter-based phase-locked loop for synchronization and signal decomposition purposes," *IEEE Trans. Ind. Electron.*, vol. 64, pp. 336-346, Jan 2017.

[11] W. Dai, et al., "A PLL Control Based on Algorithm of BP Neural Network," *CIMSA 2009*, pp. 97-101, May 2009.

[12] M. K. Ghartemani and M. R. Iravani, "A method for synchronization of power electronic converters in polluted and variable frequency environments," *IEEE Trans. Power Systems*, vol. 19, pp. 1263-1270, 2004.

[13] M. Ciobotaru, et al., "A new single-phase PLL structure based on second order generalized integrator," *Power Electronics Specialists Conference 2006*. PESC '06. 37th IEEE, 2006.

[14] Y. Yang, et al., "Benchmarking of phase locked loop based synchronization techniques for grid-connected inverter systems," *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, pp. 2167-2174, 2015.

[15] L. Hadjidemetriou, et al., "A Synchronization Method for Single-Phase Grid-Tied Inverters," *IEEE Transactions on Power Electronics*, vol. 31, pp. 2139-2149, 2016.

[16] F. Xiao, et al., "A Novel Open-loop Frequency Estimation Method for Single-Phase Grid Synchronization under Distorted Conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, Sep 2017.

[17] L. Hadjidemetriou, et al., "A Synchronization Scheme for Single-Phase Grid-Tied Inverters under Harmonic Distortion and Grid Disturbances," *IEEE Transactions on Power Electronics*, vol. 32, pp. 2784-2793, 2017.

[18] H. Ahmed, et al., "Fast Estimation of Phase and Frequency for Single Phase Grid Signal," *IEEE Transactions on Industrial Electronics*, 2018.

[19] O. Krievs, et al., "A PLL Scheme for Synchronization with Grid Voltage Phasor in Active Power Filter Systems," *Electrical, Control and Communication Engineering*, vol. 27, pp. 134-137, 2010.

[20] B. Meersman, et al., "Overview of PLL Methods for Distributed Generation Units," *In Universities' Power Engineering Conference, 45th International, Proceedings,* Cardiff, Wales, UK: Cardiff University, School of Engineering, Institute of Energy, 2010.

[21] P. Aurobinda, et al., "Single Phase Photovoltaic Inverter Control for Grid Connected System," *Indian Academy of Sciences Sadhana*, vol. 41, pp.15-30, Jan 2016.

[22] S. Golestan and J. M. Guerro, "Conventional Synchronous reference Frame Phase-Locked Loop is An Adaptive Complex Filter," *IEEE Transactions on Industrial Electronics,* vol. 62, pp. 1679-1682, 2015.