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Modified Phase-Shifted PWM Scheme for Reliability Improvement in Cascaded H-Bridge Multilevel Inverters

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ABSTRACT The cascaded H-bridge multilevel inverter (CHMI) is a modular structure that consists of many power semiconductor switches. With this increase in the number of power semiconductor switches, it is hard to predict and handle the failure of the devices, and hence reliability of CHMI decreases. The major cause of power semiconductor switch failure is junction temperature that is produced by power losses. The study proposes a multi-carrier pulse-width modulation (PWM) scheme for reduction in switching losses of CHMI. In the proposed modulation scheme, the two legs conduct switching operation at different frequencies for switching reduction. One leg conducts switching operation with high frequency, while the other leg conducts switching operation with fundamental frequency. The switching operations with different frequencies cause unbalanced switching loss to each leg. Therefore, the junction temperature that is based on power losses leads to different life-times for the power semiconductor switch. Additionally, the switching frequency of the two legs is alternated to evenly distribute switching losses and junction temperature. Simulation and experimental results verify the performance of the proposed PWM scheme.

INDEX TERMS Cascaded H-bridge multilevel inverter, phase-shifted pulse-width modulation scheme, reliability of power semiconductor switch, switching loss reduction.

I. INTRODUCTION

Multilevel inverters exhibit various advantages such as decreased blocking voltage of power semiconductor switch, lower total harmonic distortion (THD), and easy maintenance [1]. Therefore, multilevel inverters are used as an alternative to the two-level inverters in medium-voltage and high-power applications such as direct current (DC) distributions, photovoltaic generation, and solid-state transformers [2], [3]. The CHMI exhibits a multilevel inverter topology, and it consists of many cells that correspond to a full-bridge inverter [4]–[6].

Multilevel inverters require a lot of power semiconductor switches when compared to a two-level inverter. However, it is reported that power semiconductor switch is one of the most prone to failures components in power electronics systems [7]. The reliability of a power semiconductor switch is an extremely important issue for improvement reliability in a multilevel inverter [8]. The failure of power semiconductor switches is categorized in two types, namely random failure type that is caused by over-voltage, over-current, or over-temperature [9], [10] and wear-out failure that is caused by thermal stress [11]–[18]. The thermal stress is essentially produced from the power semiconductor switch as a result of power losses. Therefore, the failure of power semiconductor switch can be delayed by decreasing power losses.

The power losses consist of conduction loss and switching loss, and the power losses in CHMI are closely related to its modulation schemes. There are three major modulation schemes of CHMI: phase-shifted PWM (PS-PWM) scheme, level-shifted PWM (LS-PWM) scheme, and nearest level modulation (NLM) scheme [19]. The LS-PWM and NLM schemes provide lower switching loss than PS-PWM scheme, however the switching frequency and conduction time of the cell in CHMI differ from each other. Therefore, the power losses of LS-PWM and NLM schemes are not evenly distributed each cell. The PS-PWM scheme performs the most

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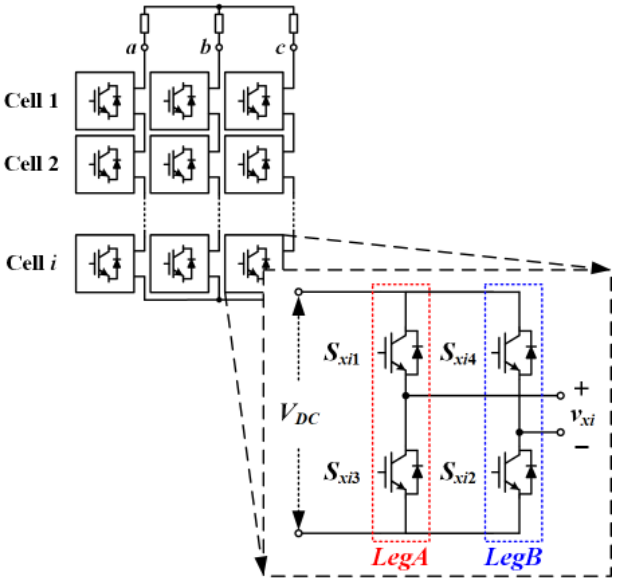


FIGURE 1. Circuit configuration of three-phase CHMI.

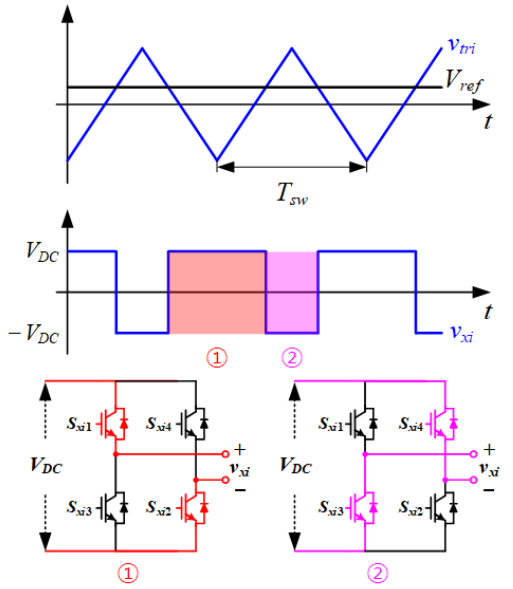
switching operation among three modulation schemes, therefore it leads to the highest switching loss. However, the power losses and delivered power in PS-PWM scheme are balanced by evenly switching operation each cell [20].

This paper proposes a modified PS-PWM scheme that is increased the life-time of power semiconductor switches by decreasing power losses. The number of switching operations are decreased by injecting clamping period in proposed PS-PWM scheme. Therefore, the switching losses of proposed PS-PWM scheme decrease compared to the conventional PS-PWM scheme. Additionally, the proposed PS-PWM scheme provides a balanced junction temperature of all power semiconductor switches by evenly distributing the thermal stress. The simulation and experimental results verify the validity of the proposed PS-PWM scheme in terms of switching loss reduction and thermal balancing.

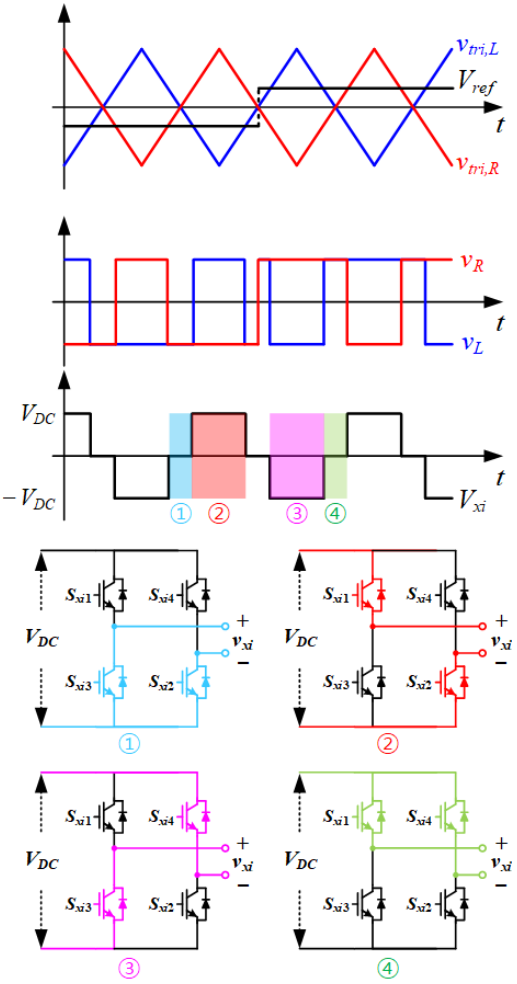
II. CONFIGURATION OF THREE-PHASE CHMI TOPOLOGY

Fig. 1 shows a simplified circuit configuration of a three-phase CHMI topology and cell where S_{xi1}, S_{xi2}, S_{xi3}, and S_{xi4} are power semiconductor switch of i-th cell ($i = 1,2,3,\ldots, N$), x is phase such as a, b, and c. The CHMI is composed by series connection of cells, and it requires many isolated direct current (DC) supplies in which each feeds a cell. The cell is H-bridge inverter that is composed by two legs with two power semiconductor switches in each leg. Generally, the DC voltage of cell (V_{DC}) is fixed although the alternating current (AC) output voltage of cell can be adjusted by either bipolar or unipolar modulation schemes.

Fig. 2(a) shows a set of simplified waveforms of the full-bridge inverter with bipolar modulation method where V_{ref} denotes the reference voltage, v_{tri} denotes the triangular



(a) Bipolar modulation method



(b) Unipolar modulation method

FIGURE 2. Modulation method of full-bridge inverter.

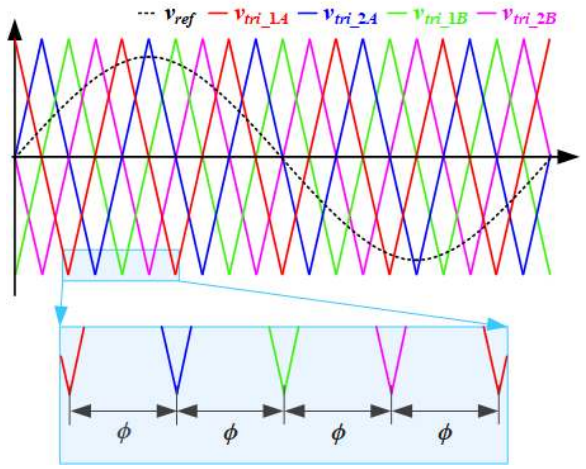


FIGURE 3. The triangular carrier waveform of conventional PS-PWM scheme.

carrier waveform, and v_{xi} denotes output voltage of the x-phase i-th cell. In bipolar modulation method, the two legs in the same cell operate in a complementary manner with one leg turned-on and the other leg turned-off. The turned-on state of leg is turn-on of upper switch and turn-off of lower switch. The turned-off state of leg is turn-on of lower switch and turn-off of upper switch. Therefore, the two legs of the same cell use same triangular carrier waveform and the one cell requires only one triangular carrier waveform. The output voltage of the cell is given in equation (1), and it switches between positive and negative DC voltages of the cell.

$$v_{xi} = V_{DC}\,(s_{xi1} - s_{xi4}) \tag{1}$$

Here, s_{xi1} and s_{xi4} denote the switching functions of power semiconductor switch S_{xi1}, S_{xi4}. The switching function has two value which are '1' or '0' representing the 'turn-on' and 'turn-off' state of each power semiconductor switch, respectively. The switching period of bipolar modulation scheme corresponds to the period of v_{tri} because the switching operations of the two legs are performed simultaneously.

Fig. 2(b) shows the waveform and switching operation of a full-bridge inverter in the unipolar modulation method. The unipolar modulation method requires two triangular carrier waveforms which are phase-shifted with respect to each other. Therefore, the unipolar modulation method generates two gating signals, namely v_R and v_L, which are generated by comparing V_{ref} with $v_{tri,L}$ and V_{ref} with $v_{tri,R}$. It is observed that the switching operation of each legs do independently, which is distinguished from the bipolar modulation method where each leg is switched at the same time. The switching frequency of cell in unipolar modulation method is twice that of the triangular carrier waveform, and thus the output current ripple of cell decreases when compared to that of a bipolar modulation method.

The number of output voltage levels in a CHMI is given as follows:

$$m = 2N + 1 \tag{2}$$

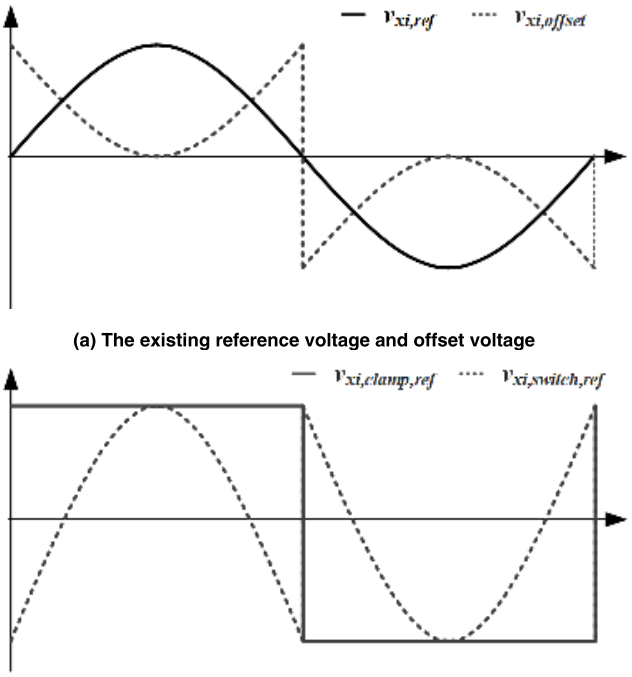


FIGURE 4. The waveforms of proposed PS-PWM.

where N denotes the number of full-bridge cells per phase and m denotes the number of output voltage levels in a CHMI. The higher level of output voltage in CHMI has attractive features, such as reduced dv/dt, smaller filter size and lower THD. However, the higher output voltage level CHMI is required more components, such as power semiconductor switch, gate driver and isolated DC supply. With this increase in the number of components, it is hard to predict and handle the failure of the CHMI. This study applies the proposed modulation scheme to a 5-level CHMI consisting of two full-bridge cells per phase. The outputs of full-bridge cells are powered by each isolated DC supplies V_{DC}, and each cell generates three different output voltages (V_{DC}, 0, $-V_{DC}$) based on the switching state of each power semiconductor switches. The total output voltage of one phase in CHMI is expressed in equation (3) because the cells are connected in series.

$$v_x = \sum_{i=1}^{N} v_{xi} = \sum_{i=1}^{N} V_{DC}\,(s_{xi1} - s_{xi4}) \tag{3}$$

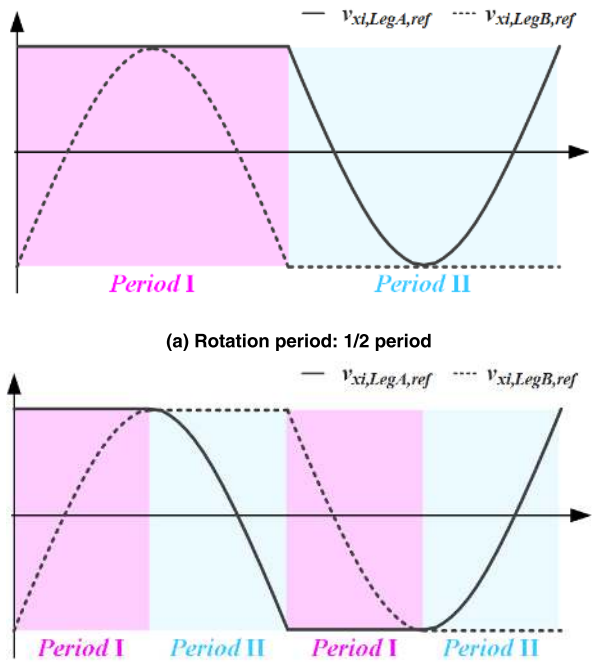
where v_x denotes output voltage of x-phase.

III. MODULATION SCHEME IN THREE-PHASE CHMI

The modulation scheme of CHMI is classified into three schemes, namely NLM, LS-PWM, and PS-PWM. The proposed modulation scheme modifies PS-PWM scheme for decreased power losses. In this section, the conventional PS-PWM scheme and proposed PS-PWM schemes are reviewed.

TABLE 1. Switching state of power semiconductor switches in clamping period.

		Period I		Period II	
		$v_{xi,LegA,ref} > 0$	$v_{xi,LegA,ref} \le 0$	$v_{xi,LegB,ref} > 0$	$v_{xi,LegB,ref} \le 0$
LegA	$S_{xi,1}$	Turn-On	Turn-Off	Switching period	
	$S_{xi,3}$	Turn-Off	Turn-On		
LegB	$S_{xi,2}$	Switching period		Turn-On	Turn-Off
	$S_{xi,4}$			Turn-Off	Turn-On



(a) Rotation period: 1/2 period

(b) Rotation period: 1/4 period

FIGURE 5. The reference voltages of rotation clamped PS-PWM scheme.

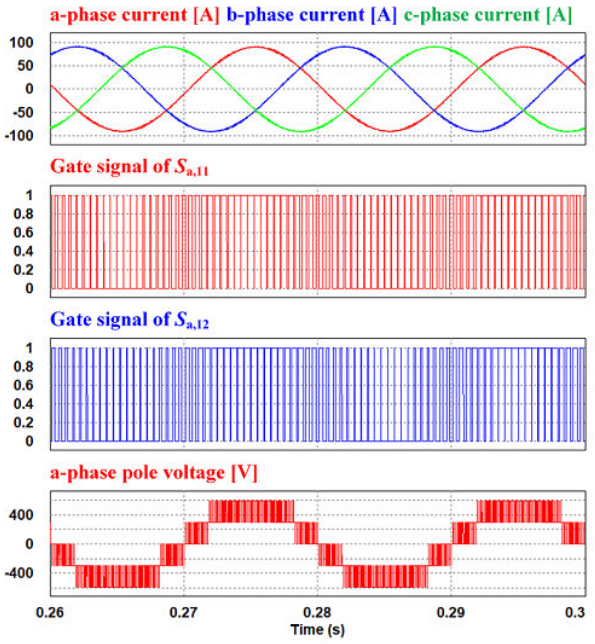


FIGURE 6. Simulation of conventional PS-PWM scheme.

A. CONVENTIONAL PS-PWM SCHEME

The proposed modulation scheme modifies PS-PWM scheme based on unipolar modulation method for decreased power losses, and thus the reference voltages of cells in same phase require only one waveform. Therefore, the reference voltages of three-phase CHMI require three waveforms as expressed in equation (4).

$$\begin{aligned} v_{a,ref} &= V_m \sin\theta \\ v_{b,ref} &= V_m \sin\left(\theta - 120^\circ\right) \\ v_{c,ref} &= V_m \sin\left(\theta + 120^\circ\right) \end{aligned} \tag{4}$$

Here, V_m denote the magnitude of the reference voltages and θ denote angle of the a-phase reference voltage. The reference voltage for each leg in a cell is expressed in equation (5) because the output voltage of each phase is generated by equation (3).

$$v_{xi,ref} = \frac{v_{x,ref}}{N} \tag{5}$$

In contrast to the reference voltages in which all cells of same phase exhibit the same waveform, the triangular carrier waveforms for all cells of same phase have a phase shift between any two adjacent cells. The shifted phase of triangular carrier waveform is expressed in equation (6) and it is determined by the number of cells that constitute the same phase or the level of output voltage. In Fig. 3, it shows all triangular carrier waveforms and reference voltage waveform for one phase of conventional PS-PWM scheme.

$$\phi = \frac{360^\circ}{2N} = \frac{360^\circ}{m-1} \tag{6}$$

The triangular carrier waveforms exhibit the same magnitude and frequency. Therefore, all power semiconductor switches of cells operate at the same switching frequency.

B. CLAMPED PS-PWM SCHEME

The proposed PS-PWM scheme modifies conventional PS-PWM scheme for improved reliability. The proposed PS-PWM scheme injects clamping period into reference voltage. Therefore, two legs of the same cell operate at

TABLE 2. Simulation parameters.

Parameters	Values
The number of cell per phase, N	2 ea
The level of output voltage, m	5 ea
DC voltage of each cell, V_{DC}	300 V
Total DC voltage	600 V
Magnitude of reference voltage	550 V
Switching frequency, f_{sw}	2 kHz
Fundamental frequency of output voltage, f_o	50 Hz
Load resistance	6 Ω
Filter inductance	2 mH

TABLE 3. Experimental parameters.

Parameters	Values
DC voltage of each cell, V_{DC}	30 V
Total DC voltage	60 V
Switching frequency, f_{sw}	10 kHz
Fundamental frequency of output voltage, f_o	60 Hz
Load resistance	10 Ω
Filter inductance	2 mH

different switching frequencies where one corresponds to the frequency of triangular carrier waveform and the other corresponds to the fundamental frequency of output voltage. The modified reference voltage is generated via the existing reference voltage and offset voltage, and the offset voltage is generated via DC voltage of a cell and existing reference voltage. The offset voltage is shown in Fig. 4(a) and is expressed as follows:

$$v_{xi,offset} = \begin{cases} -v_{xi,ref} + V_{DC} & (v_{xi,ref} > 0) \\ -v_{xi,ref} - V_{DC} & (v_{xi,ref} \le 0) \end{cases} \quad (7)$$

The modified reference voltage of cells is expressed in equation (8) and shown in Fig. 4(b).

$$\begin{aligned} v_{xi,clamp,ref} &= v_{xi,ref} + v_{offset} \\ v_{xi,switch,ref} &= v_{xi,ref} - v_{offset} \end{aligned} \quad (8)$$

The switching state of *LegA* in each cell is determined by gating signal that is generated by comparing $v_{xi,clamp,ref}$ with triangular carrier waveform. The number of switching operations in *LegA* are decreased by clamped reference voltage $v_{xi,clamp,ref}$ that injected clamping period. In *LegA*, the witching frequency of power semiconductor switches is frequency of output voltage. Therefore, the switching loss of power

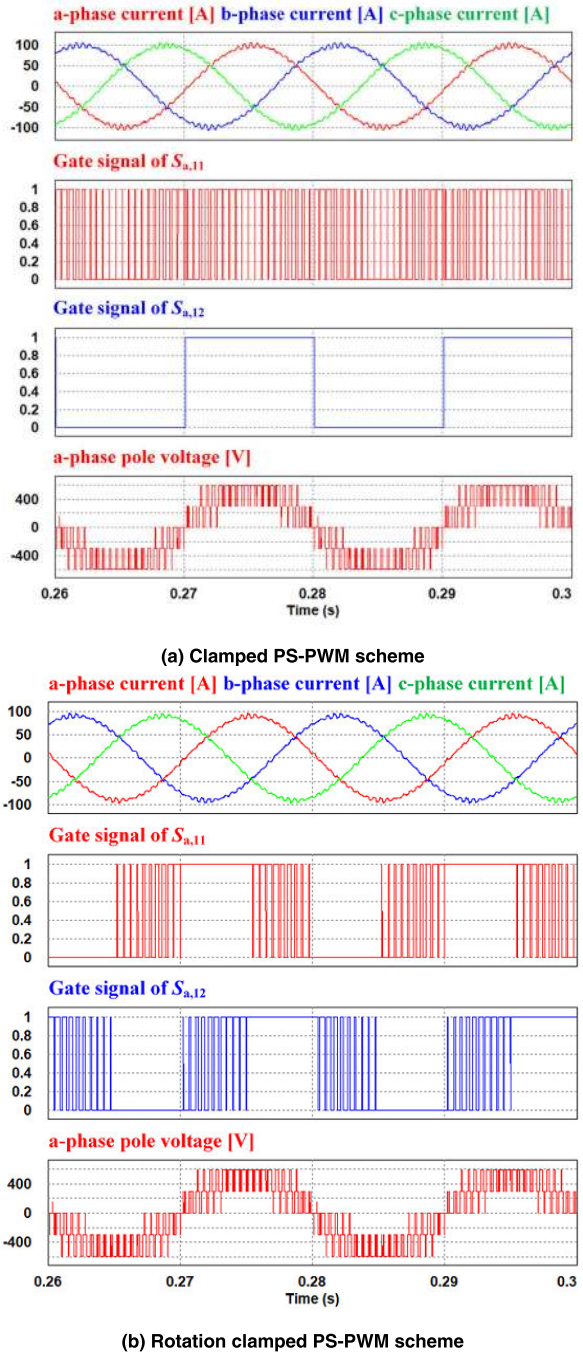
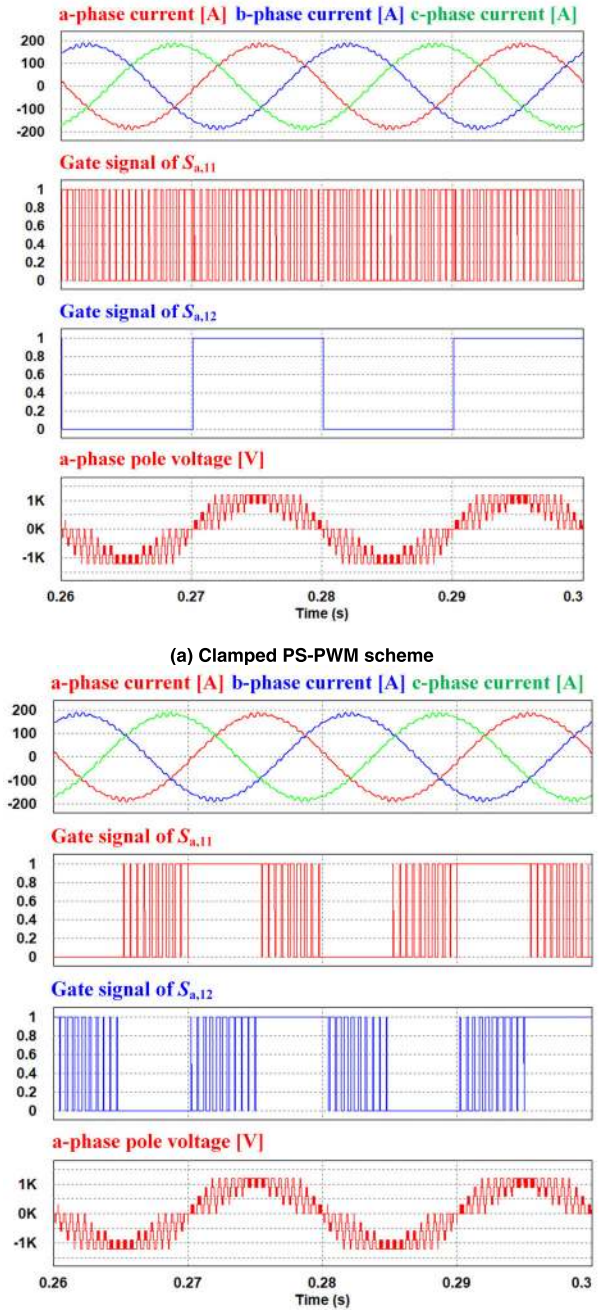


FIGURE 7. Simulation of Proposed PS-PWM scheme in 5-level CHMI.

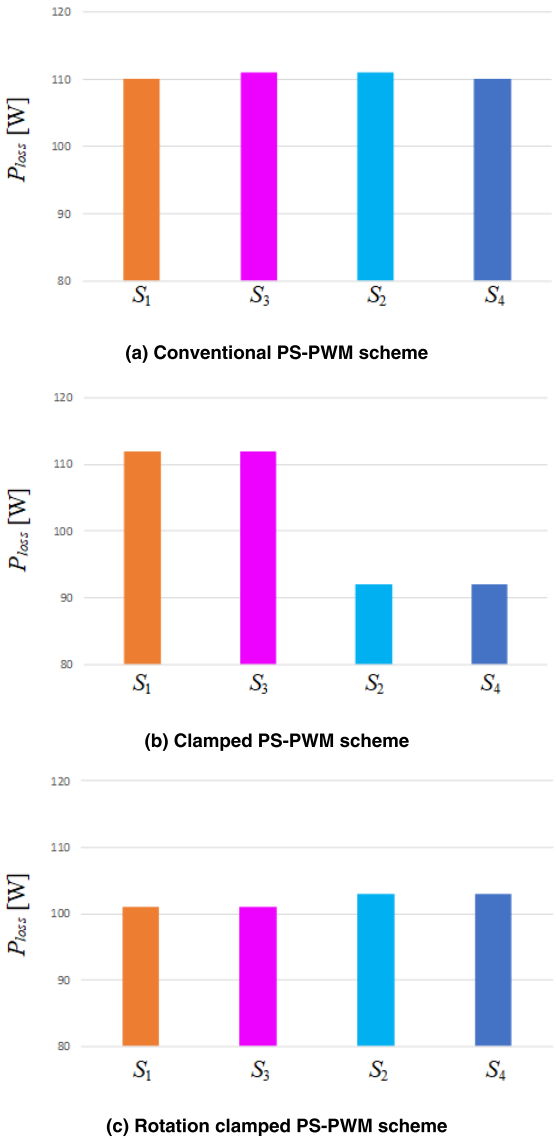
semiconductor switches in *LegA* decreases when compared to conventional PS-PWM scheme. The gating signal of *LegB* is generated by comparing $v_{xi,switch,ref}$ with triangular carrier waveform, and it determines the switching state *LegB* in each cell. Hence, the switching frequency of *LegB* corresponds to the frequency of triangular carrier waveform, and thus the switching loss and operation count is identical to that of the conventional PS-PWM scheme. The life-time of power semiconductor switch is determined by thermal



(a) Clamped PS-PWM scheme

(b) Rotation clamped PS-PWM scheme

FIGURE 8. Simulation of Proposed PS-PWM scheme in 9-level CHMI.



(a) Conventional PS-PWM scheme

(b) Clamped PS-PWM scheme

(c) Rotation clamped PS-PWM scheme

FIGURE 9. Comparison of power loss and its distribution depending on modulation scheme.

stress, and thermal stress is generated by power losses. Therefore, the life-time of power semiconductor switches in *LegA* increases compared to conventional PS-PWM scheme.

C. ROTATION CLAMPED PS-PWM SCHEME

In the clamped PS-PWM scheme, the switching frequency and switching counts differ for each leg of the same cell. Therefore, the switching losses generated by switching operation are different for each leg and it leads to unbalanced thermal stress and life-time. In clamped PS-PWM scheme, the reliability and life-time is improved only power semiconductor switches of *LegA* therefore the reliability of CHMI is identical to that of the conventional PS-PWM scheme. The rotation-clamped PS-PWM scheme applies a rotation scheme to the clamped PS-PWM scheme for even clamping period and power loss of each leg.

Fig. 5 shows the reference voltages of rotation clamped PS-PWM scheme based on the rotation period and Table 1 shows switching state of power semiconductor switches in clamping period. In Fig. 5(a) with 1/2 rotation period, the clamping period of *LegA* is located in only positive period and the clamping period of *LegB* is located in only negative period. Therefore, the turned-on power semiconductor switches are two switches that $S_{xi,1}$ of *LegA* and $S_{xi,4}$ of *LegB*. The power losses of each leg are generated evenly on an average, while the power losses of each power semiconductor switch in same leg are generated unevenly. Hence, the rotation period for

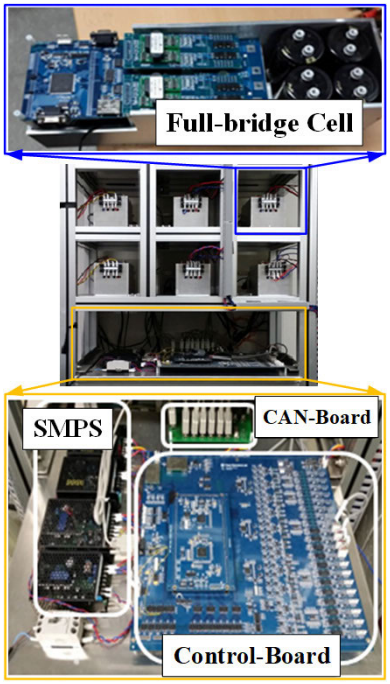


FIGURE 10. 6 kW three-phase CHMI hardware for experimental evaluation.

even power loss distribution should be shorter than 1/4 period as shown in Fig. 5(b).

IV. SIMULATION RESULTS

The simulation is conducted by PSIM to demonstrate the performance by the proposed modulation scheme. The applied circuit of simulation corresponds to the three-phase 5-level CHMI, and the parameters considered are listed in Table 2. The used modulation schemes of simulation correspond to three types of schemes: conventional PS-PWM, clamped PS-PWM, and rotation clamped PS-PWM.

In conventional PS-PWM scheme, all power semiconductor switches of cell exhibit a switching frequency corresponding to the frequency of triangular carrier waveform and they operate evenly as shown in Fig. 6. However, the switching operation of all power semiconductor switches produces significant power loss, and it leads to decreased life-time of CHMI. The simulation waveforms of the proposed PS-PWM scheme to decrease power loss are shown in Fig. 7. In the clamped PS-PWM scheme for decreased power loss, as shown in Fig. 7(a), the switching frequency of *LegB* corresponds to the fundamental frequency of output voltage and not the frequency of triangular carrier waveform. Hence, the power semiconductor switches of *LegB* decreases power loss and increases life-time, while the power loss and life-time of power semiconductor switches in *LegA* are identical to those in the conventional PS-PWM scheme. Fig. 7(b) shows a simulation waveform of rotation clamped PS-PWM scheme in which an additional rotation method is applied to the clamped PS-PWM scheme. As shown in Fig. 7(b), the clamping period for decreased power loss is evenly distributed to

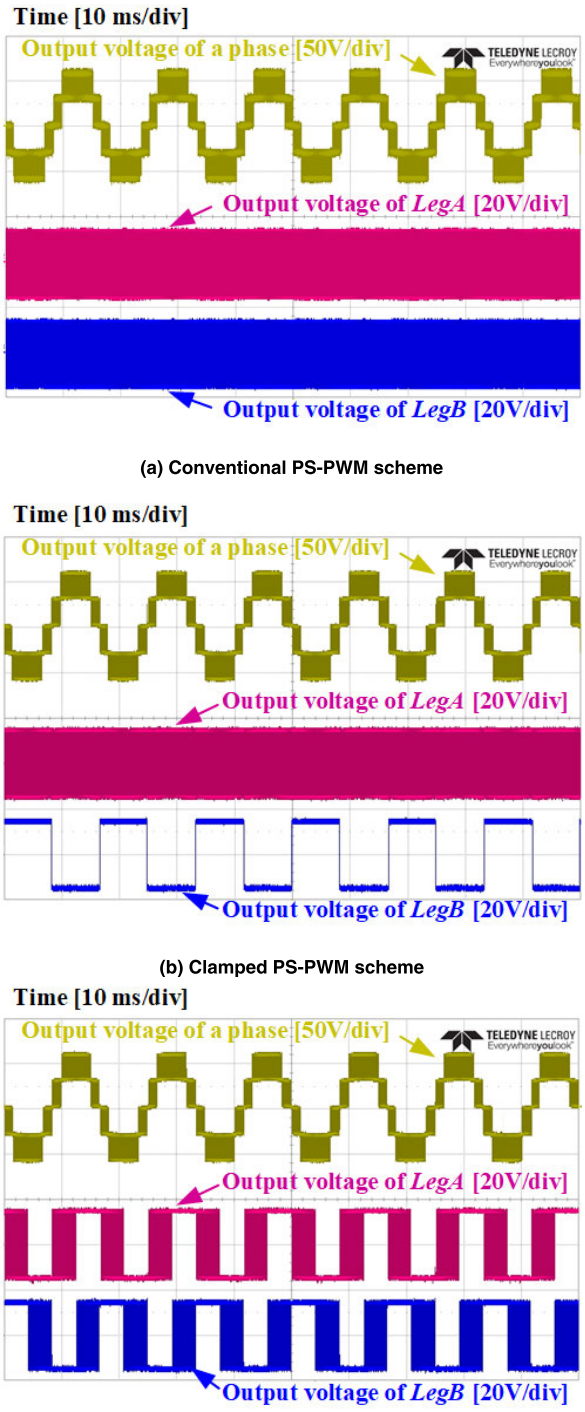
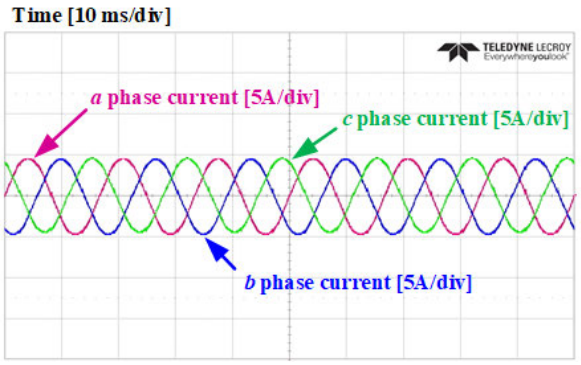
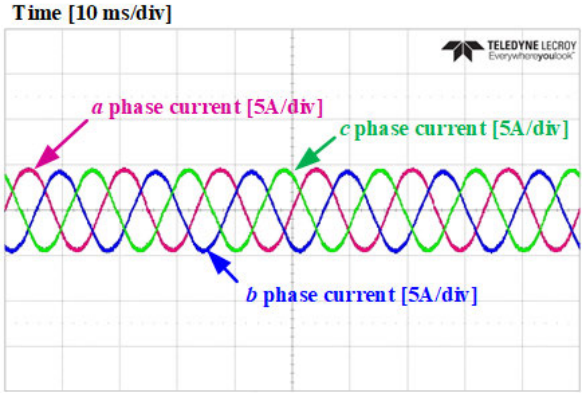


FIGURE 11. Experimental output voltage waveforms during steady state.

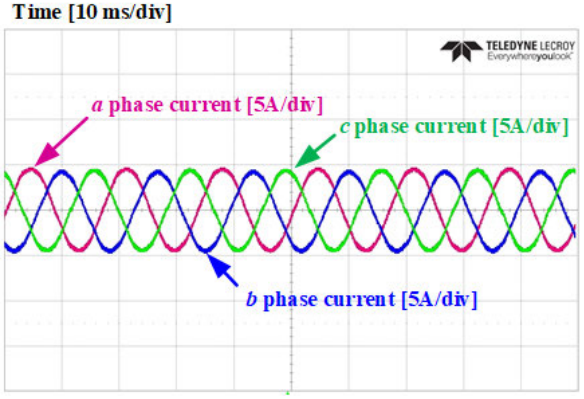
all power semiconductor switches via the rotation method. Therefore, the proposed PS-PWM scheme generates the same output voltages level as that of the conventional PS-PWM scheme while it simultaneously efficiently reduces power loss. To verified proposed method in the higher level CHMI with expanded number of cells, the simulation as shown Fig. 8 is conducted. In Fig. 8, the total DC voltage is 1200 V



(a) Conventional PS-PWM scheme



(b) Clamped PS-PWM scheme



(c) Rotation clamped PS-PWM scheme

FIGURE 12. Experimental output current waveforms during steady state.

and the magnitude of reference voltage 1100 V. The simulation results in higher level CHMI show performance of switching loss reduction that same with simulation results in 5-level CHMI. Therefore, the proposed scheme can be applied the high output level that original purpose of CHMI.

A comparison of power loss depending on modulation scheme is shown in Fig. 9. The power loss of each power semiconductor switch in the conventional PS-PWM scheme is evenly generated as shown in Fig. 9(a). In the clamped PS-PWM scheme as shown in Fig. 9(b), different power losses are generated for each leg via the modified reference voltage. In Fig. 9(c), the power loss each power

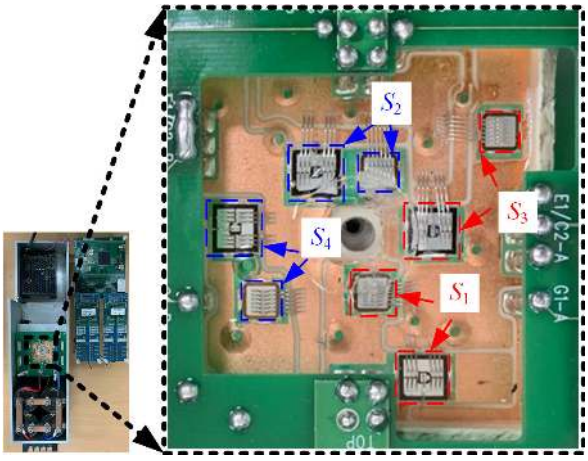


FIGURE 13. Internal structure of the IGBT module and the modified configuration of the cell.

TABLE 4. Experimental of temperature measurement parameters.

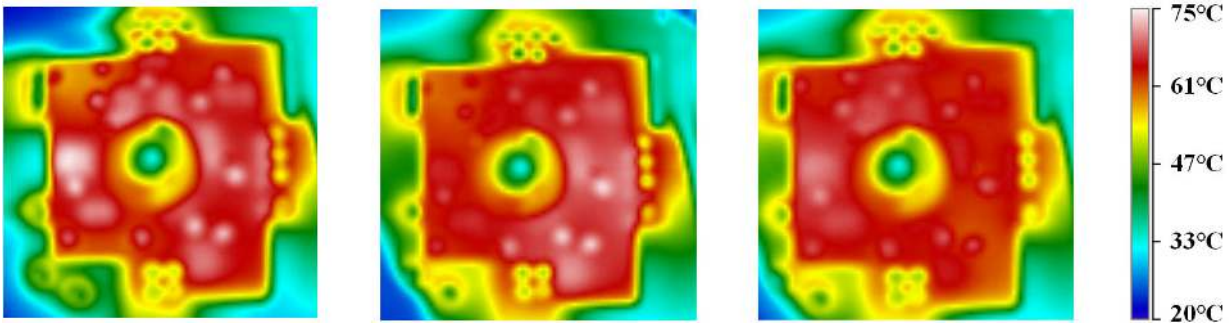
Parameters	Values
DC voltage of each cell, V_{DC}	400 V
Input power, P_{in}	200 W
Switching frequency, f_{sw}	10 kHz
Fundamental frequency of output voltage, f_o	60 Hz
Load resistance	10 Ω
Filter inductance	2 mH

semiconductor switches are generated evenly each leg by rotation method. The total power loss of rotation clamped PS-PWM scheme decreases compared to that of conventional PS-PWM scheme. Therefore, the simulation results represent the appropriateness of the proposed modulation scheme to increase the reliability of CHMI.

V. EXPERIMENTAL RESULTS

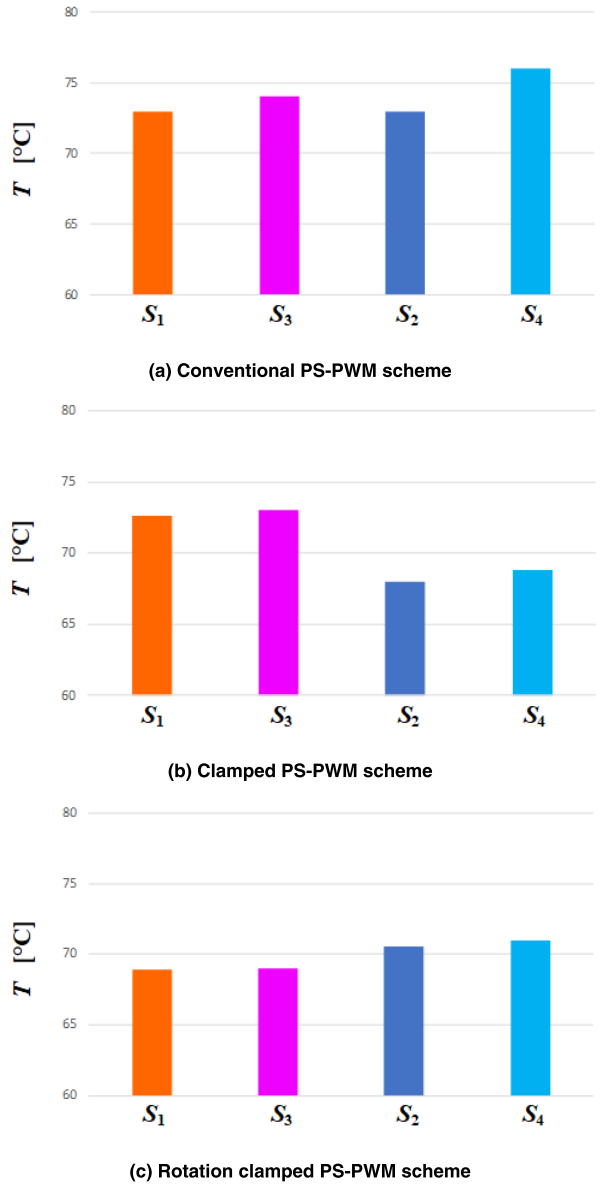
The feasibility of proposed modulation schemes was verified experimentally and Fig. 10 shows the experimental set that the 5-level three-phase CHMI. The experimental parameters are identical to those shown in Table 3. Each cell has an independent DC source of 30 V. This DC voltage source is small for the rated voltage of CHMI, while it is enough to show the switching operation results of the proposed modulation scheme.

Fig. 11 shows the output voltage waveforms of the two types in which one corresponds to the output voltage of phase, and the others correspond to output voltage of legs in the same cell. The modulation scheme of Fig. 11(a) corresponds to a conventional PS-PWM scheme and the switching of all legs operates with a high frequency to output 5-level voltage. The clamped PS-PWM scheme, as shown in Fig. 11(b), and the rotation clamped PS-PWM scheme, as shown in Fig. 11(c), inject clamping period to the output voltage of the leg



(a) Conventional PS-PWM scheme (b) Clamped PS-PWM scheme (c) Rotation clamped PS-PWM scheme

FIGURE 14. Temperature of power semiconductor switches.



(a) Conventional PS-PWM scheme

(b) Clamped PS-PWM scheme

(c) Rotation clamped PS-PWM scheme

FIGURE 15. Comparison of temperatures in power semiconductor switches.

for reduced power losses. Therefore, the power losses of the proposed modulation schemes are efficiently decreased compared to those of the conventional PS-PWM scheme. Fig. 12 shows the three-phase output current waveforms. The application of the proposed modulation method increases the THD of output current because the equivalent switching frequency of output voltage decreases. However, the THD of the proposed modulation method is within 5% when the modulation index is 0.8.

To verify the extended life-time performance of the proposed modulation method, the inner temperature measurement experiment of IGBT module is conducted and the parameters are listed in Table 4. To verified performance of proposed scheme in actual implementation, the DC voltage is set with 400 V which is rated voltage in CHMI. The internal structure of the IGBT module is shown in Fig. 13 and the configuration of the cell should be modified for the convenience of temperature measurement experiment. The inner temperature of IGBT module based on the modulation methods is shown in Fig. 14. As shown in Fig. 14(a), the average temperature of conventional PS-PWM scheme have the highest temperature among three modulation schemes. In clamped PS-PWM scheme as shown Fig. 14(b), the clamped modulation period is only injected to left part of the inside the IGBT module: S_2, S_4. Therefore, the right part in the inside of IGBT module exhibits a higher temperature compared with left part in the inside of IGBT module. In Fig. 14(c), the clamped modulation period is evenly injected to all power semiconductor switches via the rotation method, therefore, the temperature in rotation clamped PS-PWM scheme distribute evenly.

Fig. 15 shows a comparison of average temperature in power semiconductor switches based on the modulation methods. In Fig. 15(a) and (c), unexpected results which is higher temperature of *LegB* than temperature of *LegA* can be generated by hardware factors such as location of power semiconductor switches in IGBT module. In a manner similar to the trend of power loss analysis in simulation results, the temperature of the proposed modulation scheme decreases via a clamped switching operation period. Therefore, the total power losses of rotation clamped PS-PWM scheme lower than total power losses of conventional PS-PWM scheme and the average temperature of the rotation clamped PS-PWM scheme reduce about 4°C compared to the conventional PS-PWM scheme.

VI. CONCLUSION

This paper proposes a modulation method for a 5-level three-phase CHMI to extend the life-time and improve reliability of power semiconductor switches. The proposed method is based on the PS-PWM scheme and decreased power losses via the clamped modulation period. The existing reference voltage waveform is modified into two-type reference voltage waveforms to inject the clamped modulation period. The clamped signal reduces power loss, and other signal is reconfigured to maintain the quality of output waveforms such as the level of output voltage. Reduced power losses decrease the temperature of the power semiconductor switch, and thus the expected life-time of the power semiconductor switch is extended by using the proposed modulation method. Additionally, the proposed modulation scheme considers the power loss balance among the switches in the same cell to improve the reliability of the CHMI. The rotation method with 1/4 period is applied to proposed scheme for even switching loss and temperature among switches. Therefore, the all switches in proposed method are decreased temperature and increased life-time evenly. The performance of the proposed method is verified via simulation and experimental results.

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