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***Abstract* — High voltage direct current grids will require the development of dc protections that provide fast fault isolation and minimize the disturbance caused to the existing ac power networks. This paper investigates how the dc fault recovery performance of a half-bridge modular multilevel converter (HB-MMC) is impacted by different dc protection design choices. A HB-MMC point-to-point HVDC system that is protected with dc circuit breakers (CBs) is simulated on a real time digital simulator (RTDS) using detailed switch models of the converters and switch gear. A dc CB controller has been developed and implemented in a software-in-the-loop fashion, and has been made available free for download. A novel blocking scheme for the HB-MMC is proposed, which limits the prospective dc-side fault current, benefiting dc switch gear. A comparison of circulating current controllers shows that the standard dq controller is likely to be unsuitable for fault studies. Finally, benchmarking shows that a 48% reduction in power flow recovery time and a 90% reduction in the energy dissipated in the circuit breaker can be achieved, along with other benefits, depending on the protection design.**

***Index Terms* — HVDC, RTDS, protection, dc circuit breaker voltage-source converter, modular multilevel, ac grid impact.**

I. Introduction

HIGH voltage direct current (HVDC) grids are seen as a future transmission technology [1]. For this new transmission environment, the question of grid protection has to be revisited; in cases where the dc grid power level exceeds the infeed loss limitations of the ac power network, a dc fault would result in an unacceptable disturbance to the ac grid. HVDC circuit breakers (CBs) have been proposed as a suitable technology to isolate faulted parts of the dc grid [2]. Several industrial prototypes have been developed and a full scale 200 kV CB has been installed [3, 4].

Fault tolerant converters (FTCs) have been proposed to either support the dc switch gear or provide an alternative to dc CBs [5, 6]. However, such converter topologies have yet to be implemented in the power system due to the increased losses that are incurred and the maturity of the technology. While such converter technologies will be suitable in the future, there is still a need to understand how dc CBs will work with the existing converter topologies.

Presently, the preferred topology is the half-bridge modular multilevel converter (HB-MMC). It is important for power system planning to understand how quickly an HB-MMC can recover from dc faults, allowing the impact on the ac grid to be understood. How soon after a fault the pre-fault power flow is re-established, is determined by how quickly the converter's internal voltages and currents return to normal operating levels. This requires detailed models of the internal dynamics of the converter in order to understand the *grid level* limitations.

HB-MMC controls have been investigated for high impedance dc fault conditions where the converter is not required to block [7]. However, large dc-side reactors may result in voltage stability problems for the dc grid [8].

Detailed models of the breakers are required for *protection studies*, as the fault dynamics must be kept within the limitations of the dc switchgear. A *grid level* CB model and an appropriate controller has been developed in [9] based on the first industrial prototype developed by ABB [4]. This model assumes that the commutation process is guaranteed, which is appropriate for *grid level* studies.

However, to reduce dc protection equipment requirements, converters may be controlled to manipulate the dc fault current [6]. Based on the analysis presented in [10], the profile of the dc fault current may negatively influence the commutation process (movement of current between the CB's primary and secondary branches). The profile of the fault current dictates the peak voltage seen across the CB's line commutation switch (LCS) and the time it takes to reduce the primary branch current to zero. LCSs, or similar, appear in at least three industrial prototypes [3, 4, 11].

Therefore, there exists potential for unwanted interactions between converter's controls and CB's operation. For *fault studies*, a model that encapsulates the commutation process is required, and has been developed for this paper. Furthermore, the post fault recovery process has yet to be studied with dc CBs, but similar work can be found in the area of startup procedures [12].

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In protection systems with an open grid dc protection philosophy, or similar, some CBs will reclose soon after opening [13]. The converter and dc protection must ensure that power flow is reestablished quickly after opening and the other protections do not trip during recovery.

In this paper, a point-to-point HB-MMC HVDC system that is protected by hybrid CBs is modeled in a real time digital simulator (RTDS). DC protection options for the converter and CB are compared; circulating current controllers, blocking scheme, and CB fault current limitation (FCL). A combination of these options are benchmarked against *traditional* methods to highlight the potential benefits that can be gained from changing the way the converter and dc protection are operated.

This paper shows that in certain cases, the HB-MMC can limit the prospective dc fault current and be controlled to reduce the energy dissipated in the CBs. It is also shown that the standard circulating current suppressing controller (CCSC), while functional in steady-state and unbalanced grid studies, may not be suitable for *fault studies* and it is recommended that a different circulating current control technique be established for future fault studies.

II. RTDS System Setup

An 800-MVA point-to-point HB-MMC HVDC system is simulated in the first two racks of an RTDS. This switched model of the MMC is based on the average model of the CIGRE benchmark dc test system 1 from Working Group B4.57 [14]. The AC networks are modeled as infinite buses on the grid side of the converter transformers. The PCC is assumed to be on the grid side of the transformers.

Three RTDS racks are used for this work shown in Fig. 1 and the layout of the simulations is given in Fig. 2. Racks 1 and 2 are used to run the MMC switch models, cable models, CB model, and ac power system. Rack 3 simulates the dc CB controllers separately.

Racks 1 and 2 transfer analogue signals to Rack 3 via the AIO connections shown in Fig. 2. Digital signals are passed between the racks using the front panel interface (FPI). Rack 3 reads in the analogue signals from the simulated HVDC transmission system. When the CB self-protection functions are not enabled, only the total fault current (I_{M2}) and primary branch (I_{M1}) currents are required[1]. The controller then makes a decision on which state the CB should be in, based on the analogue inputs, CB control signals, and state of the CB. The control signals are then output to the front panel interface (FPI) and fed into Racks 1 and 2.

III. DC Circuit Breaker Controller

In order to ensure control actions taken by the converter have no negative influence over the dc CB's operation, a detailed switch model of a hybrid dc CB has been used in this paper. The hybrid CB chosen is the proactive hybrid CB [4]. The layout of the model is shown in Fig. 3.

[1] The RTDS CB model, controller, and an instruction manual have been made freely available for download at: http://tinyurl.com/UNSWUOM-UP. *Password:* DCCBPaper

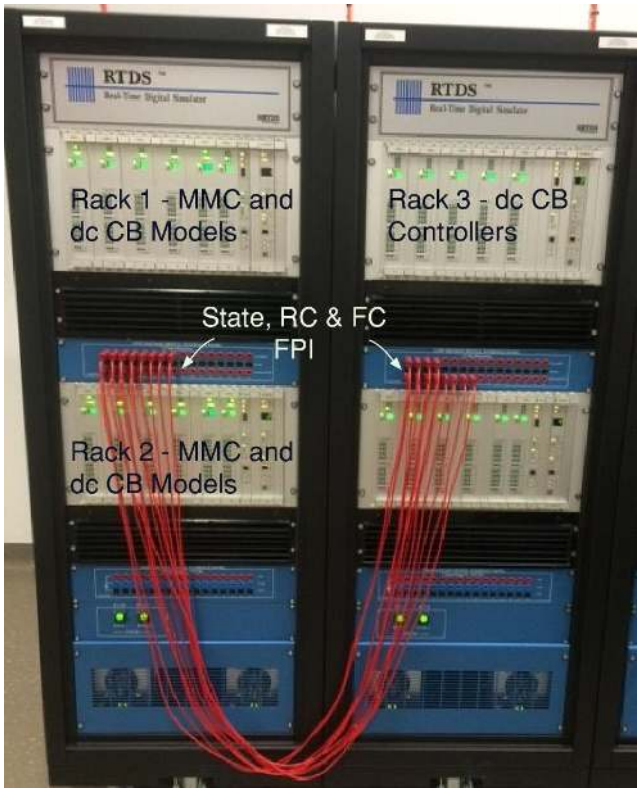

Fig. 1. RTDS system used.

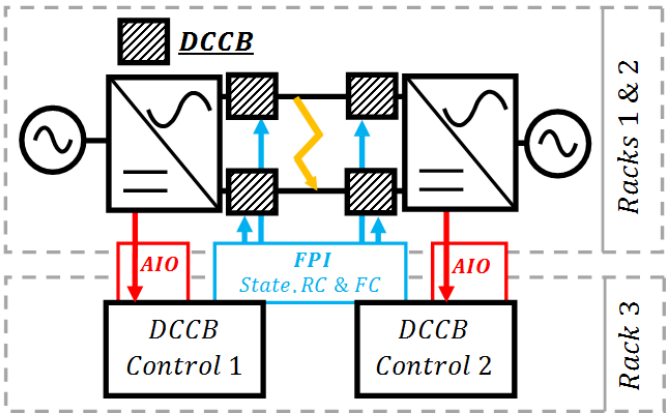

Fig. 2. Layout of RTDS simulations.

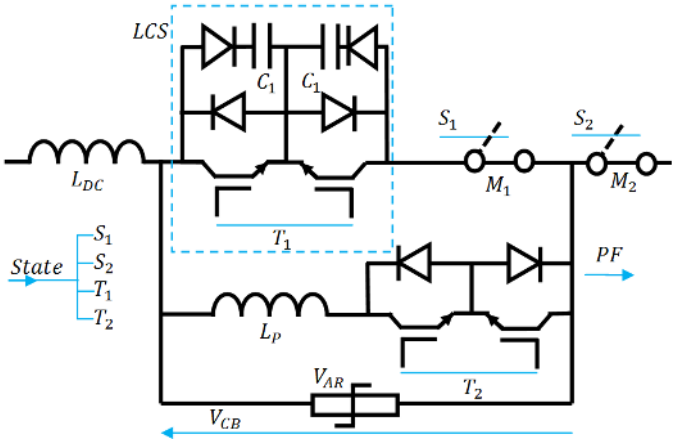

Fig. 3. RTDS proactive hybrid CB model layout[1].

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Power electronic stacks are represented by single switches parameterized with the same electrical characteristics as the required stack. Mechanical switches are modeled with a current chopping limit and minimum opening time. These switches have low impedance until the end of the opening delay time, at which point they *open*.

All hybrid CBs require a series dc-side reactor (L_{DC}), in order to limit the peak fault current they are exposed to[10]. A parasitic inductance (L_P) has been added to the secondary branch in order to obtain realistic commutation time. Based on the hardware results, this time is approximately 250 µs [4]. The LCS' snubber circuit capacitance (C_1) has been modeled to ensure reasonable LCS voltages are maintained during a protection action [10]. The voltage across the CB is limited by the varistor (V_{AR}). Each component has been modeled using the small time step components within RSCAD.

The state of the CB is controlled through a specifically designed RTDS software controller shown in Fig. 4[1]. The user provides settings for the controller and can enable the functions which are desirable for the simulation case. The state diagram for the CB is based on the operation detailed in [4] and reclose procedure in [9]. Each time step the controller makes a decision to either change state or continue to wait for one of the mechanical switches to open. This decision is based on the present state of the CB, analogue inputs from the HVDC transmission system, and CB control signals fault confirm (FC) and re-close (RC). The CB controller also has an open grid (OG) function, which allows the CB's operation to be triggered prior to signal FC becoming true.

This function pushes the current into the secondary branch and opens mechanical switch M_1, when the total fault current exceeds a pre-defined level. The CB does not fully open until the FC signal becomes true. An example of the CB opening procedure is shown in Fig. 5. The CB controller also has an output signal (protection failure or PF) which signals to the user that, due to the power system conditions, the breaker's operation has failed, and what type of failure has occurred. Details of the PF function are given in the controller's instruction manual[1].

The failure modes which can be detected are: LCS over voltage, peak current violation, commutation time violation, tail time violation, and CB overvoltage. A commutation time violation occurs when it takes too long to reduce the primary branch current to zero once the LCS has been turned off. A tail time violation occurs when the varistor is subjected to a pulse of current that is longer than it is designed to handle.

Any failure causes the mechanical switches and LCS to turn on, and T_2 to turn off. This results in an inability of the protection to isolate the fault, while protecting the secondary branch power electronics.

The controller can also have a FCL operation enabled. This feature allows the CB to limit the dc fault current by modulating the secondary branch when mechanical switch M_1 is fully open [4]. An example of the feature is shown in Fig. 6, where the CB recloses while the fault is still prevailing; if the CB reclosed when the fault has been cleared, the FCL function would stop after several *on-off* cycles, depending on the

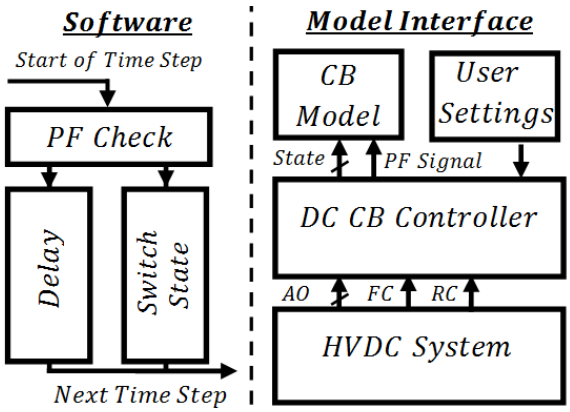

Fig. 4. Layout of DCCB controller code[1].

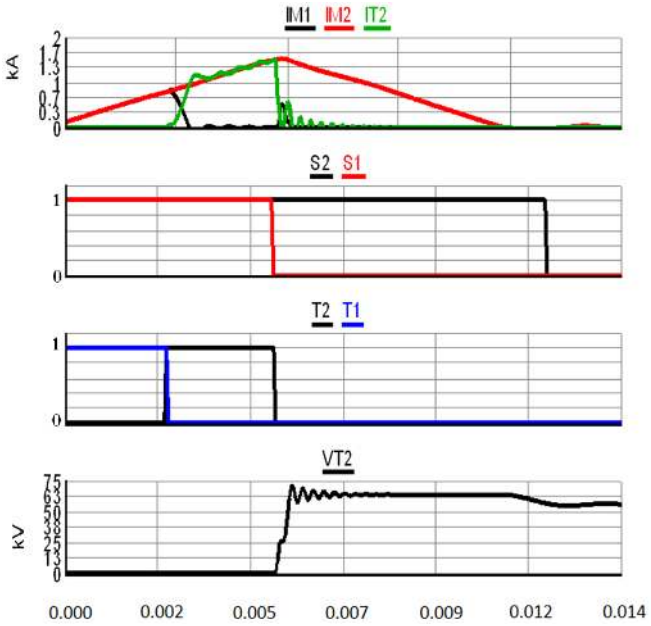

Fig. 5. RTDS results of breaking operation. The CB parameters have been exaggerated to show commutation time and switching events.

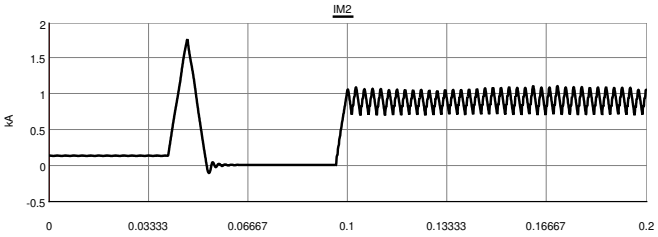

Fig. 6. Simplified system results, showing the CB that opens to isolate section of grid, then recloses onto a fault and behaves as an FCL limiting the current to a maximum of 1 kA.

amount of energy that needs to flow back into the DC grid. The DCCB would not be able to continuously operate as an FCL, due to thermal limitations, as discussed in [4]. The CB turns off the secondary branch to decrease the fault current and recloses the secondary branch once the current is below a preset value. As will be shown in Section VI, this feature can mitigate inrush currents when a CB recloses.

During a normal *restart* of the converter, insertion resistors will be used to limit the inrush of current into the dc network. Unfortunately, these cannot be used when rapidly recovering

from a dc fault as the actuators are far too slow. The FCL operation of the circuit breaker reduces the inrush currents by replicating impedance on the dc side of the converter. This limits the current flow during a rapid recovery.

IV. Blocking Strategy

Typically, once any arm current has exceeded a maximum threshold, all the converter's insulated-gate bipolar transistors (IGBTs) will be turned off. This *blocking* action prevents damage to the IGBTs. The normal type of blocking results in each converter arm behaving as a diode stack. The number of arms conducting at each moment defines the ability of the ac grid to influence the dc fault current, resulting in the ac grid being able to increase the fault current after the converter has blocked [15].

An alternative blocking strategy is proposed in this paper, which provides additional benefits to the dc-side equipment. Rather than blocking all IGBTs once the arm current threshold has been violated, the arm voltage references are set to zero. This turns off all the upper IGBTs (S_U) and turns on all the lower IGBTs (S_L) in each submodule, shown in Fig. 7. This can be done providing the current limit for the lower IGBT is not violated. This *modified* blocking structure effectively prevents the converter acting as a pseudo-rectifier during a dc fault, preventing the ac grid from imposing a significant voltage across the converter's dc terminals.

Fig. 8 shows an equivalent circuit for the MMC when it is experiencing a terminal fault. When the converter is blocked in the *normal* manner, the converter will only present a *short-circuit* to the ac system while all six diode stacks are conducting. During this time, the ac fault currents are not sufficiently large to generate zero crossings in the converter's arms. Eventually, depending on the impedances of the converter and dc network, some arm currents will decay to zero and the converter will start to act as a pseudo-rectifier; where between two and five diodes are conducting. In such configurations, the converter generates a dc-link voltage, which increases the dc fault current.

When the *modified* blocking scheme is used, the arm currents are able to flow in both directions, as the lower IGBTs (S_L in Fig. 7) are turned on in each submodule. This means that even when a zero crossing occurs in a converter arm, the *short-circuit* condition is maintained across the ac terminals of the converter. When the converter's arm inductors and ac grid's impedances are balanced, this results in a net zero voltage across the dc terminals of the converter and the dc fault current decays slowly. If the fault occurs at a distance from the converter, the cable voltage will also influence the dc fault current.

The results in Fig. 9 and Fig. 10 show the *natural* fault current response of the converters for the two blocking methods. In these results, the DCCBs make to attempt to clear the fault. They only show the natural progression of the DC fault current and arm currents. Fig. 9 shows RTDS results for the dc fault current and converter arm currents for a terminal fault for a *normal* blocking scheme.

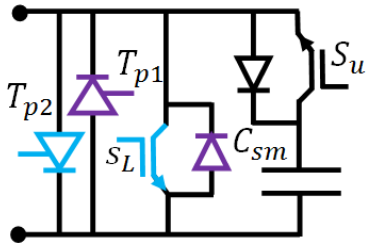

Fig. 7. Submodule architecture.[16]

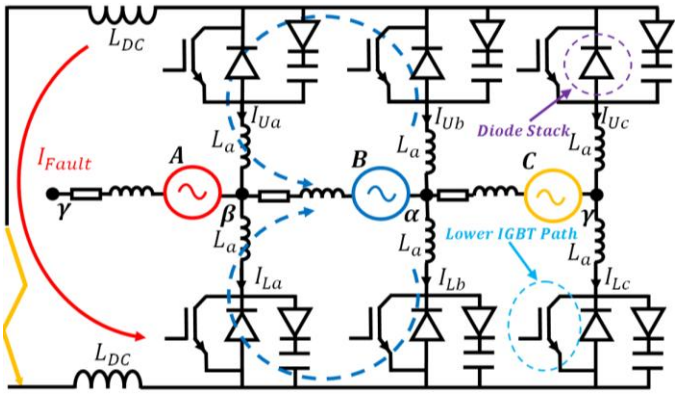

Fig. 8. *Normal* blocking converter equivalent circuit resembles rectifier. *Modified* blocking circuit shown with IGBT paths in each arm. The majority of each phase's current will flow in two arm loops, indicated by dashed lines for phase B. Each diode stack and lower IGBT shown as a single device.

Each arm current is made up of a dc component and an ac component. It can be seen that in the *normal* blocking case the lower IGBT threshold cannot be violated as current cannot flow in this direction within the arms, once the converter is blocked.

For the *modified* case in Fig. 10, because the arm currents become positive (due to the lower IGBT being turned on), the converter no longer acts as a rectifier, hence the dc fault current can be described by:

$$I_{DC\_Mod}(t) = I_{\text{peak}} e^{-\frac{R_{eq}}{L_{eq}}t}, \quad (1)$$

where the equivalent dc side inductance, L_{eq} is given by:

$$L_{\text{eq}} = 2L_{\text{DC}} + \frac{2}{3}L_{\text{a}}, \quad (2)$$

and parasitic resistance, R_{eq} is given by:

$$R_{eq} = 2R_{DC} + \frac{2}{3}R_a. \quad (3)$$

This blocking method reduces the fault current seen by the dc breaker, while increasing the RMS value of the arm currents. As the arm currents are biased down by the dc fault current, the peak positive arm current is lower in magnitude than the peak negative arm current. Providing the ac grid impedance and arm inductances are sufficient to keep the arm currents below the positive arm current threshold, there is no to need to turn off the lower IGBT.

If the current limitation is violated, then bypass thyristors (T_{p2} shown in Fig. 7) used in some HB-MMC modules can be used to support the IGBT in conducting the current. For the example shown, the current limits for TP1 and TP2 are reached 2.6 and 4.4 ms after fault inception.

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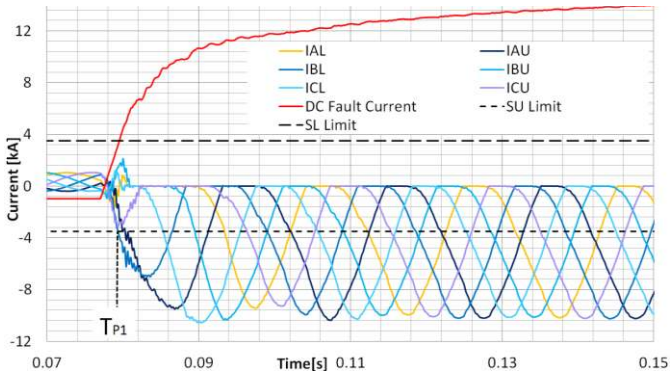

Fig. 9. Natural Fault current and arm currents for *normal* blocking. The upper (SU) and lower (SL) IGBT current limits are plotted.

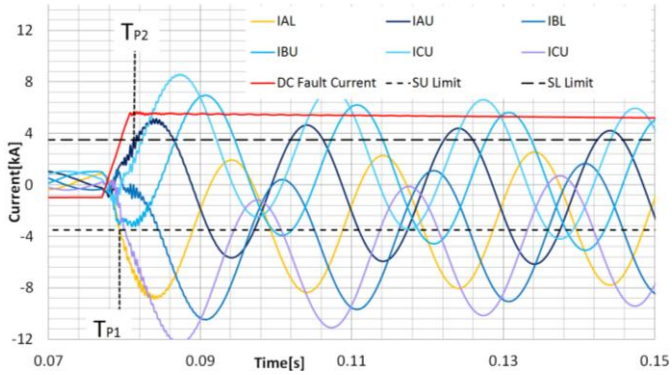

Fig. 10. Natural Fault current and arm currents for *modified* blocking.

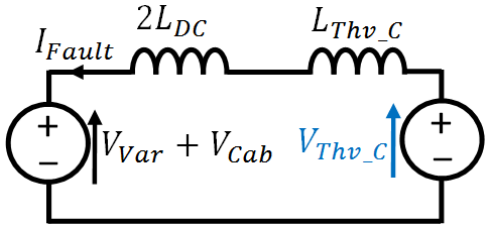

Fig. 11. Equivalent circuit for dc fault current recovery.

The fault *limitation* effect may provide sufficient time for the dc circuit breaker to open before the current limits are reached. The dc current in the *modified* case slowly decays due to the natural RL circuit formed when the ac terminals of the converter are short circuited [17]. This decay is very slow due to the large inductance and low resistance of the circuit.

The benefits for the dc CB current can be clearly seen, as the peak fault current has been reduced, at the expense of increasing the arm currents. Providing this *modified* blocking state can be maintained over the protection period, then the peak fault current experienced by the CB will be determined by how quickly the converter can block, plus any additional impact imposed by traveling waves [18]. For a terminal fault the peak current can be described by:

$$I_{\mathrm{Peak}} = \frac{\mathrm{k_{tw}V_{DC}}}{\mathrm{2L_{DC}}}\mathrm{T_{Blk}} + I_0\,. \qquad (4)$$

$\mathrm{T_{Blk}}$ is the time taken to block the converter from the inception of the terminal fault, which would be less than the operation time of the dc CB. $\mathrm{k_{tw}}$ is a multiplying factor that can be used to compensate for the additional current imposed by the cable voltage [18].

As converter's dc terminal voltage is kept low during a dc fault, when the *modified* blocking scheme is used, this reduces the current pulse requirements for the dc CB's varistor. Fig. 11 shows the equivalent circuit at the moment the dc CB attempts to interrupt the flow of current by turning off T_2. The current pulse width the varistor is subjected to can be estimated by:

$$\mathrm{T_P} = \frac{\mathrm{I_{int}}\left[L_{Thv\_C} + 2L_{DC}\right]}{V_{Thv\_C} - V_{Var} - V_{Cab}}, \qquad (5)$$

where $\mathrm{I_{int}}$ is the current that the circuit breaker attempts to interrupt when turning off the secondary branch, V_{Cab} is the cable voltage, and V_{Var} is the voltage across the varistor. When the converter is blocked in the *normal* method, the converter has a substantial Thevenin equivalent voltage source (V_{Thv_C}). For the *modified* blocking case this Thevenin equivalent voltage is zero, for a balanced system. This also reduces the converter's equivalent impedance (L_{Thv_C}) as there are more parallel paths available for current flow within the converter, both of which reduce the current pulse width.

V. Arm Current Controllers

This section compares two different arm current controllers when recovering from a dc fault. A dc fault represents an abnormal condition for the arm current controllers to operate under. Whichever control strategy is adopted, the dc fault recovery performance will be an important part of the dc protection design. How the arm currents respond during and after a fault, is critical to the recovery profile of the converter.

The power flow recovery time depends on how fast the arm currents can be restored to the normal operating condition. Arm currents of an MMC phase-leg contain i) a dc-component, ii) a fundamental frequency component (corresponding to 50% of the phase current), and iii) higher order harmonic currents which are usually suppressed by the circulating current controller. The two circulating current control methods used in the analysis are the double-frequency rotating reference frame-based circulating current suppressing control (CCSC) [19] and the stationary reference frame-based forced circulating current control (FCCC) [20] shown in Fig. 12.

Both CCSC (in the double-frequency rotating reference frame) and FCCC (in the stationary reference frame) suppress the harmonic currents. Their fundamental difference in the control of the dc component of the circulating current is that FCCC directly defines the dc reference of the circulating current based on the ac-side power (the first loop of Fig. 12 (b)), and in CCSC; the dc-component of the circulating current is naturally defined based on the converter dynamics.

Therefore, FCCC is capable of setting the arm current to the set point defined by the power at point of common coupling with improved dynamic performance. During the power flow recovery, FCCC actively controls the arm current (especially the dc component of the circulating current) in order to provide the desired output power and hence the power flow recovery process is far less oscillatory, recovers the power flow sooner compared to CCSC.

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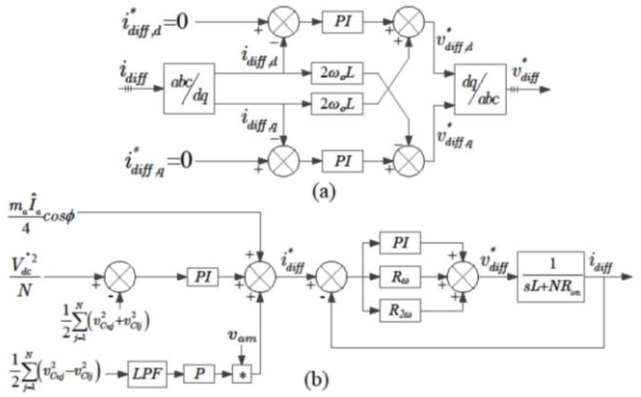

Fig. 12. Circulating current controller (a) CCSC and (b) FCCC.

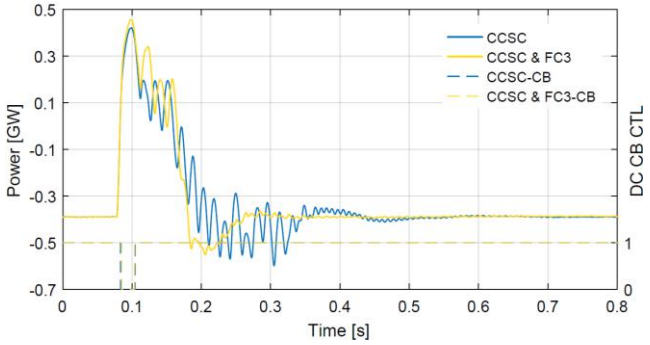

Fig. 13. Real power flow during protective action at PCC.

The arm current controller was changed at the rectifier in each case. For these results, a dc pole-to-pole fault is applied, which is then isolated by the CBs. Once the dc line current has fallen to zero and the fault has been removed, CB starts the re-closure procedure and the converter unblocks and attempts to reestablish the pre-fault power flow. The rectifying converter in each case is consuming 400 MW at unity power factor.

Fig. 13 compares the power flow recovery power at the point of common coupling (PCC), between the two control techniques. It can be seen that when FCCC control is used, the power flow recovery process is far less oscillatory. The power flow also recovers sooner, with a lower overshoot.

The additional oscillations seen in the CCSC power flow recovery are due to the sustained oscillations in the converter's arm currents, shown in Fig. 14. For CCSC the disturbance to the converter exists for a significantly longer period of time, with pre-fault operation not being reached until time 0.5s.

For the FCCC control, the arm currents are still significantly disturbed, but they recover sooner, with pre-fault operation reestablished at 0.35 s in Fig. 13.

Fig. 14 and Fig. 15 show the arm currents, feedback error of the circulating current controller ($\Delta i_{diff} = i^*_{diff} - i_{diff}$), and the output of the circulating current controller, which is the reference voltage within the arms of the converter for the control of the circulating current (v^*_{diff}), for both CCSC and FCCC respectively.

During the transient, CCSC can only track and suppress the second harmonic component of the circulating current while FCCC actively sets a reference to the circulating current. The results show the oscillatory feedback error and output of the

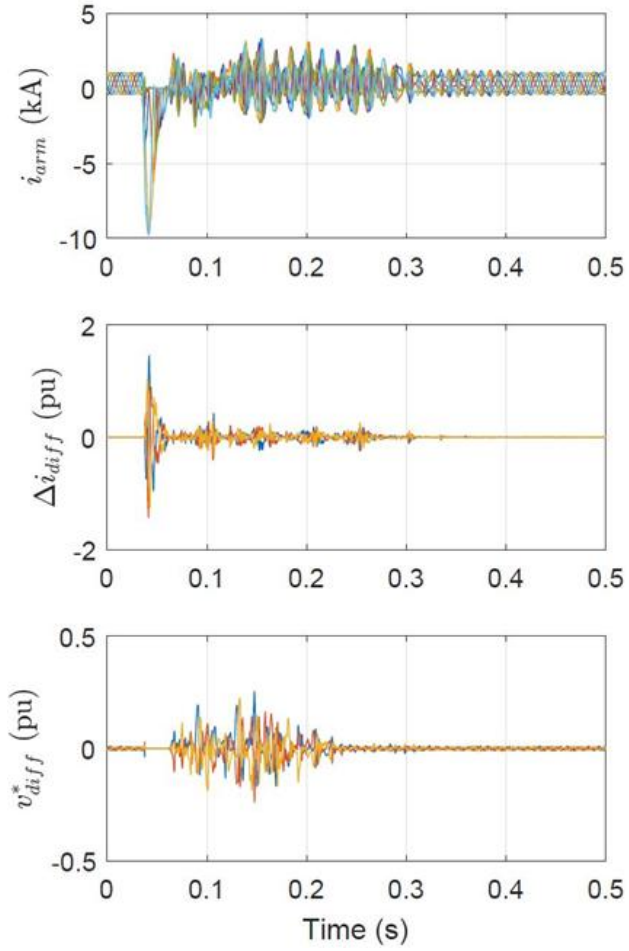

Fig. 14. Converter with CCSC response to dc fault.

CCSC as it does not actively control the circulating current but tries to suppress the harmonics. Results of Fig. 15 for the FCCC demonstrate that the controller feedback error and the output of FCCC contain a dc-transient on top of the oscillations which improves the recovery of the arm currents.

The dc fault transient is a sub-cycle disturbance (≤20ms); however its impact is seen in the converter for a significantly longer period of time. The dc fault is able to influence the converter's operation over this extended time period for two reasons. First, the isolation of a dc fault does not imply zero magnitude arm currents; hence the converter needs to return these arm currents to their desired value. Second, there are no established tuning methods for the HB-MMC that include the influence of the series dc-side inductor (L_{DC}), or attempt to mitigate the impact of the dc fault. There is a clear need to develop tuning methods and requirements for MMCs that are protected by dc CBs.

VI. Benchmark Case Study

Several topics have been discussed to reduce the impact of dc fault transient on the HB-MMC; arm current control, blocking method, and CB FCL. Each of the proposed options has advantages and disadvantages.

In order to highlight these, a benchmark comparison of three different dc protection systems was performed.

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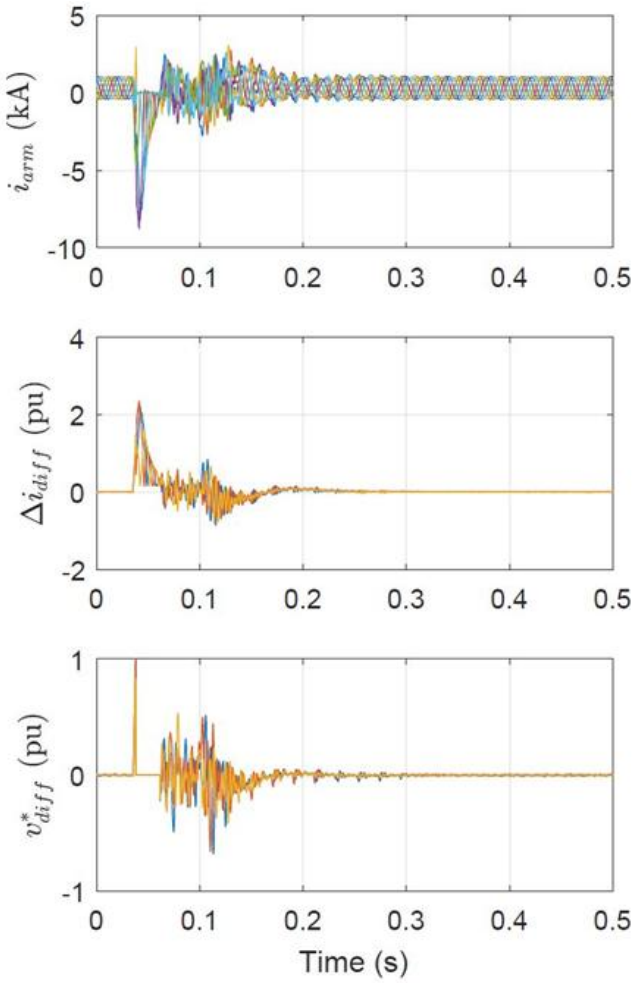

Fig. 15. Converter with FCCC control response to a dc fault.

The three cases chosen are detailed in Table I. The limitations of the dc protection system are given in Table II. Table II and Table I are used to obtain a suitable dc-side inductance value to ensure the peak fault current limit of the dc equipment was not violated.

For each case, assuming a linear increase in current and ignoring any influence traveling waves will have on the fault current, the required series inductance can be estimated as:

$$L_{DC} = \frac{V_{DC}T_1}{2[I_{Max} - I_0]} - \frac{L_a}{3}. \qquad (6)$$

For Case 1, it is assumed that the CB attempts to interrupt the flow of current at time $T_1 = T_{int}$. T_{int} is the time after fault inception that the secondary branch is turned off. For Cases 2 and 3, fault current stops increasing after the converter is blocked in the *modified* manner at time $T_1 = T_{Blk}$. T_{Blk} is the time after fault inception that the converter is blocked, which for these cases was 2 ms.

The FC signal was added to the converter's blocking logic, meaning the converter blocks once the fault is detected. Fault studies were performed using the RTDS setup described in Section II. The MMCs, hybrid breakers and power system are run with a time step of 4.1 µs. The communication between racks and the data conversion (analogue to digital and vice versa) run with a time step of 70µs.

TABLE I
DC PROTECTION SYSTEMS

Case	Arm Current Controller (Inv/Rec)	Blocking Strategy	DC CB FCL	Open Grid
1	CCSC / CCSC	Normal	No	Yes
2	CCSC / FCCC	Modified	No	Yes
3	CCSC / FCCC	Modified	Yes	No

TABLE II
DC PROTECTION PARAMETERS

Attribute	Value
Peak DC Fault Current (I_{Max})	10 kA
Mechanical Switch Opening Time	2.5 ms
Secondary Branch Inductance (L_P)	40 µH
Converter Blocking DC Current	6 kA
Fault Detection Time	2 ms
Open Grid Trigger Current	3 kA
Fault Duration	20 ms
Overvoltage Ratio (V_{Var}/V_{dc})	1.5 pu

TABLE III
PROTECTION SEQUENCE

1	A pole-to-pole dc fault is applied, resulting in an increase in the dc fault current.
2	The converter is then blocked in either the *normal* or *modified* manner, based on either an over current limit being reached or the FC signal becoming true
3	The CB will begin its operation once the open grid trigger current is reached, or once the FC signal is generated by the fault detection system
4	The CB will then isolate the converter from the dc cable and force the dc current to zero.
5	Once the dc fault current has reached zero *and* the FC has fallen to zero (20 ms after fault inception), the CB recloses.
6	Upon reclosing, the CB presents low impedance to the dc network and the converter attempts to re-establish the pre-fault power flow.

The protection action sequence for each case is given in Table III. RTDS results are shown in Fig. 16 to Fig. 18. A comparison of the recovery performance in different areas is given in Table IV.

Fig. 16 shows large differences in the requirements for the dc switch gear for each case. Case 1 presents the highest dc fault current and longest current pulse width in the varistor. Comparing the exact numbers in Table IV, the fault current has been reduced by 2.1 kA and requirements for the varistor in Cases 2 and 3 are one tenth of those seen in Case 1. This is due to the blocking strategy preventing the converter from negatively influencing the decay of the fault current and the reduced dc-side inductance used in Cases 2 and 3.

The interruption time has also been dramatically reduced, predominantly due to the reduction in the varistor current pulse width time. This would allow the CB to reclose sooner if the fault duration was shorter. The peak recovery current seen when the CB is reclosed is higher for the cases which use the *modified* blocking strategy (4.04 kA and 4.06 kA). This is due to the lower impedance condition that the ac network is subjected to with this blocking strategy.

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As the arm currents are larger, when the converter unblocks and the CB recloses, there is an associated larger inrush of current. The recovery current has not been limited with the use of the dc FCL function, however the recovery current oscillations are significantly reduced and giving a more damped response. The real power at the PCC is plotted for each protection case in Fig. 17. The power flow is re-established sooner when FCCC control is used (Cases 2 and 3) and the response does not contain high frequency oscillations, as in Case 1. The power reaches steady state 219 ms sooner than when the FCCC controller is used and the power flow reaches 90% of the post fault power flow level 28 ms sooner.

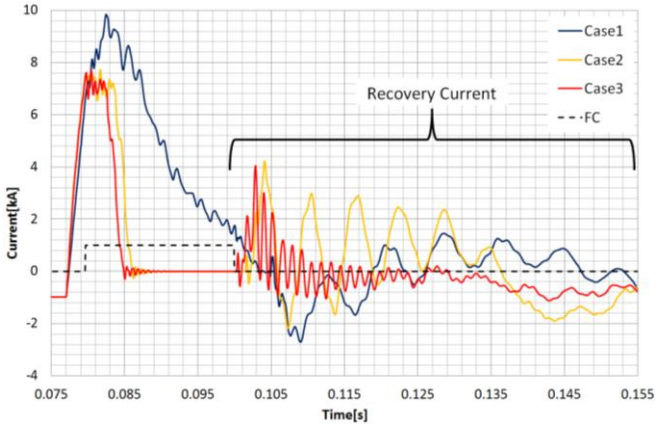

Fig. 16. Comparison of dc fault currents. FC indicates presence of fault.

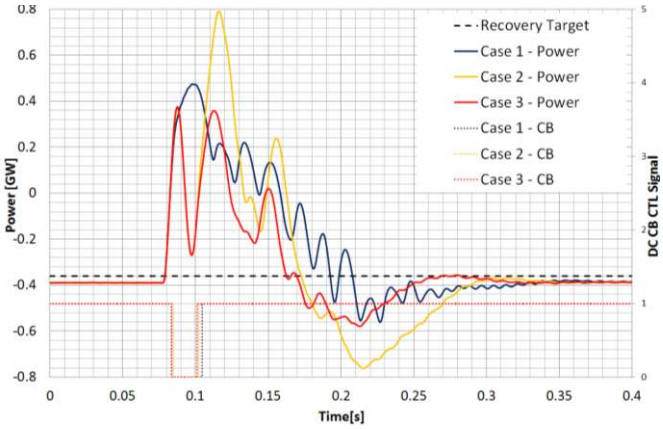

Fig. 17. Power flow recovery at rectifier's PPC. CB CTL shows when CB is open. Recovery target is 90% of pre-fault power flow.

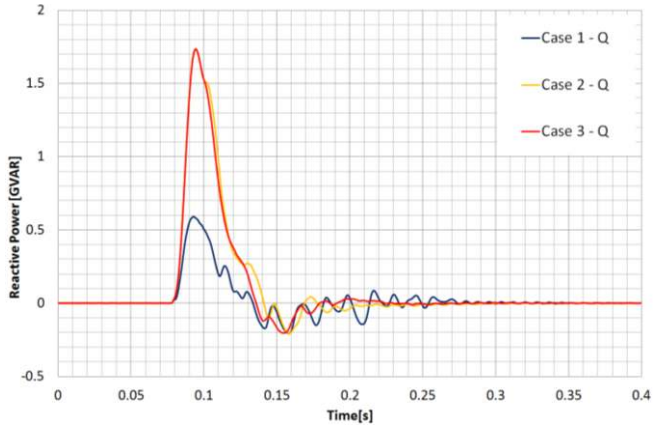

Fig. 18. Reactive power flow recovery at rectifier's PCC.

Table IV
Benchmark Comparison of Protection Cases

Benchmark	Normal	Modified	
	Case 1	Case 2	Case 3
Peak Arm Current (-ve / +ve) [kA]	9.2/3.6	10.2/9.3	9.9/9.3
90% Power Recovery Time [ms]	92.5	64.5	64.5
Power Steady State Time [ms]	454	235	235
Peak DC Current [kA]	9.85	7.72	7.71
Peak Recovery Current [kA]	1.39	4.04	4.06
Varistor Energy [MJ]	25.6	2.256	2.44
Varistor Break Pulse Width [ms]	20.9	2.38	2.66
Pole Inductor [mH]	57	35	35
Isolation Time [ms]	26.95	8.58	8.48
Max Q [GVAr]	0.59	1.73	1.74
Max P [GW]	0.48	0.79	0.38

The swing in PCC power can be reduced if the dc CB operates as a FCL during re-closure, which may have implications for ac grid angle stability.

The power flow at the point of PCC will always see a transient increase in power, due to the increase ac current at the PCC that occurs during a dc fault. For these simulations the PCC is modeled as a strong network, meaning the voltage at the PCC remains constant during this increase in current, which results in a large deviation in power. The phase currents and voltage for Case 1 are plotted in Fig. 19 and Fig. 20.

For weaker ac networks, the voltage at the PCC will collapse and result in a lower amplitude swing in power; both active and reactive. The disturbance a dc fault presents to the ac network will need further investigations, to ensure that the requirements of the ac network can be met; in terms of electrical performance and in interfacing properly with the existing ac protection systems.

The impact this power swing transient has on the converter and transformers ratings will need to be investigated further. Controllers will be able to mitigate some of the power swing after the circuit breaker has reclosed.

Fig. 18 shows that in each case there is a large swing in the reactive power at the PCC. The CCSC control here provides a superior response, as the peak reactive power is lower, potentially resulting in a reduction in ac grid voltage spikes/dips.

The recovery times are based on the time at which the converter permanently recovers 90% of its pre-fault power flow condition and when it settles back to 100% of the pre-fault power or *steady state*. The 90% recovery time is a rough indicator of the impact the protection choice will have an angular stability. The steady state settling time will give an indication of how long the dc fault disturbance will affect the ac grid.

These times give an indication of the type of ac network modeling that will be required to study the impact of a dc fault on the ac network; e.g. electromagnetic or electromechanical.

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VII. Discussion

The three protection cases investigated in Section VI show case various design options for equipment that will form parts of a dc protection system of a multi terminal HVDC system. Case 1 has been developed using *traditional* converter design options. While this may be true for existing HVDC links, once dc CBs are included in the transmission link, there is a fundamental change in the way the converter responds to a fault, and a change in the design specifications. The impact the converter has on the rating of the dc-side equipment must also be considered. This additional consideration may change the design philosophy adopted.

Case 2 shows that moving away from the CCSC reduces the disturbance caused by a dc fault. Further developments in this area are highly likely and specific controllers to mitigate dc faults will be required. This highlights that when performing simulation studies, assuming the converter has a CCSC may not be appropriate, as superior performance may be obtained using other control techniques, which may alter dynamic performance of the converters when modelling at different fidelity levels. There is a need to define a suitable arm current controller for dc fault studies and to understand how this influences the dynamic performance of the converters, and the other modeling levels.

The case studies have shown an alternative blocking method can significantly reduce the requirements for the dc switch gear. Providing the arm currents can be kept to a reasonable value, there is no need to turn on the protection thyristors (T_{P1} and T_{P2} in Fig. 7); increasing the dc side reactor, arm inductors or using fast projection would limit the arm currents during a fault; however the cost of this would need to be considered.

If the protection thyristors are triggered, then the converter may need to wait for a current zero to allow the thyristors to be turned off. This current zero would be required as the thyristors can be latched on, but cannot be forced into the off state; this *may* take up to one ac cycle (20 ms).

That being said, triggering the thyristors may allow for the converter to recover sooner, as the maximum allowable recovery current would be higher, resulting in the energy lost from the dc grid during the fault being recovered sooner.

If the arm currents cannot be kept to a reasonable level and it is undesirable to trigger T_{P1} and T_{P2}, then the converter could be put into the *modified* blocking state just before the CB interrupts the fault current. This would allow for the benefits for the varistors to be obtained, while mitigating against large converter arm currents. There would be no reduction to the peak dc fault current or in series inductance in such a case.

None of the cases are definitively the best options as this is highly dependent on the specific HVDC transmission environment under question. The *modified* blocking strategy clearly has benefits to the dc switch gear, especially for the varistors which are a major limiting technology for HVDC CBs. Advanced MMC will likely provide further benefits to the dc protection equipment and power flow recovery [6].

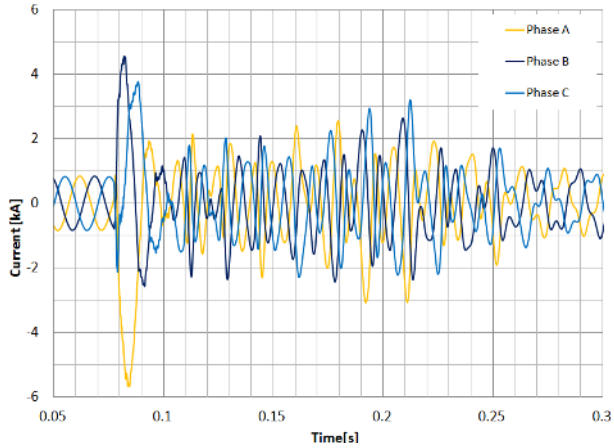

Fig. 19. AC phase currents for Case 1 during fault clearance and recovery.

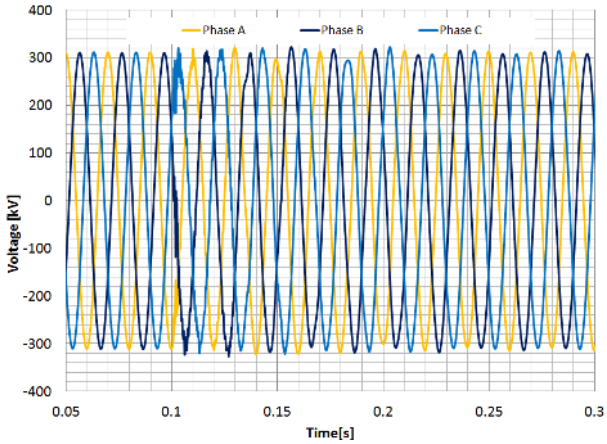

Fig. 20. AC voltages at PCC during dc fault.

The recovery process for an MMC that is protected using HVDC circuit breakers has yet to be established. There are many different options for the hardware, control and supporting circuit breaker technologies. The specific recovery process needs to be assessed in detail for each viable option. This would allow estimations of the recovery time to be made with more confidence, and allow engineers to understand the expected variation in the recovery profile.

The dc fault and how it is managed by the converter and dc protection equipment will change the fault currents that are seen on by the ac protection measurement. Mitigating the impulse of current seen while the fault is cleared, and the following recovery content is an essential piece of research which has yet to be discussed in any detail. An example of what the phase currents look like for a *typical* arrangement is shown in Fig. 19. As these currents exceed normal operational magnitudes and the voltages, shown in Fig. 20, stay fixed, this causes an apparent power spike at the PCC discussed in Section V.

The ac protection settings will need to be designed to mitigate this type of transient, to ensure that both the ac and dc protections do not open during a dc fault. In the event of a dc protection failure, the ac protection will need to act as back up. This may require additional communication between the two protection systems; such as a protection failure indicator being

supplied to the ac protection settings. For all simulations in this paper, it has been assumed that discrimination between ac and dc faults is achieved.

VIII. Conclusion

A point-to-point HB-MMC HVDC system has been implemented in an RTDS, along with detailed switching models of dc CBs. A dc CB controller has been developed in the RTDS environment which allows hybrid dc CBs to be controlled. Any hybrid CB that contains an LCS, or equivalent, in the primary branch may be controlled by this controller, which has been made available for download[1].

The standard CCSC is likely to be unsuitable for HVDC grids that contain dc CBs. Based on this preliminary assessment, fault studies should be performed with a more suitable arm current control method. The arm current controller plays a significant role during the recovery from a dc fault, and will need to be designed to meet the specifications placed on it by the ac grid connection requirements and the limitations of the MMC topology used. In this paper, significant improvements in recovery times have been shown when using FCCC control compared to the CCSC. However, neither of these controllers has been designed to deal with the dc fault.

This paper has shown, for the first time that the HB-MMC is capable of limiting the prospective dc fault current level and capable of supporting the dc CB during opening, using a *Modified* blocking scheme. This modified blocking scheme can be used to prevent pseudo-rectifier operation, just as the double bypass thyristors can [17] [16]. The modified blocking scheme may allow this to be achieved with no additional hardware and may also allow for a faster recovery.

A comparison of different dc protection systems has been made, showing that a 90% reduction in energy dissipated in the circuit breaker, 48% reduction in power flow recovery time, and a reduction in fault isolation times can be obtained through different technology choices. Protection isolation times can be reduced as the converter is able to support the suppression of the dc fault current, but reducing the voltage across its dc terminals. Further discussion has been given in the area of dc protection and where future research may be needed, specifically in developing arm controllers which can limit the power swings and arm currents during recovery.

The case studies show the dc protection system has a dramatic influence on the power flow recovery; both active and reactive swings need to be mitigated in weaker ac networks. The interactions between the dc protection and key ac grid dynamics must be investigated in further detail to establish the impact this will have on the existing ac system.

The impact the dc protection equipment has on the ac protection must also be investigated. DC faults will increase the currents on the ac side of the converters, which may trip ac protections. Selectivity and discrimination must be coherent between the ac and dc protection system, and the ac system must only respond to transients caused by the dc protective action when they are required to. Communication protocols between these protections must be established to develop a system that interface with the existing ac network.

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