Modulation and Circulating Current Suppression for Parallel Interleaved Voltage Source Converters

Gohil, Ghanshyamsinh Vijaysinh

DOI (link to publication from Publisher):
10.5278/vbn.phd.engsci.00054

Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

MODULATION AND CIRCULATING CURRENT SUPPRESSION FOR PARALLEL INTERLEAVED VOLTAGE SOURCE CONVERTERS

BY
GHANSHYAMSINH GOHIL

DISSERTATION SUBMITTED 2016

AALBORG UNIVERSITY
DENMARK

Modulation and Circulating Current Suppression for Parallel Interleaved Voltage Source Converters

Ph.D. Dissertation

Ghanshyamsinh Gohil

Dissertation submitted to Faculty of Engineering and Science at Aalborg University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

February 17, 2016

Dissertation submitted: February 17, 2016

PhD supervisor: Prof. Remus Teodorescu
Aalborg University

Assistant PhD supervisor: Assoc. Prof. Tamas Kerekes
Aalborg University

PhD committee: Professor Francesco Iannuzzo (chairman)
Aalborg University

Assistant Professor Saeedifard Maryam
Georgiatech, School of Electrical
and Computer Engineering

Professor Paolo Mattavelli
University of Padova

PhD Series: Faculty of Engineering and Science, Aalborg University

ISSN (online): 2246-1248
ISBN (online): 978-87-7112-511-5

Published by:
Aalborg University Press
Skjernvej 4A, 2nd floor
DK – 9220 Aalborg Ø
Phone: +45 99407140
aauf@forlag.aau.dk
forlag.aau.dk

Printed in Denmark by Rosendahls, 2016

Dedicated to my mother Pushpa for her endless love and encouragement
and
to my wife Vandana and son Meghdattsinh for their sacrifice and reminding me that there is life outside the office

Curriculum Vitae

Ghanshyamsinh Gohil

The author received Bachelor's degree in Electrical Engineering from the South Gujarat University and received Master of technology degree in electrical engineering with specialization in power electronics and power systems from the Indian Institute of Technology-Bombay, Mumbai, in 2011.

Since May 2013, He has been working towards the Ph.D. degree at the Department of Energy Technology, Aalborg University, Denmark. Prior to joining the Ph.D. studies, he was employed at Siemens Technology and Services, where he was involved in the research activities in the hybrid micro-grid. He also worked on the power quality issues and photo-voltaic converters during his employment at the Crompton Greaves Global R&D Center.

His research interests include parallel operation of voltage source converters, pulsewidth modulation techniques, packaging and the novel topologies for the wide band-gap semiconductor devices, medium voltage dc-dc converters, and energy internet.

Abstract

The two-level Voltage Source Converters (VSCs) are often connected in parallel to increase the current handling capability. In such systems, the multi-level voltage waveforms can be obtained by interleaving the carrier signals of the parallel connected two-level VSCs. The multi-level voltage waveform facilitates reduction in both the switching frequency and the size of the harmonic filter components. This leads to the improvement in both the system efficiency and power density. However, when VSCs are connected in parallel and share the same dc-link, the circulating current flows through the closed path due to the control asymmetry and the impedance mismatch. When the carriers are interleaved, the pole voltages (switched output voltage of the VSC leg) of the interleaved parallel legs are phase shifted and it creates instantaneous potential difference across the closed path, formed due to the parallel connection. This instantaneous potential difference further aggravates the circulating current, which results in increased losses and unnecessary oversizing of the components present in the circulating current path. Therefore, the circulating current should be suppressed to realize the full potential of the carrier interleaving.

The formation of the circulating current path can be avoided by using the line frequency isolation transformer. However, it increases the overall size of the system and should be avoided. The use of the Common-Mode (CM) inductor in series with the line filter inductor for each of the VSCs is proposed in literature. Another approach proposes the use of the Coupled Inductor (CI) to suppress the circulating current by providing magnetic coupling between the parallel interleaved legs of the corresponding phases. Although the interleaved carrier signals lead to the reduction in the value of the harmonic filter components, additional filter components (CIs) are often required to suppress the circulating current. The volume of these inductive components can be reduced by integrating both of these functionalities into a single magnetic component. Different integrated inductor solutions are presented in this thesis with an objective to reduce the overall size of the magnetic component, so that the power density can be further improved or for the given filter size, the switching frequency can be further reduced. The advantages achieved by

the magnetic integration is highlighted by comparing the volume and losses with that of the separate inductor case.

The modulation scheme has significant impact on the core losses in the CI, the harmonic performance, and the switching losses. These performance parameters for the conventional Pulse Width Modulation (PWM) schemes are evaluated and compared. The PWM schemes for the size reduction of the CM and core losses reduction in the CI is also proposed. For the multi-level converter, the Phase Disposition (PD) PWM scheme results in optimal harmonic performance. However it can not be applied to the parallel VSCs in its original form as it may lead to the saturation of the CI. A modified PD modulator is proposed, which ensures flux balancing in the CI, while ensuring the use of the nearest three vectors to synthesize the reference space voltage vector in each sampling interval.

A 3.3 kV medium voltage converter using the two-level VSCs, configured in open-end transformer topology has been studied. An integrated inductor for this topology is also proposed. The multi-objective design optimization has been performed, where the energy loss and the volume are optimized. A non-inferior (Pareto optimal) solution is obtained. The optimization process takes into account the yearly load profile and it is used to minimize the energy loss, rather than minimizing the losses at a specific operating point.

In a dual converter fed open-end transformer topology, each of the VSCs has to process the rated current. In many high power applications, single two-level VSC may not be able to handle the rated current. To overcome this problem, parallel connection of the two-level VSCs for the open-end transformer topology is proposed. Using this topology, both the voltage and the current handling capability of the converter can be increased. The carrier signals of the parallel VSCs are interleaved to improve the harmonic performance. The integrated inductor for suppressing the circulating current between the parallel VSCs and for improving the line current quality is also proposed.

Resumé

To niveau spændingskilde konverterne (VSC) er ofte forbundet I parallel for at øge strømbelastningsevnen. I sådanne systemer kan flere-niveau spændingskurve opnås ved at indflette bærersignalet af de parallelt forbundne to-niveau spændingskilde konvertere. Flere-niveau spændingskurven muliggør reduktion af både switchfrekvensen og størrelsen af de harmoniske filter komponenter. Det leder til forbedring af både systemeffektiviteten og effektdensiteten. For parallelkoblede spændingskildekonvertere, der deler den samme mellemkreds, løber der cirkulerende strøm gennem den lukkede bane pga. kontrol asymmetri og impedans mismatch. Når bæresignalet er indflettet, er polspændingerne (skiftede udgangsspænding af VSCens ben) af de indflettede parallelle ben faseforskudte, hvilket skaber øjeblikkelig potentialeforskel over den lukkede bane dannet af parallelforbindelsen. Denne øjeblikkelige potentiale forskel forværrer den cirkulerende strøm yderligere. Derfor bør den cirkulerende strøm blive undertrykket for at udnytte det fulde potentiale af at indflette bærersignalet.

Dannelsen af den cirkulerende strømbane kan undgås ved hjælp af en grundtone isolations transformer. Men det øger den samlede størrelse af systemet og bør undgås. Brug af en Common Mode (CM) spole is serie med net filter spolen for hver VSC er forslået i litteraturen. En anden metode foreslår anvendelse af en koblet spole (CI) for at undertrykke den cirkulerende strøm, ved at skabe en magnetisk kobling mellem de parallelle indflettede ben af de tilsvarende faser. Selvom de indflettede bæresignaler føre til en reduktion i værdien af de harmoniske filter komponenter, er yderligere filter komponenter (CIer) ofte nødvendig for at undertrykke den cirkulerende strøm. Volumen af disse induktive komponenter kan reduceres ved at integrere begge disse funktionaliteter i en enkelt magnetisk komponent. Forskellige integrerede spole løsninger præsenteres i denne afhandling med en målsætning om at reducere den samlede størrelse af den magnetiske komponent, så effekttætheden kan forbedres yderligere, eller for den givne filter størrelse, kan switchfrekvensen reduceres yderligere. De fordele, der opnås ved den magnetiske integration er fremhævet ved at sammenligne volumen og tabet med det separate spole tilfælde.

Modulationsmetode har betydelig indvirkning på kernetabet i den CI, den harmoniske ydeevne, og switchtabene. Disse resultatparametre for de konventionelle pulsbreddemodulation (PWM) metoder evalueres og sammenlignes. Der foreslås også PWM metoder til størrelsesreduktion af CM strøm og reduktion af kernetab i den CI. For Multiniveaukonverter resulterer fase disposition (PD) PWM metoder i optimal harmonisk ydelse. Dog kan det ikke anvendes på de parallelle VSC'er i sin oprindelige form, da det kan føre til mætning af CI. Der foreslås en modificeret PD modulation, som sikrer fluxafbalancering i CI, samtidig med at brugen af de nærmeste tre vektorer til at syntetisere reference spænding rumvektoren i hvert samplingsinterval.

En 3,3 kV mellemspændingkonverter er, ved hjælp af de to- niveau VSC'er konfigureret i åben ende transformer topologi, blevet undersøgt. Der foreslås også en integreret spole for denne topologi. Mmult-iobjektiv design optimering er blevet udført, hvor energitabet og volumen er optimeret. En ikke-inferiør (Pareto optimal) løsning er opnået. Optimeringsproces tager hensyn til den årlige belastningsprofil, og den bruges til at minimere energitabet, snarere end at minimere tabene i et bestemt arbejdspunkt. I en dobbelt konverter fødet åben ende transformer topologi, skal hver behandle hver af VSC'erne behandle mærkestrømmen. I mange højeffekt applikationer kan en enkelt to-niveau VSC ikke være i stand til at håndtere mærkestrømmen. For at overvinde dette problem, foreslås der parallelkobling af to-niveau VSC'erne for åben ende transformer topologi. Ved hjælp af denne topologi, kan både spænding- og strømhåndteringskapaciteten af konverteren øges. Bæresignalerne af de parallelle VSC'er er indflettet for at forbedre den harmoniske ydeevne. Den integrerede spole er også foreslået for at undertrykke den cirkulerende strøm mellem de parallelle VSC'er og for at forbedre netstrømskvaliteten.

Contents

Curriculum Vitae **v**

Abstract **vii**

Resumé **ix**

Preface **xxi**

I Summary **1**

Summary **3**

1 Introduction 3
1.1 Background and Motivation 3
1.1.1 Applications 3
1.1.2 Overview of the Parallel Interleaved VSCs . . . 4
1.2 Research Objectives and Contributions 14
1.2.1 Research Challenges and Objectives 14
1.2.2 Contributions 15
1.3 Thesis Overview 17
1.3.1 Summary Overview 17
1.3.2 Appended Publications 17
1.3.3 Other Publications 19
2 Harmonic Filter Design 20
2.1 Effect of the Carrier Interleaving 20
2.1.1 Design constraint 21
2.1.2 Filter Design Procedure 23
2.1.3 Comparative Evaluation 24
2.2 High-order Harmonic Filters 25
2.2.1 *LC* Trap Filter 26
2.2.2 *LCL* Filter with *LC* Trap Branch 28
3 Modulation of Parallel Interleaved VSCs 29

3.1 Comparative Evaluation of the Conventional Schemes . 29
3.1.1 Harmonic Performance 29
3.1.2 Core Losses of the Coupled Inductor 31
3.1.3 Switching losses 33
3.2 Size Reduction of the Circulating Current Filter 34
3.2.1 Coupled Inductor 34
3.2.2 Common Mode Inductor 37
3.2.3 Harmonic Performance and Switching Losses . 38
3.2.4 Reduced CM Voltage PWM Schemes 39
3.3 Nearest Three Vector Modulation 43
4 Magnetic Integration 47
4.1 Integrated Inductor 47
4.2 Integrated Inductor for Whiffletree Configuration 50
4.3 Integrated Inductor for Medium Voltage Converters . . 56
4.3.1 Design Optimization 57
4.3.2 Volumetric comparison 59
4.4 Medium Voltage Converters with Parallel VSCs 59
4.4.1 Magnetic Structure of Integrated Inductor . . . 60
5 Conclusions and Outlook 65
5.1 Conclusions 65
5.1.1 Harmonic Filter Design 65
5.1.2 Modulation Scheme 66
5.1.3 Integrated Inductor 68
5.2 Outlook 69
5.2.1 Core Loss Modeling of the Integrated Inductor 69
5.2.2 Modulation 69
5.2.3 Advance Control of the Circulating Current . . 70
References 70

II Appended Publications 79

A Design of the Trap Filter for the High Power Converters with Parallel Interleaved VSCs 81
1 Introduction 83
2 System Description 84
2.1 The Circulating Current 86
2.2 The Grid Current 88
2.3 Modulation Scheme and the Average Pole Voltage . . . 88
3 Design Constraints 89
3.1 Limits on the Injected Harmonics 89
3.2 Peak Switch Current 89

3.3 Active and Reactive Power Consumption of the Shunt Branch . . . 90
4 Filter Design . . . 91
4.1 Trap Filter . . . 92
4.2 Design . . . 93
5 Simulation and Experimental Results . . . 94
6 Conclusion . . . 96
References . . . 97

B Line Filter Design of Parallel Interleaved VSCs for High Power Wind Energy Conversion Systems 101
1 Introduction . . . 103
2 Parallel Interleaved Voltage Source Converters . . . 106
2.1 Modulation Scheme . . . 107
2.2 Voltage Harmonic Distortion . . . 108
2.3 Switch Current Ripple . . . 112
2.4 Ripple Component of the Resultant Line Current ΔI_x . . . 113
3 Line Filter . . . 115
4 Filter Design . . . 117
4.1 Design Constraints . . . 117
4.1.1 Harmonic Current Injection Limits . . . 117
4.1.2 Maximum Switch Current Ripple . . . 118
4.1.3 Reactive Power Consumption . . . 119
4.2 Filter Design Procedure . . . 119
4.2.1 Virtual Voltage Harmonics . . . 119
4.2.2 Required Filter Admittance . . . 120
4.2.3 Selection of the LC Trap Branch Parameters . . . 121
4.2.4 Selection of L_f, L_g and C . . . 121
4.2.5 Comparison with the LCL Filter . . . 125
4.3 Controller Design . . . 126
5 Simulation and Experimental Results . . . 128
5.1 Simulation Study . . . 128
5.2 Experimental Results . . . 130
6 Conclusion . . . 133
A Appendix . . . 134
References . . . 134

C Parallel Interleaved VSCs: Influence of the PWM Scheme on the Design of the Coupled Inductor 139
1 Introduction . . . 141
2 Coupled Inductor . . . 143
3 Pulsewidth Modulation Schemes and their Effect on the Coupled Inductor Design . . . 144

3.1 The Center-aligned Space Vector Modulation 147
3.2 DPWM1: 60°Clamp 148
3.3 DPWM2: 30°Lagging Clamp 149
3.4 DPWM3: 30°Clamp 150
4 Simulation and Experimental Results 152
5 Conclusion 155
References 156

D Modified Discontinuous PWM for Size Reduction of the Circulating Current Filter in Parallel Interleaved Converters 159
1 Introduction 161
2 Parallel Interleaved VSCs 164
2.1 Circulating Current 164
2.2 Flux Linkage in Circulating Current Filter 164
2.2.1 Coupled Inductor 165
2.2.2 Common-mode Inductor 165
3 Switching Sequences and their Effect on the Flux Linkage . . . 166
3.1 Conventional Space Vector Modulation 167
3.2 60°Clamped Discontinuous PWM (DPWM1) 168
4 Modified DPWM for Circulating Current Reduction 169
4.1 Effect of the Switching Sequences on the Circulating Current Filter Design 175
4.1.1 Coupled Inductor 176
4.1.2 Common-mode Inductor 178
4.2 Ripple Current Analysis 179
4.3 Semiconductor losses 181
5 Experimental Results 183
6 Conclusion 189
References 189

E Flux Balancing Scheme for PD Modulated Three Parallel Interleaved VSCs with Coupled Inductor 195
1 Introduction 197
2 PD Modulation of the Parallel Interleaved VSCs and Associated Issues 201
2.1 Operation of the Three Parallel Interleaved VSCs 201
2.2 Coupled Inductor Saturation Under PD PWM 203
3 Modulation Algorithm 205
3.1 Modulation Under Steady-state Conditions 205
3.1.1 Modulation in Band 1 205
3.1.2 Modulation in Band 2 206
3.1.3 Modulation in Band 3 208
3.2 Flux Balancing During Band Transition 208

3.2.1 Band Transition at Bottom Update 209
3.2.2 Band Transition at Top Update 211
3.3 Transition in Other Cases 211
4 Implementation of the Proposed Modulation 213
5 Comparative Evaluation and Results 215
5.1 Simulation Results 216
5.2 Hardware Results 218
6 Conclusion 220
References 222

F An Integrated Inductor for Parallel Interleaved VSCs and PWM Schemes for Flux Minimization 225
1 Introduction 227
2 Integrated Inductor 229
2.1 Simplified Reluctance Model 229
2.2 Line Filter Inductance L_f 231
2.3 Circulating Current Filter Inductance L_c 232
2.4 Flux Linkage in the Common Legs 233
3 PWM Schemes 233
3.1 Conventional PWM Schemes 234
3.2 Reduced CM Voltage PWM Schemes 234
3.2.1 Near State PWM 234
3.2.2 AZSPWM Scheme 235
3.3 Flux Linkage 236
3.3.1 NSPWM 236
3.3.2 AZSPWM 237
4 Assessment of the Line Current Quality 239
4.1 Pulse Patterns 239
4.2 Harmonic Performance 240
5 Design of Integrated Inductor 244
5.1 Design Procedure 244
5.1.1 Value of the Line Filter Inductor 244
5.1.2 Maximum Flux Density in Bridge Legs 245
5.1.3 Maximum Flux Density in Common Legs . . . 245
5.1.4 Maximum Flux Density in Phase Legs 246
5.1.5 Number of Turns and Cross-section Area of the Cores 247
5.2 Comparative Evaluation 247
5.2.1 Coupled Inductor 247
5.2.2 Line Filter Inductor 247
5.2.3 Comparison 248
6 Simulation and Experimental Results 249
6.1 Simulation Study 249

6.2 Hardware Results 252
7 Conclusion 254
References 255

G Integrated Inductor for Interleaved Operation of Two Parallel Three-phase Voltage Source Converters 259
1 Introduction 261
2 Parallel Interleaved Voltage Source Converters 262
3 Integrated Inductor 264
3.1 Magnetic Structure 264
3.2 Simplified Reluctance Model 264
3.3 Line Filter Inductor L_f 267
3.4 Circulating Current Inductor L_c 267
4 Design and Performance Comparison 267
4.1 Maximum Flux Density in Bridge Legs 268
4.2 Maximum Flux Density in Common Leg 268
4.3 Maximum Flux Density in Phase Leg 269
5 Simulation and Experimental Results 270
5.1 Simulation Results 270
5.1.1 Steady-state Considerations 271
5.1.2 Transient Considerations 273
5.2 Experimental Results 275
6 Conclusion 276
References 276

H An integrated inductor for parallel interleaved three-phase voltage source converter 279
1 Introduction 284
2 Integrated Inductor 288
2.1 Magnetic Structure 288
2.2 System Description 288
2.3 Finite Element Analysis 290
2.3.1 Effect of the In-phase Harmonic Frequency Components 291
2.3.2 Effect of the Phase Shifted Harmonic Frequency Components 291
2.4 Equivalent Electrical Circuit 293
2.5 Reluctance Network 294
3 Design and Volumetric Comparison 296
3.1 Pulse Width Modulation Scheme 296
3.2 Maximum Flux Values 296
3.2.1 Common Flux Component 297
3.2.2 Circulating Flux Component 299

3.2.3 Maximum Flux in Various Parts of the Integrated Inductor . . . 300
3.3 Design Methodology . . . 301
3.3.1 Calculation of the Line Filter Inductance L_f . . . 301
3.3.2 Area Product Requirement . . . 301
3.3.3 Core Selection for the Cell and Number of turns 302
3.3.4 Core Selection for the Bridge Legs . . . 302
3.3.5 Air Gap Geometry . . . 302
3.4 Design Example . . . 303
3.5 Volumetric Comparison . . . 304
3.5.1 Three Limb Coupled Inductor . . . 304
3.5.2 Three Phase Line Filter Inductor L_f . . . 304
4 Simulations and Experimental Results . . . 306
4.1 Simulation Study . . . 306
4.2 Hardware Results . . . 307
5 Conclusion . . . 310
A Appendix . . . 310
A.1 Derivation of Circulating Flux Component . . . 310
A.2 Derivation of Common Component of Flux . . . 313
References . . . 314

I Magnetic Integration for Parallel Interleaved VSCs Connected in a Whiffletree Configuration 318
1 Introduction . . . 320
2 Circulating Current in a Parallel Interleaved VSCs . . . 323
3 Integrated Inductor . . . 324
3.1 Magnetic Circuit Analysis . . . 325
3.2 Inductance Offered by the Integrated Inductor . . . 329
3.3 Flux Density Analysis . . . 330
3.3.1 Circulating Flux Component . . . 331
3.3.2 Common Flux Component . . . 332
3.3.3 Flux in the limbs of the cells . . . 333
4 Circulating Current Suppression Between the Two Converter Groups . . . 333
5 Finite Element Analysis and Comparative Evaluation . . . 335
5.1 Finite Element Analysis . . . 335
5.2 Comparative Evaluation . . . 338
5.2.1 Volumetric Comparison . . . 339
5.2.2 Losses Comparison . . . 339
6 Simulation and the Experimental Results . . . 340
6.1 Simulation Results . . . 341
6.2 Experimental Results . . . 342
7 Conclusion . . . 344

References . . . 346

J Optimized harmonic filter inductor for dual-converter fed open-end transformer topology 349
1 Introduction . . . 351
2 Dual-Converter Fed Open-End Transformer Topology . . . 353
3 Integrated Inductor . . . 354
4 Design of the Integrated Inductor . . . 356
4.1 Value of the converter-side inductor L_f . . . 357
4.2 Core Loss Modeling . . . 358
4.2.1 Major Loop . . . 358
4.2.2 Minor Loop . . . 359
4.3 Copper Loss Modeling . . . 360
4.4 Thermal Modeling . . . 361
4.5 Loading Profile and Energy Yield . . . 362
4.6 Optimization Process . . . 362
4.6.1 Step 1: Value of the converter-side inductor L_f 363
4.6.2 Step 2: Derive dependent design variables . . . 365
4.6.3 Step 3: Objective function evaluation . . . 365
4.6.4 Step 4: Air gap length . . . 365
4.6.5 Step 5: Temperature estimation . . . 366
4.6.6 Step 6: Pareto optima solutions . . . 366
4.6.7 Step 7: FEA analysis . . . 366
5 Designed Parameters and Volumetric Comparison . . . 366
5.1 Volumetric comparison . . . 368
6 Simulation and Hardware Results . . . 369
7 Conclusion . . . 371
References . . . 372

K Dual Converter Fed Open-end Transformer Topology with Parallel Converters and Integrated Magnetics 374
1 Introduction . . . 380
2 System Description . . . 382
2.1 Modulation . . . 383
2.2 Harmonic Quality Assessment . . . 383
3 Integrated Inductor . . . 386
3.1 Magnetic Structure of Integrated Inductor . . . 386
3.2 Flux Linking with the Coils . . . 388
3.3 Line Filter Inductor and Circulating Current Inductor . 390
4 Design Methodology . . . 392
4.1 Design Equations . . . 393
4.1.1 Fundamental Frequency Flux Component $\phi_{x_{k,f}}$ 393
4.1.2 Circulating Flux Component $\phi_{x_{k,c}}$ . . . 393

4.1.3 Maximum Flux Value in the Bridge Legs 394
4.1.4 Maximum Flux Value in the Top and the Bottom Yokes 395
4.1.5 Maximum Flux Value in the Common Yoke . . 395
4.1.6 Maximum Flux Value in the Limb 395
4.2 Design Example 396
4.2.1 Integrated Inductor Using Discrete Bridge Blocks396
4.2.2 Integrated Inductor Using Split Windings . . . 399
5 Control Schemes and Performance Evaluation 400
5.1 Control Scheme 400
5.1.1 Active and Reactive Current Control 401
5.1.2 Circulating Current Control 401
5.2 Loss Evaluation 402
5.2.1 Semiconductor Losses 402
5.2.2 Inductor Losses 402
5.3 Comparative Evaluation 404
6 Simulation and Experimental Results 406
7 Conclusion 411
References 411

Preface

This thesis presents the work that author has carried out at the Intelligent Efficient Power Electronics (IEPE) research center at the Department of Energy Technology at Aalborg University. I would like to express my gratitude to all the members of the IEPE and all of my colleagues at the Department of Energy Technology for providing exciting working environment. A special thanks should be given to Prof. Stig Munk-Nielsen and Prof. Marco Liserre for giving me an opportunity to work in the IEPE. Acknowledgments are given to the Innovation Fund Denmark, Obel Family Foundation, Otto Mønsteds Fond, and Department of Energy Technology for their financial support.

I would like to express my sincere gratitude to my supervisor Prof. Remus Teodorescu, co-supervisor Prof. Tamas Kerekes, and former supervisor Prof. Marco Liserre for their valuable guidance and support. I want to thank Prof. Frede Blaabjerg for the constructive discussion and continuous encouragement. Many thanks to Prof. Stig Munk-Nielsen for important technical discussions. A special thank should also be given to my colleague Lorand Bede and former colleague Prof. Ramkrishan Maheshwari for the collaboration.

I articulate my sincere gratitude to Prof. Paolo Mattavelli and Prof. Maryam Saeedifard for their time and effort to evaluate this thesis. Many thanks to Prof. Francesco Iannuzzo for chairing the assessment committee.

I take this opportunity to thank Prof. Philip Carne Kjær for giving me an opportunity to work on a project with Vestas Wind Systems A/S and special thanks to Tune Pedersen and Stig Lund Pallesgaard for giving me an industry perspective on the topic. Bjørn Rannestad from KK Wind Solutions, Paul Thøgersen and Flemming Abrahamsen from PowerCon Embedded A/S also deserve my sincere gratefulness for their valuable feedback and interesting discussions.

I would also articulate my gratitude to Dr. Rafael Peña Alzola for his support during the beginning of my Ph.D. and Dr. Sanjay Chaudhary, Dr. Tushar Batra, Dr. Lajos Török, Dr. Laszlo Mathe, Dr. Huai Wang for our interesting technical discussions. Special thanks to Dr. Francisco Freijedo, Paul

Dan Burlacu, and Catalin Gabriel Dancan for conducive environment in the office and our good time. I also want to thank Casper Vadstrup for helping me with the Danish translation of the abstract. I would like to acknowledge the help I received from Walter Neumayr, Jan Christiansen, Flemming Bo Larsen, Mads Lund, and Frank Rosenbeck. I also want to thank Ann Louise Henriksen, Casper Jørgensen, Corina Busk Gregersen, Tina Lisbeth Larsen, Mette Skov Jensen, and Eva Janik for their help regarding the administrative matters and making my life easy.

I wish to express my sincere gratitude to my mother Pushpa, my wife Vandana, my grandmother Gyanba and other other family members for their love and support. I want to thank my mother for loving me unconditionally and for providing formal and moral education. Sincere gratitude to my aunt Hasuba for raising me like her own son and uncle Pravinsinh for supporting my undergraduate education. I want to thank Vandana for love, understanding, and patience; this thesis would not have been possible without her support. Finally love and many thanks to my son Meghdattsinh for inspiring me to be more curious and for keeping me stress-free.

Ghanshyamsinh Gohil
Aalborg University, February 17, 2016

Part I

Summary

Summary

The extended summary is presented in this chapter.

1 Introduction

The background and motivation is presented in this section. The research questions that are addressed in this thesis are described and the technical contributions are summarized. Finally the structure of the thesis is presented along with the list of the appended papers.

1.1 Background and Motivation

1.1.1 Applications

Voltage Source Converters (VSCs) are widely used in many dc/ac power electronics applications and often connected in parallel to meet the ever increasing demand for the higher power rating converter system [1, 2] in MW-level power electronics applications. Some of these applications are as follows:

- Variable speed motor drives [3–8].
- Wind energy conversion system [9–11].
- Solar photo-voltaic system [12, 13].
- Active power filters [14–17].
- Un-interrupted power supplies [18–24].
- Solid state transformers [25].

The typical Silicon Insulated Gate Bipolar Transistors (Si-IGBT) that are used in such applications suffer from excessive losses if the switching frequency is increased beyond a few kHz. Therefore, the switching frequency is often limited [26]. As a result, large harmonic filter components are required in order to meet the stringent power quality requirements imposed by the

utility [27] in grid-connected applications. These harmonic filter components occupy significant amount of space in the overall system [28]. Moreover, considerable losses occur in the filter components and the overall conversion efficiency is compromised if large filter components are used [26]. They also result in increased cost of the overall converter system [29]. Therefore, the filter size should be made as small as possible to achieve efficient, compact and cost-effective system. In variable speed motor drives, it is highly desirable to reduce the harmonic content in the motor torque, specially for the drives with the lightly damped mechanical loads [7]. The size of the harmonic filter components and the harmonic content in the motor torque can be reduced by increasing the switching frequency and thereby pushing the major harmonic components in the modulated output voltage further away from the fundamental frequency component. However, this leads to more switching losses and the efficiency of the system is compromised. Therefore the efforts are being made to reduce both the size of filter components and the switching frequency. One of the ways to achieve this contradictory requirements is to employ a multi-level VSC.

A three-level neutral point diode clamped (3L-NPC) topology is commonly used [30]. However, an extra control efforts are required to balance the dc-link capacitor voltage [31]. Moreover, the semiconductor loss distribution is unequal [32] and this may lead to the de-rating of the VSC [33]. On the other hand, the two-level VSC is used extensively in many industrial applications due to its simple power circuitry and proven technology. Therefore, it is highly desirable to realize the converter system using the standard Two-Level (2L) VSC. For the parallel connected 2L-VSCs, multi-level voltage waveforms can be achieved by interleaving the carrier signals of the parallel connected VSC legs.

1.1.2 Overview of the Parallel Interleaved VSCs

Harmonic Performance:

The concept of harmonic quality improvement of the parallel connected pulse width modulated VSCs by interleaving the carrier signals has been first proposed in [34, 35]. The interleaved operation of two parallel VSCs and four parallel VSCs had been proposed. The symmetrical carrier interleaving was used where the carrier signals were phase-shifted by 180° in the case of two parallel VSCs (and 90° in the case of four parallel VSCs).

Two parallel voltage source converters are shown in Fig. 1. A carrier signals of both the VSCs are phase shifted by 180°. As a result, the switched output voltages of the parallel VSC legs (referred to as pole voltages) are also phase-shifted, as shown in Fig. 2(a) and Fig. 2(b). The resultant voltage is the average of the individual switched output voltage of the parallel legs of that phase and demonstrates three-level voltage waveforms, as shown in Fig. 2(c).

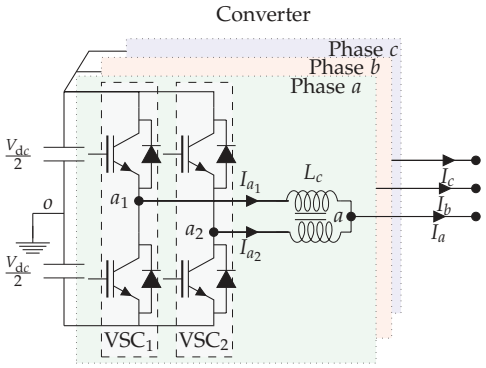


Fig. 1: Two parallel interleaved VSCs proposed in [34].

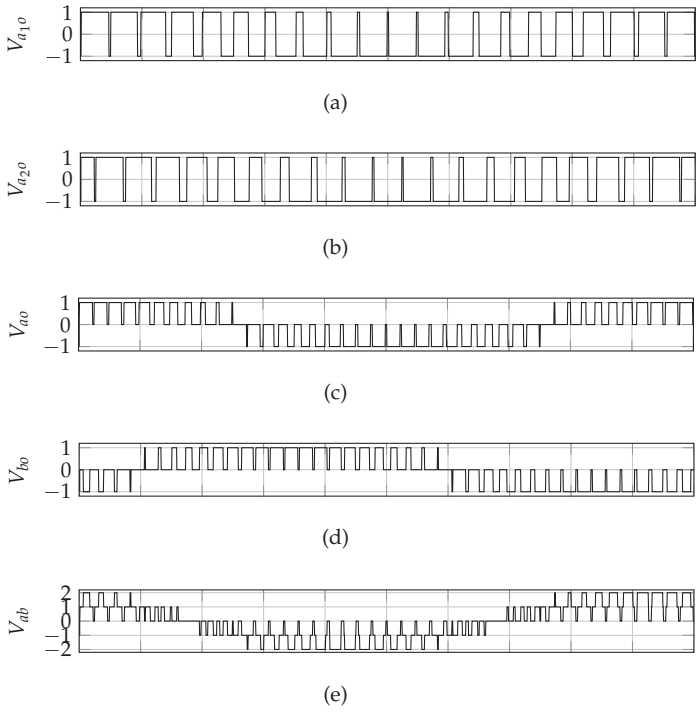


Fig. 2: Simulated voltage waveforms for two parallel interleaved voltage source converters. The carrier signals of the two voltage source converters are phase-shifted by 180°. (a) Switched output voltage of leg a_1, (b) Switched output voltage of leg a_2, (c) Resultant voltage of phase a, (d) Resultant voltage of phase b, (e) Line-to-line voltage V_{ab}. The voltage waveforms are normalized with respect to $V_{dc}/2$.

The line-to-line voltage across the phase a and phase b is also shown in Fig. 2(d). It demonstrates five-level voltage waveforms. As a result, compared to the 2L-VSC, superior harmonic performance can be achieved.

The harmonic performance for the sine triangle Pulse Width Modulation (PWM) has been investigated in [34] and it is demonstrated that for the two parallel interleaved VSCs, the carrier frequency harmonic component and its side bands can be significantly reduced in the resultant switched output voltage. Moreover, the carrier interleaving also reduces the harmonic content in the dc-link current and Common-Mode (CM) voltage [36]. So far in these studies the effects of the symmetrical interleaving were investigated. The impact of the asymmetrical interleaving angle on the harmonic performance has been investigated in [37, 38]. The concentration of the harmonic energy also depends on the modulation index and it is shown that for two parallel VSCs, modulated using the continuous Space Vector Modulation (SVM), the harmonic energy is concentrated more around the 2nd carrier frequency component for the low modulation indices. On the other hand, for the high modulation indices, the harmonic energy is concentrated around the 1st carrier frequency component [39]. Based on this findings, depending upon the modulation index, use of two different interleaving angles was proposed (interleaving angle of 90° for low modulation indices and 180° for high modulation indices). In the case of the 60° clamped discontinuous PWM (commonly referred to as DPWM1 [40]), irrespective of the modulation index, the harmonic energy is concentrated more around the 1st carrier frequency and the use of the interleaving angle of 180° was recommended. Similar conclusions were drawn in [41], where the analysis has been performed using rms grid current ripple in the synchronously rotating dq reference frame. The impact of the asymmetrical interleaving angle on the dc-link current has been also investigated in [42].

The optimal PWM scheme to improve the harmonic performance of the parallel 2L-VSCs under the Phase-Shifted (PS) PWM is presented in [43]. The effect of the combination of the several switching sequences and the different phase-shift angles between the carrier signals on the harmonic quality is investigated and optimal combination has been identified for all possible values of the reference voltage space vector having magnitude $|V_s^\star|$ and angle ψ_s. This information is then used to select the optimal combination of the switching sequences and the phase-shift during each sampling interval. Several combinations of the switching sequences and the phase-shift are used in one fundamental cycle. This would substantially increase the complexity and make it mere difficult to implement. Moreover, the Coupled Inductor (CI), that is used to suppress the circulating current, could saturate during the transition from one combination to another.

The enhanced modulator for the parallel interleaved 2L-VSCs is proposed in [44]. It uses two sets of the evenly phase-shifted carrier signals that are dy-

namically allocated using multiplexer, which makes it difficult to implement. Moreover, this implementation is equivalent to the Phase-Disposition (PD) PWM and CI saturation during the band transition could still happen. The PD carrier modulation scheme for the two parallel VSCs is presented in [45]. It uses a state machine to select the switching states. However, the complexity in this case increases with the increase in the number of parallel VSCs. The strategy to avoid the CI saturation during the transition from the positive value of the command reference signal to the negative value and vice-versa has been proposed for the two parallel VSCs. However, it does not ensure volt-sec balance to synthesize the reference space voltage vector during the band transition and introduces a disturbance in the line-to-line voltage of the three-phase system, which is highly undesirable. A PWM scheme overcome this problem has been presented in this thesis.

The interleaving of the carrier signals improve the harmonic performance. However, it is important to evaluate the reduction achieved in the value of the harmonic filter components to quantify the advantages of the carrier interleaving. The reduction in the value of the line filter inductor for the active power filter application has been investigated in [15] and it is shown that 70% reduction can be achieved with two parallel interleaved VSCs. Another study [39] shows 60% reduction in the weight of the magnetic component for the variable speed drives, considering the DO-160E Electro-Magnetic Interference (EMI) limits as a design constraints. The reduction in the weight of the EMI filters for the variable speed motor drive application has been also investigated in [46]. However, in most grid-connected applications, the impact of the interleaving on the harmonic filter components is so far not reported and it is investigated in this thesis.

Circulating Current:

When VSCs are connected in parallel, the circulating current flows between the VSCs due to the control asymmetry and the impedance mismatch. When the carriers are interleaved, the switched output voltages of the interleaved parallel legs are phase shifted. As a result, the instantaneous potential difference exists, as shown in Fig. 3. This instantaneous potential difference further increase the circulating current, which would result in increased losses and unnecessary over-sizing of the components present in the circulating current path. Therefore, the circulating current should be suppressed to realize the full potential of the interleaved carriers in parallel connected VSCs.

The use of the CI to suppress the circulating current is proposed in [34, 35, 47, 48] (referred to as a interphase reactor in [34]) and also shown in Fig. 1. The physical structure of the CI is shown in Fig. 4. The subscript x represents the phases a, b, and c ($x = \{a, b, c\}$). The core is made up of two limbs which are magnetically coupled to each other using the top and the bottom yokes. Both the limbs carry coils with the N number of turns and

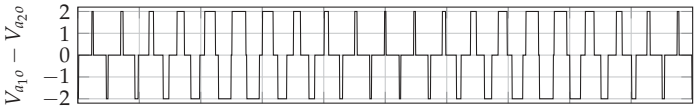


Fig. 3: Difference of the switched output voltages of the parallel legs. The voltage waveforms are normalized to $V_{\mathrm{dc}}/2$.

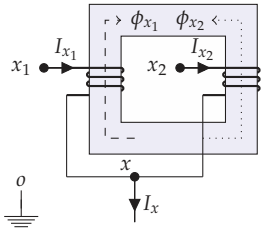


Fig. 4: Physical arrangement of the Coupled inductor. Subscript x represents the phases a, b, and c.

the coils are wound in the same direction. The starting terminals of both the coils are connected to the output of the respective VSC legs x_1 and x_2 and other terminals of both of the coils are connected together to form common connection point x, as shown in Fig. 4. The voltage across the coils are given as

$$V_{x_1x} = R_{CI} Ix_1 + L_s \frac{dI_{x_1}}{dt} - L_m \frac{dI_{x_2}}{dt} \tag{1a}$$

$$V_{x_2x} = R_{CI} Ix_2 + L_s \frac{dI_{x_2}}{dt} - L_m \frac{dI_{x_1}}{dt} \tag{1b}$$

where L_s is the self-inductance of the coil, L_m is the mutual inductance between the coils x_1 and x_2, and R_{CI} is the resistance of the coil. The mutual inductance can be represented as $L_m = kL_s$ $(0 \leq k \leq 1)$. Using (I.2), the difference of the pole voltages of the corresponding phase is given as

$$V_{x_1o} - V_{x_2o} = R_{CI}(I_{x_1} - I_{x_2}) + (L_s + L_m)\frac{d}{dt}(I_{x_1} - I_{x_2}) \tag{2}$$

For the parallel VSCs, the leg current can be decomposed into two components

- Common current component ($I_x/2$, assuming equal current sharing).
- Circulating current component $I_{x,c}$.

therefore, the leg currents can be represented as

$$I_{x_1} = \frac{I_x}{2} + I_{x,c} \text{ and } I_{x_2} = \frac{I_x}{2} - I_{x,c} \tag{3}$$

obtaining $I_{x,c}$ from (J.2) and substituting in (2) yiels

$$V_{x_1o} - V_{x_2o} = 2R_{CI}I_{x,c} + 2(L_s + L_m)\frac{dI_{x,c}}{dt} \tag{4}$$

similarly, taking the average of the pole voltages of the respective phases of both the VSCs gives

$$\frac{V_{x_1o} + V_{x_2o}}{2} = V_{xo} + \frac{R_{CI}}{2}I_x + \frac{(L_s - L_m)}{2}\frac{dI_x}{dt} \tag{5}$$

$L_m \approx L_s$, if strong magnetic coupling is ensured ($k \approxeq 1$). By neglecting the resistance of the coils, the voltage of the common connection point with respect to the reference o is

$$V_{xo} = \frac{1}{2}(V_{x_1o} + V_{x_2o}) \tag{6}$$

and the dynamics of the circulating current is represented as

$$\frac{dI_{x,c}}{dt} = \frac{1}{4L_s}(V_{x_1o} - V_{x_2o}) \tag{7}$$

As it is evident from (7), the inductance offered to the circulating current is four times the self-inductance L_s. Therefore effective suppression of the circulating current can be achieved.

The fluxes in the CI are also shown in Fig. 4, where the fluxes ϕ_{x_1} and ϕ_{x_2} (induced due to the excitation of coil x_1 and coil x_2, respectively) are in opposite direction. As a result, the common components of the fluxes are also canceled-out (which includes the dominant fundamental frequency component). Therefore, the resultant flux in the CI only experiences high frequency flux excitation with dominant harmonic frequency components concentrated around the carrier harmonic frequency. This facilitates relatively small size of the CI and still offers large inductance to the circulating current component and ensures effective suppression of the circulating current.

The use of the CI for suppressing the circulating current has been extensively studied in the literature [39, 47, 49–53]. The the design methodology is presented in [51], where the CI is referred to as InterCell Transformer (ICT). The CI based solution is also compared with the classical interleaved solution which uses single phase inductors and it has been demonstrated that the losses in the magnetic components in the CI based solution is lower than the classical solution with single phase inductors. Ewanchuk *et al.* [54] proposed the integration of three different CIs into one three-limb core. However, in order to suppress the circulating current using the three-limb core, the CM voltage difference between the two parallel VSCs should be zero. This was achieved by employing a modified Discontinuous PulseWidth Modulation

(DPWM) scheme, which has more number of commutations than the conventional (both the continuous and the discontinuous) modulation schemes. Therefore, this scheme may not be feasible for medium/high power applications due to the substantial increase in the switching losses.

A PWM scheme has a significant impact on the flux density and losses in both the CI and the CM inductor. The impact of the PWM scheme on the peak flux density in the CI has been investigated in [55]. A PWM scheme to reduce the peak value of the flux density in the CI is also presented, where the common mode signal, which is added to the reference voltage waveforms, has been optimized. However, the impact on the core losses are not investigated in the literature and it is addressed in this thesis. A PWM scheme to reduce the core losses in the CI is also proposed in this thesis.

The CI is typically designed for the high frequency flux excitations (with dominant harmonic frequency component at the carrier frequency) and the fundamental frequency flux component should be controlled to be zero in order to avoid the saturation. It is reported in [56] that the use of the DPWM1 introduces low frequency flux component due to the coexistence of two different zero voltage vectors at the discontinuous points. This may happen due to the fact that the reference space vectors of both the VSCs could lie in two different sectors of the space vector diagram at the discontinuous points. This issue has been addressed in [57] by introducing additional commutation during the sector transition. However, it is important to mention that this phenomenon is not observed during this study, where the asymmetrical regular sampling with 180° interleaving angle is employed. The detailed analysis for this case is presented in this thesis.

A single phase integrated inductor for the two parallel interleaved VSCs is proposed in [57]. The magnetic structure of this inductor has two side limbs and a central limb. Air gaps are introduced in all the three legs, out of which the length of the air gaps in both the side limbs are equal. The coils are placed around the side limbs and have equal number of turns. The flux in the magnetic core has two distinct components:

- Flux component corresponding to the line filter inductor L_f (referred to as the common flux ϕ_x).
- Flux component corresponding to the CI (referred to as the circulating flux $\phi_{x,c}$, which mainly confines to the side limbs).

The circulating flux component $\phi_{x,c}$ is given as

$$\phi_{x,c} = \frac{1}{2N} \int (V_{x_1o} - V_{x_2o})\, dt \tag{8}$$

The maximum value of the circulating flux component is given as

$$\phi_{x,c_{max}} = \frac{V_{\mathrm{dc}}}{8Nf_c} \tag{9}$$

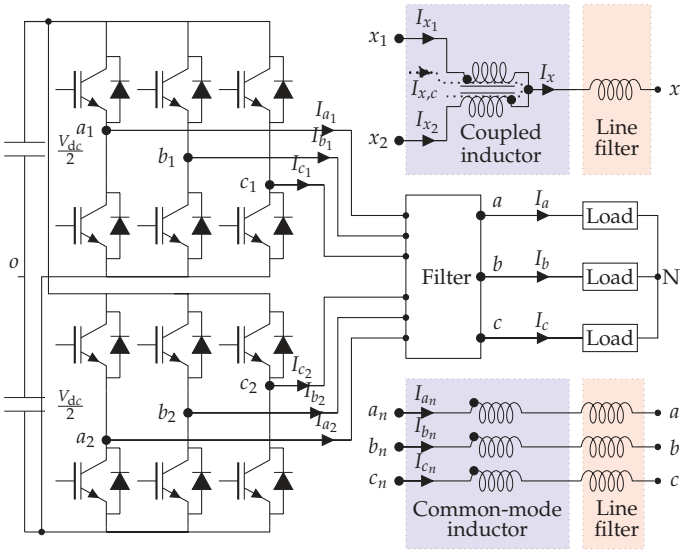


Fig. 5: Two parallel interleaved VSCs with a common dc-link. The filter arrangement for circulating current suppression using the CI and the CM inductor is depicted, where $x = \{a, b, c\}$ and $n = \{1, 2\}$.

The $\phi_{x,c_{max}}$ depends only on the dc-link voltage V_{dc}, the number of turns N, and the switching frequency f_c. Therefore, the introduction of the two air gaps in the magnetic path of the $\phi_{x,c}$ does not bring any advantage in terms of the size reduction (However depending upon the control scheme employed, small air gap may be needed to avoid the saturation). In addition, it is difficult to realize the inductor using the standard cores, when the length of the air gaps in the side limbs and the central limbs are different. Moreover, the solution presented in [57] is only applicable to two parallel interleaved VSCs.

The circulating current suppression for three parallel VSCs is presented in [53]. Three limb magnetic core is used for the CIs and single phase inductors are employed for the line current filtering of each of the phases. The magnetic integration of both the line current inductor and the CIs in a single magnetic structure can further reduce the volume of the overall system and it is investigated in this thesis.

Another approach is to use the CM inductor to suppress the circulating current [14, 15]. The basic scheme is shown in Fig. 5, where the CM inductor in series with the line filter inductor for each of the VSCs is used. In the CM inductor, the magnetic coupling between the three phases is used to suppress the circulating current. Since all three phases are wound on the same core, the flux linkage is proportional to the average of the leg currents of all three

phases, and the flux linkage is three times the CM flux linkage, where the CM flux linkage is given as

$$\lambda_{CM}(t) = \frac{\lambda_a(t) + \lambda_b(t) + \lambda_c(t)}{3} = \int (V_{CM1} - V_{CM2})\, dt \tag{10}$$

where V_{CMn} is the CM voltage of the nth VSC, and it is given by

$$V_{CMn} = \frac{V_{a_nO} + V_{b_nO} + V_{c_nO}}{3} \tag{11}$$

where n represents the VSC number ($n = \{1, 2\}$). Since, the circulating current that flows between the VSCs is due to the phase-shifted pole voltages of the parallel VSC legs of each phases and may not be fully visible in the common mode. As a result, the CM inductor may not be as effective as CI in suppressing the circulating current. On the other hand, the CM inductor based solution facilitates modular and fault tolerant operation. It also facilitates un-equal current sharing amongst the parallel VSCs, which may not be possible in the case of the CI without saturation or avoiding unnecessary oversizing of magnetic component. A PWM scheme to reduce the peak value of the flux density in the CM inductor is proposed in this thesis. As a result, the CM inductor can be made smaller.

The circulating current can be avoided by providing galvanic isolation between the parallel VSCs using the multiple winding line frequency transformer [58, 59], as shown in Fig. 6. However, use of the bulky line frequency transformer adds to the cost and increases the size. On the other hand, many grid-connected applications use transformer between the converter system and a grid for matching the voltage levels. Also in some applications, the grid codes demand galvanic isolation. In such systems, using multiple isolated primary windings is a good solution as it avoids the use of any additional inductive component. Moreover, the control is simpler compared to the CI based solution. The simulated current waveforms for three parallel interleaved VSCs for following two cases are shown in Fig. 7 and Fig. 8.

- Case 1: Galvanic isolation by using multiple isolated primary winding transformer.
- Case 2: Coupled inductor for suppressing the circulating current.

The line filter inductor and the switching frequency is taken to be the same in both the cases. The resultant line currents in both the cases are shown in Fig. 8, which shows that the quality of the resultant line current is the same in both the cases. However, the VSC leg currents demonstrate different characteristics. The circulating current, which has dominant harmonic frequency components concentrated around the 1st and the 2nd carrier frequency (for three parallel interleaved VSCs), are effectively suppressed using the CI. As

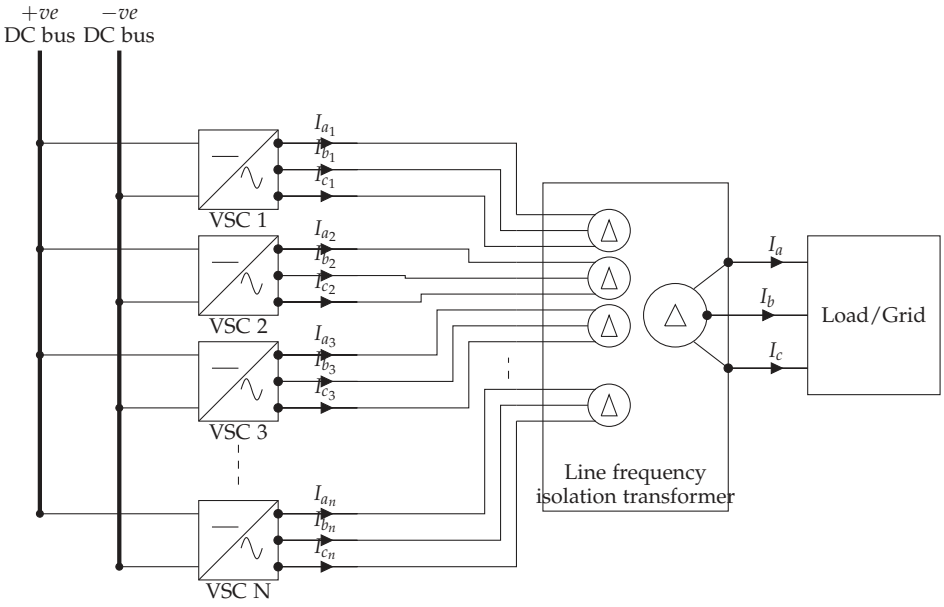


Fig. 6: N parallel interleaved voltage source converters: paralleled through a line frequency isolation transformer to avoid circulating current.

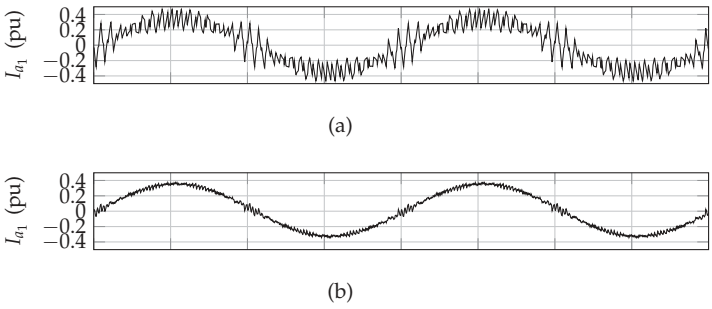


Fig. 7: Simulated leg current, normalize to the rated output current. (a) Case 1: With transformer isolation, (b) Case 2: coupled inductor.

a result, the leg current in the case of the CI has major harmonic components that are concentrated around the 3rd carrier frequency component, as shown in Fig. 7(b) and Fig. 9(b). On the contrary, the leg currents in the case 1 has a major harmonic current concentrated around the 1st carrier frequency, as shown in Fig. 7(a) and Fig. 9(a). This is due to the fact that the

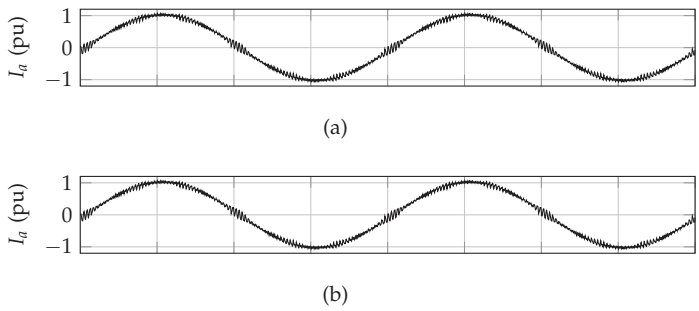


Fig. 8: Simulated resultant current, normalize to the rated output current. (a) Case 1: With transformer isolation, (b) Case 2: coupled inductor.

dominant harmonic frequency components of the switched output voltage appears across the line filter inductor and the magnitude of these harmonic components in the leg currents depends on the line filter inductance, which is relatively small in the parallel interleaved VSCs. As a result, the conduction losses in the semiconductor switches and the ohmic losses are slightly more in the case 1, compared to the case 2. Also the core losses in the line filter inductor is more in the case 1. However, additional magnetic component (CI) is required in the case 2 and it has associated core and copper losses.

1.2 Research Objectives and Contributions

The research objectives and new contributions are outlined in this section.

1.2.1 Research Challenges and Objectives

This thesis is an attempt to address following research objectives:

- To evaluate the effect of the carrier interleaving on the value of the harmonic filter components for the grid-connected applications and investigate the possibilities of using high-order filters with parallel interleaved VSCs.
- To identify best PWM scheme for parallel interleaved VSCs, considering harmonic distortion, semiconductor losses, and core losses in CI as the performance parameters.
- To investigate/propose PWM scheme to reduce the size of the circulating current filter (CI and CM inductor).

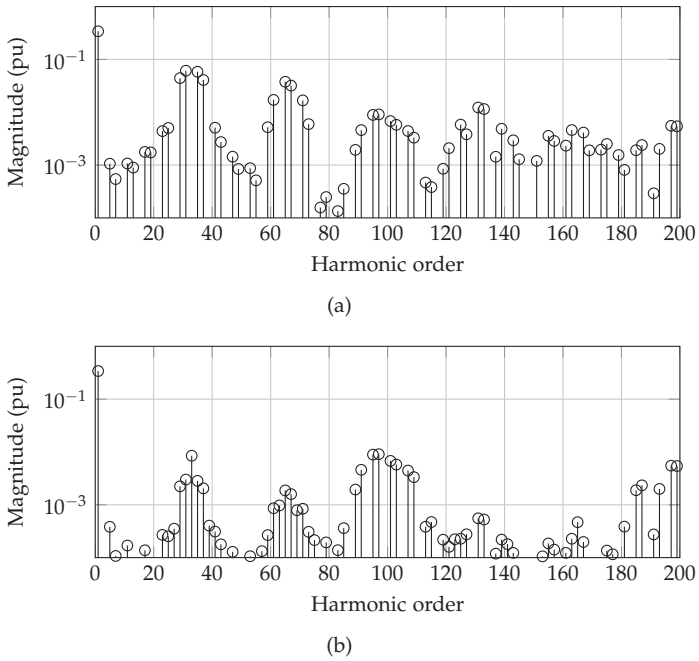


Fig. 9: Harmonic spectra of the leg current. (a) Case 1: With transformer isolation, (b) Case 2: coupled inductor.

- To investigate the possibility of magnetic integration of circulating current filter and the harmonic filter inductor of all three phases in to a single magnetic component.
- Two-level VSC is used extensively in many industrial applications due to its simple power circuitry and proven technology. Therefore, it is highly desirable to realize the medium voltage converter system using the standard two-level VSC. The research objective is to investigate the possibility of using two-level VSCs in medium voltage applications and identify the possibility of reducing the size of the harmonic filter components.

1.2.2 Contributions

The contributions of this work can be broadly classified into two categories:

- Integrated inductors for the parallel interleaved VSCs.
- Modulation schemes for the parallel interleaved VSCs.

Integrated inductors

- A novel three-phase integrated inductor for two parallel VSCs is proposed. The integrated inductor combines the functionalities of the circulating current suppression and the line current filtering. Compared to the state-of-the-art solution, the magnetic integration leads to substantial reduction in the volume of the inductive components.

- Common-mode flux component flows through some parts of the proposed integrated inductor. The existing PWM schemes are analyzed and suitable PWM schemes are identified with an objective to reduce the peak value of the common-mode flux component, without compromising other important performance parameters such as the harmonic performance and the switching losses. 68% reduction in the peak value of the common-mode component, compared to the space vector modulation has been demonstrated.

- A novel three-phase integrated inductor for any arbitrary number of parallel connected VSCs has been proposed.

- The dual-converter fed open-end transformer topology is modified, where both ends of the open-end transformer windings are fed from the converter groups and each converter group comprises parallel VSCs to enhance the current rating. The interleaved operation of the parallel VSCs is proposed to improve the harmonic performance. The integrated inductor is also proposed, which suppresses the circulating current between the parallel VSCs. In addition, it also magnetically integrated the converter-side inductor of the *LCL* filter of both the converter groups.

- Considering a harmonic profile of the parallel interleaved VSCs and harmonic injection limits imposed by the utilities for grid-connected applications, a high-order harmonic filter is proposed. The *LC* trap branch is added along with the *LCL* filter to reduce the value of the harmonic filter components.

Modulation schemes

- A PWM scheme to reduce the size of the CM inductor and losses in the CI is proposed. This PWM scheme uses the division of the active vectors within a half-carrier cycle to ensure simultaneous occurrence of the same zero vector in both of the VSCs. As a result, the peak value of the common-mode flux in the CM inductor is reduced to 66% compared to the space vector modulation. When used in the system which uses CI for the circulating current suppression, the losses in CI can be reduced by 28%.

- A modified modulator to ensure the balancing of the flux in the CI, while ensuring the use of the nearest three vectors to synthesize reference space voltage vector is proposed. Compared to the conventional carrier interleaving, the use of the proposed scheme can substantially reduce the value of the converter-side inductor and shunt capacitance.

1.3 Thesis Overview

The thesis includes extended summary and collection of the published and submitted scientific papers. Parts of the papers are used directly or indirectly in the extended summary of the thesis.

1.3.1 Summary Overview

The extended summary has been divided into five sections. The impact of the interleaving on the harmonic filter components for the grid-connected applications is evaluated in section 2. The high-order harmonic filter, where the *LC* trap branch is added along with the *LCL* filter, is proposed and analyzed. The modulation scheme to improve the harmonic performance is proposed in Section 3. Section 3, also includes a novel modulation scheme to reduce the size of the circulating current filter. The conventional modulation schemes are also evaluated for modulation of parallel interleaved VSCs and compared. The magnetic integration of the circulating current filter and the harmonic filter inductor is presented in Section 4. Various possible solutions for the integrated inductor are proposed and analyzed in detail. The advantages achieved by the integrated inductor are demonstrated by comparing the volume and losses of the proposed solution with the state-of-the-art solutions. The conclusions and the research outlook are summarized in Section 5.

1.3.2 Appended Publications

The list of the appended papers are as follows:

A. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Design of the trap filter for the high power converters with parallel interleaved VSCs "*in Proc. 40th Annual Conference on IEEE Industrial Electronics Society*, IECON 2014, Oct 2014, pp. 2030-2036.

B. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved VSCs for high power wind energy conversion systems,"*IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6775 - 6790, Dec 2015.

C. **G. Gohil**, L. Bede, R. Maheshwari , R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Parallel interleaved VSCs: influence of the PWM scheme on the design of the coupled inductor,"*in Proc. 40th Annual Conference on IEEE Industrial Electronics Society*, IECON 2014, Oct 2014, pp. 1693-1699.

D. **G. Gohil**, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre and F. Blaabjerg, "Modified discontinuous PWM for size reduction of the circulating current filter in parallel interleaved converters, "*IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3457 - 3470, July 2015.

E. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Modulation Scheme For Balancing Flux In PD Modulated Three Parallel Interleaved VSCs With Coupled Inductor,", (under peer review, *IEEE Transactions on Power Electronics*)

F. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved VSCs and PWM schemes for flux minimization, "*IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7534-7546, Dec 2015.

G. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Integrated Inductor for Interleaved Operation of Two Parallel Three-phase Voltage Source Converters,"*in Proc. 17th European Conference on Power Electronics and Applications*, EPE'15 ECCE-Europe, Sept 2015, pp. 1-10.

H. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved three-phase voltage source converter, "*IEEE Transactions on Power Electronics*, [Online early access], DOI: 10.1109/TPEL.2015.2459134, 2015.

I. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Magnetic integration for parallel interleaved VSCs connected in a whiffletree configuration,"*IEEE Transactions on Power Electronics*, [Online early access], DOI: 10.1109/TPEL.2015.2514182, 2016.

J. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Optimized harmonic filter inductor for dual-converter fed open-end transformer topology,", (under peer review, *IEEE Transactions on Power Electronics*)

K. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Dual converter fed open-end transformer topology with parallel converters and integrated magnetics,", (Provisionally accepted, *IEEE Transactions on Industrial Electronics*)

1.3.3 Other Publications

In addition to the appended papers, the following publications have also been made.

Journal Publications

J1. R. Maheshwari, **G. Gohil**, L. Bede and S. Munk-Nielsen, "Analysis and Modeling of Circulating Current in Two Parallel-Connected Inverters, "*IET Power Electronics*, vol. 8, no. 7, pp. 1273 - 1283, 2015.

Conference Publications

C1. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Analytical method to calculate the DC link current stress in voltage source converters, "*in Proc. IEEE International Conference on Power Electronics, Drives and Energy Systems*, PEDES 2014, Dec 2014.

C2. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved VSCs connected in a whiffletree configuration,"*in Proc. IEEE Energy Conversion Congress and Exposition*, ECCE'15, Sept 2015, pp. 5952-5959.

C3. **G. Gohil**, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Magnetic integration of the harmonic filter inductor for dual-converter fed open-end transformer topology,"(Accepted for publication in APEC 2016)

2 Harmonic Filter Design

This section evaluates the impact of the interleaving on the harmonic filter design for the grid-connected applications. Following appended papers provides detailed technical discussion.

- Paper A: Design of the trap filter for the high power converters with parallel interleaved VSCs.
- Paper B: Line filter design of parallel interleaved VSCs for high power wind energy conversion systems.

2.1 Effect of the Carrier Interleaving

The advantages achieved by the carrier interleaving in terms of the reduction in the value of the harmonic filter components has been demonstrated by comparing the value of the harmonic filter components with that of the conventional system with the synchronized gate pulses (with no carrier interleaving). The comparative evaluation has been carried out for the the grid-connected Wind Energy Conversion System (WECS) and the system specifications are given in Table B.1. The use of the LCL filter is considered, as shown in Fig. 11. The WECS is connected to a medium voltage network using a step-up transformer. The leakage inductance of a step-up transformer often ranges from 0.04-0.06 pu [60], and it is considered as a part of the grid side inductance L_g. L_f and C_f represent the converter-side inductance and the shunt-capacitance of the LCL filter. In the case of the carrier interleaving, the circulating current flows between the parallel VSCs and it is suppressed using the CI, as shown in Fig. 11. In the case of the conventional scheme with no interleaving, the CI is not needed. In this case, each of the VSCs

Table 1: System specifications and base values for per-unit system.

Parameters	Values (Base values)
Power	2.2 MVA (2 MW)
Line-to-line voltage	690 V
DC-link voltage	1080 V
Current	1840 A
Line frequency	50 Hz
Inductance	688 μH
Capacitance	14709 μF
Switching frequency	2550 Hz

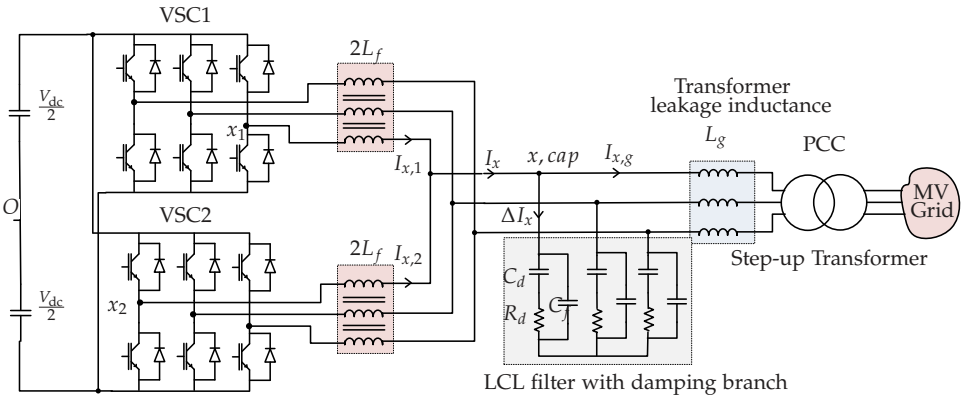


Fig. 10: The grid side converter of the WECS, comprised of two parallel VSCs with synchronized gate pulses (without carrier interleaving). The WECS is connected to the medium voltage network by using a step-up transformer. $x = \{a, b, c\}$

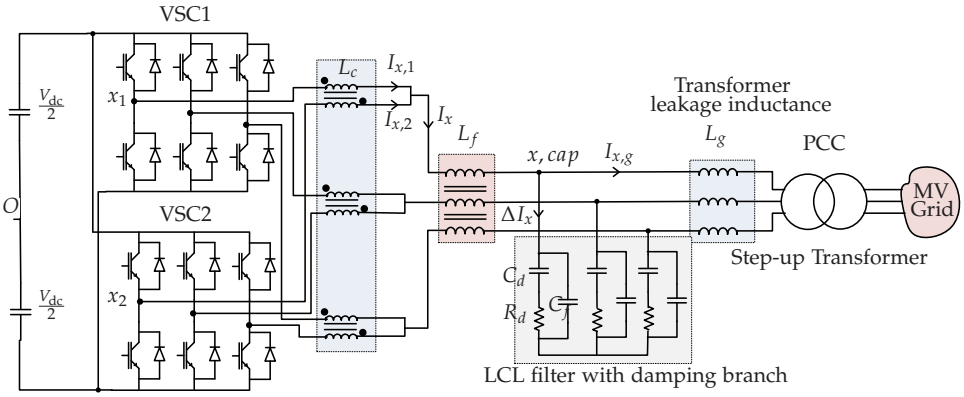


Fig. 11: The grid side converter of the WECS, comprised of two parallel VSCs with interleaved carriers, connected to the medium voltage network by using a step-up transformer. $x = \{a, b, c\}$

has a separate converter-side inductor with the inductance value of $2L_f$, as shown in Fig. 10.

2.1.1 Design constraint

Harmonic Current Injection Limits:

The harmonic current injection limit for a generator connected to the medium-voltage network, specified by the German Association of Energy and Water Industries (BDEW) [27, 61, 62], is considered. The permissible harmonic current injection is determined by the apparent power of the WECS and the Short-Circuit Ratio (SCR) at the Point of the Common Coupling (PCC). The maximum current injection limit of the individual harmonic components up

Table 2: BDEW harmonic current injection limits for the WECS connected to the 10 KV Medium Voltage Network

Harmonic Order h	Current Injection Limit (A/MVA/SCR)
5	0.058
7	0.082
11	0.052
13	0.038
17	0.022
19	0.018
23	0.012
25	0.01
Even-ordered $h < 40$	0.06 / h
$40 < h < 180$	0.18 / h

to 9 kHz is specified in the standard and the limits for the WECS connected to the 10 KV medium-voltage network are given in Table B.2. Special limits are set for the odd-ordered integer harmonics below the 25th harmonic, as given in Table B.2. The SCR is taken to be 20 and the allowable injection limits of individual harmonic components on the low voltage side (690 V) for the 2.2 MVA WECS are calculated.

Maximum Switch Current Ripple:

The controllability of the system is affected if the switch current has a high ripple content [28]. Therefore, the maximum value of the peak-to-peak switch current ripple is restricted to 0.45 pu in this design.

Reactive Power Consumption:

The current flowing through the semiconductor devices, the converter side filter inductor L_f and the circulating current filter L_c can be minimized by limiting the current drawn by the shunt branches of the harmonic filter. Moreover, when VSCs are modulated using DPWM1, the switching losses increase with the increase in the phase difference between the reference voltage and the fundamental component of the switch current. Therefore, the switching losses can also be minimized by making the reactive power consumption of the line filter as small as possible. The grid voltage may vary over a range of 1 ± 0.1 pu and the reactive power consumption of the shunt branches of the line filter is restricted to 0.2 pu.

2.1.2 Filter Design Procedure

The value of the line filter components are mainly determined based on:

- The individual voltage harmonic components that appear across the line filter.
- The maximum value of the switch current ripple.

The magnitude of the individual harmonic frequency components that appears across the line filter is determined by the difference of the magnitude of the corresponding harmonic frequency component in the average of the phase voltages of the parallel interleaved legs and the magnitude of the same harmonic frequency component in the grid voltage. The average of the phase voltages of the parallel interleaved legs is independent of the arrangement of the CI. Therefore, the design of the line filter can be carried out independently. The interleaved operation of the parallel VSCs partially or completely eliminates some of the voltage harmonic components in the average of the phase voltages of the interleaved legs. Therefore, the reduction in the value of the line filter components can also be achieved. A step-by-step design procedure for the harmonic filter is described hereafter.

Virtual Voltage Harmonics:

The magnitude of the individual harmonic components in the injected grid current is the multiplication of the magnitude of the respective harmonic component in the averaged phase voltage and the admittance offered by the filter at that harmonic frequency. The harmonic coefficients are the function of the dc-link voltage V_{dc} and the modulation index M. Therefore, for a given value of the dc-link voltage, the magnitude of the individual harmonic components varies with the modulation index M. In order to satisfy the harmonic current injection limit over the entire operating range, the worst case magnitude of the individual harmonic components of average of the phase voltages is required. The spectrum comprises the maximum values of the individual voltage harmonic components over the entire operating range is defined as a Virtual Voltage Harmonic Spectrum (VVHS) [61] and used for calculating the values of the harmonic filter components.

Required Filter Admittance:

The worst case filter admittance requirement is obtained from the harmonic current injection limit and the VVHS of the phase voltage. The required admittance for the h*th* harmonic component is given as

$$Y_h^* = \frac{I_{h,BDEW}^*}{V_{h,VVHS}} \tag{12}$$

where $I^*_{h,BDEW}$ is the BDEW current injection limit of the h*th* harmonic component and $V_{h,VVHS}$ is the voltage magnitude of the corresponding harmonic component in VVHS. The admittance transfer function of the LCL filter is given as

$$Y_{LCL}(s) = \frac{I_g(s)}{V_{PWM}(s)}\bigg|_{V_g=0} = \frac{1}{L_f L_g C_f} \frac{1}{s(s^2+\omega^2_{r,LCL})} \tag{13}$$

where V_g is the grid voltage and V_{PWM} is the switched voltage of the VSC. The LCL filter has a resonant frequency at $\omega_{r,LCL}$ and may magnify the harmonic components in vicinity to resonant frequency at $\omega_{r,LCL}$. Therefore, the R_d/C_d damping branch is used and the admittance transfer function of the LCL filter with the R_d/C_d damping branch is given as

$$Y_{LCL}(s) = \frac{1}{L_f L_g C_f} \frac{s+\frac{1}{R_d C_d}}{s\left(s^3+\frac{C_f+C_d}{R_d C_f C_d}s^2+\frac{L_f+L_g}{L_f L_g C_f}s+\frac{L_f+L_g}{L_f L_g R_d C_f C_d}\right)} \tag{14}$$

The filter parameters are chosen to ensure that the admittance of the designed filter is always less the required value of the filter admittance for all the harmonic frequency components of interest.

2.1.3 Comparative Evaluation

The VVHS for both the cases are shown in Fig. 12. In the case of the interleaved carriers, the major harmonic components appear at the 2nd carrier frequency, as shown in Fig. 12(b), whereas for without carrier interleaving case, the major harmonic components appear at the 1st carrier frequency, as shown in Fig. 12(a). For without carrier interleaving case, the required value of the filter admittance along with the admittance of the designed filter is shown in Fig. 13. The parameters of the designed filter are listed in Table 3. The filter parameters for the case of the carrier interleaving are also given in Table 3, where it is evident that by interleaving the carrier signals, the value of the harmonic filter inductor and the shunt capacitance can be reduced by the 48% and 20%, respectively.

Table 3: Filter Parameters of the LCL filter

Parameters	Without interleaving	With interleaving
$L_f + L_g$	206.4 μH (0.3 pu)	106.75 μH (0.155 pu)
$(C_f + C_d)$	3000 μF (0.2 pu)	2400 μF (0.16 pu)

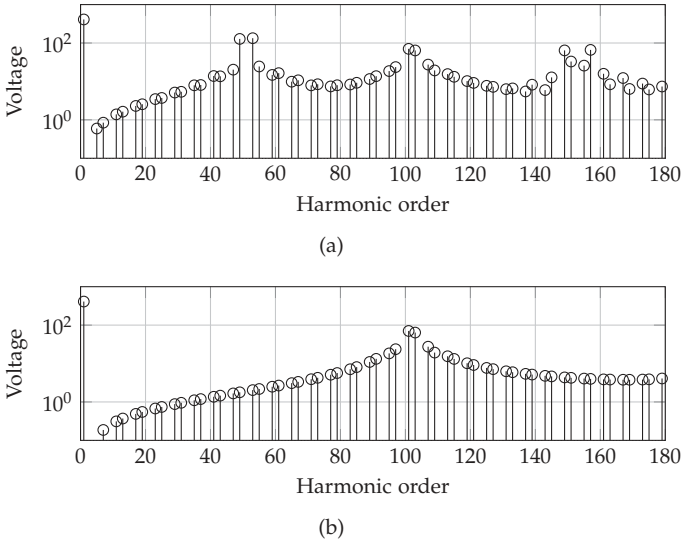


Fig. 12: Virtual voltage harmonic spectrum. The switching frequency is taken to be 2.55 kHz in both the cases. (a) Without carrier interleaving, (b) with the interleaving angle of 180°.

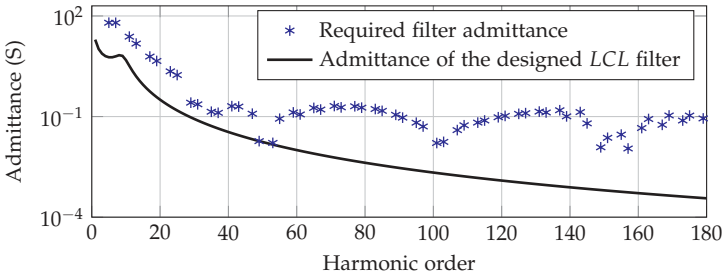


Fig. 13: Admittance plot of the designed LCL filter for without carrier interleaving case, with $L_f = 0.133$ pu (91.7 μH), $L_g = 0.166$ pu (114.7 μH), $C_f = 0.1$ pu (1500 μF), $C_d = 0.1$ pu (1500 μF).

2.2 High-order Harmonic Filters

The resonant frequency of the LCL filter is given as

$$\omega_{r,LCL} = \sqrt{\frac{L_f + L_g}{L_f L_g C_f}} \tag{15}$$

Due to the presence of the complex conjugate poles, the roll-off of the high frequency components (higher than the $\omega_{r,LCL}$) is -60 dB/decade. Therefore, the LCL filter offers good attenuation to the high frequency harmonic com-

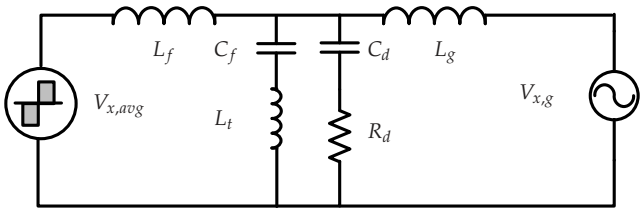


Fig. 14: Trap filter with parallel R_d/C_d damping.

ponents, and it can effectively reduce the differential mode electromagnetic interference (above 150 kHz) [63]. For two parallel VSCs, the switched voltages at the VSC terminals have harmonic components concentrated around the odd multiple of the carrier frequency. Due to the limited switching capability of the semiconductor devices used in the high power applications, a fairly high value of the filter components are required for the *LCL* filter to attenuate the major harmonic components.

2.2.1 *LC* Trap Filter

The value of the filter components can be reduced by using a *LC* trap branch, which is tuned to attenuate the major carrier harmonics and its sideband harmonics. This can be realized by inserting an inductor in series with the capacitor of the *LCL* filter [64], as shown in Fig. 14. The use of the *LC* trap branch to attenuate the sideband harmonic components around the carrier frequency is proposed in [64, 65]. The multiple *LC* trap branches are used, to attenuate the carrier harmonic and its sideband harmonic components around the carrier frequency and its multiple, in [66, 67]. The admittance transfer function of the line filter with the *LC* trap branch, commonly known as trap filter, is given as

$$Y_{trap}(s) = \left(\frac{1}{(L_f + L_g) + \frac{L_f L_g}{L_t}}\right)\frac{s^2 + \omega_t^2}{s(s^2 + \omega_{r,trap}^2)} \tag{16}$$

The resonant frequencies are given as

$$\begin{aligned} \omega_t &= \frac{1}{\sqrt{L_t C_f}} \\ \omega_{r,trap} &= \frac{1}{\sqrt{\left(\frac{L_f L_g}{L_f + L_g} + L_t\right)C_f}} \end{aligned} \tag{17}$$

where L_t is the inductor inserted in series with the capacitor C_f of the *LCL* filter.

Table 4: Parameters of the harmonic filter with *LC* trap branch.

Parameters	Values
L_f	18.6 μH (0.027 pu)
L_g (Transformer leakage)	41.3 μH (0.06 pu)
Filter capacitor C_f	147 μF (0.01 pu)
Trap inductor L_t	6.62 μH (0.0094 pu)
Damping capacitor C_d	147 μF (0.01 pu)

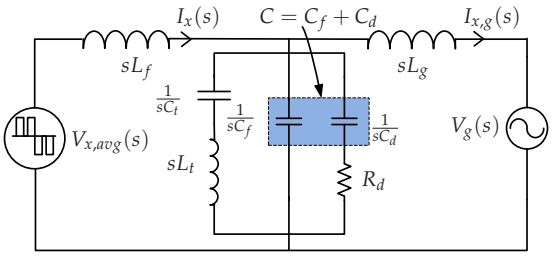


Fig. 15: The single phase equivalent circuit of the *LCL* filter with additional *LC* trap and a C_d/R_d damping branch.

Table 5: Parameters for *LCL* filter with *LC* trap branch

Parameters	Values
L_f	13.76 μH (0.02 pu)
L_g (+ Transformer leakage)	48.16 μH (0.07 pu)
Trap capacitor C_t	294 μF (0.02 pu)
Trap inductor L_t	3.3 μH (0.0048 pu)
Capacitor $C_f = C_d$	136 μF (0.0093 pu)

The VSCs are modulated using the SVM and the filter parameters for the *LC* trap filter are designed using the procedure outlined before and they given in Table 4. Although one more inductor in the form of the trap inductor L_t is required compared to the *LCL* filter, the values of the in-line components (both L_f and L_g) reduce significantly.

2.2.2 *LCL* Filter with *LC* Trap Branch

Due to the introduction of the complex conjugate zeros by the *LC* trap branch, the roll-off of the high frequency components (higher than the ω_t) is -20 dB/decade. This leads to a poor attenuation of the high frequency harmonic components. On the contrary, the *LCL* filter offers good attenuation to the high frequency harmonic components. Therefore, the *LC* trap branch along with the *LCL* filter can be used to achieve the desired filtering performance (both at the low and the high frequency components) with small values of the filter components. The use of such filter for single VSC is presented in [68]. However, the high frequency attenuation is compromised due to insertion of the damping resistor in series with the capacitive branch. To overcome this issue, *LC* trap branch along with the *LCL* filter with R_d/C_d damping branch is proposed. The single line diagram of the proposed harmonic filter configuration is shown in Fig. 15.

The parameters of the designed harmonic filter are given in Table 5. The value of the filter parameters are almost the same as that of the trap filter. However, significant improvement in the attenuation to the high frequency harmonic components is achieved using the proposed filter. This is verified experimentally and the results are given in the appended papers.

3 Modulation of Parallel Interleaved VSCs

The modulation schemes of the parallel interleaved VSCs have been discussed in this section. The detailed analysis and results are included in the following appended papers.

- Paper C: Parallel interleaved VSCs: influence of the PWM scheme on the design of the coupled inductor.
- Paper D: Modified discontinuous PWM for size reduction of the circulating current filter in parallel interleaved converters.
- Paper E: Modulation Scheme For Balancing Flux In PD Modulated Three Parallel Interleaved VSCs With Coupled Inductor
- Paper F: An integrated inductor for parallel interleaved VSCs and PWM schemes for flux minimization.

3.1 Comparative Evaluation of the Conventional Schemes

The PWM scheme significantly influence following performance parameters of the parallel interleaved VSCs:

- Harmonic performance.
- Core losses in the CI.
- Switching losses.

On this performance parameters, following conventional two-level PWM schemes are evaluated and compared:

- SVM: Center aligned space vector modulation.
- DPWM1: 60° clamp.
- DPWM2: 30° lagging clamp.
- DPWM3: 30° clamp.

The modulation waveform of all of these schemes are shown in Fig. 16.

3.1.1 Harmonic Performance

For the pulse width modulated VSC, the reference vector is sampled and the active and zero vectors are applied for predetermined intervals to synthesize the reference vector such that the volt-second balance is maintained. At any given instant, the error between the applied voltage vector and reference

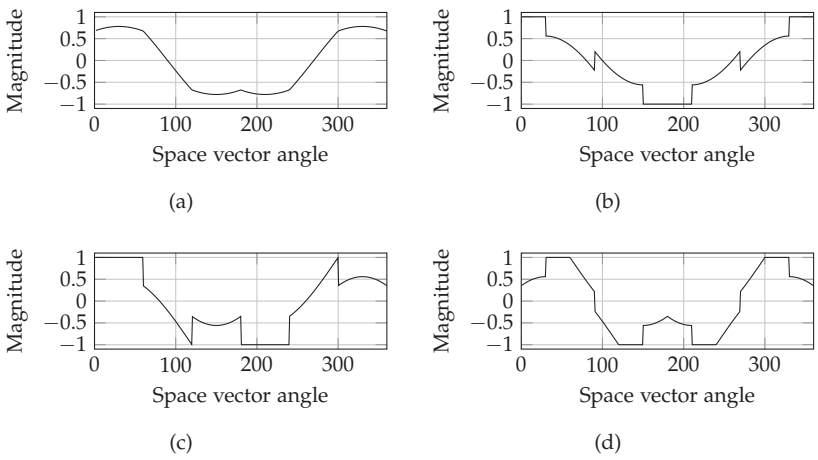


Fig. 16: Modulation waveforms for modulation index $M = 0.9$. (a) SVM, (b) DPWM1, (c) DPWM2, (d) DPWM3.

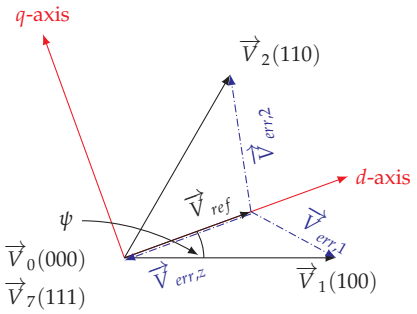


Fig. 17: The active and zero vectors to synthesize given reference vector and corresponding error voltage vectors.

vector exists. The error voltage vectors for a given sampling instance are shown in Fig. J.6. The stator flux ripple vector, which is a time integral of the error voltage vector is directly related to the ripple current [43, 69–71].

In the synchronously rotating reference frame, the instantaneous error voltage vectors depicted in Fig. J.6 are given as;

$$\overrightarrow{V}_{err,1} = [\cos\psi - V_{ref}] - j\sin\psi \tag{18a}$$

$$\overrightarrow{V}_{err,2} = [\cos(60^\circ - \psi) - V_{ref}] + j\sin(60^\circ - \psi) \tag{18b}$$

$$\overrightarrow{V}_{err,z} = -V_{ref} \tag{18c}$$

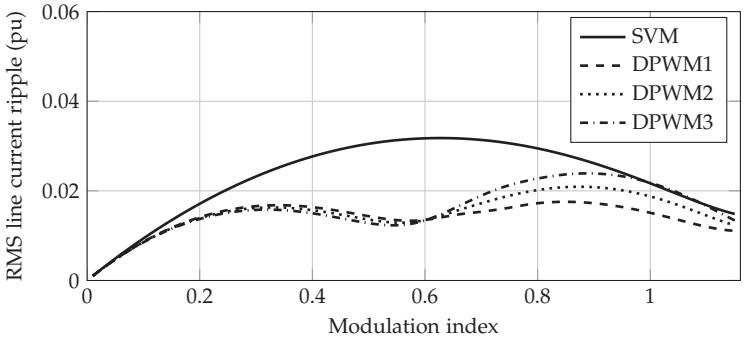


Fig. 18: Total rms value of the line current ripple (normalized) as a function of modulation index.

The time integral of the error voltage vector is known as harmonic flux vector. The harmonic flux vector can be decomposed into d-axis and q-axis components, and used to evaluate the ripple current/harmonic content. The variation of the total rms value of the line current ripple over the entire modulation range is also shown in Fig. 18. The carrier frequency is taken to be the same in all cases, thus the number of commutations in DPWM schemes are 2/3 than the number of commutation in the SVM. The DPWM schemes demonstrates superior harmonic performance compared to the SVM in the entire operating modulation range. In low modulation indices range, all the DPWM schemes have a similar harmonic distortion, far more superior than the SVM. For modulation indices higher than 0.6, DPWM1 has a lowest harmonic distortion compared to other methods, followed by the DPWM2 and DPWM3.

3.1.2 Core Losses of the Coupled Inductor

The CI suppresses the circulating current by providing magnetic coupling between the parallel legs of each phase. Assuming tight magnetic coupling between the windings, the excitation frequency seen by the CI has frequency components which are concentrated around the odd multiple of the carrier frequency (for two parallel VSCs). The high frequency excitation could lead to significant size reduction of CI. However, more losses due to the high frequency flux excitation and relatively small size may result into increased loss density, and considerable thermal management is required [72, 73].

The size of the CI can be reduced by allowing operation at high peak flux density, which leads to increased losses. Thus the volume optimized design of the CI may result into thermally limited design, where the maximum flux density in the core is determined by the heat dissipation capability of the CI [74]. For parallel interleaved converter, the PWM scheme has a strong

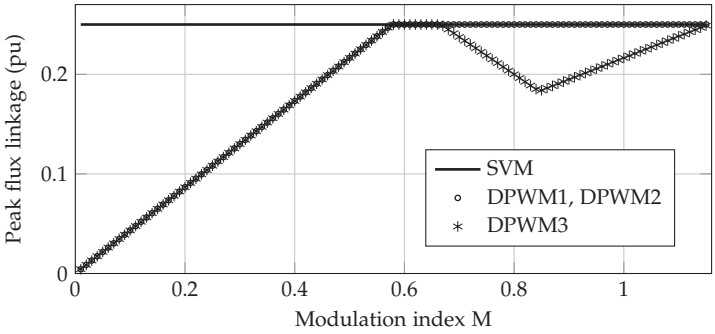


Fig. 19: Variation of the the maximum peak flux linkage with the modulation index. The flux-linkage is normalized with respect to the $V_{dc}T_s$.

influence on maximum peak flux density and the losses in CI. The variation in the peak flux-linkage with the modulation index for different PWM schemes [75] is plotted in Fig. C.7. The maximum value of the peak flux linkage is the same in all PWM schemes, however the flux-linkage pattern is different. As a result, the core losses would be different in each of the scheme, which is an important factor in determining size and efficiency of the CI.

The Improved Generalized Steinmetz Equation (IGSE) [76, 77] is used to calculate core losses. Considering tightly coupled system, the effect of the leakage flux is neglected. The loss per unit volume P_v is evaluated using

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{19}$$

where α, β and k_i are the constants determined by the material characteristics. To compare the PWM method independent of the design parameters, the volumetric losses in each of the DPWM scheme is normalized with respect to the volumetric losses of the SVM. Fig. C.8 shows that the DPWM3 outperforms other schemes in terms of the core losses. All the DPWM schemes have a lower core losses compared to SVM at lower modulation indices. The switching sequences of DPWM2 are the same as the switching sequences of DPWM1 in one sub-sector ($0^\circ < \psi \leqslant 30^\circ$), and switching sequences of DPWM3 in other sub-sector ($30^\circ < \psi \leqslant 60^\circ$). Therefore, the core losses in case of DPWM2 is an average of core losses of DPWM1 and core losses of DPWM3 as depicted in Fig. C.8. For higher modulation indices, the DPWM1 has a highest core losses in CI, followed by the DPWM2 and SVM.

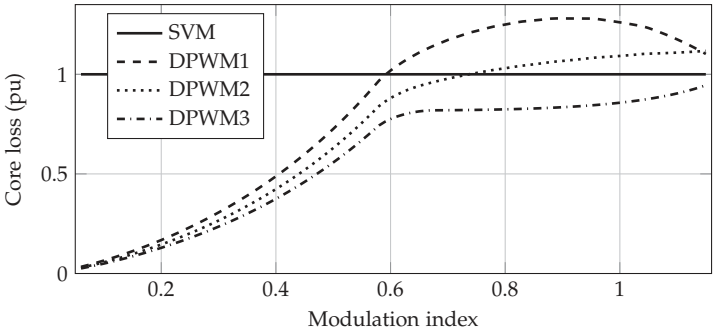


Fig. 20: The core losses in the CI with different PWM schemes. The core losses are normalized with respect to that of the SVM. The carrier frequency is taken to be the same in all cases.

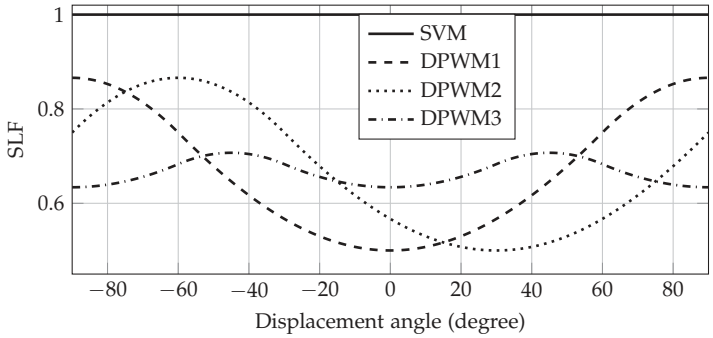


Fig. 21: Switching loss characteristics of different PWM schemes. The carrier frequency is taken to be the same in all cases.

3.1.3 Switching losses

Although the switching losses behavior of PWM scheme in parallel interleaved VSCs is not different than the single inverter case (Assuming that the circulating current is suppressed and has no effect on the switching losses), the switching loss comparison is derived from [78] for the sake of completion. The switching loss characteristics of different PWM schemes, characterized by the Switching Loss Function (SLF) [78] is plotted in Fig. 21. The DPWM1 has minimum switching losses for a displacement angle close to zero. The DPWM2 is most efficient for a lagging power factor load with the displacement angle varying from 15°to 75°.

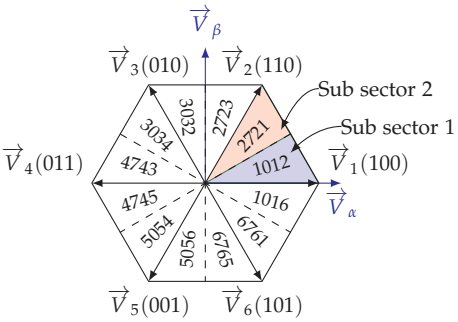


Fig. 22: Switching sequences of the proposed scheme in each sub-sector.

3.2 Size Reduction of the Circulating Current Filter

The circulating current can be suppressed by using the CI ot the CM inductor. A PWM scheme to reduce the size of these components is proposed hereafter.

3.2.1 Coupled Inductor

The design of the CI may be thermally limited, specially when the 0.35 mm grain-oriented laminated steel is used as a core material. A PWM scheme to reduce the core losses in the CI is presented in this paper. This PWM scheme uses the division of the active vectors within a half-carrier cycle to ensure simultaneous occurrence of the same zero vector in both of the VSCs.

The sequences used in the proposed PWM scheme are depicted in Fig. D.5. The numbers shown in Fig. D.5 represent the sequence in which the voltage vectors are applied, e.g. 1012 represents that $\overrightarrow{V}_1$, $\overrightarrow{V}_0$, $\overrightarrow{V}_1$, and $\overrightarrow{V}_2$ are applied in sequence. The discussion is restricted to the first sector of the space vector diagram. The same discussion applies to other sectors due to the symmetry. From Fig. D.5, it is evident that each phase discontinues switching for one third period of the fundamental cycle. For example, phase A is clamped twice to the positive dc-link for $30^\circ \leqslant \psi < 60^\circ$ and $300^\circ \leqslant \psi < 330^\circ$ and clamped twice to the negative dc-link for $120^\circ \leqslant \psi < 150^\circ$ and $210^\circ \leqslant \psi < 240^\circ$ in a fundamental period. The active voltage vector with the maximum dwell time is divided into two intervals and applied twice in a half-carrier cycle. Therefore, one of the phase legs is switched twice, whereas one phase does not switch in a given sampling interval. Hence, it is referred to as the modified DPWM in this paper.

If the reference vector is in sub-sector 1, as shown in Fig. D.5, the dwell time of $\overrightarrow{V}_1$ is more than the dwell time of $\overrightarrow{V}_2$. Thus, the dwell time of $\overrightarrow{V}_1$ is divided, and $\overrightarrow{V}_0$ is applied in between to ensure simultaneous occurrence

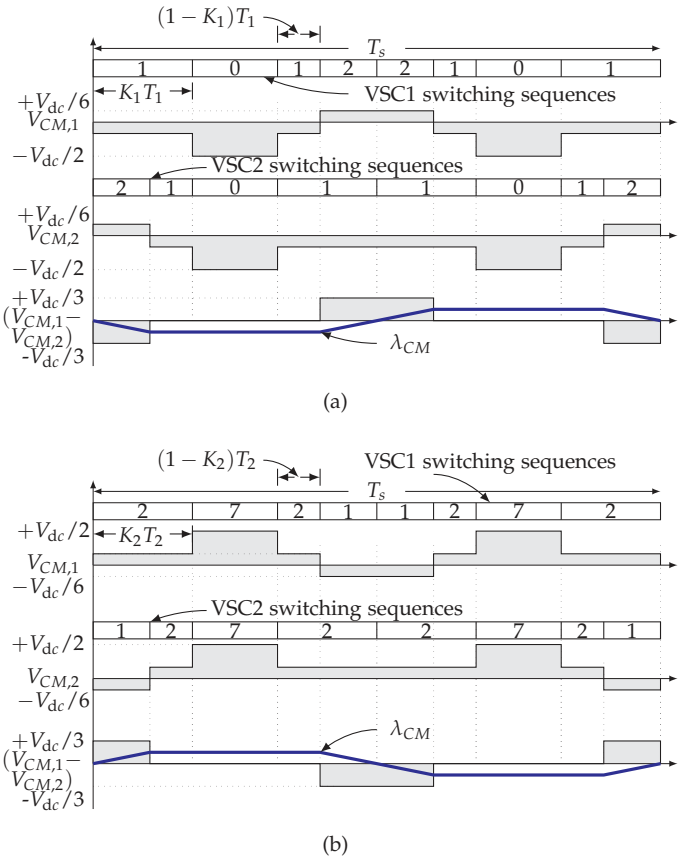


Fig. 23: Proposed modulation scheme: Switching sequences and CM voltages of both the VSCs with an interleaving angle of 180°. (a) sub-sector 1: $0° \leq \psi < 30°$, (b) sub-sector 2: $30° \leq \psi < 60°$.

of the same zero vector in both VSCs. The reverse is true for sub-sector 2. Therefore, in sub-sector 1 ($0° \leqslant \psi < 30°$), T_1 is divided into two intervals and can be given as

$$T_1 = K_1T_1 + (1-K_1)T_1 \tag{20}$$

where $0 \leqslant K_1 \leqslant 1$. Similarly, in sub-sector 2 ($30° \leqslant \psi < 60°$), T_2 is divided into two intervals;

$$T_2 = K_2T_2 + (1-K_2)T_2 \tag{21}$$

where $0 \leqslant K_2 \leqslant 1$. The flexibility offered by the division of the active vectors is used to ensure simultaneous occurrence of the same zero vectors in both

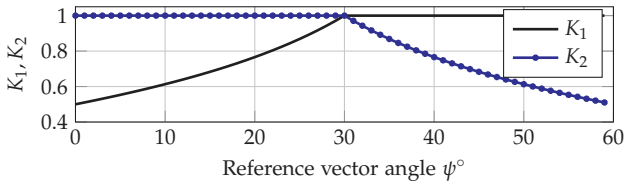


Fig. 24: Variation in parameter K_1, K_2 with reference vector angle ψ. Due to the symmetry the plot is restricted to the first sector.

VSCs.

The switching sequences and the CM voltages in sub-sector 1 and sub-sector 2 for the proposed scheme are shown in Fig. D.6(a) and Fig. D.6(b), respectively for a switching cycle. In sub-sector 1, the value of K_1 is updated in each half-carrier cycle, while K_2 is equal to one. In sub-sector 2, K_2 is varied, and K_1 is equal to one. The careful observation of the switching sequence depicted in Fig. D.6 reveals that the same zero vector of both VSCs can coexist if

$$K_1 = \frac{T_1 + T_2}{2T_1}, K_2 = 1 \tag{22}$$

in sub-sector 1 and

$$K_1 = 1, K_2 = \frac{T_1 + T_2}{2T_2} \tag{23}$$

in sub-sector 2. The variation of K_1 and K_2 over a sector is depicted in Fig. D.7. The peak value of the flux linkage as a function of the modulation

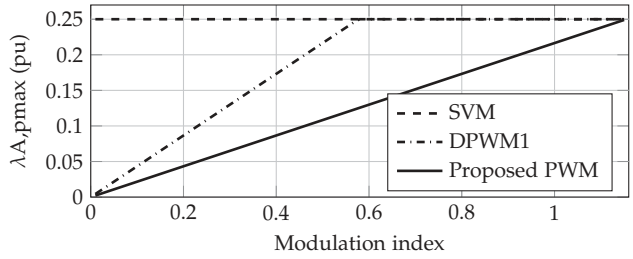


Fig. 25: Comparison of the maximum value of the peak flux linkage as a function of the modulation index. The flux linkage is normalized with respect to the $V_{dc}T_s$.

index is shown in Fig. D.9. The maximum value of the peak flux linkage is the same in all cases. However, the flux linkage pattern is different, which affects the core losses, and thus the design of the CI. Lower core losses over the entire modulation range are observed for the proposed method compared to the other considered schemes, as shown in Fig. D.11.

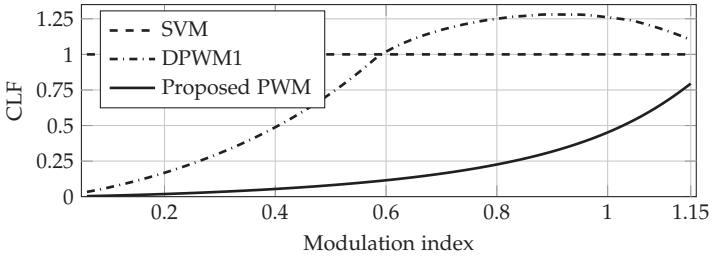


Fig. 26: CLF as a function of the modulation index.

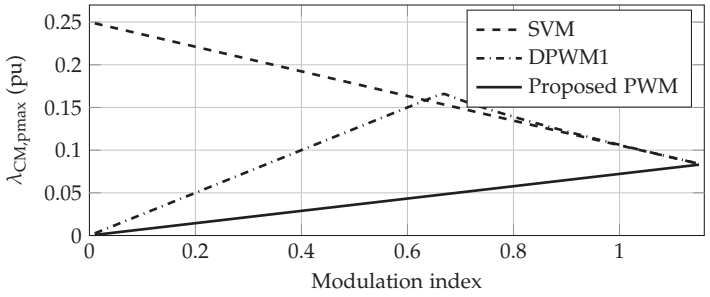


Fig. 27: Comparison of the maximum values of the peak CM flux linkage as a function of the modulation index. The flux linkage is normalized with respect to $V_{dc}T_s$.

3.2.2 Common Mode Inductor

In the CM inductor, the magnetic coupling between the phases is used to suppress the circulating current. Since all three phases are wound on the same core, the flux linkage is proportional to the average of the phase currents. The flux linkage is three times the CM flux linkage, where the CM flux linkage is given as

$$\lambda_{CM}(t) = \frac{\lambda_A(t) + \lambda_B(t) + \lambda_C(t)}{3} = \int (V_{CM1} - V_{CM2})\, dt \tag{24}$$

where V_{CMn} is the CM voltage of the nth VSC. The CM inductor can be made smaller by reducing the peak value of the CM flux linkage. The maximum value of the peak CM flux linkage as a function of the modulation index is shown in Fig. D.12.

For SVM, the maximum value of the peak flux linkage increases as the modulation index decreases. Therefore, for applications demanding operation over the full modulation range, the CM inductor has to be designed for the maximum flux linkage, which occurs at low modulation indices. On the other hand, the CM is subjected to maximum flux linkage for a modulation

index $M = 2/3$ if DPWM1 is employed. The proposed PWM scheme has the lowest peak flux linkage, compared to other PWM schemes, for the entire modulation range. As a result, small CM inductor can be realized.

3.2.3 Harmonic Performance and Switching Losses

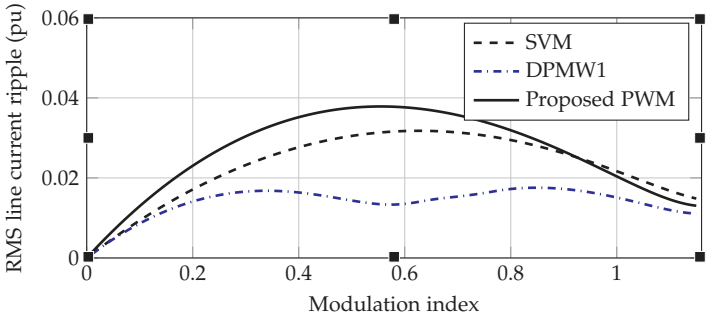


Fig. 28: Total rms value of the line current ripple (normalized) as a function of modulation index.

The variation of the rms value of the line current ripple over the entire modulation range is shown in Fig. D.16. The total rms value of the line current ripple for the proposed PWM scheme closely matches that of the SVM. For SVM, the harmonic content for low modulation indices is slightly less compared to the proposed PWM scheme. On the other hand, the line current quality in the case of the proposed PWM scheme is marginally better than that of the SVM at higher modulation indices (M>0.9).

Although one of the phase legs is clamped to dc-link for one third period of the fundamental cycle in the proposed scheme, an additional commutation is introduced in another leg due to the active vector division. Thus, the switching losses are also evaluated. The switching loss function (SLF) [78] is used to compare the switching losses of the proposed PWM with other PWM schemes. The turn-on and turn-off characteristics of the semiconductor devices are assumed to be linear with respect to time. The contribution of the ripple current towards the switching losses is also neglected. Since the SLF normalizes the switching loss of the proposed method with respect to the switching loss of SVM, the relative error is small despite the simplified loss model [78] used. The SLF for the proposed method is given as

$$\text{SLF} = \begin{cases} 1 + (\frac{2-\sqrt{3}}{2})\cos\phi, & 0 \leqslant |\phi| < \frac{\pi}{6} \\ \cos\phi + \frac{1}{2}\sin\phi, & \frac{\pi}{6} \leqslant |\phi| < \frac{\pi}{3} \\ 2 - (\frac{2\sqrt{3}-1}{2})\sin\phi, & \frac{\pi}{3} \leqslant |\phi| \leqslant \frac{\pi}{2} \end{cases} \tag{25}$$

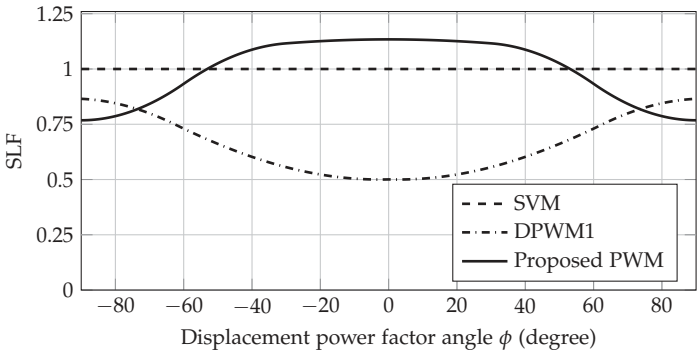


Fig. 29: Comparison of the switching losses.

where ϕ is the displacement power factor angle. The SLFs for the proposed PWM scheme along with that of the SVM and DPWM1 are plotted in Fig. D.17. For the unity power factor applications, the switching losses are minimum if DPWM1 is used. For a displacement power factor angle higher than 53°, the proposed method has lower switching losses compared to that of the SVM. However, for a displacement power factor angle in the vicinity of zero, the proposed method has high switching losses. On the other hand, for the reactive power compensation applications, the use of the proposed PWM scheme results in the lowest switching losses, as shown in Fig. D.17.

3.2.4 Reduced CM Voltage PWM Schemes

The dwell time of the zero voltage vector has significant impact on the peak value of the CM flux linkage λ_{CM} and the peak value of the CM flux linkage λ_{CM} can be reduced by avoiding the use of the zero voltage vector. Several PWM schemes, which do not use zero vectors to synthesize the $\overrightarrow{V}_{ref}$, are reported in the literature [79]. Out of these reported schemes, the most suitable schemes for parallel interleaved VSCs with the proposed integrated inductor are identified and their effect on the λ_{CM} is discussed.

An Active Zero State PWM (AZSPWM) scheme uses two adjacent active voltage vectors and two near opposing active vectors [80–83]. The active voltage vectors that are 120° apart are used in a Remote State PWM (RSPWM) scheme [84]. However, the number of commutations in a switching cycle is increased compared to that of the SVM and may not be feasible in high power applications due to the high switching losses. A Near State PWM (NSPWM) employs three nearest active voltage vectors to synthesize the $\overrightarrow{V}_{ref}$ [85, 86]. Out of these PWM schemes, the AZSPWM and the NSPWM are adopted to modulate the parallel interleaved VSCs because of their superior harmonic

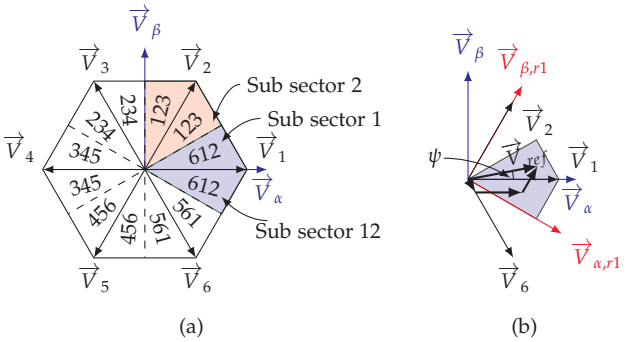


Fig. 30: NSPWM. (a) Switching sequences involved in the near state PWM. Numbers represents the switching sequence, (b) Formation of a reference space vector V_{ref} by the geometrical summation of the three nearest voltage vectors in the region 1.

performance, as discussed hereafter.

Near State PWM:

The NSPWM scheme employs three nearest active voltage vectors to synthesize the reference voltage vector $\overrightarrow{V}_{ref}$. Fig. F.4(a), shows the switching sequences used in the different sectors of the space vector diagram, where the number represents the sequence in which the corresponding voltage vectors are applied. Depending on the switching sequences involved, the space vector diagram is divided into six regions. The switching sequence 612 is used in both sub-sector 1 ($0^\circ \leq \psi < 30^\circ$) and sub-sector 12 ($330^\circ \leq \psi < 360^\circ$) and these two sub-sector together constitute region 1.

The geometrical formation of the $\overrightarrow{V}_{ref}$ in region 1 is depicted in Fig. F.4(b). The active voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_6}$ are used and their respective dwell times are given as

$$T_1 = (\sqrt{3}\frac{V_{\alpha,r}}{V_{\rm dc}} + \frac{V_{\beta,r}}{V_{dc}} - 1)T_s \tag{26a}$$

$$T_2 = (1 - \frac{2}{\sqrt{3}}\frac{V_{\alpha,r}}{V_{\rm dc}})T_s \tag{26b}$$

$$T_6 = (1 - \frac{1}{\sqrt{3}}\frac{V_{\alpha,r}}{V_{\rm dc}} - \frac{V_{\beta,r}}{V_{\rm dc}})T_s \tag{26c}$$

where $V_{\alpha,r}$ and $V_{\beta,r}$ are the α and β components at the start of the region. For the region 1, these components are given as

$$V_{\alpha,r1} = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta\,,\; V_{\beta,r1} = \frac{1}{2}V_\alpha + \frac{\sqrt{3}}{2}V_\beta \tag{27}$$

Let the modulation index M be the ratio of the amplitude of the reference phase voltage to the half of the dc-link voltage. In NSPWM, the value of

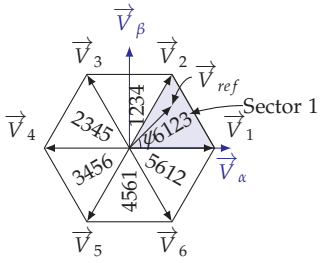


Fig. 31: Switching sequences involved in the active zero state PWM.

M should not fall below 0.769 in order to ensure positive dwell times of the active voltage vectors. Therefore, the modulation index M should be restricted within a range of 0.769 to 1.154, which is sufficient for most grid-connected applications in a normal operating mode. However, the VSC is required to operate in a low modulation index region during the low voltage ride through and AZSPWM is used in this region.

AZSPWM Scheme:

The adjacent active voltage vectors and the two near opposing active voltage vectors are used to formulate the reference voltage vector $\overrightarrow{V}_{ref}$ [80–82]. The switching sequences involved in the AZSPWM are shown in Fig. F.5. The active voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_3}$, and $\overrightarrow{V_6}$ are used in sector 1, and their respective dwell times are given as

$$T_1 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V_{ref}}|}{V_{\mathrm{dc}}} T_s \sin(60^\circ - \psi) \tag{28a}$$

$$T_2 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V_{ref}}|}{V_{\mathrm{dc}}} T_s \sin(\psi) \tag{28b}$$

$$T_3 = T_6 = (T_s - T_1 - T_2)/2 \tag{28c}$$

The dwell time of the adjacent active vectors (T_1, T_2) is the same as that of the conventional SVM. However, instead of using the zero vectors, two near opposing active voltage vectors ($\overrightarrow{V_3}$, $\overrightarrow{V_6}$) are used. As a result, the linear operation over the entire modulation range ($0 \leq M < 2/\sqrt{3}$) is achieved.

The variation in the peak CM flux linkage $\lambda_{CM,pmax}$ with respect to the modulation index M for both the NSPWM and the AZSPWM is plotted in Fig. F.7 and compared with that of the SVM and the DPWM1. The maximum values of the CM flux linkage for the entire linear modulation range for each of the PWM schemes are shown in Table F.2. The CM flux linkage values are normalized with respect to the $V_{\mathrm{dc}}T_s$. Considering the maximum value of the CM flux linkage of the SVM as a base value, the reduction achieved

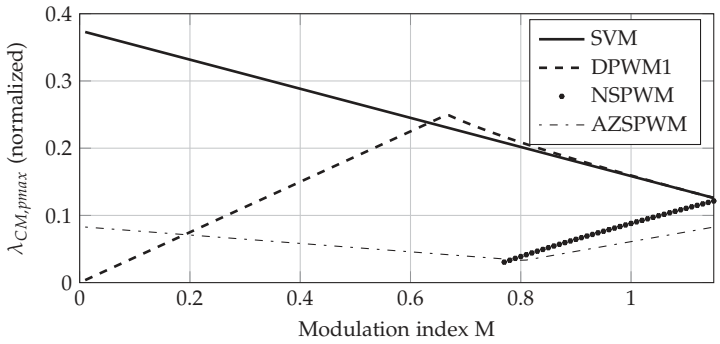


Fig. 32: The variation of the maximum value of the flux linkage in the common leg as a function of the modulation index. The $\lambda_{CM,pmax}$ is normalized with respect to the $V_{\mathrm{dc}}T_s$. For the NSPWM, the $\lambda_{CM,pmax}$ is plotted only for the linear modulation range of $0.769 \leqslant M \leqslant 1.154$.

Table 6: Maximum value of the CM flux linkage over the entire linear modulation range

PWM	Maximum flux-linkage (normalized)	Reduction
SVM	0.37 ($M = 0$)	100%
DPWM1	0.25 ($M = 2/3$)	67%
NSPWM	0.12 ($M = \frac{2}{\sqrt{3}}$)	32%
AZSPWM	0.082 ($M = 0$, $M = \frac{2}{\sqrt{3}}$)	22%

by other PWM schemes is given in Table F.2. A considerable reduction in the maximum CM flux-linkage is achieved using the AZSPWM (78% reduction compared to SVM and 66% reduction compared to the DPWM1). The use of the NSPWM also results in substantial reduction in the maximum value of the CM flux-linkage.

The harmonic performance is evaluated by obtaining Normalized Weighted Total Harmonic Distortion (NWTHD) of the line-to-line voltage, where NWTHD is defined as

$$\mathrm{NWTHD} = \frac{M\sqrt{\sum_{h=2}^{\infty}(V_h/h)^2}}{V_f} \tag{29}$$

The NWTHD for all of the PWM schemes are shown in Fig. F.11. The NWTHD of SVM is the same as that of the AZSPWM. Similarly, the NWTHD in the case of the NSPWM in the linear modulation range ($0.769 \leq M < 2/\sqrt{3}$) is the same as the DPWM1. Although NSPWM is a discontinuous PWM scheme, it demonstrates better harmonic performance compared to the AZSPWM. Therefore, the use of the NSPWM results in improved har-

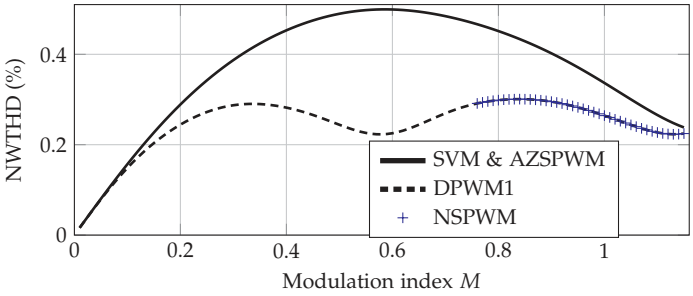


Fig. 33: Theoretical variation of the NWTHD with a modulation index M of the parallel interleaved VSCs with an interleaving angle of 180°.

monic performance and reduced switching losses. In order to operate the VSCs in the full modulation range, AZSPWM in the low modulation index range ($0 \leq M < 0.769$) and NSPWM in the high modulation index range ($0.769 \leq M < 2/\sqrt{3}$) can be used.

3.3 Nearest Three Vector Modulation

For the parallel connected 2L-VSCs, multi-level voltage waveforms can be achieved by interleaving the carrier signals. Therefore, the parallel connected 2L-VSCs can be treated as a multi-level converter. For the multi-level converter, the harmonic profile of the synthesized voltage can be improved by using the Nearest Three Vector (NTV) [40, 87, 88]. For the carrier comparison implementation, NTV can be achieved using the Phase-Disposition (PD) modulator. However, the CI would saturate due to the dc flux injection, if the conventional PD PWM implementation is applied to the parallel VSCs. A PD PWM scheme to ensure flux balancing in the CI and the volt-sec balance to synthesize the reference voltage space vector, even during the band transition is proposed. The proposed implementation uses only a single carrier signal and can easily be implemented using a digital signal processor. The CI saturation issue during the band transition under the PD PWM scheme is also explored and the band strategy to avoid this problem is presented.

The harmonic performance of two parallel interleaved VSCs for all the considered PWM schemes is shown in Fig. 34. The proposed PD modulator demonstrate significant improvement in the harmonic performance. The harmonic performance for three parallel VSCs is also compared and shown in Fig. E.19. The proposed modulator avoids the CI saturation by introducing additional commutation during the band transition, which will increase the switching losses. Therefore, the semiconductor losses in both the cases are evaluated. A 3.45 MW, 690 V converter system with three parallel VSCs is

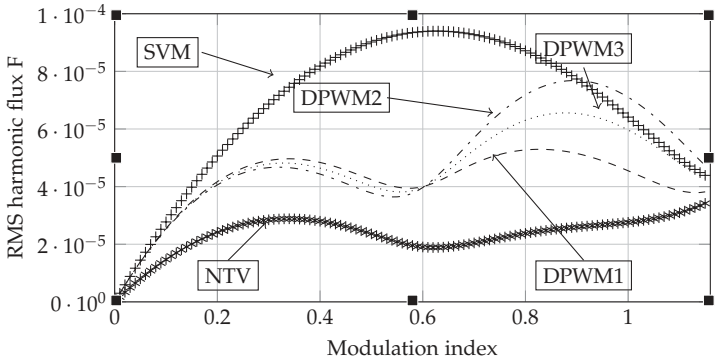


Fig. 34: Harmonic performance comparison of various PWM schemes for two parallel VSCs. The carrier frequency is taken to be the same in all PWM schemes.

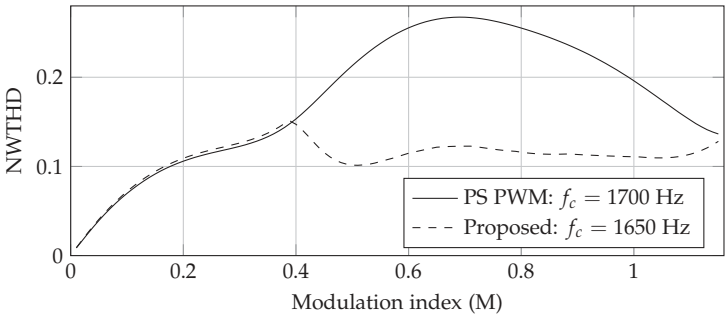


Fig. 35: Harmonic performance of the PS PWM and the proposed scheme, evaluated under the constant loss condition for the full load unity power factor application.

considered as an example system. The VSCs are assumed to be operated to share the equal current. The 1700 V, 1000 A IGBT with anti-parallel diode from Infineon (FF1000R17IE4) is considered. The conduction losses of the IGBT and the diodes, the turn-on and turn-off losses of the IGBTs and the recovery losses of the diodes are calculated using the parameters given in the datasheet. The dc-link voltage is set to be 1100 V. The effects of the junction temperature on the losses is also considered, where the junction-to-case thermal behavior of the IGBTs and the diodes is modeled using the Foster network representation of the thermal equivalent circuit. The case temperature is assumed to be constant at 60°C.

The semiconductor losses are evaluated at full load conditions with a displacement power factor of one. The carrier frequency is taken to be $f_c = 3 \times 1650$ Hz for the proposed scheme. Three 120° phase-shifted carrier

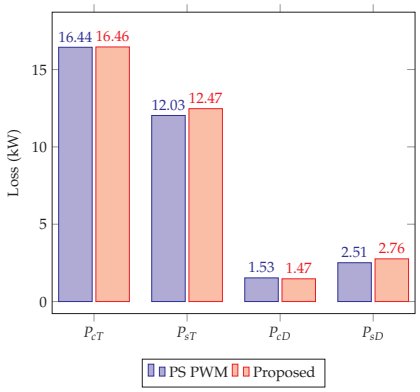


Fig. 36: Total semiconductor losses in the case of the PS PWM and the proposed scheme evaluated at the full load condition with the power factor of one. Switching frequency is 1.65 kHz in both cases. P_{cT}, P_{sT}, P_{cD}, and P_{sD} are the IGBT conduction losses, IGBT switching losses, diode conduction losses, and diode switching losses, respectively.

Table 7: Filter Parameters of the proposed filter and the *LCL* filter

Parameters	Phase-shifted Carriers	Proposed PD modulator
L_f	36 μH	22 μH
L_g	32.6 μH	32.6 μH
$C_f + C_d$	1500 μF	1100 μF

signals with the carrier frequency of 1650 Hz are used for the PS PWM. The total semiconductor losses (of all three VSCs) in both the cases are shown in Fig. E.18. The conduction losses in both the cases are almost the same, whereas the switching losses in the case of the proposed scheme is slightly higher than that of the PS PWM, as expected due to the additional commutations during the band transition. The switching losses in the IGBTs are higher by 0.47 kW, whereas the switching losses in the diodes are higher by 0.25 kW.

In order to evaluate the harmonic performance under the constant loss conditions, the carrier frequency in the case of the PS PWM is increased to 1700 Hz. The NWTHD over the full modulation range is shown in Fig. E.19. As the proposed scheme realizes the PD PWM, it demonstrates a better harmonic performance over a wide modulation indices region ($0.4 \leq M \leq 2/\sqrt{3}$). For the grid connected applications, where the converters typically operates with a modulation index in vicinity to one, the use of the proposed scheme results in the 44% reduction in the NWTHD compared to the PS PWM (at $M = 1$). The PS PWM is marginally better than the proposed

scheme at lower modulation index due to the higher carrier frequency (constant loss condition).

The advantages achieved by the proposed PD modulator is also evaluated for the grid-connected applications. A 3.45 MW, 690 V WECS is considered. The LCL filter with the R_d/C_d damping branch is designed for both the proposed PD modulator and the conventional phase-shifted carrier scheme. The parameters of the designed filter are given in Table 7. The use of the proposed modulator leads to 39% reduction in the value of the inductor and 27% reduction in the shunt capacitance.

4 Magnetic Integration

The circulating current between the parallel VSCs can be suppressed by introducing impedance in the circulating current path. This can be achieved using the CI. Therefore, for interleaved operation of parallel VSCs, two distinct magnetic components may be required:

- Circulating current inductor L_c (CI).
- Line filter inductor L_f (commonly referred to as a boost inductor) for improving the line current quality.

The volume of the inductive components can be reduced by integrating both of these functionalities into a single magnetic component and it is presented in this section. The detailed analysis and results are included in the following appended papers.

- Paper F: An integrated inductor for parallel interleaved VSCs and PWM schemes for flux minimization.
- Paper G: Integrated Inductor for Interleaved Operation of Two Parallel Three-phase Voltage Source Converters.
- Paper H: An integrated inductor for parallel interleaved three-phase voltage source converter.
- Paper I: Magnetic integration for parallel interleaved VSCs connected in a whiffletree configuration.
- Paper J: Optimized harmonic filter inductor for dual-converter fed open-end transformer topology.
- Paper K: Dual converter fed open-end transformer topology with parallel converters and integrated magnetics.

4.1 Integrated Inductor

A three-phase integrated inductor for arbitrary number of parallel interleaved VSCs is proposed. The proposed integrated inductor combines the functionality of both the line filter inductor L_f and the circulating current inductor L_c. The magnetic structure of the proposed three-phase integrated inductor for n number of parallel VSCs is shown in Fig. H.2(a) (n = 4 in the illustration). The magnetic core is composed of three identical magnetic structure belonging to each of the phases of the three-phase system. Such magnetic structure is referred to as a cell. Each cell contains n limbs, magnetically coupled to each other using the yokes, as shown in Fig. H.2(a). Small inherent

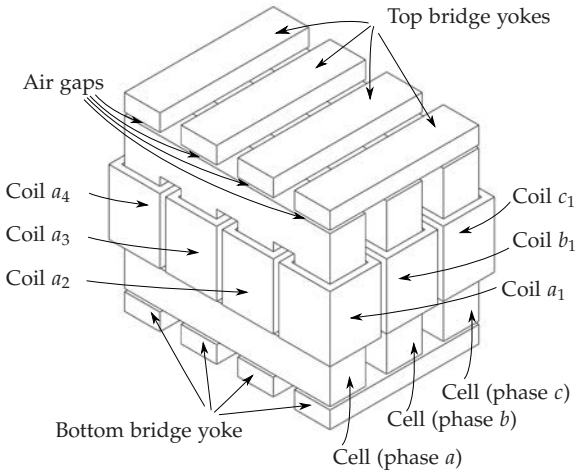


Fig. 37: Magnetic structure of the proposed integrated three-phase inductor for n number of parallel connected VSCs (n = 4 in this illustration).

air gap exists when the limbs and the yokes are arranged together to form the cell structure. Therefore an intentional air gap is avoided (which otherwise may be needed to avoid saturation) to achieve high circulating current filter inductance L_c. Each limb carries a coil having N turns and all the coils are wound in the same direction. For a three phase system, three such cell are used, as shown in Fig. H.2(a). The cells of all the three phases are magnetically coupled using the top and bottom bridge yokes. The necessary air gaps are inserted between the cells and the bridge yokes. The magnetic structure shown in Fig. H.2(a) has six ventilation channels that can be used for guiding the air flow from bottom to top for better cooling. The start terminal of the coils of a cell belonging to phase x is connected to the output terminal of the respective VSC leg x_k of the corresponding phase and the end terminal is connected to a common connection point of that phase x_c.

The line filter inductance offered by the integrated inductor is obtained using the simplified reluctance model and it is given as

$$L_f \approx \frac{\mu_0 N^2 A_g}{2nl_g} \tag{30}$$

where μ_0 is the permeability of the air, A_g is the cross-section area of the air gap, and l_g is the length of the air gap. As it is evident from (H.29), the line inductance value mainly depends on the geometry of the air gap.

The behavior of the circulating current can be expressed as

$$\overrightarrow{\boldsymbol{V_{S_x}}} = \boldsymbol{L_c} \frac{d}{dt} \overrightarrow{\boldsymbol{I_{x,c}}} + V_{x_v o} \tag{31}$$

Table 8: System Specifications

Parameters	Values
No. of parallel VSCs n	3
Power P	15 kW
Switching frequency f_s	1.65 kHz
AC voltage (line-to-line)	400 V
DC-link voltage V_{dc}	650 V
Line filter inductor L_f	0.85 mH

where $\overrightarrow{\boldsymbol{V_{S_x}}}$ is the switched output voltage vector, $\overrightarrow{\boldsymbol{I_{x,c}}}$ is the circulating current vector, $V_{x_v o}$ is the average of the switched output voltages, and $\boldsymbol{L_c}$ is the circulating current inductance matrix and given as

$$\overrightarrow{\boldsymbol{V_{S_x}}} = \begin{bmatrix} V_{x_1 o} & V_{x_2 o} & \dots & V_{x_n o} \end{bmatrix}^T \tag{32}$$

$$\overrightarrow{\boldsymbol{I_{x,c}}} = \begin{bmatrix} I_{x_1,c} & I_{x_2,c} & \dots & I_{x_n,c} \end{bmatrix}^T \tag{33}$$

$$\boldsymbol{L_c} = \begin{bmatrix} (n-1)L_{m_1} & -L_{m_1} & \cdots & -L_{m_1} \\ -L_{m_1} & (n-1)L_{m_1} & \cdots & -L_{m_1} \\ \vdots & \vdots & \vdots & \vdots \\ -L_{m_1} & -L_{m_1} & \cdots & (n-1)L_{m_1} \end{bmatrix} \tag{34}$$

where L_{m_1} is given as

$$L_{m_1} = \frac{1}{n}\frac{N^2}{\Re} = \frac{1}{n}\frac{N^2}{\Re_l + \Re_y} \tag{35}$$

It is evident that L_{m_1} is independent of the air gap geometry and depends only on the reluctances of the limb and yokes (and the reluctance of the inherent air gaps). The value of the L_{m_1} and therefore the inductance offered to the circulating current can be increased by using high permeability magnetic material for the cells.

The advantages offered by the proposed integrated inductor is demonstrated by comparing it with the system with three separate CIs and a three phase line filter inductor L_f for three parallel interleaved VSCs. The system parameters are given in Table H.1. The integrated inductor is designed and build for this system and photograph of the implemented integrated inductor is shown in Fig. I.12. In the case of the conventional solution, separate CI is used for each of the phases. For three parallel VSCs, three limb magnetic structure is required for the CI. Similarly, three limb magnetic structure is also used for the line filter inductor to accommodate all three-phases.

The volume of the different materials in case of both the solutions are

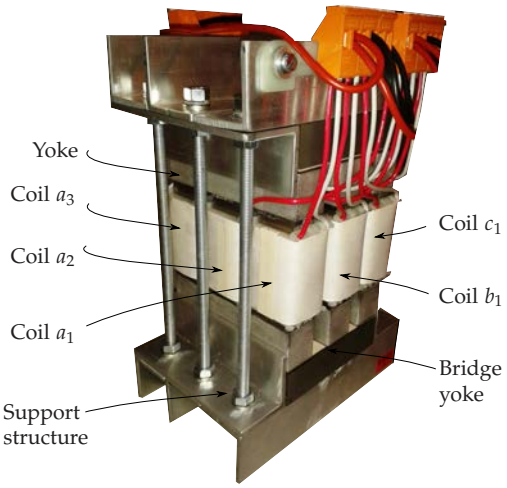


Fig. 38: Photograph of the implemented integrated inductor.

Table 9: Volume comparison of integrated inductor with a combination of three CIs and L_f

Volume (in ltr.)	Integrated inductor	Three CIs + L_f	% Change
Copper	0.322	0.44	73%
Amorphous alloys	1.046	0.947	110%
Laminated steel	0.226	0.470	48%
Total	1.594	1.857	85%

calculated and the results are presented in Table 9. For the system parameters considered in this paper, the use of integrated inductor results in a volume reduction of the copper by 27% and a volume reduction of the laminated steel by 52%. However, the volume of the amorphous alloys increases by 10%. The total volume the integrated inductor is 15% less than that of the state-of-the-art solution.

4.2 Integrated Inductor for Whiffletree Configuration

The integrated inductor presented in previous section is very effective in suppressing the circulating current. However, the magnetic structure is asymmetrical (for more than two limbs). The symmetry can be achieved by using a whiffletree configuration, as shown in Fig. I.3. Two limb CI is used as a basic building block and the filter arrangement is shown in Fig. I.2(b) can be realized using it. Two interleaved VSC legs of a respective phase are magnetically coupled using the CI_H, whereas CI_L used to couple remaining two VSC legs (refer Fig. I.3). The magnetic coupling between these two groups is achieved using the third CI (CI_G). One of the main advantages of the

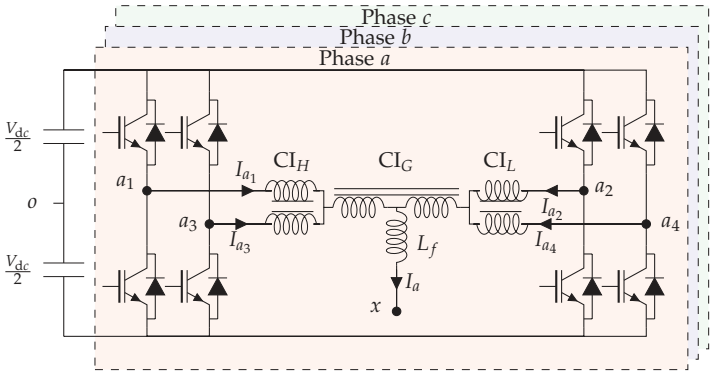


Fig. 39: Whiffletree configuration for parallel interleaved voltage source converters [48].

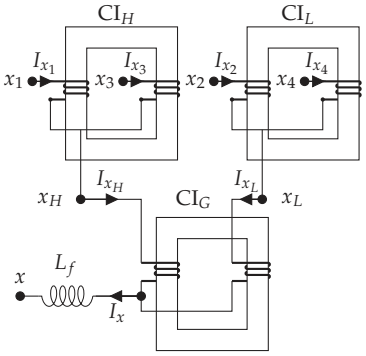


Fig. 40: Whiffletree configuration using the two limb CIs as a basic building block. The subscript x represents phases $x = \{a, b, c\}$.

whiffletree configuration is the magnetically symmetrical structure of all CIs. However, it can only be only used for the even number of parallel VSCs. The integrated inductor is proposed for four parallel VSCs, which combines the functionality of the line filter inductor L_f and the CI_H and the CI_L.

The system comprises of four parallel VSCs with the proposed integrated inductor is shown in Fig. I.4(a). All four VSCs share a common dc-link and the carrier signals are symmetrically interleaved, i.e. the carrier signals are phase shifted from each other by 90°. The carrier signals of the VSC1 and VSC3 are phase shifted by 180° from each other and these two VSCs form the High-Side Converter Group (HSCG). Similarly, VSC2 and VSC4 forms the Low-Side Converter Group (LSCG), and use the carrier signals that are phase shifted from each other by 180°.

The proposed integrated inductor for such systems is shown in Fig. I.5,

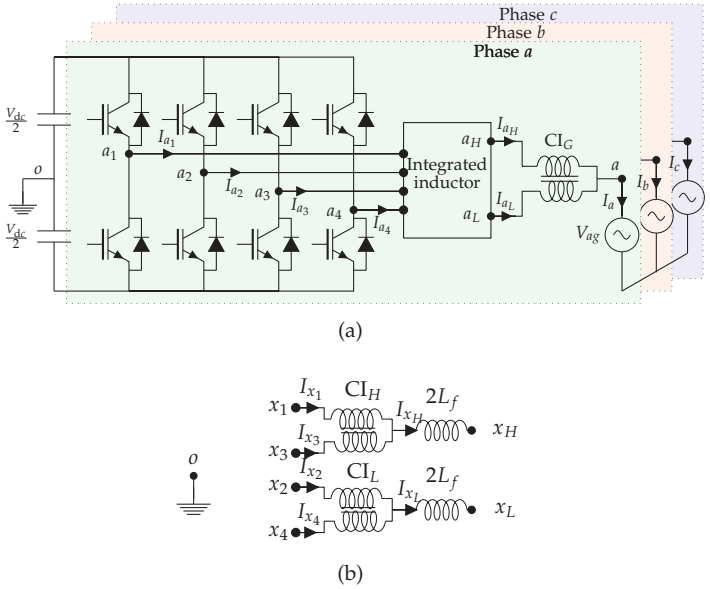


Fig. 41: Four parallel interleaved VSCs with the proposed integrated inductor. (a) System schematic, (b) Equivalent electrical model of the integrated inductor. The subscript x represents phases $x = \{a, b, c\}$

where two different core geometries are shown. The magnetic structure comprises of two cells. The cell is a two limb CI structure and each limb carries a coil with N number of turns. Both of these coils in the given cell are wound in the same direction. The limbs are magnetically coupled to each other using the top and the bottom yokes.

Out of these two cells, one of the cells magnetically couples the interleaved legs of the respective phases of the HSCG, whereas the other cell belongs to the LSCG. The input terminals of the coils of the high-side cell are connected to the output of VSC1 (x_1) and VSC3 (x_3) and the output terminals of these coils are connected together to form the common output x_H. Similarly, the output of VSC2 (x_2) and VSC4 (x_4) are connected to the input terminal of the coils of the low-side cell. Whereas, the other end of the coils are connected together to form the common output terminal x_L. The winding direction of the coils of the high-side cell is opposite to that of the coils of the low-side cell. The high-side and the low-side cells are magnetically coupled to each other using the bridge legs, as shown in Fig. I.5(a). The necessary air gaps have been inserted between the cells and the bridge legs. The output terminals of the HSCG and the LSCG are connected to another CI (CI_G), as shown in Fig. I.4(a).

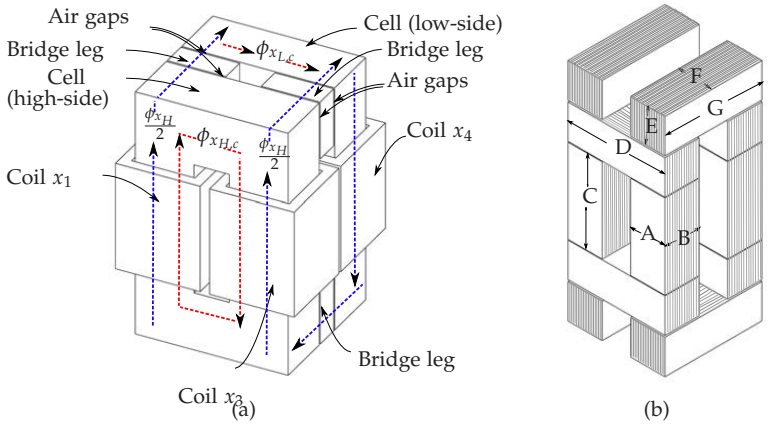


Fig. 42: Magnetic structures of the proposed integrated inductor. Two different arrangements of the bridge legs are shown. Based on the direction of the laminations, one of the arrangement can be used. The subscript x represents the phase, $x = \{a, b, c\}$ (a) Suitable for the ferrite cores. It can be also used when the cells are made from the tape wound core, (b) Suitable for the laminated cores.

Table 10: System Parameters for simulation and experimental studies

Parameters	Values
Total power S	11 kVA
No. of VSCs	4
Interleaving angle	90°
DC-link voltage V_{dc}	650 V
Switching frequency f_s	1250 Hz
PWM scheme	Space vector modulation
Line filter inductance L_f	2.3 mH (0.05 pu)

The prototype of the realized integrated inductor is shown in Fig. I.12(a). The volume of the different active materials of the proposed filter arrangement is compared with the volume of the state-of-the-art solution, shown in Fig. I.2(b) for the the system parameters specified in the Table I.1. Moreover, the losses in the magnetic components in both the cases are also compared.

The bridge legs of the integrated inductor and the line filter inductor in Fig. I.2(b) is assumed to be made from the 0.35 mm laminated silicon steel, whereas the amorphous alloys 2605SA1 is considered as a magnetic material for the cells of the integrated inductor and for the CI_H, CI_L, and CI_G in Fig. I.2(b). As the core losses in the amorphous alloys 2605SA1 is lower compared to the laminated silicon steel, it is used for cells of the magnetic structures

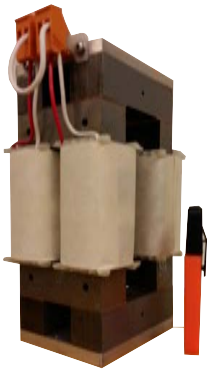


Fig. 43: Pictures of the implemented inductor.

Table 11: Volume comparison of the active materials of the magnetic components in the proposed solution with the state-of-the-art solution shown in Fig. I.2(b)

Material	State-of-the-art	Proposed	% reduction
Amorphous alloy 2605SA1	1.477 Ltr.	1.221 Ltr.	17.3%
Laminated steel	1.28 Ltr.	0.63 Ltr.	49%
Copper	0.385 Ltr.	0.337 Ltr.	12.4 %

which carry the switching frequency circulating flux component. However, the price of the amorphous alloys 2605SA1 is higher compared to the laminated silicon steel. Therefore to reduce the cost, laminated silicon steel is used for the bridge legs, which carry the common flux component with predominant fundamental frequency component. The design of the CI_G that is used to suppress the current between the HSCG and the LSCG is taken to be the same in both cases. The flux densities in the cores and the current density in the coils are taken to be the same in both the cases.

The volume of the different materials in both the cases for all the three phases are given in Table I.5. In the filter arrangement shown in Fig. I.2(b), the windings of the line filter inductor carries full line current and it is completely eliminated in the proposed solution. Therefore, the designer may choose to increase the number of turns in the coils of the integrated inductor to reduce the size of the amorphous alloy. In this comparison, the number of turns in the integrated inductor is taken to be 10% higher than the number of turns in the CI_H and CI_L in the filter arrangement shown in Fig. I.2(b). This results in the 17.3% saving in the amorphous alloy and 12.4% reduction in copper. Furthermore, the volume of the laminated steel is reduced by 49% in the proposed solution.

Table 12: Core and copper losses comparison. The losses of all the three phases are listed.

Item	load	State-of-the-art	Proposed	% reduction
Core losses (W)	0.5 pu	35.6	27.3	23%
	1 pu	39.8	29	27%
Copper losses (W)	0.5 pu	21.5	15.1	29%
	1 pu	76.3	55.8	26%

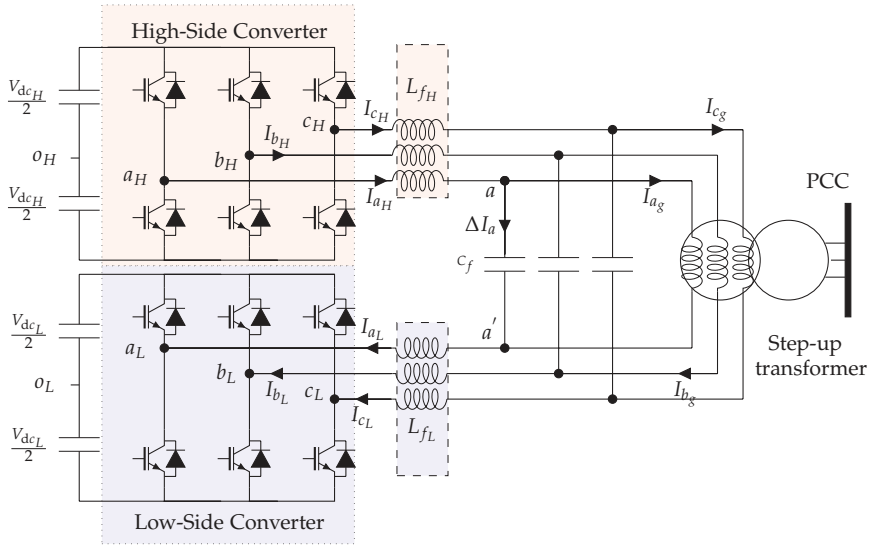


Fig. 44: The system configuration of the dual converter fed open-end winding transformer topology with two separate dc-links. The open-end primary windings are fed from two-level voltage source converters.

The core and the copper losses of the proposed integrated inductor are evaluated and the total losses of all the three integrated inductor (for three phase system) are given in Table I.7. The inductor losses in the case of the state-of-the-art solution are also evaluated at the 50% of the rated load and 100% of the rated load conditions. The losses in the integrated inductor are low compared to the state-of-the-art solution at both the loading conditions. The total losses in the integrated inductors at the rated load conditions are 84.8 W, compared to the 116.1 W in the case of the state-of-the-art solutions (27% reduction).

4.3 Integrated Inductor for Medium Voltage Converters

Many high power converter systems are often connected to the medium voltage network and a step-up transformer is used to match the voltage levels of the converter with the medium voltage grid. In some applications, the transformer is also required for providing galvanic isolation. In such systems, the converter-side windings of the transformer can be configured as an open-end. This open-end transformer winding can be fed from both the ends using the two-level Voltage Source Converters (VSCs) [89], as shown in Fig. J.1. The number of levels in the output voltages is the same as that of the three level Neutral point clamped (NPC) converter and each of the two-level VSC operates with the half of the dc-link voltage than the dc-link voltage required for the three level NPC. This enables the simple and proven two-level VSC to be used in medium voltage applications. For example, converter system connected to the 3.3 kV grid can be realized using the dual-converter with two-level VSCs having a switch voltage rating of 4.5 kV.

An *LCL* filter is commonly used in high power grid-connected applications [90] and one of the possible arrangement of the *LCL* filter for the dual-converter fed open-end transformer topology is shown in Fig. J.1. The leakage inductance of the transformer is considered to be a part of the grid-side inductor of the *LCL* filter. Two VSCs (denoted as High-Side Converter (HSC) and Low-Side Converter (LSC) in Fig. J.1) are connected to a common shunt capacitive branch of the *LCL* filter through the converter-side inductors L_{f_H} and L_{f_L}, respectively. The magnetic integration of the L_{f_H} and L_{f_L} is presented in this paper. As a result of this magnetic integration, the flux in the common part of the magnetic core is completely canceled out. This leads to substantial reduction in the size of the converter-side inductor.

The three-phase three-limb converter-side inductor for both the HSC and the LSC are shown in Fig. J.3(a). These two inductors can be magnetically integrated as shown in Fig. J.3(b), where both the inductors share a common magnetic path. The magnetic structure has six limbs, on which the coils are wound. The upper three limbs belong to the L_{f_H}, whereas the lower three limbs receive the coils corresponding to the L_{f_L}. The upper limbs are magnetically coupled using the top bridge yoke, whereas the lower three limbs are magnetically coupled using the bottom bridge yoke. The upper and the lower limbs share a common yoke, as shown in Fig. J.3(b). The flux components in the common yoke are zero and therefore the common yoke can be completely removed, as shown in Fig. J.3(c). The integrated inductor has only two yokes, compared to four in the case of the separate inductors. As a result, substantial reduction in the volume of the inductor can be achieved through magnetic integration of L_{f_H} and L_{f_L}.

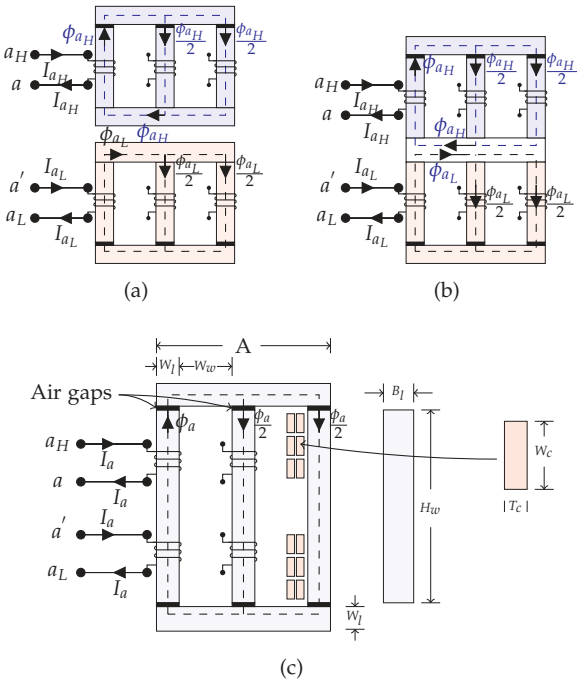


Fig. 45: Magnetic structure. (a) Separate inductors for the HSC and the LSC, (b) Flux cancellation through magnetic integration, (c) Proposed integrated inductor.

Table 13: System specifications

Parameters	Values
Power S	6.6 MVA (6 MW)
Switching frequency f_{sw}	900 Hz
AC voltage (line-to-line) V_{ll}	3300
Rated current	1154 A
DC-link voltage ($V_{\mathrm{dc}_H} = V_{\mathrm{dc}_L}$)	2800 V
Modulation index range	$0.95 \leq \mathrm{M} \leq 1.15$
L_g (including transformer leakage)	525 μH (0.1 pu)

4.3.1 Design Optimization

The design optimization of the integrated inductor for the high power WECS is carried out. The system specifications of the WECS is given in Table 13. The typical wind profile and the power output of a wind turbine over an one year span is shown in Fig. J.8. As it is evident from Fig. J.8, the power

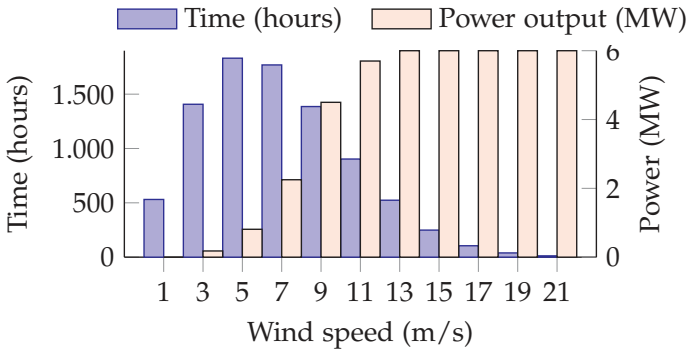


Fig. 46: Wind profile and associated output power of a typical 6 MW wind turbine.

processes by the converter varies in large range and optimizing the inductor for a specific loading condition may result in the suboptimal overall performance. Therefore, instead of optimizing the inductor efficiency at specific loading condition, the energy loss is minimized. In addition to the energy loss minimization, the volume minimization is also considered and multi-objective optimization has been carried out. The energy loss (kWh) per year is calculated using the loading profile and loss modeling and it is used into the optimization algorithm. The multi-objective optimization has been performed, which minimize a vector of objectives $F(X)$ and returns the optimal parameters values of X.

$$\min F(X) \tag{36}$$

where

$$F(X) = [F_1(X), F_2(X)] \tag{37}$$

where $F_1(X)$ returns the energy loss (kWh) and $F_2(X)$ returns the volume of the active parts of the inductor (ltr.). The objective functions $F_1(x)$ and $F_2(x)$ are evaluated for the given set of parameters and specific mission profile. The core losses and the copper loss for each of the specific loading conditions, shown in Fig. J.8, are evaluated. Using this information, the energy loss over one year period is evaluated. Similarly, the volume of both the core and the copper is also calculated.

A non-inferior (Pareto optimal) solution is obtained as shown in Fig. J.10, where the reduction in the energy loss requires increase in the volume. Out of these several possible design solutions, one that suits the application the most, has been selected. The parameter values of the selected design are given in Table J.3.

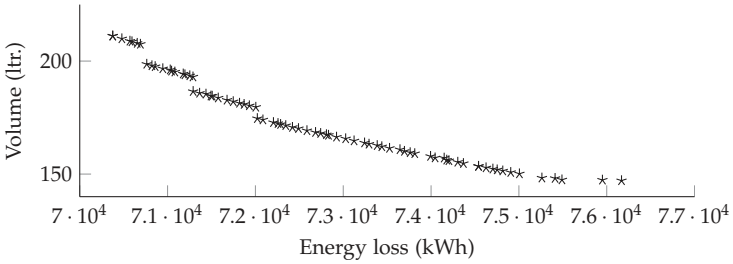


Fig. 47: Calculated volume and energy loss of the integrated inductor for different Pareto optimal solutions.

Table 14: Parameter values of the selected design.

Item	Value	Item	Value	Item	Value
N	25	A_c	30200 mm^2	B_m	1.36 T
W_w	140 mm	J	4.08 A/mm^2	W_c	33 mm
A_{cu}	396 mm^2	H_w	980 mm	k_s	0.92
k_w	0.6	T_c	12 mm	m	2
k_i	0.96	α	1.55	β	1.87

4.3.2 Volumetric comparison

The magnetic integration leads to a reduction in the size of the inductor. This has been demonstrated by comparing the volume of the integrated inductor with the volume of the inductors in a separate inductor case. The values of the current density of the copper, the maximum flux density in the core and the number of turns N are taken to be the same in both the cases. The volume of the magnetic material of the integrated inductor is calculated to be 132.2 ltr, compared to the 177.3 ltr. for the separate inductors. This demonstrates around 25.4% reduction in the magnetic material, which translates to 314 kg reduction in the weight of the magnetic material (assuming the use of the grain oriented steel).

4.4 Medium Voltage Converters with Parallel VSCs

In a dual converter fed open-end transformer topology discussed previously, each of the VSCs has to process the rated current. In many high power applications, single two-level VSC may not be able to supply the rated current. To overcome this problem, parallel connection of the two-level VSCs in each of the converter groups of the open-end transformer topology is proposed, as shown in Fig. K.1. In this way, both the voltage and the current han-

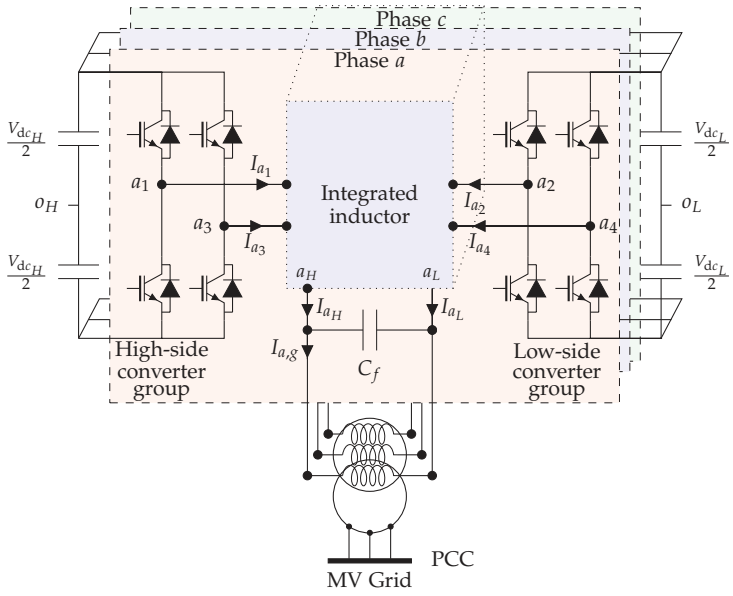


Fig. 48: The system configuration of the dual converter fed open-end winding transformer topology with two separate dc-links. The open-end primary windings are connected to the two converter groups, with each converter groups having two parallel interleaved two-level voltage source converters. The integrated inductor is used to suppress the circulating current between the parallel VSCs of both the converter groups and also used for the line current filtering.

dling capability of the converter can be increased. Moreover, the parallel connected VSCs are operated with the interleaved carrier signals to improve the harmonic quality. The circulating current between the parallel VSCs can be suppressed by providing magnetic coupling between the parallel interleaved legs of the corresponding phases [47, 48, 52]. Therefore, in addition to a line filter inductor, a circulating current filter inductor is also required. A magnetic integration of both the circulating filter inductor and the line filter inductor of both the converter groups is presented.

4.4.1 Magnetic Structure of Integrated Inductor

The physical layout of the proposed integrated inductor is shown in Fig. K.6. The magnetic core is composed of three identical cells for each of the phases of the three-phase system. Each cell has two limbs and these limbs are magnetically coupled to each other using the top, the common, and the bottom yokes. This arrangement forms two windows in each of the cells. Top window provides the space to receive the coils corresponding to the HSCG (coils x_1 and x_3). Similarly, the coils of the LSCG are also placed around the limbs

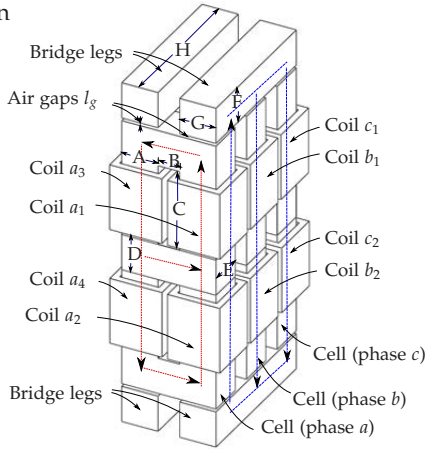


Fig. 49: Physical layout of the proposed integrated inductor.

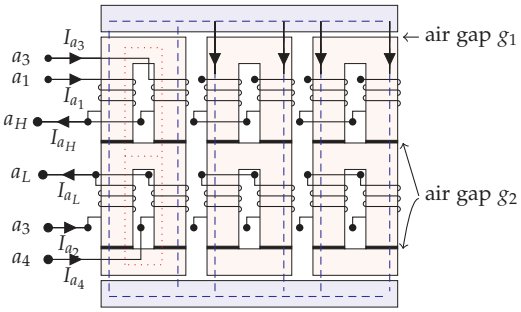


Fig. 50: Magnetic core structure of the integrated inductor. The flux paths are illustrated when the coils of phase a are excited.

and accommodated in the bottom window area of the cell, as shown in Fig. K.6. The cells of all the three phases are magnetically coupled to each other using the bridge legs. Necessary air gaps (g_1 as shown in Fig. K.7) are introduced between the cells and the bridge legs in order provide energy storage to achieve desired value of the converter-side inductor L_f. Similarly small air gaps (g_2 as shown in Fig. K.7) are also provided in the cell structure to obtain the desired value of the circulating current inductance.

The starting terminals of both the coils of phase x, housed in the top window, are connected to the output terminals of phase x of the VSCs of the HSCG (x_1 and x_3), whereas the ending terminals are connected together to from the common connection point x_H, as shown in Fig. K.7. Similarly, the output terminals of the phase x of the VSCs of the LSCG (x_2 and x_4) are connected to the starting terminals of the coils housed in the bottom window and ending terminals are connected to the common point x_L. Both of the coils

Fig. 51: Photograph of the implemented inductor for a 11 kVA prototype.

Table 15: System Parameters for Simulation and Experimental Study

Parameters	Simulation study	Experiment
Power	13.2 MVA (12 MW)	11 kVA (10 kW)
Switching frequency	750 Hz	750 Hz
AC voltage (line-to-line)	3300 V	400 V
$V_{\mathrm{dc}_H} = V_{\mathrm{dc}_L}$	2900 V	350 V
Base impedance	0.825 Ω	14.54 Ω
Base inductance	2.6 mH	46.3 mH
Base capacitance	3.9 mF	0.218 mF
L_f	370 μH (0.14 pu)	6.1 mH (0.135 pu)
L_g	290 μH (0.11 pu)	5 mH (0.11 pu)
$C_f = C_d$	193 μF (0.05 pu)	11 μF (0.05 pu)
L_c	2.2 mH (0.85 pu)	39 mH (0.85 pu)

of the particular converter group are wound in the same direction. However, the direction of the coils of the HSCG cell is opposite to the direction of the coils of the LSCG cell, as shown in Fig. K.7.

The integrated inductor is designed for the 13.2 MVA, 3.3 kV WECS. The system parameters of both the systems are specified in Table K.3. A small scale prototype has been also designed and built as shown in Fig. K.11(c).

The line filter inductor for the high power systems generally requires large air gap and it is often realized by having several discrete air gaps. However, in the case of the proposed integrated inductor, the length of the air gap in the cell structure (l_{g_2}) is limited by the required value of the circulating current inductance. To overcome this issue, two different approaches are presented in the appended paper.

The advantages offered by the integrated inductor is demonstrated by comparing its volume and losses with that of the separate inductor case for the WECS with the system parameters specified in Table K.3. The values

Table 16: Design parameters of the coupled inductor and harmonic filter inductor in the separate inductor case.

Parameter	Turns	Coil current	Core cross-sectional area
Coupled inductor	14	1154 A	32.6×10^{-3} m^2
Line inductor	9	2308 A	47.43×10^{-3} m^2

Table 17: Volumetric comparison in ltr.

Material	Amorphous	Laminated steel	Copper
Separate inductor	336	373	105
Integrated inductor	351	172	62
% change	+ 4.4%	- 53.8%	- 40.9%

Table 18: Core and copper losses of the integrated inductor at different loading conditions

Load	0.25 pu	0.5 pu	0.75 pu	1 pu
Copper losses (kW)	1.03	2.85	5.89	10.17
Core losses (kW)	5.1	5.52	5.88	6.26
Total (kW)	6.13	8.37	11.77	16.43

of the inductance, the flux density, the current density, and the window utilization factor are assumed to be the same in both the cases. Typically the Coupled Inductor (CI) is used to suppress the circulating current between the parallel VSCs and it is considered for circulating current suppression between the parallel VSCs in both the converter groups for the separate inductor case. Each of the converter groups are assumed to have separate line filter inductor with the value $L_f/2$ and with the coil current of $I_x = I_{x_H} = -I_{x_L}$. Two limb magnetic structure is considered for the CI, whereas the line filter inductor is assumed to be realized using the three-phase three-limb inductor. The design parameters of the CIs and the line filter inductors, considered for the separate inductor case, are given in Table K.8.

The line filter inductor is assumed to be made from the grain oriented laminated steel with lamination thickness of 0.35 mm, whereas the use of the amorphous alloys 2605SA1 is considered for the CIs. The volume of the various materials is compared and given in Table K.9. The integrated inductor leads to the 26.2% reduction in the volume of the magnetic material and 40.9% reduction in the volume of the copper.

The core and the copper losses in the separate inductor case are evaluated and given in Table K.10. As evident from Table K.7 and Table K.10, the losses

Table 19: Total core and copper losses for the separate inductors case at different loading conditions

Load	0.25 pu	0.5 pu	0.75 pu	1 pu
Copper losses (kW)	1.55	4.64	9.81	17.04
Core losses (kW)	6.27	7.08	8.12	8.93
Total (kW)	7.82	11.72	17.93	25.97

in the case of the integrated inductor are less compared to the separate inductor case over the whole operating range. This not only increase the system efficiency but also reduces the cooling requirement.

5 Conclusions and Outlook

Different modulation schemes and the filtering solutions for the circulating current suppression for parallel interleaved VSCs have been investigated in this work. The conclusions drawn in this study and the outlook are presented in this section.

5.1 Conclusions

The work carried out during this study has been divided in three categories:

1. Harmonic filter design.
2. Modulation schemes.
3. Integrated inductors.

The concluding remarks for each of these categories are summarized.

5.1.1 Harmonic Filter Design

The impact of the interleaving on the harmonic filter design for the grid-connected applications has been investigated. The analysis has been carried out for the 2.2 MVA, 690 V, gird-connected WECS with two parallel VSCs (refer Table 1 for detailed system specifications). The use of the LCL filter with the R_d/C_d damping branch is considered and it is designed to meet the BDEW harmonic current injection limits. The VSCs are assumed to be modulated using the DPWM1. For two parallel VSCs, the major harmonic components in the resultant switched voltages are concentrated around the 2nd carrier harmonic as against the major harmonic energy concentration around the 1st carrier harmonic in the case of the synchronized gate pulses (without carrier interleaving). As a result, 48% reduction in the value of the filter inductance and 20% reduction in the shunt capacitance of the LCL can be achieved by interleaving the carrier signals. For n number of parallel interleaved VSCs, the major harmonic components are concentrated around the nth carrier harmonic. Therefore, the reduction in the value of the harmonic filter component is more pronounced with increase in the number of parallel VSCs.

Although the LCL filter is commonly employed in WECS, the use of the high-order filter further reduces the value of the harmonic filter components. The high-order filter with the LC trap branch can be achieved by inserting a small inductor in series with the shunt capacitor branch of the LCL filter. For two parallel interleaved VSCs, the major harmonic components are concentrated around the 2nd carrier harmonic, which can be effectively attenuated by choosing the proper values of the LC trap branch parameters (so

that the resonant frequency of the LC trap branch is equal to the 2nd carrier harmonic). The theoretical harmonic solution of the resultant voltages of two parallel interleaved VSCs, modulated using SVM, is derived and the harmonic filter design procedure is illustrated in **paper A**. Compared to the LCL filter, one more inductor in the form of the trap inductor is required. However, the use of the LC trap filter leads to 38% reduction in the inductance and 87% reduction in the capacitance compared to the LCL filter.

The shunt LC trap branch introduces complex conjugate zeros in the admittance transfer function. This leads to a roll-off of -20 dB/decade for the frequency components higher than the resonant frequency of the LC trap branch. As a result, the attenuation offered to the high frequency harmonic components is poor compared to the LCL filter. This issue has been addressed by introducing LC trap branch with the conventional LCL filter. The detailed analysis has been presented in **paper B** and it is demonstrated that good attenuation at both the low and the high frequency harmonic components are achieved with relatively small value of the harmonic filter components.

5.1.2 Modulation Scheme

The PWM scheme has a significant impact on the harmonic performance and the losses in the CI. These performance parameters, for two parallel VSCs modulated using the conventional PWM schemes (both the continuous and the discontinuous), have been evaluated and compared in **paper C**. The use of the symmetrical interleaving (180° interleaving angle) is considered. The carrier frequency is taken to be the same for all the PWM schemes. The DPWM1 demonstrates superior harmonic performance, followed by the DPWM2, the DPWM3, and the SVM. For the same carrier frequency, the number of commutations in the discontinuous schemes are 2/3 times than the continuous scheme. As a result, the use of the discontinuous schemes leads to superior harmonic performance and better semiconductor efficiency.

The impact of the PWM on the core losses in the CI has been also investigated. Amongst the conventional modulation schemes, the DPWM3 incurs lowest core losses in the CI. Whereas, the core losses in the case of the DPWM1 is highest for high modulation indices (for modulation index $M > 0.6$). The core losses in the CI is very critical, specially when the 0.35 mm grain oriented laminated steel is used a core material. A novel PWM scheme to reduce the core losses in the CI is proposed in **paper D**. During the normal operation in most grid-connected applications, the modulation index varies in close proximity to one. For the modulation index of $M = 1$, the use of the proposed PWM scheme leads to 55% reduction in the core losses compared to the SVM. When compared with the DPWM1, 64% reduction in the core losses can be achieved using the proposed PWM scheme. How-

ever, the switching losses are higher compared to the conventional schemes for the unity power factor applications. On the other hand, the proposed PWM scheme demonstrates lowest switching losses for the reactive power compensation applications.

The circulating current between the parallel VSCs can be also suppressed using the CM inductor. The size of the CM inductor depends on the peak value of the CM flux linkage. The PWM scheme proposed in **paper D** also leads to 50% reduction the peak value of the CM flux linkage compared to the DPWM1. Compared to the SVM, 66% reduction in the peak value of the CM flux linkage can be achieved using the proposed PWM scheme. As a result, substantial reduction in the size of the CM inductor can be achieved using the proposed PWM scheme.

The conventional reduced CM voltage PWM schemes are also evaluated for the modulation of the parallel interleaved VSCs with an objective to achieve small size of the CM inductor. A PWM scheme, which employs AZSPWM in the low modulation index range ($0 \leq M < 0.769$) and NSPWM in the high modulation index range ($0.769 \leq M < 2/\sqrt{3}$) is analyzed for two parallel interleaved VSCs in **paper F**. It reduces the maximum value of the CM flux-linkage by 68 % compared to that of the SVM and 52 % compared to that of the DPWM1. The major disadvantage of the reduced CM voltage PWM schemes for the single VSC is the poor harmonic performance. However, it is proven that the magnitude of the harmonic frequency components in the NSPWM is the same as that of the DPWM1 for an interleaving angle of 180°. Similarly, the harmonic performance of the AZSPWM is the same as that of the SVM. Therefore, the use of the NSPWM and the AZSPWM result in size reduction of the CM inductor, without compromising the harmonic performance.

For the parallel connected 2L-VSCs, multi-level voltage waveforms can be achieved by interleaving the carrier signals. Therefore, the parallel connected 2L-VSCs can be treated as a multi-level converter. For the multi-level converter, the harmonic profile of the synthesized voltage can be improved by using the NTV. For the carrier comparison implementation, NTV can be achieved using the PD modulator. However, the CI would saturate due to the dc flux injection, if the conventional PD PWM implementation is applied to the parallel VSCs. A PD PWM scheme to ensure flux balancing in the CI and the volt-sec balance to synthesize the reference voltage space vector, even during the band transition is proposed in **paper E**. Significant improvement in the harmonic performance is demonstrated. Compared to the phase-shifted carrier signals, 39% reduction in the inductance and 27% reduction in the capacitance of the harmonic *LCL* filter can be achieved by using the proposed modulation scheme (for 3.45 MVA, 690 V WECS with three parallel VSCs, having switching frequency of 1.7 kHz).

5.1.3 Integrated Inductor

The circulating current between the parallel VSCs can be suppressed by introducing impedance in the circulating current path. This can be achieved using the CI. Therefore, for interleaved operation of parallel VSCs, two distinct magnetic components may be required:

1. Circulating current inductor L_c (CI).
2. Line filter inductor L_f (commonly referred to as a boost inductor) for improving the line current quality.

The volume of the inductive components can be reduced by integrating both of these functionalities into a single magnetic component.

A three-phase integrated inductor for arbitrary number of parallel interleaved VSCs is proposed in **paper H**. The proposed integrated inductor combines the functionality of both the line filter inductor L_f and the circulating current inductor L_c. Compared to the conventional system with two separate inductors L_c and L_f, the proposed integrated inductor leads to 52% reduction in the volume of the grain oriented laminated steel and 27% reduction in the volume of the copper for three parallel VSCs (with 1.65 kHz switching frequency). However, the magnetic structure is asymmetrical (for more than two limbs). The symmetry can be achieved by using a whiffletree configuration. The integrated inductor for four parallel VSCs, connected in a whiffletree configuration, is proposed in **paper I**. The magnetic structure is analyzed in detail. Both the volume and the losses of the inductive component can be reduced using the proposed solution. Compared to the state-of-the-art solution, 25% reduction in the losses in the inductive component at half of the rated load and 27% reduction at the full load is demonstrated for the system parameters considered in **paper I**.

An integrated inductor for the the dual-converter fed open-end transformer topology is proposed in **paper J**. The dual-converter system often comprises of two identical VSCs. These two VSCs use two separate converter-side inductors for the LCL filter implementation. For the dual-converter system, the output currents of the given phase of both VSCs are equal. This property of the dual-converter system is exploited to cancel out the flux in one of the yokes of both the inductors through the magnetic integration. Moreover, a multi-objective optimization has been performed to identify best possible solutions which leads to the minimization of the energy loss and the volume of the inductor. The size reduction achieved through magnetic integration is demonstrated by comparing the volume of the proposed solution with the separate inductor case. The integrated inductor leads to 25.4% reduction in the volume of the magnetic material. This translates to 314 kg reduction in the weight of the magnetic component for the 6.6 MVA, 3.3 kV WECS system.

Each of the VSCs has to process the rated current in a dual converter fed open-end transformer topology discussed in paper **paper J**. In many high power applications, single two-level VSC may not be able to supply the rated current. To overcome this problem, parallel connection of the two-level VSCs in each of the converter groups of the open-end transformer topology is proposed in **paper K**. The carrier signals of the parallel VSCs are interleaved to improve the harmonic performance. The integrated inductor is also proposed, which suppresses the circulating current between the parallel interleaved VSCs and also offer the desired inductance for the line current filtering. The line filter inductors of both the converter groups are also integrated. The use of the integrated inductor leads to 26.2% reduction in the volume of the magnetic material and 40.9% reduction in the volume of the copper for the 12 MW, 3.3 kV WECS. The integrated inductor is analyzed and the design methodology is proposed. The scheme to control the active and the reactive component of the injected current and the fundamental component of the circulating current is also proposed.

5.2 Outlook

For the interleaved operation of the parallel VSCs, future research may be related to the accurate loss modeling of the integrated inductor, advance control of the circulating current, and discontinuous modulation of the odd number of parallel VSCs.

5.2.1 Core Loss Modeling of the Integrated Inductor

The Improved Generalized Steinmetz Equation (IGSE) has been used to calculate the core losses in this work. The IGSE neglects the effects of the dc bias conditions. However, flux in some parts of the integrated inductor is subjected to the dc bias. Therefore, for future study, the accurate loss model should be used to analyze and evaluate the core losses of the integrated inductor.

5.2.2 Modulation

The switching losses and the size of the circulating current filter can be reduced by using the discontinuous PWM scheme. It is reported in [56] that for two parallel VSCs, the use of the DPWM1 introduces low frequency flux component due to the coexistence of two different zero voltage vectors at the discontinuous points. This may happen due to the fact that the reference space vectors of both the VSCs could lie in two different sectors of the space vector diagram at the discontinuous points. However, it has been demonstrated in this dissertation that the DPWM1 scheme can be employed without such issue if the asymmetrical regular sampling with 180° interleaving angle is

used. However, use of the DPWM1 for the odd number of parallel VSCs may saturate the CI. It may also introduce disturbance in the line-to-line voltage. This issue may be investigated in the future.

5.2.3 Advance Control of the Circulating Current

The carrier interleaving significantly improves the harmonic performance, which leads to the reduction in the size of the harmonic filter components. However, an additional inductive components in terms of the circulating current filters may be required. The CI is commonly employed for suppressing the circulating current and it is important to control the fundamental component of the circulating current to be zero in order to avoid the over sizing/saturation of the CI. The advanced control scheme for controlling the circulating may be investigated in future, which ensures the dc flux component to be zero in each and every sampling interval, even during the transient conditions.

References

[1] M. Baumann and J. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link current balancing," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042–3053, 2007.

[2] Z. Xu, R. Li, H. Zhu, D. Xu, and C. Zhang, "Control of parallel multiple converters for direct-drive permanent-magnet wind power generation systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1259–1270, March 2012.

[3] M. Honbu, Y. Matsuda, K. Miyazaki, and Y. Jifuku, "Parallel operation techniques of gto inverter sets for large ac motor drives," *IEEE Trans. Ind. Appl.*, vol. IA-19, no. 2, pp. 198–205, March 1983.

[4] M. Hashii, K. Kousaka, and M. Kaimoto, "New approach to a high-power gto pwm inverter for ac motor drives," *IEEE Trans. Ind. Appl.*, vol. IA-23, no. 2, pp. 263–269, March 1987.

[5] S. Ogasawara, J. Takagaki, and A. Nabae, "A novel control scheme of a parallel current-controlled PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 5, pp. 1023–1030, 1992.

[6] B. Shi and G. Venkataramanan, "Parallel operation of voltage source inverters with minimal intermodule reactors," in *39th IEEE Industry Applications Conference*, vol. 1, Oct 2004, p. 162.

[7] S. Schroder, P. Tenca, T. Geyer, P. Soldi, L. Garces, R. Zhang, T. Toma, and P. Bordignon, "Modular high-power shunt-interleaved drive system: A realization up to 35 MW for oil and gas applications," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 821–830, March 2010.

[8] T. Geyer and S. Schroder, "Reliability considerations and fault-handling strategies for multi-mw modular drive systems," *IEEE Trans. Ind. Appl.*, vol. 46, no. 6, pp. 2442–2451, Nov 2010.

[9] B. Andresen and J. Birk, "A high power density converter system for the gamesa G10x 4,5 MW wind turbine," in *Proc. European Conference on Power Electronics and Applications, 2007*, Sept 2007, pp. 1–8.

[10] J. Birk and B. Andresen, "Parallel-connected converters for optimizing efficiency, reliability and grid harmonics in a wind turbine," in *Proc. European Conference on Power Electronics and Applications, 2007*, Sept 2007, pp. 1–7.

[11] R. Jones and P. Waite, "Optimised power converter for multi-MW direct drive permanent magnet wind turbines," in *Proc. European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–10.

[12] C.-C. Hua, K.-A. Liao, and J.-R. Lin, "Parallel operation of inverters for distributed photovoltaic power supply system," in *33rd Annual Power Electronics Specialists Conference, pesc 02l*, vol. 4, 2002, pp. 1979–1983.

[13] E. Romero-Cadaval, M. Milanes-Montero, E. Gonzalez-Romera, and F. Barrero-Gonzalez, "Power injection system for grid-connected photovoltaic generation systems based on two collaborative voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4389–4398, 2009.

[14] L. Asiminoaei, E. Aeloiza, J. Kim, P. Enjeti, F. Blaabjerg, L. Moran, and S. Sul, "An Interleaved Active Power Filter with Reduced Size of Passive Components," *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, pp. 969–976.

[15] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[16] P. Xiao, G. Venayagamoorthy, and K. Corzine, "Seven-level shunt active power filter for high-power drive systems," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 6–13, Jan 2009.

[17] J. Chivite-Zabalza, M. Rodriguez Vidal, P. Izurza-Moreno, G. Calvo, and D. Madariaga, "A large-power voltage source converter for FACTS applications combining three-level neutral-point-clamped power electronic

building blocks," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4759–4772, Nov 2013.

[18] J. Reed and N. Sharma, "Large parallel UPS systems utilizing pwm technology," in *International Telecommunications Energy Conference, INTELEC '84.*, Nov 1984, pp. 282–289.

[19] T. Kawabata and S. Higashino, "Parallel operation of voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 24, no. 2, pp. 281–287, Mar 1988.

[20] J. Chen, C. Chu, and C. Huang, "The parallel operation of two UPS by the coupled-inductor method," in *IEEE International Symposium on Industrial Electronics*, May 1992, pp. 733–736 vol.2.

[21] J.-f. Chen and C.-l. Chu, "Combination voltage-controlled and current-controlled PWM inverters for UPS parallel operation," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 547–558, 1995.

[22] T. Wu, Y. Chen, and Y. Huang, "3C strategy for inverters in parallel operation achieving an equal current distribution," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 273–281, 2000.

[23] S. Chiang, C. Lin, and C. Yen, "Current limitation control for multi-module parallel operation of UPS inverters," *IEEE Trans. onElectric Power Applications*, vol. 151, no. 6, 2004.

[24] J. Guerrero, L. Hang, and J. Uceda, "Control of distributed uninterruptible power supply systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2845–2859, 2008.

[25] R. Pena-Alzola, G. Gohil, L. Mathe, M. Liserre, and F. Blaabjerg, "Review of modular power converters solutions for smart transformer in distribution system," in *Energy Conversion Congress and Exposition (ECCE)*, Sept 2013, pp. 380–387.

[26] H. Zhang and L. Tolbert, "Efficiency impact of silicon carbide power electronics for modern wind turbine full scale frequency converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 21–28, Jan 2011.

[27] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[28] J. Muhlethaler, M. Schweizer, R. Blattmann, J. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, 2013.

[29] M. Liserre, R. Cardenas, M. Molinas, and J. Rodriguez, "Overview of multi-MW wind turbines and wind parks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1081–1095, April 2011.

[30] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sept 1981.

[31] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, July 2010.

[32] T. Bruckner, S. Bernet, and P. Steimer, "Feedforward loss control of three-level active npc converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1588–1596, Nov 2007.

[33] F. Blaabjerg and K. Ma, "Future on power electronics for wind turbine systems," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 139–152, Sept 2013.

[34] K. Matsui, Y. Murai, M. Watanabe, M. Kaneko, and F. Ueda, "A pulsewidth-modulated inverter with parallel connected transistors using current-sharing reactors," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 186–191, Apr 1993.

[35] K. Matsui, "A pulsewidth-modulated inverter with parallel-connected transistors by using current sharing reactors," in *proc. IEEE Industry Applications Society Annual Meeting*, 1985, pp. 1015–1019.

[36] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[37] D. Zhang, F. Wang, R. Burgos, R. Lai, T. Thacker, and D. Boroyevich, "Interleaving impact on harmonic current in dc and ac passive components of paralleled three-phase voltage-source converters," in *Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2008, pp. 219–225.

[38] T. Beechner and J. Sun, "Harmonic cancellation under interleaved pwm with harmonic injection," in *IEEE Power Electronics Specialists Conference*, June 2008, pp. 1515–1521.

[39] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[40] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[41] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[42] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "DC-Link Ripple Current Reduction for Paralleled Three-Phase Voltage-Source Converters With Interleaving," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1741–1753, 2011.

[43] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[44] G. Capella, J. Pou, S. Ceballos, G. Konstantinou, J. Zaragoza, and V. Agelidis, "Enhanced phase-shifted pwm carrier disposition for interleaved voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1121–1125, March 2015.

[45] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, 2012.

[46] X. Zhang, D. Boroyevich, and R. Burgos, "Impact of interleaving on common-mode emi filter weight reduction of paralleled three-phase voltage-source converters," in *IEEE Energy Conversion Congress and Exposition*, Sept 2013, pp. 1669–1675.

[47] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[48] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[49] F. Forest, T. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire, "Optimization of the supply voltage system in interleaved converters using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 934–942, 2007.

[50] E. Laboure, A. Cuniere, T. Meynard, F. Forest, and E. Sarraute, "A theoretical approach to intercell transformers, application to interleaved converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 464–474, Jan 2008.

[51] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[52] J. Salmon, J. Ewanchuk, and A. Knight, "PWM inverters using split-wound coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2001–2009, 2009.

[53] R. Hausmann and I. Barbi, "Three-phase DC-AC converter using four-state switching cell," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1857–1867, July 2011.

[54] J. Ewanchuk and J. Salmon, "Three-limb coupled inductor operation for paralleled multi-level three-phase voltage sourced inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1979–1988, 2013.

[55] B. Cougo, T. Meynard, and G. Gateau, "Parallel three-phase inverters: Optimal pwm method for flux reduction in intercell transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug 2011.

[56] K. Xing, F. Lee, D. Borojevic, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, 1999.

[57] D. Zhang, F. Wang, R. Burgos, and D. Boroyevich, "Total flux minimization control for integrated inter-phase inductors in paralleled, interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1679–1688, 2012.

[58] H. Akagi, A. Nabae, and S. Atoh, "Control strategy of active power filters using multiple voltage-source PWM converters," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 3, pp. 460–465, 1986.

[59] R. Wagoner, A. Ritter, and A. Klodowski, "Wind turbine with parallel converters utilizing a plurality of isolated generator windings," Apr. 19 2011, uS Patent 7,928,592. [Online]. Available: https://www.google.com/patents/US7928592

[60] "Geafol,cast-resin transformers, 100 to 16000 kva, catalog tv1," Siemens AG, Power Transmission and Distribution Transformers Division, [Online]. Available: http://www.siemens.com/energy, 2007.

[61] A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, 2011.

[62] S. Araujo, A. Engler, B. Sahan, and F. Antunes, "LCL filter design for grid-connected NPC inverters in offshore wind turbines," in *Proc. Power Electronics, 2007. ICPE '07. 7th Internatonal Conference on*, 2007, pp. 1133–1138.

[63] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sept 2005.

[64] W. Wu, Y. He, and F. Blaabjerg, "An LLCL power filter for single-phase grid-tied inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 782–789, Feb 2012.

[65] Y. Patel, D. Pixler, and A. Nasiri, "Analysis and design of trap and LCL filters for active switching converters," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE), 2010*, July 2010, pp. 638–643.

[66] J. Bloemink and T. Green, "Reducing passive filter sizes with tuned traps for distribution level power electronics," in *Proc. of the 14th European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–9.

[67] J. Xu, J. Yang, J. Ye, Z. Zhang, and A. Shen, "An LTCL filter for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4322–4338, Aug 2014.

[68] A. Cantarellas, E. Rakhshani, D. Remon, and P. Rodriguez, "Design of the LCL+trap filter for the two-level VSC installed in a large-scale wave power plant," in *Proc. Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, Sept 2013, pp. 707–712.

[69] G. Narayanan and V. T. Ranganathan, "Analytical evaluation of harmonic distortion in PWM AC drives using the notion of stator flux ripple," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 466–474, 2005.

[70] G. Narayanan, H. Krishnamurthy, D. Zhao, and R. Ayyanar, "Advanced bus-clamping PWM techniquesbased on space vector approach," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 974–984, 2006.

[71] G. Narayanan, V. T. Ranganathan, D. Zhao, H. Krishnamurthy, and R. Ayyanar, "Space vector based hybrid PWM techniques for reduced current ripple," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1614–1627, 2008.

[72] G. Ortiz, J. Biela, and J. Kolar, "Optimized design of medium frequency transformers with high isolation requirements," in *Proc. 36th Annual Conference on IEEE Industrial Electronics Society, IECON 2010*, Nov 2010, pp. 631–638.

[73] R. Wrobel and P. Mellor, "Thermal design of high-energy-density wound components," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4096–4104, Sept 2011.

[74] A. V. d. Bossche and V. C. Valchev, *Inductors and Transformers for Power Electronics*. Boca Raton, FL: CRC Press, 2004.

[75] B. Cougo, T. Meynard, and G. Gateau, "Parallel Three-Phase Inverters: Optimal PWM Method for Flux Reduction in Intercell Transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[76] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, 2002, pp. 36–41.

[77] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Thirty-Sixth IAS Annual Meeting, IEEE Industry Applications Conference.*, vol. 4, 2001, pp. 2203–2210 vol.4.

[78] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based PWM-vsi drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan 1999.

[79] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, April 2013.

[80] G. Oriti, A. Julian, and T. Lipo, "A new space vector modulation strategy for common mode voltage reduction," in *Proc. of 28th Annual IEEE Power Electronics Specialists Conference*, vol. 2, Jun 1997, pp. 1541–1546 vol.2.

[81] Y.-S. Lai and F.-S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part i: basic development," *IEEE Trans. Ind. Appl.*, vol. 40, no. 6, pp. 1605–1612, 2004.

[82] Y.-S. Lai, P.-S. Chen, H.-K. Lee, and J. Chou, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part ii: applications to im drives with diode front end," *Ind. Appl., IEEE Trans. on*, vol. 40, no. 6, pp. 1613–1620, 2004.

[83] W. Hofmann and J. Zitzelsberger, "PWM-control methods for common mode voltage minimization - a survey," in *Proc. International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006.*, 2006, pp. 1162–1167.

[84] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 469–476, 1999.

[85] A. Hava and E. Un, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008, 2011.

[86] E. Un and A. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 782–793, 2009.

[87] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar 2001.

[88] J. H. Seo, C. H. Choi, and D.-S. Hyun, "A new simplified space-vector pwm method for three-level inverters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul 2001.

[89] G. Grandi, C. Rossi, D. Ostojic, and D. Casadei, "A new multilevel conversion structure for grid-connected pv applications," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4416–4426, Nov 2009.

[90] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 708–719, March 2012.

Part II

Appended Publications

Paper A

Design of the Trap Filter for the High Power Converters with Parallel Interleaved VSCs

Ghanshyamsinh Gohil,
Lorand Bede, Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been published in the
in Proc. 40th Annual Conference on IEEE Industrial Electronics Society, pp.
2030-2036, Oct 2014.

The layout has been revised.

Abstract

The power handling capability of the state-of-the-art semiconductor devices is limited. Therefore, the Voltage Source Converters (VSCs) are often connected in parallel to realize high power converter. The switching frequency semiconductor devices, used in the high power VSCs, is also limited. Therefore, large filter components are often required in order to meet the stringent grid code requirements imposed by the utility. As a result, the size, weight and cost of the overall system increase. The use of interleaved carriers of the parallel connected VSCs, along with the high order line filter, is proposed to reduce the value of the filter components. The theoretical harmonic spectrum of the average pole voltage of two interleaved VSCs is derived and the reduction in the magnitude of some of the harmonic components due to the carrier interleaving is demonstrated. A shunt LC trap branch is used to sink the dominant harmonic frequency components. The design procedure of the line filter is illustrated and the filter performance is also verified by performing the simulation and the experimental study.

1 Introduction

The focus on producing electricity from the renewable energy sources is increasing and Wind Energy Conversion System (WECS) is receiving considerable attention [1]. In order to achieve increased penetration of the wind energy sources, better power quality output and the ability to control the inductive/capacitive reactive power is required [2]. The power electronics converters play a vital role in integrating these energy sources to the power system [3]. The wind turbines with a power rating in Megawatts range are often connected to the power system using full power converter. This converter is often realized using a three-phase two-level Pulse Width Modulated (PWM) Voltage Source Converter (VSC) [2].

The switching frequency of the semiconductor devices, employed in the high power converters, is limited and large filters are often required in order to meet the stringent grid code requirements imposed by the utility [4]. These filters occupy significant amount of space in the overall system [5] and hampers the achievable power density. As a result, the cost of the overall converter system including platform cost [1] increases. Due to the limited power handling capability of the semiconductor switches, the VSCs are often connected in parallel [6–9] to achieve higher power rating and can be operated with interleaved carriers. The interleaved carriers can help reducing the requirement of both ac line filter and dc-link capacitor [10–15].

The phase shift in the respective pole voltages (measured with respect to the center point of the dc link O in Fig. H.4) due to the interleaved carriers, give rise to the high frequency circulating current between the parallel

connected VSCs. This unwanted current introduces additional losses and increases the stress on both the semiconductor devices and the filter components. Therefore, the circulating current should be suppressed by introducing additional impedance in the circulating current path. Using Coupled Inductor (CI) with inverse coupling can effectively reduce the circulating current [12, 16–20]. If the current between the parallel VSCs are shared equally, the fundamental frequency component in flux in the core is zero. As a result, the core is only subjected to the high frequency excitation. The magnetic flux has frequency components concentrated around the odd multiple of the switching frequency. Due to the high frequency operation of the CI, its impact on the power density is minimal.

For the line current filtering, the use of the high order filter is advisable, specially in the high power grid-connected converters. The *LCL* filter is commonly used in the WECS [2]. The design guidelines for the selection of the *LCL* filter parameters is discussed in [21–23]. The converter-side inductor limits the current ripple through the semiconductor switches and the minimum value of this inductor is determined by the maximum value of the allowable switch current ripple. The high value of converter-side inductor and grid-side inductor cause more voltage drop across them and requires high value of the dc-link voltage. The shunt capacitive branch in the *LCL* filter draws reactive power, and it should be made as small as possible. Parallel *RC* damping is often used and selecting the damping capacitor equal to the the filter capacitance is a good design choice [5]. Therefore, small filter capacitance would also result in low reactive current drawn by the damping capacitor and low losses in the damping resistor. Moreover, the value of the filter components can be further reduced by using shunt trap branch, tuned to attenuate the major harmonic components [24, 25].

This paper presents the use of a line filter with *LC* trap branch for the high power WECS, comprised of two parallel interleaved VSCs. The analysis shows that the substantial reduction in the value of the filter parameters can be achieved. The paper is organized as follows: The operation of the parallel interleaved VSCs is briefly described in Section II. The design constraints are stated in Section III. The design of the line filter is given in Section IV. The simulation and the experimental results are finally presented in Section V.

2 System Description

Two parallel interleaved VSCs with a common dc-link is considered for the WECS, and its schematic is shown in Fig. H.4. The pole voltages of phase A of both VSCs for center aligned Space Vector Modulation (SVM) are shown in Fig. B.3. The pole voltages (V_{A10}, V_{A20}) are phase shifted by an interleaving angle. The resultant pole voltage ($V_{A,avg}$) is an average of the individual

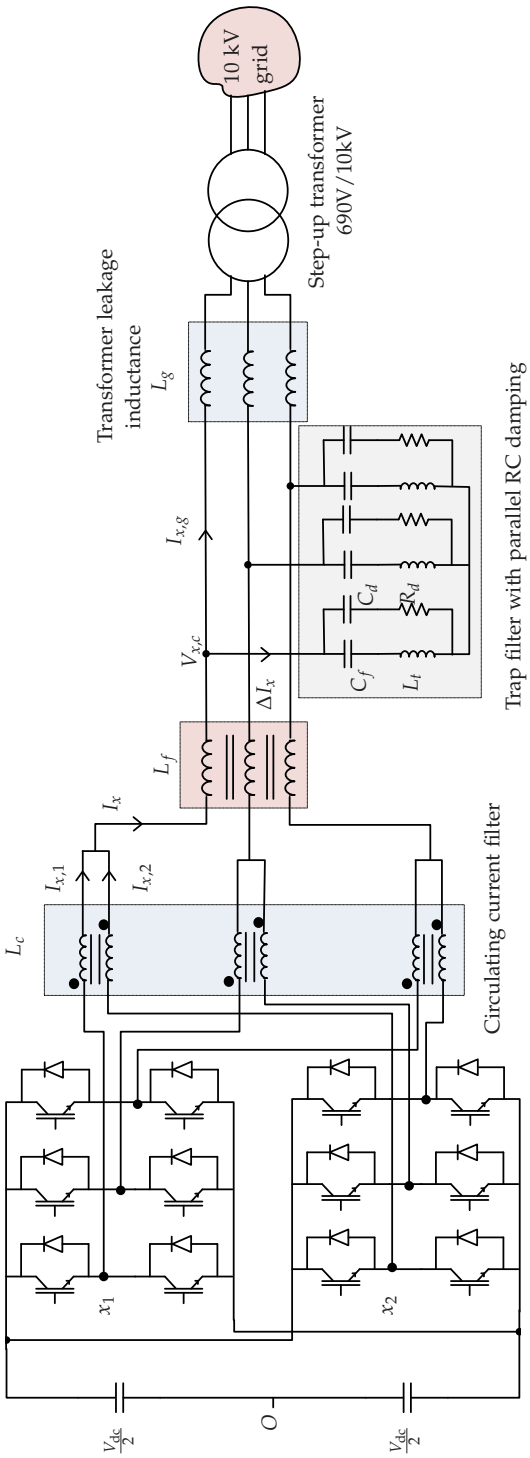


Fig. A.1: Parallel interleaved VSCs with circulating current filter and line filter for WECS. A step-up transformer is used for WECS integration to the 10 kV power system. $x = \{A, B, C\}$.

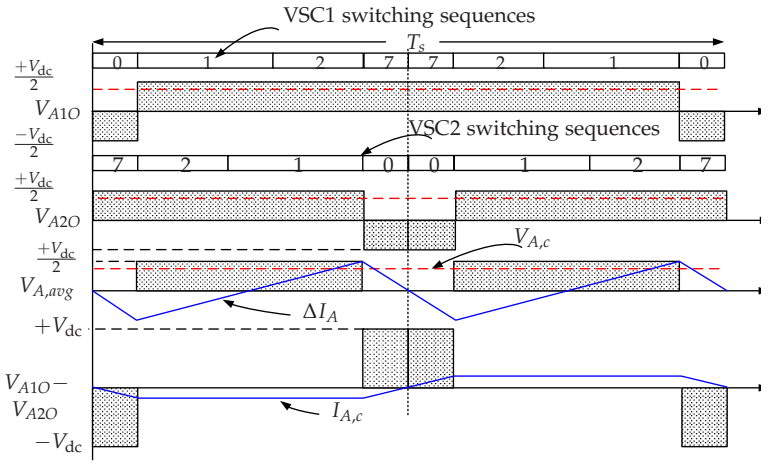


Fig. A.2: Pole voltages and currents of phase A of interleaved VSCs: Modulation index=1 and reference vector angle $\psi = 20°$. The interleaving angle is taken to be 180°.

pole voltages, and it is also depicted in Fig. B.3. The difference between the resultant pole voltage and the voltage across the LC shunt branch appears across the converter side filter inductor L_f. Due to the unipolar nature of the resultant pole voltage, the ripple in the resultant current is small. Moreover, the frequency of the ripple current is two times the switching frequency. As a result the size of the grid side inductor and capacitive filter can be reduced. For a high power, low switching frequency VSCs, this feature greatly helps in meeting the Total Harmonic Distortion (THD) requirement with the small value of the filter components.

2.1 The Circulating Current

The instantaneous voltage difference between the pole voltages give rise to the circulating current and causes additional loss and stress in the semiconductor switches and the passive components. The phase currents $I_{x,1}$ and $I_{x,2}$ have two distinct components. One contributes to the resultant current (I_x), while the other one is the circulating current. Therefore, the phase current can be decomposed into two components, and it is given as

$$\begin{aligned} I_{x,1} &= I_{x1} + I_{x,c} \\ I_{x,2} &= I_{x2} - I_{x,c} \end{aligned} \tag{A.3}$$

where, x = Phase $[A, B, C]$. I_{x1} and I_{x2} are the components of the phase currents contributing to the resultant current and $I_{x,c}$ is the circulating current. Neglecting the effect of the hardware/control asymmetry, the current components of both the VSCs, contributing to the resultant current are considered

$$Amn,1 = \frac{4V_{\mathrm{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{6}\sin[(m+n)\frac{\pi}{2}]\{J_n(q\frac{3\pi}{4}M) + 2\cos(\frac{n\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)\} \\ +\frac{1}{n}\sin(\frac{m\pi}{2})\cos(\frac{n\pi}{2})\sin(\frac{n\pi}{6})\{J_0(q\frac{3\pi}{4}M) - J_0(q\frac{\sqrt{3}\pi}{4}M)\}|n \neq 0 \\ + \sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}\sin\left([m+k]\frac{\pi}{2}\right)\cos\left([n+k]\frac{\pi}{2}\right)\sin\left([n+k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n+3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \\ + \sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}\sin\left([m+k]\frac{\pi}{2}\right)\cos\left([n-k]\frac{\pi}{2}\right)\sin\left([n-k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n-3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \end{pmatrix} \tag{A.1}$$

$$Amn,avg = \frac{4V_{\mathrm{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{6}\cos(m\frac{\pi}{2})\sin(n\frac{\pi}{2})\{J_n(q\frac{3\pi}{4}M) + 2\cos(\frac{n\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)\} \\ + \sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n+k]\frac{\pi}{2}\right)\sin\left([n+k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n+3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \\ + \sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n-k]\frac{\pi}{2}\right)\sin\left([n-k]\frac{\pi}{6}\right) \\ \times\left\{J_k(q\frac{3\pi}{4}M) + 2\cos\left([2n-3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \end{pmatrix} \tag{A.2}$$

where V_{dc} is the dc-link voltage, M is the modulation index, and $q = m + n(\omega_0/\omega_c)$.

---

equal (I_{x1}=I_{x2}) and the resultant current is given as

$$I_x = 2I_{x1} \tag{A.4}$$

The circulating current is given as

$$I_{x,c} = \frac{I_{x,1} - I_{x,2}}{2} \tag{A.5}$$

and the dynamic behavior of the circulating current is described as

$$\frac{dI_{x,c}}{dt} = \frac{V_{x1O} - V_{x2O}}{L_c} \tag{A.6}$$

where L_c is the inductance offered to the circulating current. The CI is used as a circulating current filter in this system. The construction of the CI without any intentional air-gap offers high inductance to the circulating current. As a result, the circulating current is suppressed effectively, which is demonstrated in the experimental results in Section V.

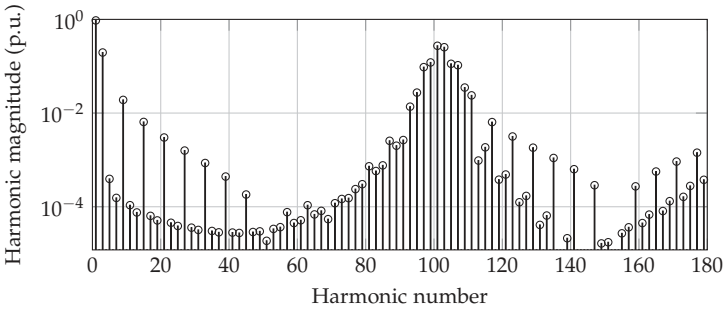


Fig. A.3: Theoretical harmonic spectrum of the average pole voltage of the interleaved VSCs with SVM. The interleaving angle is 180°. The modulation index M=0.95 and ω_c/ω_0 = 51.

2.2 The Grid Current

The resultant current is given as

$$I_x = I_{x,1} + I_{x,2} = I_{x,f} + \Delta I_x \tag{A.7}$$

where $I_{x,f}$ is the fundamental frequency component of the line current and the ΔI_x is the ripple current component. The resultant pole voltage is the average of the individual pole voltages, and it is given as

$$V_{x,avg} = \frac{V_{x1O} + V_{x2O}}{2} \tag{A.8}$$

This difference between the resultant pole voltage and the grid voltage appears across the line filter. To design the line filter, the harmonic spectrum of the $V_{x,avg}$ for a given modulation strategy is required, and it is derived in the following subsection.

2.3 Modulation Scheme and the Average Pole Voltage

The SVM scheme is considered. The theoretical harmonic spectra of the $V_{x,avg}$ for the asymmetrical regular sampled SVM is derived for an interleaving angle of 180°. The pole voltages can be represented as a summation series of sinusoids [26], characterized by the carrier index variable m and the baseband index variable n. The harmonic coefficients in the summation series is given by the double Fourier integral, evaluated in each 60°sextant. The closed form solution for the first VSC is given by (B.7) [26]. The harmonic solution for the second VSC is evaluated for an interleaving angle of 180°. The average of the pole voltages with an interleaving angle of 180°is given by (B.8). From (B.8), it is evident that the contribution to the individual harmonic components from the odd multiple of the carrier frequency components is zero.

This is evident from (B.8), where each summation term has a multiplication factor of $\cos(m\frac{\pi}{2})$. The theoretical harmonic spectra for the average pole voltage is also shown in Fig. B.5(b). The harmonic components in the average pole voltage are mainly concentrated around the even multiple of the carrier frequency. The side-band components of the odd multiple of the carrier frequency harmonics are reduced considerably as a result of the interleaved carriers.

3 Design Constraints

The WECS, connected to the 10 kV medium-voltage network through a step-up transformer, is considered. The grid voltage is assumed to vary by $\pm 10\%$. For grid support functions, the WECS is required to inject inductive/capacitive reactive power within a specified range. An interleaving angle of 180°cancels the dominant first order side band harmonics [14], and it is used in this paper.

3.1 Limits on the Injected Harmonics

The harmonic injection limit, set by the German Association of Energy and Water Industries (BDEW) standard [4, 23, 27] for the renewable energy sources connected to the medium voltage network, is considered in this paper. Based on the Short-Circuit Ratio (SCR) at the point of common coupling, the individual harmonic current injection limit is specified [4]. The grid filter design should ensure that the individual harmonic component in the grid current meets the specified harmonic injection limits for the given switching frequency and the modulation scheme. The SCR of 20 is taken for the filter design in this paper and the limits on the individual harmonic components are calculated on the low voltage side as per BDEW standard.

3.2 Peak Switch Current

The semiconductor switch current rating along with the permissible stress on the semiconductor switch determine allowable the maximum switch current ripple. For the VSC modulated using SVM and operating at unity power factor, the maximum ripple current occurs when the fundamental current component is also at its peak. The voltage difference between the resultant pole voltage and the voltage across the LC trap branch appears across the converter side filter L_f. The time integral of this voltage difference, along with the inductance value of L_f, decides the current ripple in the line current. therefore, the current ripple is a function of the dc-link voltage, the switching frequency, the modulation depth and the converter side inductor L_f, and it is derived hereafter.

Due to the use of discrete vectors to synthesize the reference vector, an error between the applied voltage vector and the reference vector exists. The harmonic flux vector, which is a time integral of the error voltage vector, is directly related to the ripple current [28, 29], and it is used to derive the maximum peak-to-peak current ripple. For phase A, the peak current occurs when the reference vector angle is $\psi = 0^\circ$. At this instant, it is sufficient to evaluate only d-axis current component in order to obtain the phase A current. The d-axis harmonic flux vector is given by

$$\overrightarrow{\boldsymbol{Vd}}_{\boldsymbol{err,1}} T_1 = \tfrac{2}{3} V_{\mathrm{dc}} [\cos\psi - \tfrac{3}{4} M] T_1 \tag{A.9a}$$

$$\overrightarrow{\boldsymbol{Vd}}_{\boldsymbol{err,2}} T_2 = \tfrac{2}{3} V_{\mathrm{dc}} [\cos(60^\circ - \psi) - \tfrac{3}{4} M] T_2 \tag{A.9b}$$

$$\overrightarrow{\boldsymbol{Vd}}_{\boldsymbol{err,z}} T_z = -\tfrac{1}{2} V_{\mathrm{dc}} M T_z \tag{A.9c}$$

where T_1, T_2 and T_z are the dwell time of voltage vector $\overrightarrow{\boldsymbol{V_1}}$, $\overrightarrow{\boldsymbol{V_2}}$ and $\overrightarrow{\boldsymbol{V_0}}$ / $\overrightarrow{\boldsymbol{V_7}}$, respectively. V_{dc} is the dc-link voltage and the M is the modulation index. For $\psi = 0^\circ$, the reference space vector is synthesized by applying the voltage vectors $\overrightarrow{\boldsymbol{V_1}}$ and $\overrightarrow{\boldsymbol{V_0}}$ / $\overrightarrow{\boldsymbol{V_7}}$.

The peak-to-peak ripple current is given as,

$$\Delta I_{x1,pp} = \Delta I_{x2,pp} = \frac{V_{\mathrm{dc}} M (1 - \frac{3}{4} M)}{8 L_f f_s} \tag{A.10}$$

where f_s is the switching frequency. For M=2/3, the peak-to-peak ripple current is maximum. However, for the grid-connected applications, the modulation index is close to one in normal operating condition. The M is minimum when the grid voltage is 0.9 pu. Once the range of M is fixed, the minimum converter side inductance $L_{f,min}$ can be obtained for the desired maximum value of the differential peak-to-peak ripple current from (A.10).

3.3 Active and Reactive Power Consumption of the Shunt Branch

The grid voltage may vary over a range of 1±0.1 pu. The leakage inductance of the step-up transformer often ranges between 4-6%, and it is considered as a part of the grid side inductance L_g. The voltage across the shunt branch, and therefore the losses and the reactive power consumption also depends on the grid side filter inductance in addition to the grid voltage. The reactive power consumption of the shunt branch is maximum when the grid voltage is 1.1 pu and the constraint on the maximum reactive power consumption is evaluated at this voltage level.

The current injected to the grid is controlled, thus the current flowing through the semiconductor switches, the converter side filter inductor L_f

Table A.1: Base values for per-unit system

Parameters	Base Values for analysis	Base Values for experiments
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Voltage	690 V	400 V
Current	1840 A	15.87 A
Frequency	50 Hz	50 Hz
Inductance	688 μH	46 mH
Capacitance	14709 μF	218 μF

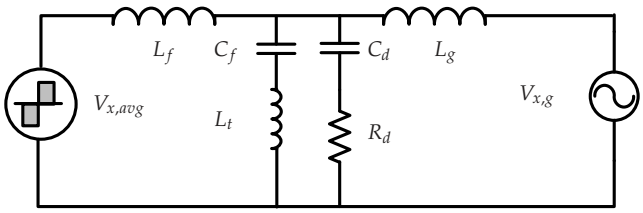


Fig. A.4: Trap filter with parallel R_d/C_d damping.

and the circulating current filter L_c can be reduced by reducing the current through the shunt filter branch. The reactive power consumption of the shunt branch is constrained to 0.05 pu with grid voltage of 1.1 pu. The power loss in the damping resistor R_d is also restricted to 0.003 pu.

4 Filter Design

The filter is designed for a 2.2 MVA system. The analysis and the filter performance is verified by designing a line filter for a small scale setup with a power rating of 11 kVA and performing experiments on the same. The base values for both are given in Table B.1.

The harmonic coefficients for the average pole voltage of the two interleaved VSCs with an interleaving angle of 180°are given by (B.8) and the harmonic spectrum is also plotted in Fig. B.5(b). The effect of the sampling on the harmonic distribution is considered in the analytical expression. However, the system unbalances cause odd harmonics, and the dead-time along with the minimum pulse filter generate even harmonics [21]. To consider the effect of these non-ideal conditions, the safety margin of 20% is considered for each harmonic component during the design stage.

For the two parallel interleaved VSCs, the major harmonic components

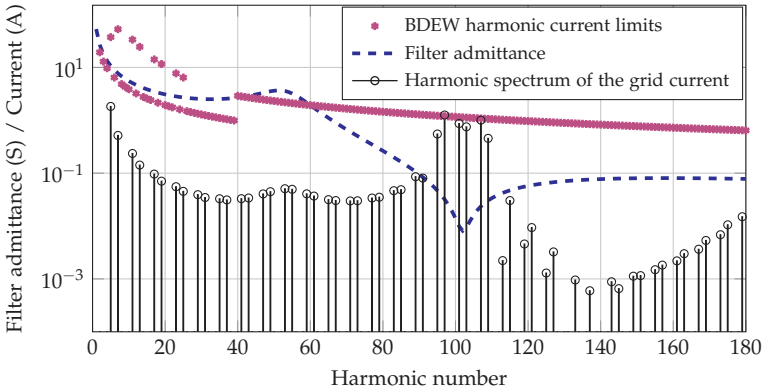


Fig. A.5: Trap filter performance: L_f=0.027 pu, L_g=0.06 pu, $C_f + C_d$=0.02 pu, L_t=0.0094 pu.

are concentrated around the 2nd carrier frequency harmonic, as shown in Fig. B.5(b). Considering the safety margin and the dc-link voltage of 1080 V, the admittance required at 2nd carrier frequency harmonic to meet the BDEW standard is -40 dB. The design constraints of 0.1 pu voltage drop across inductors (both converter-side inductor and grid-side inductor) at fundamental frequency and admittance requirement of -40 dB at the double switching frequency translate in the resonant frequency of the *LCL* filter close to 0.9 kHz. Lower value of the resonant frequency is not desirable, since it requires large value of the filter components and may cause instabilities, if falls within a control bandwidth. Therefore, a *LC* trap branch tuned to attenuate the 2nd carrier frequency harmonic and its side bands is used, instead of the capacitive branch of the *LCL* filter to selectively suppress the dominant harmonic components and it is discussed in the following subsection.

4.1 Trap Filter

In order to provide good attenuation to side bands of the 2nd carrier frequency harmonic, a *LC* trap branch is used as shown in Fig. H.4 and A.4. The parameters of the *LC* trap branch are tuned to resonate at $2 \times f_s$. The choice of values of C_f and L_t affects the quality factor of the trap branch, the peak resonant frequency ω_r, and the reactive power consumption at the fundamental frequency. Assuming the grid to be harmonic free, the filter transfer function for all harmonic components except the fundamental one is given as

$$\frac{I_{x,g}(s)}{V_{x,avg}(s)} = \left(\frac{1}{(L_f + L_g) + \frac{L_f L_g}{L_t}}\right) \frac{s^2 + s\frac{\omega_t}{Q_t} + \omega_t^2}{s(s^2 + s\frac{\omega_r}{Q_r} + \omega_r^2)} \tag{A.11}$$

The resonant frequency of the trap branch ω_t and the resonant frequency ω_r are

$$\omega_t = \frac{1}{\sqrt{L_t C_f}} = 2f_s, \text{ and } \omega_r = \frac{1}{\sqrt{\left(\frac{L_f L_g}{L_f + L_g} + L_t\right) C_f}} \tag{A.12}$$

and the quality factors are

$$Q_t = \frac{1}{R_t}\sqrt{\frac{L_t}{C_f}}, \text{ and } Q_r = \frac{1}{R_t}\sqrt{\frac{L_t(L_f + L_g) + L_f L_g}{C_f(L_f + L_g)}} \tag{A.13}$$

where R_t is the equivalent series resistance of the trap branch. Due to the presence of the complex conjugate poles with the natural frequency of ω_r, the slope of the magnitude plot changes from -20 dB/decade to -60 dB/decade at ω_r. The complex conjugate zeros are located at the natural frequency of ω_t, the slope of the magnitude plot again changes to -20 dB/decade. As per the BDEW standard, the limits on the permissible harmonic current injection up to 180^{th} harmonics are specified. The values of both ω_r and ω_t are chosen to meet the specified harmonic limits. The value of ω_t is taken to be equal to $2 \times f_s$ in order to offer maximum attenuation to 2nd carrier frequency harmonics and its side bands. The selectivity of the trap filter is a measure of its ability to sink any frequencies on either side of the ω_t and the desired selectivity can be obtained by choosing the appropriate values of the LC trap branch. Also the quality factor of the LC trap branch depends on the value of R_t, which is primarily determined by the winding arrangement of the trap inductor L_t.

4.2 Design

The converter side inductor L_f is selected to comply with the constraint imposed on the peak switch current rating. The peak-to-peak current ripple in the semiconductor switches is to be restricted to 0.4 pu. This maximum switch current restriction translates into the converter-side inductance of L_f = 0.027 pu. The transformer leakage inductance is taken to be 0.06 pu, and it is used as the grid side inductor. This leakage inductance is sufficient enough to meet the harmonic requirements. Thus the use of an additional grid-side inductor is avoided. The value of C_f is taken as 0.01 pu. This results in low reactive power consumption. Also the losses in the damping resistor are small. Due to the use of the trap filter, the grid current harmonics around ω_t are reduced. However, the harmonics around ω_r may get amplified. This may violate the BDEW harmonic limits. Thus passive damping is used to avoid resonance in the line filter.

Table A.2: Parameters for simulation and experimental study

Parameters	Simulation study	Experiment
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Switching frequency	2.55 kHz	2.55 kHz
AC voltage (line-to-line)	690 V	400 V
DC-link voltage	1080 V	650 V
L_f	18.6 μH (0.027 pu)	1.3 mH (0.027 pu)
L_g (Transformer leakage)	41.3 μH (0.06 pu)	3.1 mH (0.06 pu)
Filter capacitor C_f	147 μF (0.01 pu)	2.2 μF (0.01 pu)
Trap inductor L_t	6.62 μH (0.0094 pu)	464 μH (0.0094 pu)
Damping capacitor C_d	147 μF (0.01 pu)	2.2 μF (0.01 pu)

The R_dC_d parallel damping structure [22] is adopted due to it's easy realization [5], and it is shown in Fig. A.4. The selection of the damping branch components affects the reactive power consumption and the power loss. The values of C_d and R_d are optimized to reduce the active and reactive power consumption with the required damping at ω_r. The theoretical harmonic spectrum of the grid current is derived and the filter parameters are chosen to limit the individual harmonic current injection within a specified limit. The magnitude plot of the filter transfer function, along with the theoretical harmonic spectrum of the grid current are plotted in Fig. A.5.

5 Simulation and Experimental Results

The parameters used for the simulation and the experimental studies are given in Table K.3. The simulation results are shown in Fig. C.9, where the waveforms corresponding to phase A are depicted. The circulating current is effectively suppressed by using the CI, as shown in Fig. A.6(b). Therefore, $I_{A,1} \approx I_{A,2}$ and only phase A current of VSC1 is presented, as shown in Fig. C.9(a). The resultant current is the summation of the individual currents, and it is also depicted in Fig. A.6(c). The *LC* trap branch effectively sinks the harmonic frequency components around the $2 \times f_s$. As a result, the desired grid current quality is achieved, as shown in Fig. J.17.

The experiments have been performed on a small scale laboratory setup with the filter parameters specified in Table. K.3. The AC power source (MX-35) from California Instruments is used as a harmonic free grid emulator. The 3.1 mH inductor is used to mimic the transformer leakage inductance. The rated active power is injected into the grid at the unity power factor. The experimental results are depicted in Fig. H.16. The circulat-

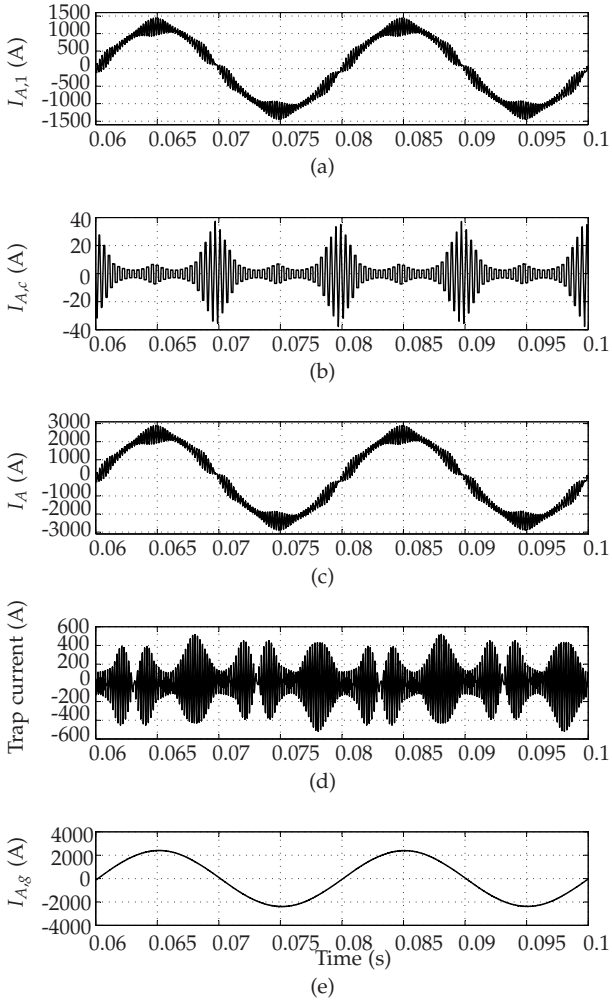
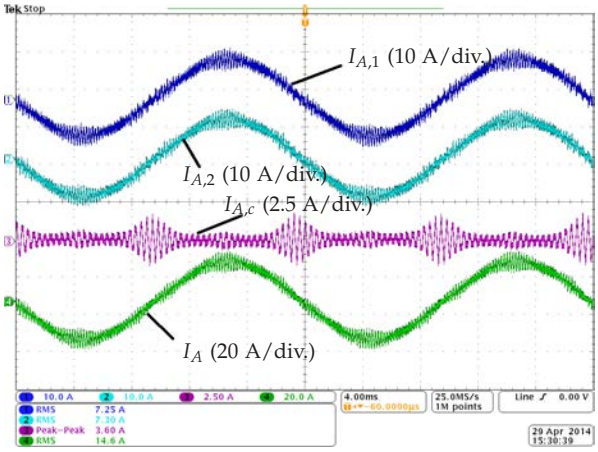
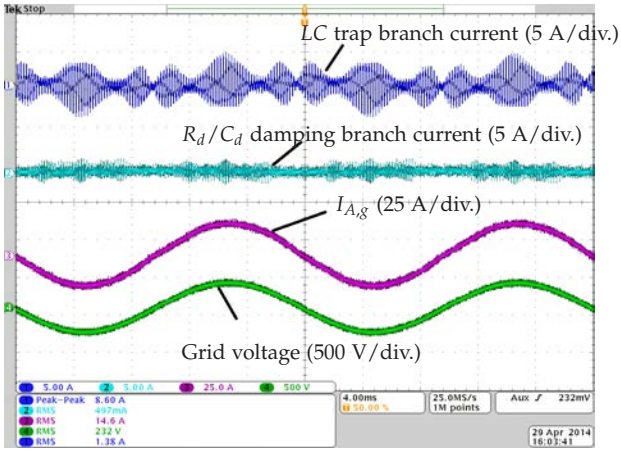


Fig. A.6: Simulated VSC currents of phase A with asymmetrical regular sampled SVM. (a) VSC1: Phase A current, (b) Circulating current, (c) Resultant current, (d) Current in trap branch, (e) Grid current.

ing current is effectively suppressed by using the CI, and it is shown in Fig. A.7(a). The currents through the trap branch and the damping branch are shown in Fig. A.7(b). The THD of the grid current is measured to be 1.9 %. The harmonic spectrum of the measured grid current is shown in Fig. A.8 along with the specified harmonic current injection limits. Almost all harmonics are within the allowable limits. However, some of the harmonics around the $2f_s$ are violating the limits due to the high value of ac resistance



(a)



(b)

Fig. A.7: The experimental results for phase A are obtained at full load with unity power factor.

of the trap branch R_t.

6 Conclusion

The filter design for the high power converter using parallel interleaved VSCs is demonstrated. The 2.2 MVA, 690V WECS is considered for the analysis. The theoretical harmonic solution of the average pole voltage of two interleaved VSCs, modulated using SVM with an interleaving angle of 180°is

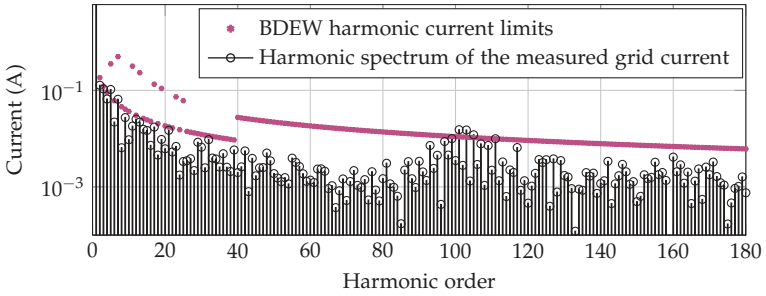


Fig. A.8: The filter performance verification: Harmonic spectrum of the measured grid current.

derived. Due to the interleaving the major harmonics in the average pole voltage is concentrated around the twice of the carrier frequency. The filter with *LC* trap branch is designed to restrict the individual harmonic injection within the limit prescribed by the BDEW standard. The desired harmonic performance is achieved with a small value of the converter-side inductor. The transformer leakage inductance is used as a grid-side inductance and the use of any additional inductor on the grid-side is avoided. The capacitor requirement in the shunt branch is 0.02 pu, which results in low reactive power consumption and low losses in the damping branch.

References

[1] M. Liserre, R. Cardenas, M. Molinas, and J. Rodriguez, "Overview of multi-MW wind turbines and wind parks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1081–1095, April 2011.

[2] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 708–719, March 2012.

[3] Z. Chen, J. Guerrero, and F. Blaabjerg, "A review of the state of the art of power electronics for wind turbines," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1859–1875, Aug 2009.

[4] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[5] J. Muhlethaler, M. Schweizer, R. Blattmann, J. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, 2013.

[6] M. Baumann and J. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link current balancing," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042–3053, 2007.

[7] B. Andresen and J. Birk, "A high power density converter system for the gamesa G10x 4,5 MW wind turbine," in *Proc. European Conference on Power Electronics and Applications, 2007*, Sept 2007, pp. 1–8.

[8] J. Birk and B. Andresen, "Parallel-connected converters for optimizing efficiency, reliability and grid harmonics in a wind turbine," in *Proc. European Conference on Power Electronics and Applications, 2007*, Sept 2007, pp. 1–7.

[9] R. Jones and P. Waite, "Optimised power converter for multi-MW direct drive permanent magnet wind turbines," in *Proc. European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–10.

[10] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[11] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[12] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[13] T. Bhavsar and G. Narayanan, "Harmonic analysis of advanced bus-clamping PWM techniques," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2347–2352, 2009.

[14] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[15] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[16] F. Forest, T. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire, "Optimization of the supply voltage system in interleaved converters using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 934–942, 2007.

[17] R. Hausmann and I. Barbi, "Three-phase multilevel bidirectional DC-AC converter using three-phase coupled inductors," in *Proc. IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, Sept 2009, pp. 2160–2167.

[18] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[19] B. Cougo, T. Meynard, and G. Gateau, "Parallel Three-Phase Inverters: Optimal PWM Method for Flux Reduction in Intercell Transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[20] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, 2012.

[21] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sept 2005.

[22] P. Channegowda and V. John, "Filter optimization for grid interactive voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4106–4114, Dec 2010.

[23] A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, 2011.

[24] Y. Patel, D. Pixler, and A. Nasiri, "Analysis and design of trap and LCL filters for active switching converters," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE), 2010*, July 2010, pp. 638–643.

[25] W. Wu, Y. He, and F. Blaabjerg, "An LLCL power filter for single-phase grid-tied inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 782–789, Feb 2012.

[26] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[27] S. Araujo, A. Engler, B. Sahan, and F. Antunes, "LCL filter design for grid-connected NPC inverters in offshore wind turbines," in *Proc. Power Electronics, 2007. ICPE '07. 7th Internatonal Conference on*, 2007, pp. 1133–1138.

[28] G. Narayanan, H. Krishnamurthy, D. Zhao, and R. Ayyanar, "Advanced bus-clamping PWM techniquesbased on space vector approach," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 974–984, 2006.

[29] G. Narayanan, V. T. Ranganathan, D. Zhao, H. Krishnamurthy, and R. Ayyanar, "Space vector based hybrid PWM techniques for reduced current ripple," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1614–1627, 2008.

Paper B

Line Filter Design of Parallel Interleaved VSCs for High Power Wind Energy Conversion Systems

Ghanshyamsinh Gohil,
Lorand Bede, Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been published in the
IEEE Transactions on Power Electronics Vol. 30, no. 12, pp. 6775-6790, Dec 2015.

The layout has been revised.

Abstract

The Voltage Source Converters (VSCs) are often connected in parallel in a Wind Energy Conversion System (WECS) to match the high power rating of the modern wind turbines. The effect of the interleaved carriers on the harmonic performance of the parallel connected VSCs is analyzed in this paper. In order to achieve low switching losses, the 60° clamp Discontinuous PulseWidth Modulation (DPWM1) is used to modulate the VSCs. A step-by-step design procedure of the line filter, which ensures the desired harmonic performance under all operating conditions, is presented. The analytical harmonic solution for the two parallel interleaved VSCs is derived in order to obtain the worst case voltage magnitude of the individual harmonic components. The required value of the filter admittance for the specific harmonic component is obtained by using the worst case voltage magnitude and the allowable harmonic injection limit. In order to achieve the desired filter performance with optimal values of the filter parameters, the use of a LC trap branch with the conventional LCL filter is proposed. The expressions for the resonant frequencies of the proposed line filter are derived and used in the design to selectively choose the values of the line filter components. The analysis and design methodology are also verified experimentally.

1 Introduction

The power electronics converters play a vital role in integrating a wind turbine into the power system [1]. The full scale power converter is often used in modern Wind Energy Conversion System (WECS) due to its ability to provide the reactive power compensation and a smooth grid connection for the entire speed range, and it is generally realized using three-phase two-level pulsewidth modulated Voltage Source Converter (VSC) [2]. The general trend is to use the wind turbines with high output power (megawatt scale) [3] and the switching frequency of the semiconductor devices employed in these systems is often limited [4]. Therefore, large filters are required in order to meet the stringent power quality requirements imposed by the utility [5]. These filters occupy significant amount of space in the overall system [6]. Moreover, considerable losses occur in the filter components and the overall conversion efficiency is compromised if large filter components are used [4]. They also result in increased cost of the overall converter system [7]. Therefore, the filter size should be made as small as possible to achieve efficient, compact and cost-effective WECS system.

Due to the limited power handling capability of the existing semiconductor devices, the two level VSCs are often connected in parallel [8–11] to match the high power rating of the wind turbine. The parallel connected VSCs can be operated with interleaved carriers to reduce the value of the filter components [12–18]. However, the carrier interleaving results in common-mode

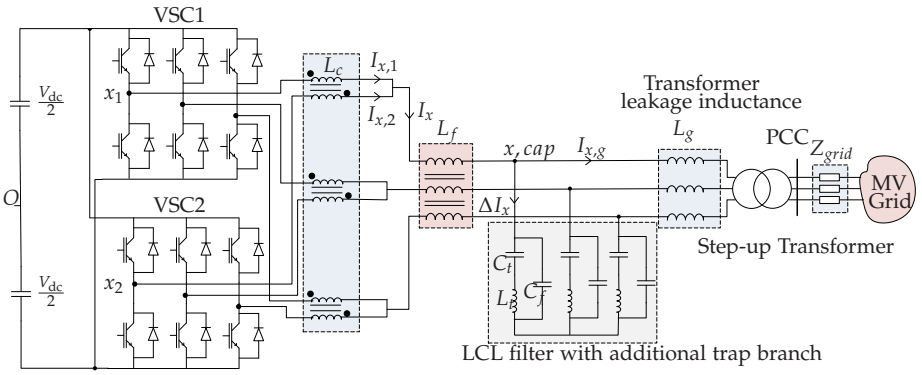


Fig. B.1: The grid side converter of the WECS, comprised of two parallel VSCs with interleaved carriers, connected to the medium voltage network by using a step-up transformer. $x = \{A, B, C\}$

voltage difference across the parallel VSCs. If the conventional three limb three-phase differential mode inductor is used without any additional circulating current filter, high common-mode circulating current flows as there is no high permeability magnetic path available for the common-mode flux in the three limb three-phase differential mode inductor [19]. Another approach is to use the single phase inductor, which acts as both the circulating current filter and the line filter and permits the use of the interleaved carriers without having any additional circulating current filter. However, the use of the single phase inductor does not bring any advantages in terms of size reduction of the filter components [20] and a dedicated filter to suppress the circulating current is often required.

The use of the parallel interleaved VSCs for the active power filter application is presented in [13, 14], where a common-mode inductor is employed to suppress the circulating current and the reduction in the size of the passive components is demonstrated. A use of Coupled Inductor (CI) for suppressing the circulating current is presented in [21] and substantial size reduction of the filter components can be achieved by using the CI over the single phase line inductor solution [20]. However, the control complexity increases as the precise control over the fundamental frequency circulating current is required in order to avoid the saturation of the CI [22].

Some of the harmonic components that are present in the switched output voltage of the individual VSCs can be canceled by using the interleaved carriers. Miller *et al.* [12] studied the line current harmonic cancellation effect of N parallel interleaved VSCs. The effects of the PulseWidth Modulation (PWM) scheme, the interleaving angle, and the modulation indices on the line current quality are analyzed in [15]. The optimal interleaving angle to improve the line current quality is discussed in [16]. Mao *et al.* [17] presented

a hybrid PWM scheme, involving multiple switching sequences and different interleaving angles to improve the line current quality.

The interleaved carriers in the parallel VSCs can reduce the filtering requirement by phase shifting some of the harmonic components and thus fully or partially cancel their contribution in the line current. Further reduction in the values of the filter components can be achieved by using a high-order filter [23]. The LCL filter is an attractive option [24–26], and it is commonly used in the WECS [2]. For the LCL filter, the admittance transfer function is given as

$$Y_{LCL}(s) = \left.\frac{I_g(s)}{V_{PWM}(s)}\right|_{V_g=0} = \frac{1}{L_f L_g C_f}\frac{1}{s(s^2+\omega_{r,LCL}^2)} \tag{B.1}$$

where L_f is the converter side inductor, L_g is the grid side inductor, C_f is the filter capacitor, I_g is the grid current, V_g is the grid voltage, and V_{PWM} is the switched voltage of the VSC. The resonant frequency of the LCL filter is given as

$$\omega_{r,LCL} = \sqrt{\frac{L_f + L_g}{L_f L_g C_f}} \tag{B.2}$$

Due to the presence of the complex conjugate poles, the roll-off of the high frequency components (higher than the $\omega_{r,LCL}$) is -60 dB/decade. Therefore, the LCL filter offers good attenuation to the high frequency harmonic components, and it can effectively reduce the differential mode electromagnetic interference (above 150 kHz) [24]. The switched voltages at the VSC terminals have harmonic components concentrated around the multiple of the carrier frequency. Due to the limited switching capability of the semiconductor devices used in the high power applications, a fairly high value of the filter components are required for the LCL filter to attenuate the major harmonic components (first carrier frequency and its sideband harmonics).

The value of the filter components can be reduced by using a LC trap branch, which is tuned to attenuate the major carrier harmonics and its sideband harmonics. This can be realized by inserting an inductor in series with the capacitor of the LCL filter [27]. The use of the LC trap branch to attenuate the sideband harmonic components around the carrier frequency is proposed in [27, 28]. The multiple LC trap branches are used, to attenuate the carrier harmonic and its sideband harmonic components around the carrier frequency and its multiple, in [29, 30]. The admittance transfer function of the line filter with the LC trap branch, commonly known as trap filter, is given as

$$Y_{trap}(s) = \left(\frac{1}{(L_f + L_g) + \frac{L_f L_g}{L_t}}\right)\frac{s^2+\omega_t^2}{s(s^2+\omega_{r,trap}^2)} \tag{B.3}$$

The resonant frequencies are given as

$$\omega_t = \frac{1}{\sqrt{L_t C_f}}$$
$$\omega_{r,trap} = \frac{1}{\sqrt{\left(\frac{L_f L_g}{L_f + L_g} + L_t\right) C_f}} \tag{B.4}$$

where L_t is the inductor inserted in series with the capacitor C_f of the LCL filter. From (B.4), it is evident that the $\omega_{r,trap}$ is less than the ω_t. Due to the introduction of the complex conjugate zeros, the roll-off of the high frequency components (higher than the ω_t) is -20 dB/decade. This leads to a poor attenuation of the high frequency harmonic components. On the contrary, the LCL filter offers good attenuation to the high frequency harmonic components. Therefore, the LC trap branch along with the LCL filter can be used to achieve the desired filtering performance (both at the low and the high frequency components) with small values of the filter components. The use of such a filter for single VSC is presented in [31]. However, the high frequency attenuation is compromised due to insertion of the damping resistor in series with the capacitive branch.

The VSCs are often connected in parallel in the WECS and the use of interleaved carriers to fully or partially cancel the effect of some of the harmonic frequency components is proposed in this paper. The design procedure of the LCL filter with additional LC trap branch of two parallel interleaved VSCs is presented. The paper is organized as follows: the operation of the parallel interleaved VSCs is briefly described in Section II. The analysis of the proposed high-order line filter is discussed in Section III and the filter design constraints along with the step-by-step design procedure are presented in Section IV. The simulation and the experimental results are finally presented in Section V to verify the analysis.

2 Parallel Interleaved Voltage Source Converters

The carrier signals, of the parallel connected VSCs in WECS (shown in the Fig. H.4), are interleaved to reduce the value of the filter components. The effect of the interleaved carriers on the operation of the parallel VSCs is analyzed in this section.

The interleaved operation of the parallel VSCs:

1. Improves the line current quality.
2. Reduces the switch current ripple of each VSC, provided the circulating current is suppressed effectively.

Therefore, the value of the filter components can be reduced. However, additional inductive filter is required to suppress the circulating current. A CI is used as a circulating current filter [15, 20–22, 32–34] due to its effectiveness in suppressing the circulating current. Multiple parallel interleaved VSCs with magnetic coupling between the parallel interleaved legs of the corresponding phase can be realized using the following configurations [21]:

1. Whiffletree configuration.
2. Cyclic cascade configuration.
3. Using a magnetic structure with multiple parallel magnetic limbs.

In addition to suppress the circulating current, the CI also performs the function of averaging the switched output voltage of the parallel interleaved legs [21]. The values of the line filter components depend on the magnitude of the individual harmonic component in the average output voltage, which is the same in all of the above mentioned CI configurations. Therefore, the line filter design can be carried out independently, without considering the circulating current filter arrangement.

In this paper, the WECS with two parallel interleaved VSCs is considered. However, the line filter design approach, presented in this paper, can be used for any number of parallel interleaved VSCs. The use of the LC trap branch with the conventional LCL filter is proposed. The converter side inductor L_f, the grid side inductor L_g, and the capacitor C_f forms the LCL filter. The series connection of the L_t and C_t forms the LC trap branch. The WECS is connected to a medium voltage network by using a step-up transformer. The leakage inductance of a step-up transformer often ranges from 0.04-0.06 pu [35], and it is considered as a part of the grid side inductance L_g.

The interleaving angle of 180° is used as it results in optimal harmonic performance at high modulation indices [16]. The closed form analytical solution to determine the individual voltage harmonic components of the pulsewidth modulated voltage is derived. Moreover, the relationship between the maximum value of the switch current ripple and the converter side inductor is also obtained in this section.

2.1 Modulation Scheme

The 60° clamp discontinuous PWM (DPWM1) [36] scheme clamps the output terminals of the VSCs to the positive and the negative terminals of the dc-link for a 60° interval each in a fundamental cycle, as shown in Fig. B.2. The clamping intervals of 60° are arranged around the positive and negative peak of the fundamental reference voltage. For the applications, where the displacement power factor is close to unity, the switching is avoided when

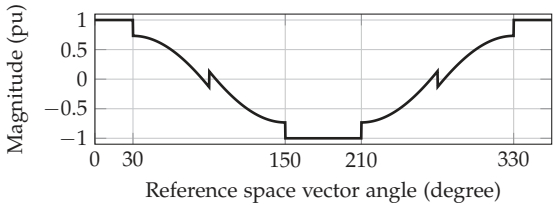


Fig. B.2: Modulation waveform of 60° clamp PWM (DPWM1) scheme with modulation index $M = 1$.

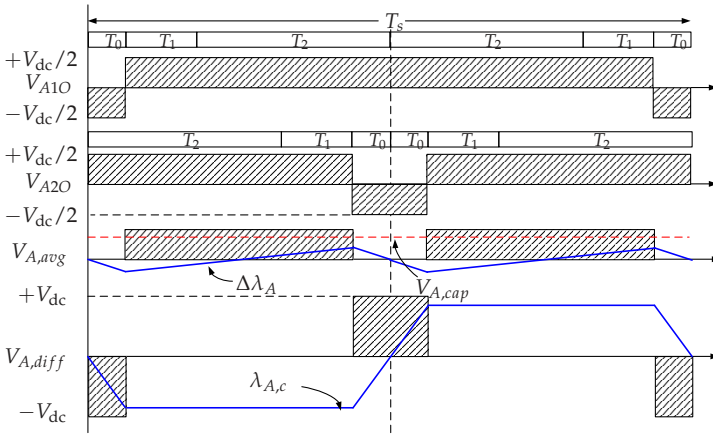


Fig. B.3: The effect of the interleaved carriers. The pole voltages of phase A of the individual VSCs and their average $V_{A,avg}$ and difference $V_{A,diff}$ are depicted. The modulation index is M=1, the interleaving angle is 180° and the reference space vector angle is $\psi = 45°$.

the current through the devices is near its peak [37]. In addition to the active power, the WECS is also required to provide reactive power within a power factor range of 0.95 leading to 0.95 lagging. In this case, the use of the DPWM1 would result in the switching losses reduction up to 45% compared to that of the continuous space vector modulation [38].

2.2 Voltage Harmonic Distortion

As a result of the interleaved carriers, the pole voltages (measured with respect to the dc-link midpoint O in Fig. H.4) of the VSC2 are phase shifted by the interleaving angle with respect to that of the VSC1. The pole voltages of phase A of two interleaved VSCs are shown in Fig. B.3. The resultant switched voltage is an average of the individual pole voltages. The difference between the average of the pole voltages and the grid voltage ($V_{A,avg} - V_{A,g}$)

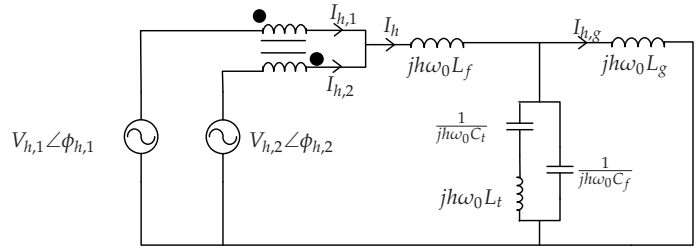


Fig. B.4: The equivalent circuit of the h^{th} harmonic with two parallel interleaved VSCs ($h \neq 1$).

appears across the line filter, whereas the difference in the pole voltages ($V_{A10} - V_{A20}$) is the potential across the circulating current filter L_c. The equivalent circuit of the hth harmonic component with two parallel interleaved VSCs is shown in Fig. B.4. The harmonic components in the grid current depend on the magnitude of the individual harmonic components in the average pole voltage and the line filter admittance. Therefore, the magnitude of the individual harmonics components of the average pole voltage is derived hereafter.

As a result of the modulation, the pole voltages have undesirable harmonic components in addition to the desired fundamental component. This harmonic components can be represented as the summation series of sinusoids [36], characterized by the carrier index variable m and the baseband index variable n and it is given as

$$\begin{aligned} f(t) =& \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n}\cos(n[\omega_0 t + \theta_0]) + B_{0n}\sin(n[\omega_0 t + \theta_0])] \\ &+ \sum_{m=1}^{\infty} [A_{m0}\cos(m[\omega_c t + \theta_c]) + B_{m0}\sin(m[\omega_c t + \theta_c])] \\ &+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} [A_{mn}\cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0]) \\ &\qquad + B_{mn}\sin(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0])] \end{aligned} \tag{B.5}$$

The hth harmonic component is defined in terms of m and n, and it is given as

$$h = m(\frac{\omega_c}{\omega_0}) + n \tag{B.6}$$

where ω_0 is the fundamental frequency and ω_c is the carrier frequency.

The harmonic coefficients A_{mn} and B_{mn} in (F.27) are evaluated for each 60° sextant using the double Fourier integral. The closed form theoretical harmonic solution for the first VSC for asymmetrical regular sampled DPWM1

is evaluated and it is given as

$$Amn1 = \frac{4V_{\mathrm{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{3} J_n(q\frac{\pi}{2}\sqrt{3}M)\cos(\frac{n\pi}{6})\sin[(m+n)\frac{\pi}{2}]\cos(\frac{q\pi}{2}) \\ +\frac{1}{2n}\sin(\frac{n\pi}{6})\Big(\sin[(q+m)\frac{\pi}{2}] - \cos(n\pi)\sin[(q-m)\frac{\pi}{2}]\Big)|n \neq 0 \\ +\frac{1}{n}\sin(\frac{n\pi}{6})\cos(\frac{n\pi}{3})J_0(q\frac{\pi}{2}\sqrt{3}M) \\ \Big(\sin[(q+m)\frac{\pi}{2}]\cos(n\pi) - \sin[(q-m)\frac{\pi}{2}]\Big)|n \neq 0 \\ +\sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k} J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n+k)\frac{\pi}{6}]\cos[(2n+k)\frac{\pi}{6}] \\ \Big(\cos[(n+k)\pi]\sin[(k+q+m)\frac{\pi}{2}] + \sin[(k-q+m)\frac{\pi}{2}]\Big) \\ +\sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k} J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n-k)\frac{\pi}{6}]\cos[(2n-k)\frac{\pi}{6}] \\ \Big(\cos[(n-k)\pi]\sin[(k+q+m)\frac{\pi}{2}] + \sin[(k-q+m)\frac{\pi}{2}]\Big) \end{pmatrix} \tag{B.7}$$

The coefficients in (B.7) contains $J_y(z)$, which represents the Bessel functions of the first kind of the order y and argument z. The carrier signal for the second VSC is phase shifted by an interleaving angle of 180°. The theoretical harmonic solution for the second VSC is also evaluated. The magnitude of the individual harmonic components is the same in both of the VSCs. However, some of the harmonic components in the pole voltage of VSC2 are in phase opposition to that of the VSC1. As a result, these harmonic components do not appear in the harmonic spectra of the average pole voltage.

The theoretical closed form harmonic solution of the average pole voltage is given as

$$Amn,avg = \frac{4V_{\mathrm{dc}}}{q\pi^2} \times \begin{pmatrix} \frac{\pi}{3} J_n(q\frac{\pi}{2}\sqrt{3}M)\cos(\frac{n\pi}{6})\cos(\frac{m\pi}{2})\sin(\frac{n\pi}{2})\cos(\frac{q\pi}{2}) \\ +\frac{1}{2n}\sin(\frac{n\pi}{6})\sin(\frac{q\pi}{2})\cos(\frac{m\pi}{2})[1-\cos(n\pi)] \\ [1-2\cos(\frac{n\pi}{3})J_0(q\frac{\pi}{2}\sqrt{3}M)]|n \neq 0 \\ +\sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k} J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n+k)\frac{\pi}{6}]\cos(\frac{m\pi}{2})\cos[(2n+k)\frac{\pi}{6}] \\ \Big(\cos[(n+k)\pi]\sin[(k+q)\frac{\pi}{2}] + \sin[(k-q)\frac{\pi}{2}]\Big) \\ +\sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k} J_k(q\frac{\pi}{2}\sqrt{3}M)\sin[(n-k)\frac{\pi}{6}]\cos(\frac{m\pi}{2})\cos[(2n-k)\frac{\pi}{6}] \\ \Big(\cos[(n-k)\pi]\sin[(k+q)\frac{\pi}{2}] + \sin[(k-q)\frac{\pi}{2}]\Big) \end{pmatrix}$$

where V_{dc} is the dc-link voltage, M is the modulation index, and $q = m + n(\omega_0/\omega_c)$. (B.8)

The harmonic spectrum for the modulation index $M = 0.95$ is also depicted in Fig. B.5(b). The double summation term in (F.27) is the ensemble of all possible frequencies, formed by taking the sum and the difference between the carrier harmonics, the fundamental waveform and its associated baseband

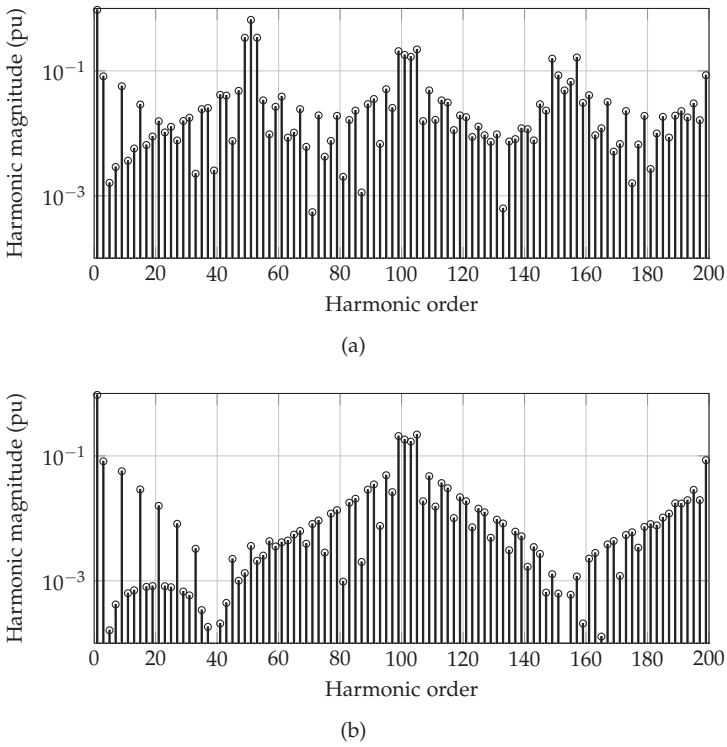


Fig. B.5: Theoretical harmonic spectrum with the modulation index $m = 0.95$ and pulse ratio $\omega_c/\omega_0 = 51$. (a) Harmonic spectrum of the pole voltage of the individual VSC, (b) Harmonic spectrum of the average pole voltage of the interleaved VSCs with an interleaving angle of 180°.

harmonics [36]. Careful examination of (B.8) reveals that the $\cos(\frac{m\pi}{2})$ term appears as a multiplication factor in each summation term. As a result, the harmonic coefficients in (B.8) are zero for all the odd multiple of the carrier index variable m. Therefore, the side band harmonics around the odd multiple of the carrier harmonic frequencies are reduced. This is evident from Fig. B.5(b), where the pulse ratio is $\omega_c/\omega_0 = 51$. The magnitude of the harmonic components around the $51th$ harmonic and its odd multiple is reduced considerably compared to that of the individual VSC, as shown in Fig. B.5. Also the magnitude of all even harmonic components is negligible. This happens due to the presence of the $\sin(\frac{n\pi}{2})$ as a multiplication term in the nth order Bessel function, as given in (B.8).

2.3 Switch Current Ripple

The switch current ripple influences the design of both the passive and the active components. Therefore, the maximum value of the peak-to-peak switch current ripple for interleaved VSCs is derived in this subsection. Due to the phase symmetry, only the current through the semiconductor devices of phase A is analyzed.

Even when the carriers are not interleaved, small circulating current flows due to the hardware and control asymmetries. Due to the interleaved carriers, this current further increases. Therefore, the switch currents $I_{x,1}$ and $I_{x,2}$ have the following two distinct components:

1. The component contributing to the resultant line current
2. The circulating current

and the switch current can be given as

$$\begin{aligned} I_{x,1} &= I_{x1} + I_{x,c} \\ I_{x,2} &= I_{x2} - I_{x,c} \end{aligned} \tag{B.9}$$

where, x = phase $[A, B, C]$. I_{x1} and I_{x2} are the components of the switch currents contributing to the resultant line current and $I_{x,c}$ is the circulating current. By neglecting the effect of the hardware and the control asymmetries, the line current is assumed to be shared equally between the VSCs ($I_{x1} = I_{x2}$). From (F.2), the circulating current can be given as

$$I_{x,c} = \frac{I_{x,1} - I_{x,2}}{2} \tag{B.10}$$

and the dynamic behavior of the circulating current can be described as

$$\frac{dI_{x,c}}{dt} = \frac{V_{x1O} - V_{x2O}}{L_c} \tag{B.11}$$

where L_c is the inductance offered to the circulating current. A CI is used as a circulating current filter due to its effectiveness in suppressing the circulating current. The CI is constructed without introducing any intentional air gap in the magnetic flux path. As a result, it offers high inductance to the circulating current and thus the contribution of the circulating current towards the switch current can be neglected. This assumption is also verified by the experimental studies given in section V.

The resultant current I_x is assumed to be shared equally between the VSCs and by neglecting the contribution of the circulating current, the switch current is given as

$$\begin{aligned} I_{x,1} = I_{x,2} &\approxeq \frac{I_x}{2} \\ &\approxeq \frac{I_{x,f}}{2} + \frac{\Delta I_x}{2} \end{aligned} \tag{B.12}$$

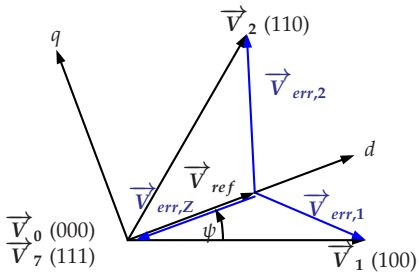


Fig. B.6: The active and the zero vectors to synthesize a given reference vector and corresponding error voltage vectors.

where $I_{x,f}$ is the fundamental frequency component of the line current and the ΔI_x is the ripple current.

2.4 Ripple Component of the Resultant Line Current ΔI_x

The switch current ripple is half of the ripple component of the resultant line current ΔI_x and the relationship between the ΔI_x and L_f is derived in this sub-section. In the interest of brevity, following assumptions are made:

1. The grid voltage is assumed to be free from the harmonic distortions.
2. The fundamental component of the switch current is assumed to be in phase with the fundamental component of the reference voltage.

The reference space voltage vector is synthesized using the discrete voltage vectors such that the volt-second balance is maintained. The difference between the applied voltage vector and the reference space vector is known as the error voltage vector, and it is illustrated in Fig. J.6. The harmonic flux vector is a time integral of this error voltage vector, and it is directly proportional to the ripple current [39–41]. For the parallel interleaved VSCs, the flux linkage in the converter-side inductor L_f is the average of the harmonic flux vectors of the individual VSCs.

The harmonic flux vector can be decomposed into d-axis and q-axis components. For the unity power factor operation, the switch current ripple for phase A becomes maximum for the reference space vector angle $\psi = 0^\circ$. At this instant, the ripple current of phase A can be obtained by only evaluating the d-axis component of the harmonic flux vector, and it is given as

$$\overrightarrow{Vd}_{err,1} T_1 = \tfrac{2}{3} V_{\mathrm{dc}} [\cos\psi - \tfrac{3}{4} M] T_1 \tag{B.13a}$$

$$\overrightarrow{Vd}_{err,2} T_2 = \tfrac{2}{3} V_{\mathrm{dc}} [\cos(60^\circ - \psi) - \tfrac{3}{4} M] T_2 \tag{B.13b}$$

$$\overrightarrow{Vd}_{err,z} T_z = -\tfrac{1}{2} V_{\mathrm{dc}} M T_z \tag{B.13c}$$

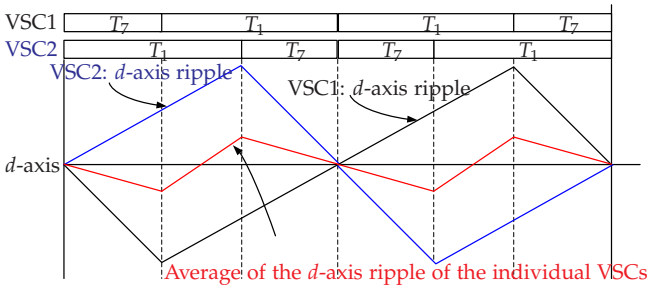


Fig. B.7: d-axis component of the harmonic flux ripple over a carrier cycle of two parallel VSCs and their average. The interleaving angle is 180° and reference space vector angle $\psi = 0°$.

where T_1, T_2 and T_z are the dwell time of voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_0}$ / $\overrightarrow{V_7}$, respectively. The d-axis component of the harmonic flux ripple for individual VSCs and their average flux ripple for $\psi = 0°$ are depicted in Fig. D.14.

The peak-to-peak value of the resultant d-axis harmonic flux for $\psi = 0°$ is given as

$$\lambda_{d(pp)} = \frac{V_{\mathrm{dc}}(1 - \frac{3}{4}M)(\frac{3}{2}M - 1)}{3f_c} \tag{B.14}$$

This is equal to the peak-to-peak value of the flux linkage in the L_f and the peak-to-peak current ripple in the I_x is given as

$$\Delta I_{x(pp)} = \frac{V_{\mathrm{dc}}(1 - \frac{3}{4}M)(\frac{3}{2}M - 1)}{3f_c L_f} \tag{B.15}$$

Considering an equal current sharing between the VSCs, the peak-to-peak value of the switch current ripple is half of the $\Delta I_{x(pp)}$. From (B.15), it is evident that the switch current ripple is the function of a dc-link voltage V_{dc}, the modulation index M, and the switching frequency f_c. For the given V_{dc} and f_c, the peak-to-peak value of the switch current ripple is maximum for the modulation index of $M = 1$, and it is given as

$$\Delta I_{x1(pp,max)} = \frac{V_{\mathrm{dc}}}{48 f_c L_f} \tag{B.16}$$

Once the desired maximum value of the switch current is chosen, the minimum value of the converter side inductance $L_{f,min}$ can be obtained using (B.16).

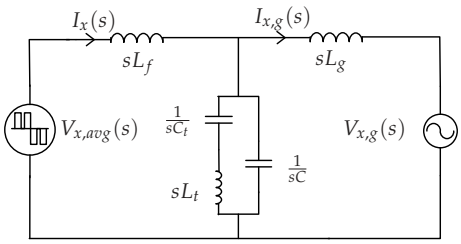


Fig. B.8: The single phase equivalent circuit of the *LCL* filter with additional *LC* trap branch.

3 Line Filter

The line filter arrangement for the parallel interleaved VSCs is shown in Fig. H.4 and its single phase equivalent circuit is also depicted in Fig. B.8. The converter side inductor L_f, the grid side inductor L_g, and the capacitor C_f forms the *LCL* filter. The series connection of the L_t and C_t forms the *LC* trap branch. The L_f and L_g are designed to carry the rated current and the Equivalent Series Resistance (ESR) of these inductors are normally small [42] compared to the L_t and its effect in the low frequency region (upto 9 kHz) can be neglected for the filter design. The admittance transfer function of the filter (only considering the ESR of the *LC* trap branch) is given as

$$\left.\frac{I_{x,g}(s)}{V_{x,avg}(s)}\right|_{V_g=0} = \left(\frac{1}{L_f L_g C}\right)\frac{s^2+\frac{\omega_t}{Q_t}s+\omega_t^2}{s(s^2+\frac{\omega_{r1}}{Q_{r1}}s+\omega_{r1}^2)(s^2+\frac{\omega_{r2}}{Q_{r2}}s+\omega_{r2}^2)} \tag{B.17}$$

The resonant frequencies of the complex conjugate poles are given as

$$\begin{aligned}\omega_{r1} &= \frac{1}{\sqrt{2}}\sqrt{\left(\frac{1}{LC}+\frac{1}{L_tC_{eq}}\right)-\sqrt{\frac{1}{LC^2}\left[\frac{1}{L}+\frac{2(C_t-C)}{L_tC_t}\right]+\frac{1}{L_t^2C_{eq}^2}}}\\ \omega_{r2} &= \frac{1}{\sqrt{2}}\sqrt{\left(\frac{1}{LC}+\frac{1}{L_tC_{eq}}\right)+\sqrt{\frac{1}{LC^2}\left[\frac{1}{L}+\frac{2(C_t-C)}{L_tC_t}\right]+\frac{1}{L_t^2C_{eq}^2}}}\end{aligned} \tag{B.18}$$

where

$$\text{where } L = \frac{L_fL_g}{L_f+L_g}, \text{and } C_{eq} = \frac{CC_t}{C+C_t} \tag{B.19}$$

The complex conjugate zeros are also introduced due to the presence of the *LC* trap branch, and it is given as

$$\omega_t = \frac{1}{\sqrt{L_tC_t}} \tag{B.20}$$

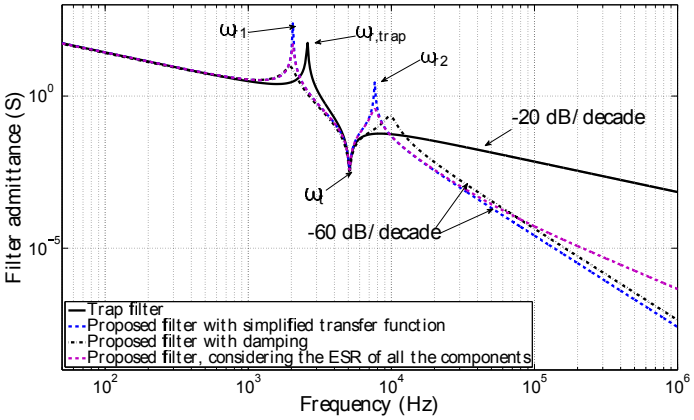


Fig. B.9: The variation of the magnitude of the admittance transfer function of the line filter with frequency.

The quality factors are given as

$$
\begin{aligned}
Q_t &= \frac{1}{R_t}\sqrt{\frac{L_t}{C_t}} \\
Q_{r1} &= \frac{1}{R_t C_t}\frac{1}{\omega_{r1}}\frac{(\omega_{r2}^2-\omega_{r1}^2)}{(\omega_{r2}^2-\omega_t^2)} \\
Q_{r2} &= \frac{1}{R_t C_t}\frac{1}{\omega_{r2}}\frac{(\omega_{r2}^2-\omega_{r1}^2)}{(\omega_t^2-\omega_{r1}^2)}
\end{aligned}
\tag{B.21}
$$

where R_t is the ESR of the LC trap branch.

The variation of the magnitude of the admittance transfer function of the line filter with respect to the frequency is depicted in Fig. B.9. The magnitude of the simplified admittance transfer function closely matches with magnitude of the actual filter transfer function (considering the ESR of all the filter components) in the low frequency region, as shown in Fig. B.9. The effect of the additional LC trap branch is evident in the vicinity of the frequency of $2f_c$, as shown in Fig. B.9. The magnitude of the admittance transfer function of the trap filter proposed in [27, 28] is also plotted in Fig. B.9 for comparison. Due to the presence of the capacitive branch C, the line filter offers a good attenuation to the high frequency components. Therefore, it can effectively reduce the differential mode electromagnetic interference (above 150 kHz). However, the additional pole pairs with a resonant frequency ω_{r2} are present in the proposed filter, as shown in Fig. B.9. The value of the resonant frequency ω_{r1} of the proposed filter is slightly less than that of the trap filter $\omega_{r,trap}$ and it is important to incorporate necessary damping

Table B.1: Base values for per-unit system

Parameters	Base Values (analysis)	Base Values (experiments)
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Voltage	690 V	400 V
Current	1840 A	15.87 A
Frequency	50 Hz	50 Hz
Inductance	688 μH	46 mH
Capacitance	14709 μF	218 μF

to avoid amplification of the harmonic components, present in close proximity of ω_{r1}. The parallel R_d/C_d branch is used to provide necessary damping at ω_{r1}. However, the introduction of the damping branch slightly reduces the attenuation offered to the high frequency harmonic components, as shown in Fig. B.9.

4 Filter Design

The filter is designed for a 2.2 MVA WECS system shown in Fig. H.4. The WECS is connected to a medium voltage network using a step-up transformer. The leakage inductance of a step-up transformer often ranges from 0.04-0.06 pu [35], and it is considered as a part of the grid side inductance L_g. The analysis and the design methodology are also verified by performing experiments on a small scale (11 kVA) laboratory setup. The base values for both of the systems are given in Table B.1. The filter design constraints and the step-by-step design procedure are given in this section.

4.1 Design Constraints

4.1.1 Harmonic Current Injection Limits

The harmonic current injection limit for a generator connected to the medium-voltage network, specified by the German Association of Energy and Water Industries (BDEW) [5, 26, 43], is considered in this paper. The permissible harmonic current injection is determined by the apparent power of the WECS and the Short-Circuit Ratio (SCR) at the Point of the Common Coupling (PCC). The maximum current injection limit of the individual harmonic components up to 9 kHz is specified in the standard and the limits for the WECS connected to the 10 KV medium-voltage network are given in Table B.2. Special limits are set for the odd-ordered integer harmonics below the

Table B.2: BDEW harmonic current injection limits for the WECS connected to the 10 KV Medium Voltage Network

Harmonic Order h	Current Injection Limit (A/MVA/SCR)
5	0.058
7	0.082
11	0.052
13	0.038
17	0.022
19	0.018
23	0.012
25	0.01
Even-ordered $h < 40$	0.06 / h
$40 < h < 180$	0.18 / h

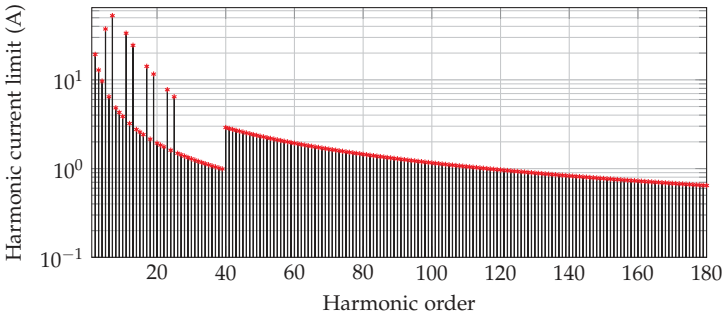


Fig. B.10: BDEW [5] harmonic current injection limits for 2.2 MVA WECS on the low voltage side of the transformer with SCR=20.

25th harmonic, as given in Table B.2. The SCR is taken to be 20 and the allowable injection limits of individual harmonic components on the low voltage side (690 V) for the 2.2 MVA WECS are calculated. The calculated current injection limits for the individual harmonic components are shown in Fig. B.10.

4.1.2 Maximum Switch Current Ripple

The controllability of the system is affected if the switch current has a high ripple content [6]. Therefore, the maximum value of the peak-to-peak switch current ripple is restricted to 0.45 pu in this design.

4.1.3 Reactive Power Consumption

The current flowing through the semiconductor devices, the converter side filter inductor L_f and the circulating current filter L_c can be minimized by limiting the current drawn by the shunt branches of the line filter. Moreover, when VSCs are modulated using DPWM1, the switching losses increase with the increase in the phase difference between the reference voltage and the fundamental component of the switch current. Therefore, the switching losses can also be minimized by making the reactive power consumption of the line filter as small as possible. The grid voltage may vary over a range of 1 ± 0.1 pu and the reactive power consumption of the shunt branches of the line filter is restricted to 0.05 pu for the maximum grid voltage of 1.1 pu.

4.2 Filter Design Procedure

The value of the line filter components are mainly determined based on:

1. The individual voltage harmonic components that appear across the line filter.

2. The maximum value of the switch current ripple.

The magnitude of the individual harmonic frequency components that appears across the line filter is determined by the difference of the magnitude of the corresponding harmonic frequency component in the average of the phase voltages of the parallel interleaved legs and the magnitude of the same harmonic frequency component in the grid voltage. The average of the phase voltages of the parallel interleaved legs is independent of the arrangement of the CI. Therefore, the design of the line filter can be carried out independently. The interleaved operation of the parallel VSCs partially or completely eliminates some of the voltage harmonic components in the average of the phase voltages of the interleaved legs. Therefore, the reduction in the value of the line filter components can also be achieved. A step-by-step design procedure for the proposed line filter is illustrated in this sub-section.

4.2.1 Virtual Voltage Harmonics

The magnitude of the individual harmonic components in the injected grid current is the multiplication of the magnitude of the respective harmonic component in the averaged pole voltage and the admittance offered by the filter at that harmonic frequency. The theoretical harmonic solution of the $V_{x,avg}$ can be obtained using (B.8). From (B.8), it is evident that the harmonic coefficients are the function of the dc-link voltage V_{dc} and the modulation index M. Therefore, for a given value of the dc-link voltage, the magnitude of the individual harmonic components varies with the modulation index M.

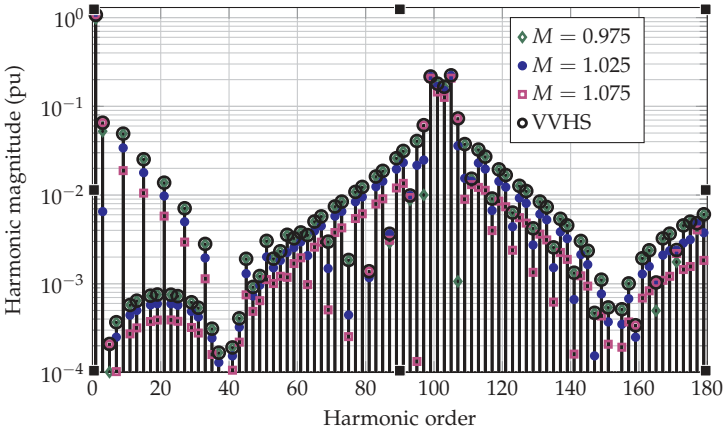


Fig. B.11: The magnitude of the individual voltage harmonic component of the average pole voltage.

The magnitudes of the individual voltage harmonic component of $V_{x,avg}$ for the different modulation indices are shown in Fig. B.11. In order to satisfy the harmonic current injection limit over the entire operating range, the worst case magnitude of the individual harmonic components of $V_{x,avg}$ is required. The spectrum comprises the maximum values of the individual voltage harmonic components over the entire operating range and it is defined as a Virtual Voltage Harmonic Spectrum (VVHS) [26].

VVHS for the considered modulation range and the maximum value of the dc-link voltage is calculated and it is depicted in Fig. B.11. The magnitude of most of the harmonic components (except those harmonic components, which are present around the even multiple of the carrier harmonic) increases as the modulation index approaches the lower limit. On the other hand, the harmonic components around the even multiple of carrier frequency harmonic increases with increase in the modulation index, as shown in Fig. B.11.

4.2.2 Required Filter Admittance

The worst case filter admittance requirement is obtained from the harmonic current injection limit and the VVHS of the phase voltage. The required admittance for the h*th* harmonic component is given as

$$Y_h^* = \frac{I_{h,BDEW}^*}{V_{h,VVHS}} \tag{B.22}$$

where $I_{h,BDEW}^*$ is the BDEW current injection limit of the h*th* harmonic component and $V_{h,VVHS}$ is the voltage magnitude of the corresponding harmonic

component in VVHS of the phase voltage. The VVHS of the average pole voltages comprises a common mode component in all phase, which gets canceled out in the line-to-line output voltage. The VVHS of the phase voltages is obtained by removing this common mode component from the VVHS of average pole voltages.

4.2.3 Selection of the LC Trap Branch Parameters

As a result of the interleaved carriers with an interleaving angle of 180°, the magnitude of the harmonic components around the odd multiple of the carrier frequency is reduced considerably. Therefore, the major voltage harmonic components appear around the 2nd carrier frequency harmonic ($2f_c$), as shown in Fig. B.11. The line filter should offer small admittance to these harmonic components, which can be achieved by tuning the LC trap branch, such that the resonant frequency ω_t is equal to $2f_c$.

The resonant frequency of the LC trap branch is given by (B.20). The attenuation offered by the filter to the base band harmonics of the 2nd carrier frequency harmonic depends on the quality factor of the LC trap branch, given by (B.21). The magnitude of the voltage harmonic components in vicinity of the 2nd carrier frequency harmonic increases with increase in the modulation index, as shown in Fig. B.11. Therefore, the required value of the quality factor of the LC trap branch strongly depends on the maximum operating value of the modulation index M.

The capacitors are available in standard values and the selection of the values of the L_t and C_t to realize the required value of the quality factor is driven by the availability of the capacitor. The value of C_t is chosen to be 0.02 pu in this design. The value of L_t is taken to be 0.0048 pu in order to have the resonant frequency of the trap branch at twice the switching frequency. The quality factor of the trap branch is 25, which is sufficient to achieve the required attenuation around the 2nd carrier frequency harmonics.

4.2.4 Selection of L_f, L_g and C

As a result of an interleaved carrier, the voltage magnitude of the odd multiple of the carrier harmonics and its side bands is reduced considerably, as shown in Fig. B.11. The proposed line filter introduces a resonance at ω_{r1} and ω_{r2}. The damping requirement can be reduced by choosing the filter parameters such that the resonances occur at the frequencies where the magnitude of the voltage harmonics are small.

The values of ω_{r1} and ω_{r2} are chosen to be 2.05 kHz and 7.65 kHz, respectively. Once the values of ω_t, ω_{r1}, and ω_{r2} are decided, the Q_{r1} and Q_{r2} are obtained using (B.21). From these values, the C_{eq} is calculated, which is

given as

$$C_{eq} = \Big(\frac{1}{L_t}\Big)\frac{1}{\omega_{r1}^2 + \omega_{r2}^2 + \frac{\omega_{r1}\omega_{r2}}{Q_{r1}Q_{r2}} - \frac{\omega_{r1}^2\omega_{r2}^2}{\omega_t^2}} \tag{B.23}$$

For the given values of the ω_t, ω_{r1}, and ω_{r2}, the product of L and C is given as

$$LC = \frac{\omega_t^2}{\omega_{r1}^2\omega_{r2}^2} \tag{B.24}$$

As the value of C_t is already fixed, the value of C can be obtained using (I.11) and (B.23). The desired value of the L can be achieved by selecting the proper values of L_f and L_g. Many possible combinations of L_f and L_g exist. Let,

$$L_g = \alpha L \tag{B.25}$$

where α is a constant, and it is greater than one. Using (I.11) and (B.25), L_f can be given as

$$L_f = \Big(\frac{\alpha}{\alpha - 1}\Big)L \tag{B.26}$$

For the given range of grid voltage variation, the maximum value of the dc-link voltage, which is required to ensure the VSC operation in a linear modulation range, is decided by the value of the inductance ($L_f + L_g$). Therefore, $L_f + L_g$ should be made as small as possible. The minimum value of $L_f + L_g$ can be obtained by selecting $\alpha = 2$, where the values of L_f and L_g are equal. However, from a cost point of view, this combination may not be optimal. For $\alpha > 2$, the value of L_g is more than the value of L_f. The reverse is true for $1 \leqslant \alpha \leqslant 2$. The value of $\alpha = 2$ is taken as the starting point. In case a harmonic injection limit is violated, the design is discarded and a new value of the α will be selected. The maximum value of the α is limited by the switch current ripple, and it is given as

$$\alpha_{max} = \frac{1}{1 - \frac{48 L f_c \Delta I_{x1(pp,max)}}{V_{\mathrm{dc}}}} \tag{B.27}$$

In case a harmonic injection limit is violated even with α_{max}, the design is discarded and new design will be evaluated by changing the parameters of the LC trap branch. The filter admittance plot for different values of α is shown in Fig. B.12.

As mentioned earlier, appropriate damping is required to avoid amplification of the harmonic components around ω_{r1} and ω_{r2}. Therefore, a C_d/R_d branch has been added. The capacitive branch is split into two separate branches and a resistor is inserted in one of the branches, as shown in Fig. B.13. Let,

$$\begin{aligned} C_d &= \beta C \\ C_f + C_d &= C \end{aligned} \tag{B.28}$$

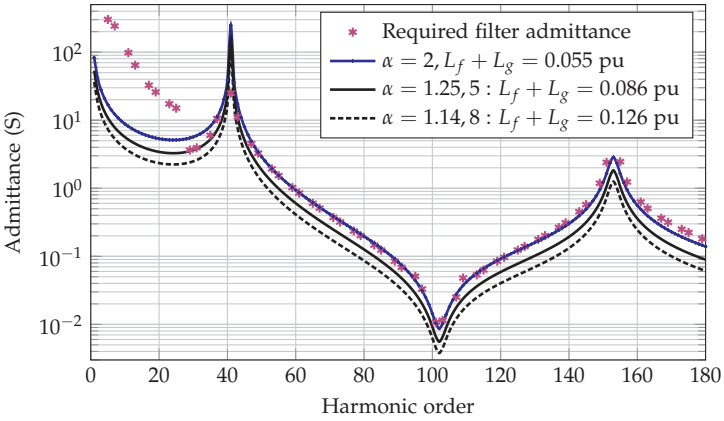


Fig. B.12: Filter admittance plot for different values of α.

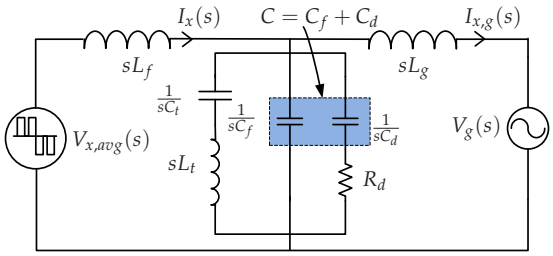


Fig. B.13: The single phase equivalent circuit of the *LCL* filter with additional *LC* trap and a C_d/R_d damping branch.

The introduction of the C_d/R_d damping branch changes the resonant frequencies ω_{r1} and ω_{r2}. The worst case change in the resonant frequency can be obtained by setting $R_d = \infty$ [44]. The worst case variation in the resonant frequencies as a function of β is shown in Fig. B.14. The ω_{r1} varies in a small range, whereas the variation in ω_{r2} is more and increases sharply as β approaches one. For a given value of R_d, the losses in the damping branch and admittance offered to the high frequency components also increase as β approaches one. In order to restrict the variation in the resonant frequencies in a narrow range and to reduce the inventory [25], β is taken to be 0.5.

The C_d/R_d damping branch introduces an additional zero ($z = -1/C_dR_d$) and a pole ($p = z/\gamma$ and $\gamma < 1$) in the admittance transfer function of the line filter. The value of γ can be obtained by solving the denominator polynomial, as given in the Appendix. Considering the complexity involved in solving the quintic function, only the information of the additional zero is used to obtain

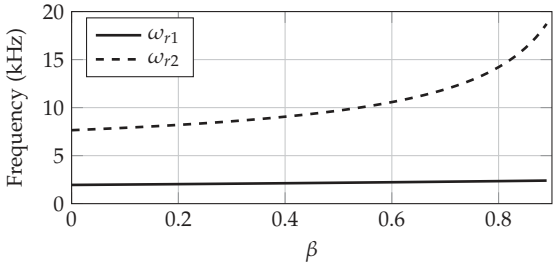


Fig. B.14: Worst case variation in the resonant frequencies as a function of β.

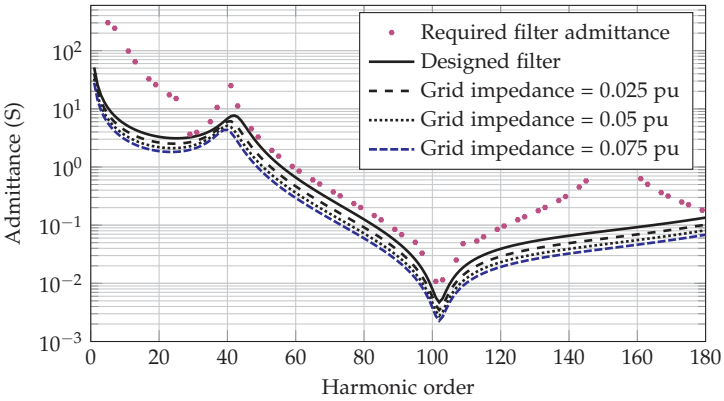


Fig. B.15: Admittance plot of the designed filter. The effect of the grid inductance variation is also depicted.

the minimum value of the damping resistor $R_{d,min}$. Once $R_{d,min}$ is obtained, the required value of the damping resistor R_d is determined by using the frequency response characteristic of the filter admittance transfer function given in the Appendix. The improved resonance damping can be achieved by selecting R_d and C_d such that the $|z| < \omega_{r1}$ [44]. Using this relation, the minimum value of the required damping resistor $R_{d,min}$ can be obtained, and it is given as

$$R_{d,min} = \frac{1}{\omega_{r1} C_d} \tag{B.29}$$

The line filter is designed by following the above mentioned procedure. The final filter parameters are given in Table K.3 and the its admittance plot is also depicted in Fig. B.15. The effect of the line impedance (L_{grid}) variation on the filter performance is also shown. The value of ω_{r1} reduces slightly with the increase in the grid impedance, whereas the ω_t remains unaltered.

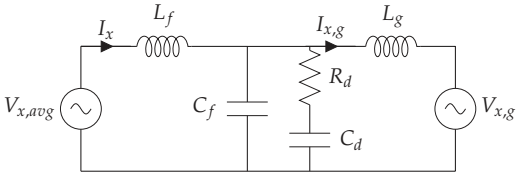


Fig. B.16: Single phase equivalent circuit of the LCL filter with parallel R_d/C_d damping branch.

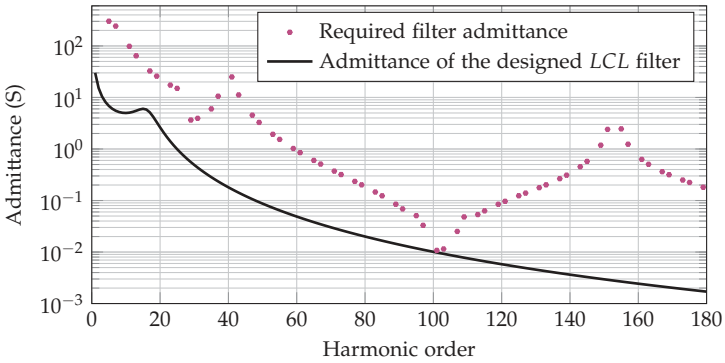


Fig. B.17: Admittance plot of the designed LCL filter, with $L_f = 0.065$ pu (44.75 μH), $L_g = 0.09$ pu (62 μH), $C_f = 0.08$ pu (1200 μF), $C_d = 0.08$ pu (1200 μF).

4.2.5 Comparison with the LCL Filter

Reduction in the value of the filter components is achieved using the proposed high order filter. This has been verified by comparing the values of the filter components of the proposed filter with that of the LCL filter.

The single phase equivalent circuit of the LCL filter with the parallel R_d/C_d damping branch is shown in Fig. B.16. L_f is the converter side inductor, L_g is the grid side inductor, and C_f is the filter capacitor. The parameters of the damping branch are chosen as per the procedure specified in [6]. The admittance transfer function of the LCL filter is given by (B.1). The value of the filter components of the LCL filter is chosen such that the filter admittance is less than the required value of the filter admittance for the harmonic frequency components upto 9 kHz (as per the BDEW limits). The admittance plot of the LCL filter along with the required filter admittance is shown in Fig. B.17.

The values of the filter components of the designed LCL filter are given in Table I.5, along with the filter parameters of the proposed filter. The total shunt capacitance ($C_f + C_d + C_t$) in the proposed filter is 0.0386 pu, against the 0.16 pu in the LCL filter. The reduction in the value of the shunt capac-

Table B.3: Filter Parameters of the proposed filter and the *LCL* filter

Parameters	Proposed filter	*LCL* filter
$L_f + L_g$	61.92 μH (0.09 pu)	106.75 μH (0.155 pu)
Capacitor	$(C_f + C_d + C_t)$ 566 μF (0.0386 pu)	$(C_f + C_d)$ 2400 μF (0.16 pu)
Trap inductor L_t	3.3 μH (0.0048 pu)	-

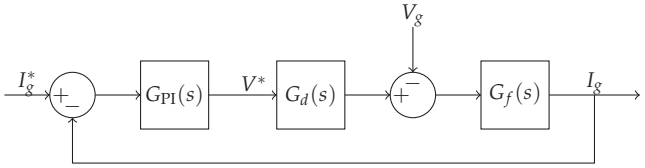


Fig. B.18: Grid current controller structure.

itor improves the efficiency, as shunt capacitors draws reactive current and increases resistive losses. In addition, it also increases switching losses when the VSCs are modulated using the DPWM1 scheme. The use of the proposed line filter result in 42 % reduction in the values of the series inductors $(L_f + L_g)$. This reduces the volume of the inductive components, as inductors L_f and L_g are designed to carry the rated value of the current and occupy significant amount of space. The proposed line filter requires an additional trap inductor $L_t = 0.0048$ pu. However, the value of L_t is very small. In addition, L_t is placed in the shunt branch and carries small current. Therefore, the volume of this additional inductor is small compared to the reduction achieved in L_f and L_g.

4.3 Controller Design

The grid current is controlled using the Proportional-Integral (PI) controller, as shown Fig. B.18. The control variables are transformed to a synchronously rotating frame, which rotates at the fundamental frequency of the grid voltage. The transfer function of the PI controller is given by

$$G_{\mathrm{PI}}(s) = K_p + \frac{K_i}{s} \tag{B.30}$$

where K_i is the integral gain and the K_p is the proportional gain of the PI controller. The control and PWM delay is represented by the $G_d(s)$. The transfer function of the filter $G_f(s)$ is given in the Appendix. The parameters of the designed filter are given in Table K.3. The continuous transfer functions

Table B.4: Parameters for simulation and experimental study

Parameters	Simulation study	Experiment
Power	2.2 MVA (2 MW)	11 kVA (10 kW)
Switching frequency	2.55 kHz	2.55 kHz
AC voltage (line-to-line)	690 V	400 V
DC-link voltage	1080 V	650 V
L_f	13.76 μH (0.02 pu)	0.87 mH (0.019 pu)
L_g (+ Transformer leakage)	48.16 μH (0.07 pu)	3.1 mH (0.0675 pu)
Trap capacitor C_t	294 μF (0.02 pu)	4.4 μF (0.02 pu)
Trap inductor L_t	3.3 μH (0.0048 pu)	220 μH (0.0048 pu)
Capacitor $C_f = C_d$	136 μF (0.0093 pu)	2 μF (0.0093 pu)

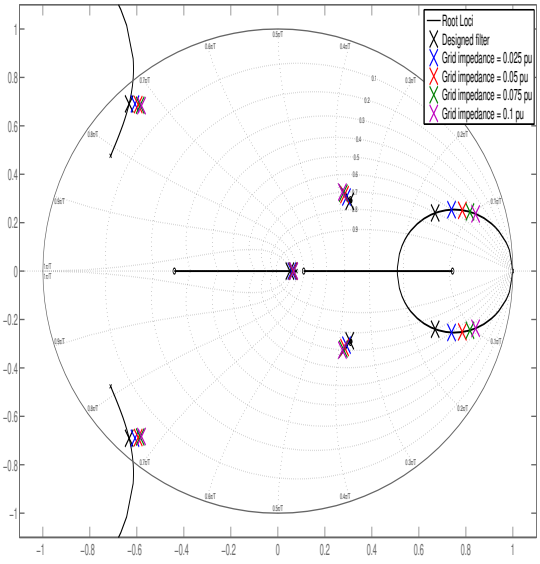


Fig. B.19: Root loci of the closed loop system with the designed controller. The closed loop poles are marked using 'x'.

are discretized and the controller parameters are calculated in the discrete time domain using the root locus theory. The controller is designed to have a damping factor of 0.707. The parameters of the PI controller to meet the given

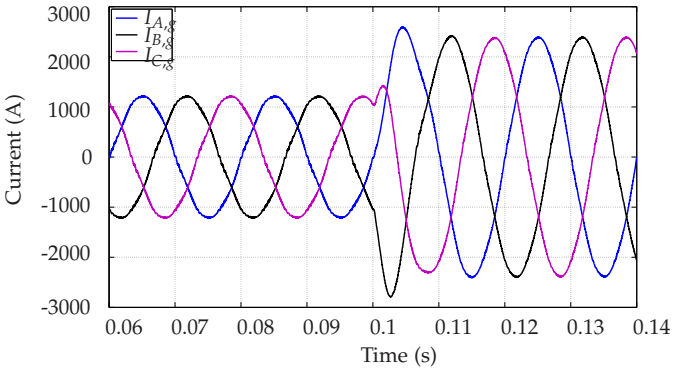


Fig. B.20: Step response of the controller. The d-axis current reference is changed from 0.5 pu to 1 pu at $t = 0.1$ s.

damping factor requirement are $K_p = 0.168$ and $K_i = 1310$. Fig. B.19 shows the root locus in the z-plane of the closed-loop system with the designed controller parameters.

The pole map of the closed-loop system for varying values of the grid side inductance L_g is also shown in Fig. B.19, where L_g is the summation of the leakage inductance of the step-up transformer and the line inductance L_{grid} (inductance of the electrical network between the PCC and the source). The value of the L_g is varied from 0.07 pu to 0.17 pu. With the increase in the value of the L_g, the damping factor decreases from 0.707 to 0.5. However, the system remains stable with the designed PI controller, as evident from Fig. B.19.

5 Simulation and Experimental Results

The simulation study and the experimental verification is carried out to verify the analysis and the design methodology and the results are presented in this section.

5.1 Simulation Study

The simulations have been carried out using the PLECS simulation tool. The parameters used for the simulation study are given in Table K.3. The controller behavior to the step change in the reference signal is shown in Fig. B.20. The d-axis current reference is changed from 0.5 pu to 1 pu. The grid current tracks the reference and transient performance is also found to be satisfactory. Fig. C.9, shows the simulated waveforms of the system, operating under rated conditions with the unity power factor operation. The

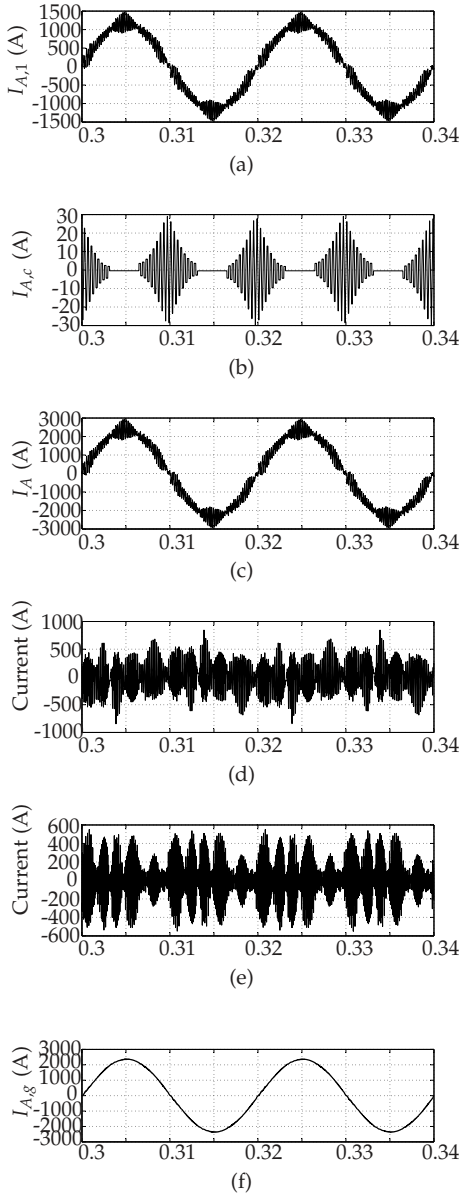


Fig. B.21: Simulated currents of phase A with asymmetrical regular sampled DPWM1 with an interleaving angle of 180°. (a) VSC1: Phase A current, (b) Circulating current, (c) Resultant current, (d) Current in *LC* trap branch, (e) Current through the C_f, (f) Grid current.

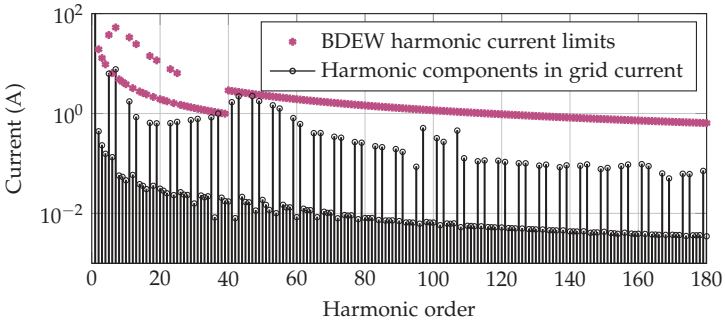


Fig. B.22: Performance verification of the line filter. The harmonic spectrum of the simulated grid current is depicted.

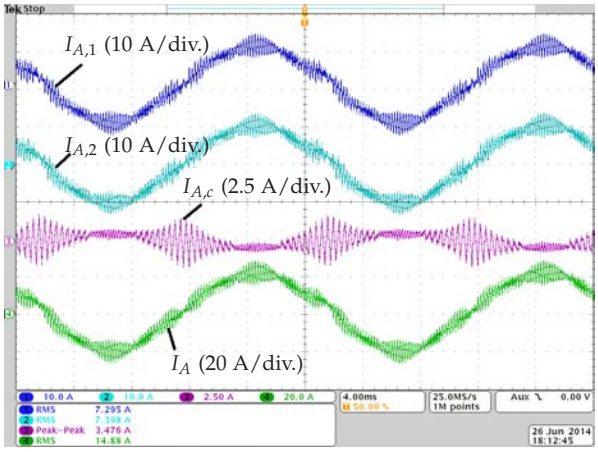
harmonic spectrum of the simulated grid current is obtained by using fast Fourier transform (FFT) and plotted along with the BDEW harmonic current injection limit in Fig. B.22. The major harmonic components around the 2nd carrier harmonic frequency are effectively suppressed. All harmonic components are within the specified harmonic current injection limits.

5.2 Experimental Results

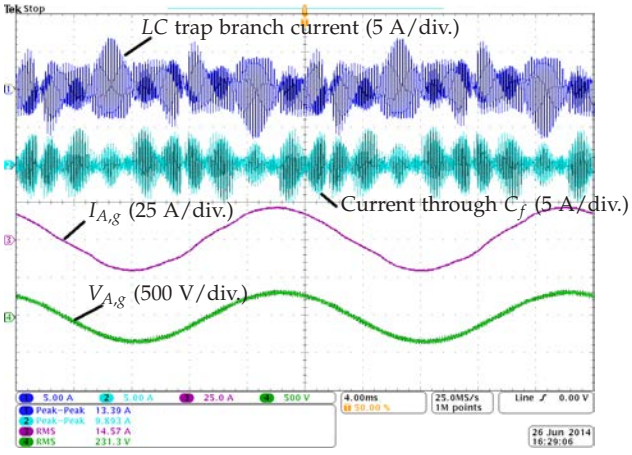
To verify the analysis and the design methodology, a line filter for a small scale (11 kVA) laboratory prototype with two interleaved VSCs was designed. The parameters of the line filter used in this setup are listed in Table K.3. In order to avoid the effect of the background harmonics present in the grid voltage, an AC power source MX-35 from the California Instruments is used as a harmonic free grid emulator. The grid impedance is taken to be Z_{grid} =0.04 pu. The control is implemented using TMS320F28346 floating-point digital signal processor.

A 0.6 mH, three phase inductor is used as a converter side inductor. The circulating current filter L_C has a leakage inductance of 0.27 mH. Therefore, the total converter side inductance L_f = 0.87 mH (0.019 pu). A three phase, 10 kVA, 1:1 transformer is used. The leakage inductance of this transformer is measured to be 3.1 mH (0.0675 pu), which is nearly equal to the required value of the 0.07 pu. Therefore, L_g is comprised of the leakage inductance of the transformer only and an additional inductor is avoided.

The experiment was performed at rated conditions with unity power factor operation. Fig. E.20, shows the experimental waveforms. The circulating current is effectively suppressed by using CI, as shown in Fig. B.23(a). As a result, the effect of the circulating current in the individual VSC currents can be conveniently neglected. Therefore $I_{A,1} \approx I_{A,2}$ and the sum of these two



(a)



(b)

Fig. B.23: The experimental results. (a) Ch1: VSC1 phase A current ($I_{A,1}$), Ch2: VSC2 phase A current ($I_{A,2}$), Ch3: Circulating current ($I_{A,c}$), Ch4: Resultant current (I_A), (b) Ch1: Current through the LC trap branch, Ch2: Current through the C_f branch, Ch3: Grid current ($I_{A,g}$), Ch4: Grid voltage at PCC.

currents (I_A) is also shown in Fig. B.23(a). The maximum value of the switch current ripple is 0.4 pu against the design constraint of 0.45 pu.

The current through the LC trap branch and the capacitive branch C_f is shown in Fig. B.23(b). The LC trap branch provides low impedance path to the 2nd carrier frequency harmonic and its side bands. Whereas, the capacitive branch C_f sinks the high frequency harmonic components. The injected

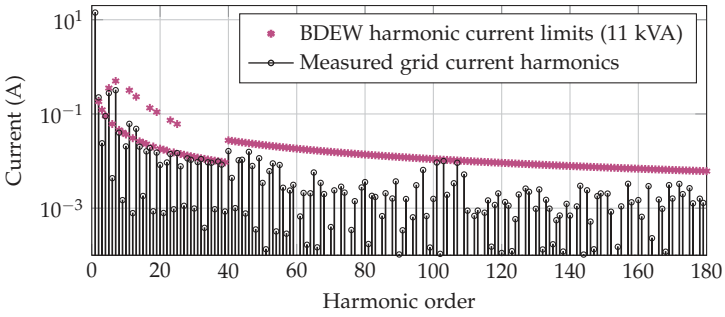


Fig. B.24: Performance verification of the line filter of the laboratory prototype.

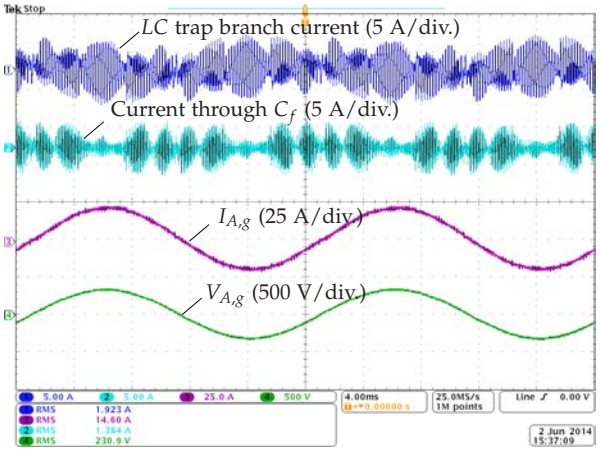


Fig. B.25: The experimental results obtained by replacing transformer with equivalent three phase inductor. Ch1: Current through the LC trap branch, Ch2: Current through the C_f branch, Ch3: Grid current ($I_{A,g}$), Ch4: Grid voltage.

current and voltage at the PCC are also shown in Fig. B.23(b). The measured grid current had a THD of 3.1 % and the magnitude of the individual harmonic component is plotted in Fig. B.24. The magnitude of all the harmonic frequency components of the grid current is lower than the specified BDEW harmonic current injection limits. The major harmonics components around the 2nd carrier harmonic are suppressed effectively and the magnitude of these components are also within the prescribed current injection limits. The relative amplitude of the harmonic components in the low frequency range is more in the measured grid current than on the simulated grid current. The even order harmonics are mainly present due to the asymmetrical three limb structure of the inductor L_f and the transformer (L_g). The transformer also

Table B.5: Magnitude of the characteristic harmonics with the transformer and with equivalent inductor

Harmonic	With transformer	With eq. inductor
5^{th}	294 mA	112 mA
7^{th}	310 mA	77 mA
11^{th}	67 mA	12 mA
13^{th}	43 mA	32 mA
17^{th}	20 mA	20 mA
19^{th}	26 mA	17 mA
23^{rd}	18 mA	12 mA
25^{th}	19 mA	18 mA

draws nonlinear magnetizing current and increases the magnitude of the odd order harmonics as well. To validate the filter performance, the experiment was also performed by replacing the transformer with a 3.1 mH, three limb inductor. The grid impedance is also set to zero. The grid current waveform is shown in Fig. H.16 and the measured grid current had a THD of 1.38 %. The magnitude of the low order odd harmonic components present in the grid current is given in Table B.5 and it is compared with the magnitude of the corresponding harmonic components of a grid current with a transformer. The magnitude of the low order harmonic components is significantly smaller with the equivalent inductor than that with the transformer. Therefore, it is concluded that the magnetizing current of the transformer significantly contributes towards the low order odd harmonic components of the grid current.

6 Conclusion

A step-by-step design procedure of the line filter for the high power WECS is presented in this paper. In-depth analysis of the effect of the interleaved carriers on the harmonic performance of the parallel connected VSCs has been made. The closed form analytical harmonic solution for the two parallel interleaved VSCs, modulated by asymmetrical regular sampled DPWM1 scheme, is derived and the reduction in the magnitude of some of the harmonic components is demonstrated. The effect of the interleaved carriers on the switch current ripple is also analyzed. The set of the worst case individual voltage harmonic components in the entire operating range (VVHS) is derived, and it is used to obtain the required value of the filter admittance for each harmonic components. The additional *LC* trap branch with

the conventional *LCL* filter is used. The characteristics of the proposed line filter is analyzed and the design procedure to select the filter parameters, such that the filter admittance closely matches with the required admittance at all concerned harmonic frequencies is presented. Although the design example presented in the paper considers DPWM1 as the modulation scheme, the proposed filter design approach can be equally applicable to other PWM schemes as well. The performance of the filter has been tested. The magnitude of the individual harmonic components in the grid current is within the harmonic current injection limits, specified by the BDEW standards.

A Appendix

Considering the single phase equivalent circuit of the proposed filter, as shown in Fig. B.13, the admittance transfer of the filter is given as

$$\left.\frac{I_{x,g}(s)}{V_{x,avg}(s)}\right|_{V_g=0} = G\frac{s^3 + A_2s^2 + A_1s + A_0}{s(s^5 + B_4s^4 + B_3s^3 + B_2s^2 + B_1s + B_0)}$$

where

$$\begin{aligned}
G &= \left(\frac{1}{L_fL_gC_f}\right)\\
A_0 &= \frac{1}{L_fC_tC_dR_d}, A_1 = \frac{1}{L_tC_t} + \frac{R_t}{L_tC_dR_d}\\
A_2 &= \frac{R_t}{L_t} + \frac{1}{C_dR_d}\\
B_0 &= \frac{L_f + L_g}{L_fL_gL_tC_tC_fC_dR_d}, B_1 = \frac{L_f + L_g}{L_fL_gL_tC_f}\left(\frac{1}{C_t} + \frac{R_t}{C_dR_d}\right),\\
B_2 &= \frac{L_f + L_g}{L_fL_gC_f}\left(\frac{R_t}{L_t} + \frac{1}{C_dR_d}\right) + \frac{C_f + C_d + C_t}{L_tC_fC_tC_dR_d}\\
B_3 &= \frac{L_f + L_g}{L_fL_gC_f} + \frac{C_f + C_t}{L_tC_fC_t} + \frac{R_t(C_f + C_d)}{L_fC_fC_dR_d}\\
B_4 &= \frac{R_t}{L_t} + \frac{C_f + C_d}{C_fC_dR_d}
\end{aligned} \tag{B.31}$$

References

[1] Z. Chen, J. Guerrero, and F. Blaabjerg, "A review of the state of the art of power electronics for wind turbines," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1859–1875, Aug 2009.

[2] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 708–719, March 2012.

[3] F. Blaabjerg and K. Ma, "Future on power electronics for wind turbine systems," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 139–152, Sept 2013.

[4] H. Zhang and L. Tolbert, "Efficiency impact of silicon carbide power electronics for modern wind turbine full scale frequency converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 21–28, Jan 2011.

[5] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[6] J. Muhlethaler, M. Schweizer, R. Blattmann, J. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, 2013.

[7] M. Liserre, R. Cardenas, M. Molinas, and J. Rodriguez, "Overview of multi-MW wind turbines and wind parks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1081–1095, April 2011.

[8] M. Baumann and J. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link current balancing," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042–3053, 2007.

[9] B. Andresen and J. Birk, "A high power density converter system for the gamesa G10x 4,5 MW wind turbine," in *Proc. European Conference on Power Electronics and Applications, 2007*, Sept 2007, pp. 1–8.

[10] J. Birk and B. Andresen, "Parallel-connected converters for optimizing efficiency, reliability and grid harmonics in a wind turbine," in *Proc. European Conference on Power Electronics and Applications, 2007*, Sept 2007, pp. 1–7.

[11] R. Jones and P. Waite, "Optimised power converter for multi-MW direct drive permanent magnet wind turbines," in *Proc. European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–10.

[12] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[13] L. Asimmoaei, E. Aeloiza, J. Kim, P. Enjeti, F. Blaabjerg, L. Moran, and S. Sul, "An interleaved active power filter with reduced size of passive components," in *Proc. Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, pp. 1–7.

[14] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[15] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[16] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[17] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[18] K. Xing, F. Lee, D. Borojevic, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, 1999.

[19] J. Ewanchuk and J. Salmon, "Three-limb coupled inductor operation for paralleled multi-level three-phase voltage sourced inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1979–1988, 2013.

[20] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[21] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[22] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, 2012.

[23] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, May 1997.

[24] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sept 2005.

[25] P. Channegowda and V. John, "Filter optimization for grid interactive voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4106–4114, Dec 2010.

[26] A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, 2011.

[27] W. Wu, Y. He, and F. Blaabjerg, "An LLCL power filter for single-phase grid-tied inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 782–789, Feb 2012.

[28] Y. Patel, D. Pixler, and A. Nasiri, "Analysis and design of trap and LCL filters for active switching converters," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE), 2010*, July 2010, pp. 638–643.

[29] J. Bloemink and T. Green, "Reducing passive filter sizes with tuned traps for distribution level power electronics," in *Proc. of the 14th European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–9.

[30] J. Xu, J. Yang, J. Ye, Z. Zhang, and A. Shen, "An LTCL filter for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4322–4338, Aug 2014.

[31] A. Cantarellas, E. Rakhshani, D. Remon, and P. Rodriguez, "Design of the LCL+trap filter for the two-level VSC installed in a large-scale wave power plant," in *Proc. Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, Sept 2013, pp. 707–712.

[32] F. Forest, T. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire, "Optimization of the supply voltage system in interleaved converters using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 934–942, 2007.

[33] R. Hausmann and I. Barbi, "Three-phase multilevel bidirectional DC-AC converter using three-phase coupled inductors," in *Proc. IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, Sept 2009, pp. 2160–2167.

[34] B. Cougo, T. Meynard, and G. Gateau, "Parallel Three-Phase Inverters: Optimal PWM Method for Flux Reduction in Intercell Transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[35] "Geafol,cast-resin transformers, 100 to 16000 kva, catalog tv1," Siemens AG, Power Transmission and Distribution Transformers Division, [Online]. Available: http://www.siemens.com/energy, 2007.

[36] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[37] J. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a pwm converter system," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063–1075, 1991.

[38] A. Hava, R. Kerkman, and T. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, 1998.

[39] G. Narayanan and V. T. Ranganathan, "Analytical evaluation of harmonic distortion in PWM AC drives using the notion of stator flux ripple," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 466–474, 2005.

[40] G. Narayanan, H. Krishnamurthy, D. Zhao, and R. Ayyanar, "Advanced bus-clamping PWM techniquesbased on space vector approach," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 974–984, 2006.

[41] G. Narayanan, V. T. Ranganathan, D. Zhao, H. Krishnamurthy, and R. Ayyanar, "Space vector based hybrid PWM techniques for reduced current ripple," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1614–1627, 2008.

[42] J. Dannehl, F. Fuchs, S. Hansen, and P. Thøgersen, "Investigation of active damping approaches for pi-based current control of grid-connected pulse width modulation converters with lcl filters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1509–1517, July 2010.

[43] S. Araujo, A. Engler, B. Sahan, and F. Antunes, "LCL filter design for grid-connected NPC inverters in offshore wind turbines," in *Proc. Power Electronics, 2007. ICPE '07. 7th Internatonal Conference on*, 2007, pp. 1133–1138.

[44] W. Wu, Y. He, T. Tang, and F. Blaabjerg, "A new design method for the passive damped LCL and LLCL filter-based single-phase grid-tied inverter," *IEEE Trans. Ind. Appl.*, vol. 60, no. 10, pp. 4339–4350, Oct 2013.

Paper C

Parallel Interleaved VSCs: Influence of the PWM Scheme on the Design of the Coupled Inductor

Ghanshyamsinh Gohil,
RamKrishan Maheshwari,Lorand Bede,
RamKrishan Maheshwari,Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been published in the
in Proc. 40th Annual Conference on IEEE Industrial Electronics Society, pp.
1693-1699, Oct 2014.

The layout has been revised.

Abstract

The line current ripple and the size of the dc-link capacitor can be reduced by interleaving the carriers of the parallel connected Voltage Source Converters (VSCs). However, the interleaving of the carriers gives rise to the circulating current between the VSCs, and it should be suppressed. To limit the circulating current, magnetic coupling between the interleaved legs of the corresponding phase is provided by means of a Coupled Inductor (CI). The design of the CI is strongly influenced by the Pulsewidth Modulation (PWM) scheme used. The analytical model to evaluate the flux-linkage in the CI is presented in this paper. The maximum flux density and the core losses, being the most important parameters for the CI design, are evaluated for continuous PWM and discontinuous pulsewidth modulation (DPWM) schemes. The effect of these PWM schemes on the design of the CI is discussed. The simulation and the experimental results are finally presented to validate the analysis.

1 Introduction

The magnetic excitation in the core of the line filter inductor has a line frequency component along with the small high frequency ripple components. By improving the line current quality, a small filter and therefore higher power density can be achieved. The line current quality can be improved by interleaving the carrier signals of the parallel Voltage Source Converters (VSCs) [1–6]. The discussion on the optimal interleaving angle to minimize the line current ripple is presented in [2]. The optimized PulseWidth Modulation (PWM) scheme involving multiple sequences and different interleaving angles to reduce the line current ripple is also presented [6]. The zone division plot, showing the spatial regions within a sector where a combination of a certain switching sequence and interleaving angle result in lower rms current ripple in a switching cycle, is also discussed.

The interleaving of the carriers leads to the phase shifted pole voltages (measured with respect to the center point of the dc-link O in Fig. F.1.) of the corresponding phases of the parallel interleaved VSCs. This gives rise to the circulating current between VSCs, and it should be limited in order to reduce the losses and the stresses in both active and passive components, present in the circulating current path. The magnetic coupling between the interleaved parallel legs, by means of a Couple Inductor (CI) is proposed in [7–10], and the schematic is shown in Fig. C.2(a). To achieve high power density, the size of this additional circulating current filter should be reduced.

If a strong magnetic coupling between the windings is ensured, the CI is only subjected to high frequency magnetic excitation, which is determined by the switching frequency of the VSCs. As a result of the high frequency excitation, small size of the CI can be achieved. Moreover, the maximum

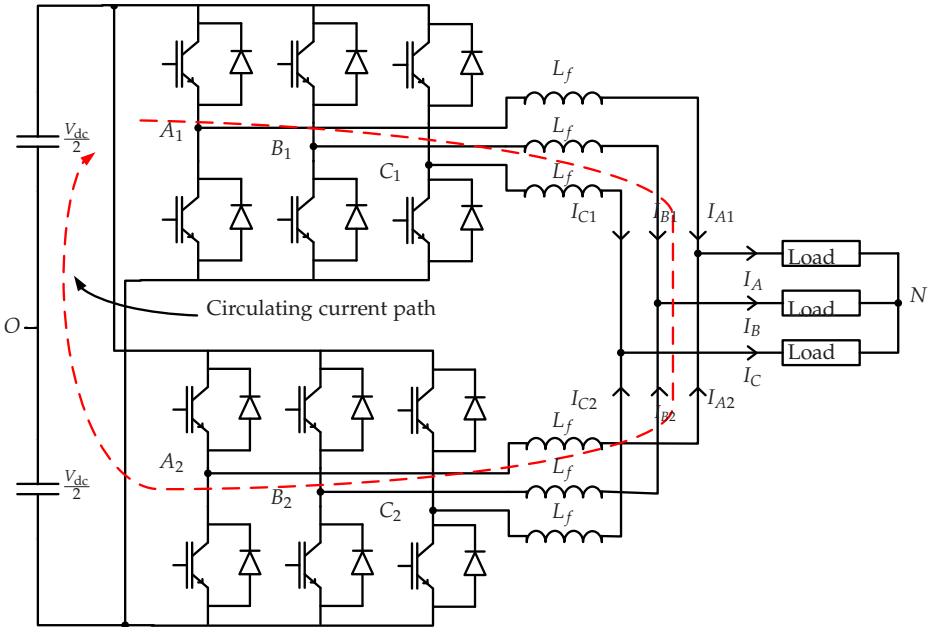


Fig. C.1: Parallel interleaved VSCs with the common dc-link.

value of the flux-density in the core should be close to the saturation flux density, in order to utilize the core effectively. High frequency flux reversal along with the high flux-density in the core results in more core losses. On the other hand, limited surface area is available for heat dissipation due to the small size of the CI. This may lead to a thermally limited design. As the core losses also depend on the peak flux density, the design of the thermally limited inductor can be realized by either decreasing the peak value of the flux density in the core or by providing more cooling. Both of these options lead to reduced power density.

The core losses depend on the peak flux density and the rate of change of flux density. Both of these parameters are strongly influenced by the PWM scheme used. The peak flux density in the core of the CI for different PWM schemes are discussed in [9], and a modulation scheme to reduce the flux in the CI is also proposed. However, discussion on the core losses is not given, which is an important factor in determining the size of the thermally limited magnetic component, and it should be considered carefully for a proper design of the CI.

The CI is a preferred solution for suppressing the circulating current in the parallel interleaved VSCs, and the effect of the carrier based PWM schemes on the design of the CI is analyzed in this paper. The core experiences high

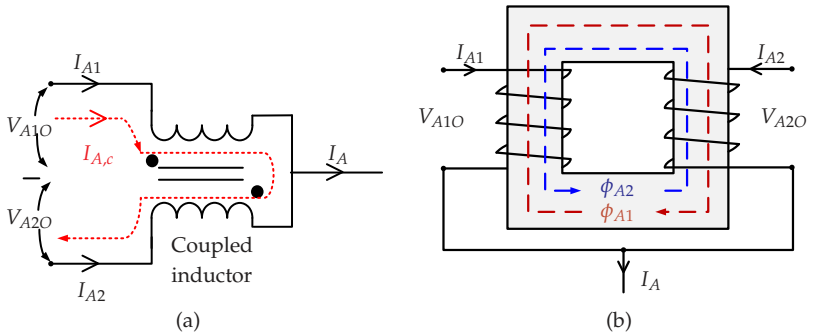


Fig. C.2: Coupled inductor. (a) schematic for phase A, (b) physical arrangement of CI.

frequency excitation and therefore, small size of the CI can be achieved. However, due to the small size, the surface area available for the heat dissipation is limited. The effect of the PWM scheme on the parameters affecting the design of the CI is discussed. Moreover, an analytical method to evaluate the maximum flux-density and losses in the CI for different PWM schemes is presented. The basic operation of the CI is discussed in Section II. The effect of the PWM schemes on the flux density in the magnetic core of the CI is presented in Section III. The influence of the flux density pattern on the design of the CI is presented in Section IV. In Section VI, the simulation results and the experimental results are presented to validate the analysis.

2 Coupled Inductor

The instantaneous potential difference in the pole voltages of the interleaved phase of the parallel VSCs gives rise to the circulating current. The individual leg current (I_{A1} and I_{A2}) carries the circulating current in addition to the line current, and it can be decomposed into two components given as

$$\begin{aligned} I_{A1} &= I_{A1,l} + I_{A,c} \\ I_{A2} &= I_{A2,l} - I_{A,c} \end{aligned} \tag{C.1}$$

where, $I_{A1,l}$ and $I_{A2,l}$ are the components of the phase currents contributing to the resultant line current, and $I_{A,c}$ is the circulating current component. Assuming ideal VSCs and neglecting the effect of the hardware/control asymmetry, the current components contributing to the line current of the VSCs are considered equal. Therefore, the resultant line current is given as

$$I_A = 2I_{A1,l} = 2I_{A2,l} \tag{C.2}$$

and the circulating current between the VSCs is given as

$$I_{A,c} = \frac{I_{A1} - I_{A2}}{2} \tag{C.3}$$

The magnetic coupling between the parallel interleaved legs provided by the CI is used to suppress the circulating current, as discussed below.

The schematic of the CI is shown in Fig. C.2(a), and one of the possible physical arrangements of the CI is depicted in Fig. C.2(b). The flux linkage in the CI is given as

$$\lambda_A(t) = \lambda_{A1}(t) + \lambda_{A2}(t) = \int (V_{A1O} - V_{A2O})dt \tag{C.4}$$

where V_{A1O} and V_{A1O} are the pole voltages measured with respect to the fictitious dc-link mid-point O, as shown in Fig. F.1. The flux density in the core is given as

$$B_A(t) = \frac{1}{2NA_c} \int (V_{A1O} - V_{A2O})dt \tag{C.5}$$

where N is the number of turns and A_c is the core cross-sectional area. The maximum value of the flux density and the core losses are the important parameters to consider in the design of the CI. From (D.4), it can be inferred that the flux density depends on the time integral of the pole voltage differences, which in turn depends on the dc-link voltage, the interleaving angle,the modulation index, and the PWM scheme used. Therefore, the effect of the PWM schemes on the design of the CI is analyzed in the following section.

3 Pulsewidth Modulation Schemes and their Effect on the Coupled Inductor Design

The reference space vector $\overrightarrow{V}_{ref}$ is sampled, and it's magnitude (V_{ref}) and angle (ψ) information is used for the selection of the two adjacent active state vectors along with the zero vectors to synthesize the $\overrightarrow{V}_{ref}$ [11–13]. The respective dwell time of the active vectors is chosen to maintain the volt-sec balance. Let T_1, T_2, and T_z be the dwell times of the vectors $\overrightarrow{V}_1$, $\overrightarrow{V}_2$, and $\overrightarrow{V}_0/\overrightarrow{V}_7$, respectively, and it is given by

$$T_1 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V}_{ref}|}{V_{\text{dc}}} T_s \sin(60^\circ - \psi) \tag{C.6a}$$

$$T_2 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V}_{ref}|}{V_{\text{dc}}} T_s \sin(\psi) \tag{C.6b}$$

$$T_z = T_s - T_1 - T_2 \tag{C.6c}$$

Table C.1: SVM: Flux density description in a half switching cycle using piecewise linear equations

Sub-sector	Peak flux density B_p	Flux density $B(t)$
$0^\circ \leq \psi \leq 60^\circ$	$B_p = \frac{V_{dc}(T_z)}{8NA_c}$	$B(t) = \frac{4B_p}{T_z}t$ for $0 \leq t \leq \frac{T_z}{4}$
		$B(t) = B_p$ for $\frac{T_z}{4} \leq t \leq (\frac{T_s}{2} - \frac{T_z}{4})$
		$B(t) = B_p - \frac{4B_p}{T_z}[t - (\frac{T_s}{2} - \frac{T_z}{4})]$ for $(\frac{T_s}{2} - \frac{T_z}{4}) \leq t \leq \frac{T_s}{2}$
$60^\circ \leq \psi \leq 90^\circ$	$B_p = \frac{V_{dc}(T_z+2T_3)}{8NA_c}$	$B(t) = \frac{4B_p}{T_z+2T_3}t$ for $0 \leq t \leq \frac{T_z+2T_3}{4}$
		$B(t) = B_p$ for $\frac{T_z+2T_3}{4} \leq t \leq (\frac{T_s}{2} - \frac{T_z+2T_3}{4})$
		$B(t) = B_p - \frac{4B_p}{T_z+2T_3}[t - (\frac{T_s}{2} - \frac{T_z+2T_3}{4})]$ for $(\frac{T_s}{2} - \frac{T_z+2T_3}{4}) \leq t \leq \frac{T_s}{2}$

Table C.2: DPWM1: Flux density description in a half switching cycle using piecewise linear equations

Sub-sector	$\overrightarrow{V}_{ref}$ position	Peak flux density B_p	Flux density $B(t)$
$0^\circ \leq \psi \leq 30^\circ$	-	$B_p = 0$	$B(t) = 0$
$30^\circ \leq \psi \leq 60^\circ$	$M\cos(30^\circ - \psi) \geqslant \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{\mathrm{dc}} T_z}{4NA_c}$	$B(t) = \frac{-2B_p}{T_z}t, \quad \text{for } 0 \leq t \leq \frac{T_z}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_z}{2} \leq t \leq \frac{T_s - T_z}{2}$ $B(t) = -B_p + \frac{2B_p}{T_z}[t - (\frac{T_s - T_z}{2})], \quad \text{for } \frac{T_s - T_z}{2} \leq t \leq \frac{T_s}{2}$
	$M\cos(30^\circ - \psi) < \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{\mathrm{dc}}(T_1 + T_2)}{4NA_c}$	$B(t) = \frac{-2B_p}{T_1 + T_2}t, \quad \text{for } 0 \leq t \leq \frac{T_1 + T_2}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_1 + T_2}{2} \leq t \leq \frac{T_s - T_1 + T_2}{2}$ $B(t) = -B_p + \frac{2B_p}{T_1 + T_2}[t - (\frac{T_s - T_1 - T_2}{2})], \quad \text{for } \frac{T_s - T_1 - T_2}{2} \leq t \leq \frac{T_s}{2}$
$60^\circ \leq \psi \leq 90^\circ$	$M\sin(60^\circ - \psi_s) \geqslant \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{\mathrm{dc}}(T_z + T_3)}{4NA_c}$	$B(t) = \frac{-2B_p}{T_z + T_3}t, \quad \text{for } 0 \leq t \leq \frac{T_z + T_3}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_z + T_3}{2} \leq t \leq \frac{T_s - T_z - T_3}{2}$ $B(t) = -B_p + \frac{2B_p}{T_z + T_3}[t - (\frac{T_s - T_z - T_3}{2})], \quad \text{for } \frac{T_s - T_z - T_3}{2} \leq t \leq \frac{T_s}{2}$
	$M\sin(60^\circ - \psi_s) \geqslant \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{\mathrm{dc}} T_2}{4NA_c}$	$B(t) = \frac{-2B_p}{T_2}t, \quad \text{for } 0 \leq t \leq \frac{T_2}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_2}{2} \leq t \leq \frac{T_s - T_2}{2}$ $B(t) = -B_p + \frac{2B_p}{T_z + T_3}[t - (\frac{T_s - T_2}{2})], \quad \text{for } \frac{T_s - T_2}{2} \leq t \leq \frac{T_s}{2}$

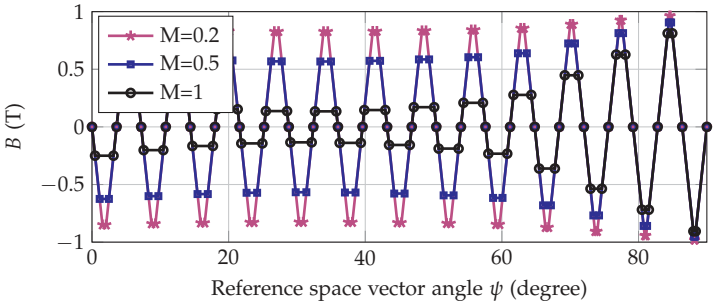


Fig. C.3: The flux density in the CI when VSCs are modulated using SVM. The switching frequency is 2.5 kHz and maximum flux density in the core is restricted to 1 T.

where V_{dc} sis the dc-link voltage and T_s is the switching cycle. The time during which the zero vector is applied can be written as

$$\begin{aligned} T_z &= K_z T_z + (1 - K_z) T_z \\ &\text{where, } 0 \leqslant K_z \leqslant 1 \end{aligned} \tag{C.7}$$

Different modulation possibilities exist with variation in the parameter K_z [12]. $K_z = 0.5$ results in a classical center aligned Space Vector Modulation (SVM). Similarly, sequences for Discontinuous PWM (DPWM) schemes can be generated by choosing the appropriate value of K_z. The SVM, DPWM1 (60°clamp), DPWM2 and DPWM3 (30°) clamp PWM schemes are considered for comparison [12–14].

3.1 The Center-aligned Space Vector Modulation

The opposite polarity zero vectors are applied at the same time for the duration of $T_z/4$. For low modulation indices, the dwell time of the zero vectors is dominant. As a result, the CI is subjected to more flux-linkage at low modulation indices. In a thermally limited CI design, the power density decreases due to the high core losses as a result of the more flux-linkage at low modulation indices. The flux density pattern is identical in every quarter period of the fundamental cycle and can be described using piecewise linear equations as given in Table D.1. The asymmetrical regular sampled PWM scheme is considered [14]. Therefore, the peak flux-linkage $\lambda_{A,p}$ changes in every half switching cycle. As can be inferred from the flux density description given in Table D.1, the $\lambda_{A,p}$ is a function of the modulation index M and the reference space vector angle ψ. The maximum value of the peak flux-linkage as a function of modulation index is given as

$$\lambda_A, pmax = \frac{1}{4} V_{\mathrm{dc}} T_s \tag{C.8}$$

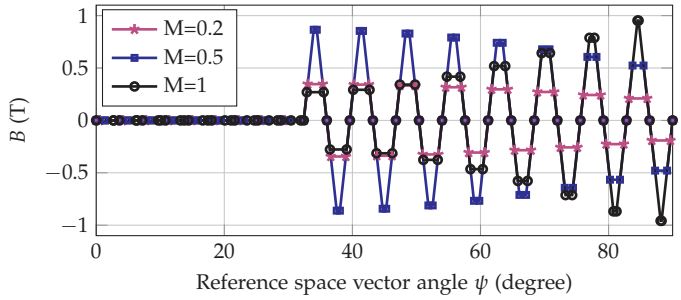


Fig. C.4: The flux density in the CI core when DPWM1 is used. The switching frequency is 2.5 kHz and maximum flux density in the core is restricted to 1 T.

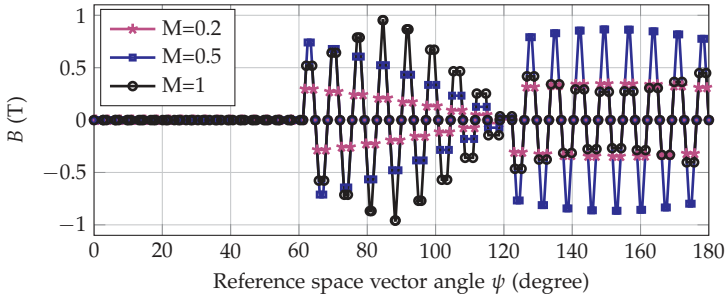


Fig. C.5: The flux density in the CI core when DPWM2 is used. The switching frequency is 2.5 kHz and maximum flux density in the core is restricted to 1 T.

Although the maximum value of the peak flux-linkage is the same for all modulation indices, the flux-linkage pattern is different. The flux density in the CI for different modulation indices is shown in Fig. C.3. The peak flux density in each half switching cycle is higher for lower modulation indices and reduces with the increase in the modulation index as evident from Fig. C.3.

3.2 DPWM1: 60°Clamp

In most grid connected application, the grid current has a power factor close to unity and the use of the 60° clamp PWM (DPWM1) results in low switching loss reduction [11, 13, 15]. The non-switching interval for each phase leg is arranged around the positive and negative peaks of the respective reference voltage. The switching losses are reduced since each phase leg is not switched in a region where the current through the semiconductor devices of that leg is at its maximum value [14].

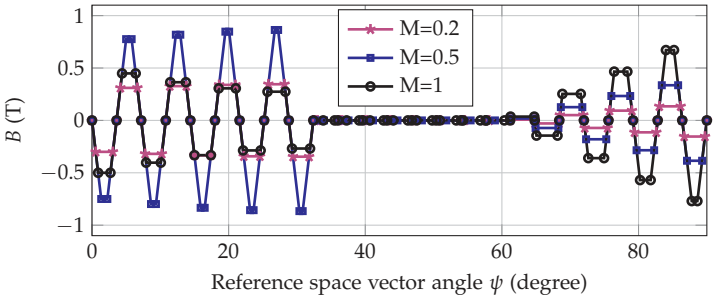


Fig. C.6: The flux density in the CI core when DPWM3 is used. The switching frequency is 2.5 kHz and maximum flux density in the core is restricted to 1 T.

The flux density in the CI depends on the magnitude and angle of the reference space vector $\overrightarrow{V}_{ref}$. The flux density in the CI for DPWM1 can be described using piecewise linear equations as given in Table D.3. The flux density for the first quarter of the fundamental cycle is plotted in Fig. C.4 for modulation indices of 0.2, 0.5, and 1. The maximum peak flux-linkage varies with the modulation index, and it is given as

$$\lambda_{A,pmax} = \begin{cases} V_{\mathrm{dc}} T_s \left(\frac{1}{\sqrt{3}} \frac{|\overrightarrow{V}_{ref}|}{V_{\mathrm{dc}}}\right), & 0 \leq M < 1/\sqrt{3} \\ \frac{1}{4} V_{\mathrm{dc}} T_s, & 1/\sqrt{3} \leq M < 2/\sqrt{3} \end{cases} \tag{C.9}$$

For modulation indices less than $1/\sqrt{3}$, the maximum value of the peak flux density in case of DPWM1 is less than that of the SVM. However, for a modulation indices higher than $1/\sqrt{3}$, the $\lambda_{A,pmax}$ for DPWM1 is the same as that of the SVM.

3.3 DPWM2: 30°Lagging Clamp

For a lagging power factor load, the use of DPWM2 can results in low switching losses [16]. Due to the asymmetrical switching sequence in each subsector, the flux density pattern is no longer identical in a quarter period of the fundamental cycle. Instead, the flux-density pattern is identical in every half period of the fundamental cycle. Similarly to DPWM1, the flux density in the CI for the DPWM2 can be also described by the piecewise linear equations. The flux density variation for different values of the modulation indices is plotted in Fig. C.5. The maximum value of the peak flux density $\lambda_{A,pmax}$ is the same as that of the DPWM1, and can be described by (C.9).

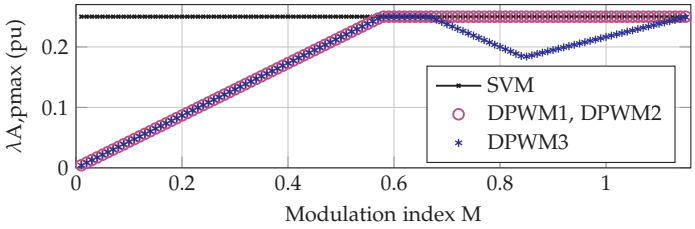


Fig. C.7: The maximum peak flux linkage $\lambda_{A,pmax}$ variation with the modulation index. The flux-linkage is normalized with respect to the $V_{dc}T_s$.

3.4 DPWM3: 30°Clamp

In this PWM scheme, each phase leg is clamped to the opposite dc-link in each 60°segment. Different zero vectors are applied in each subsector (half of a 60°sector). The flux density pattern is plotted in Fig. C.6. The peak flux-density $\lambda_{A,pmax}$ is given as

$$\lambda_{A,pmax} = \begin{cases} V_{\mathrm{dc}}T_s(\frac{1}{\sqrt{3}}\frac{|\overrightarrow{V}_{ref}|}{V_{\mathrm{dc}}}), \\ \qquad \text{for } 0 \leq M < 1/\sqrt{3} \\ \frac{1}{4}V_{\mathrm{dc}}T_s, \\ \qquad \text{for } 1/\sqrt{3} \leq M < 2/3 \\ V_{\mathrm{dc}}T_s(\frac{1}{2} - \frac{1}{2}\frac{|\overrightarrow{V}_{ref}|}{V_{\mathrm{dc}}}), \\ \qquad \text{for } 2/3 \leq M < 4/(3+\sqrt{3}) \\ V_{\mathrm{dc}}T_s(\frac{1}{2\sqrt{3}}\frac{|\overrightarrow{V}_{ref}|}{V_{\mathrm{dc}}}), \\ \qquad \text{for } 4/(3+\sqrt{3}) \leq M < 2/\sqrt{3} \end{cases} \tag{C.10}$$

The CI suppresses the circulating current by providing magnetic coupling between the interleaved parallel legs. Assuming strong magnetic coupling between the windings, the flux in the core has only high frequency components, which are concentrated around the odd multiple of the carrier frequency. The high frequency excitation could lead to significant size reduction of the CI. However, more losses due to the high frequency excitation may result into increased loss density, and considerable thermal management is required [17, 18]. In order to achieve higher power density, active cooling is preferred [17]. However, active cooling increases complexity and should be avoided.

The size of the CI can also be reduced by operating with high flux density. However, this also results in increased losses. Thus, the volume optimized design of the CI may result in thermally limited design, where the maximum flux density in the core is determined by the heat dissipation capability of

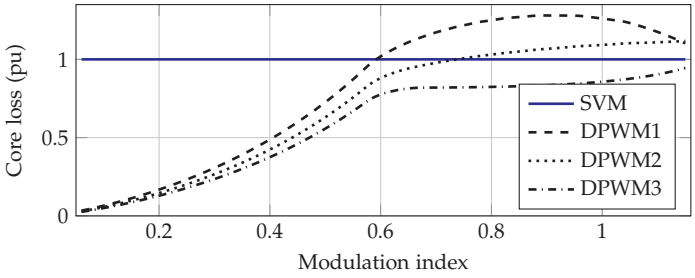


Fig. C.8: The core losses in the CI for different PWM schemes. The core losses are normalized with respect to that of the SVM. The carrier frequency is taken to be the same in all cases.

the CI [19], and not by the saturation flux density. For parallel interleaved VSCs, the PWM scheme has a strong influence on the maximum value of the peak flux density and the losses in the CI. The variation in the maximum value of the peak flux-linkage with the modulation index for different PWM schemes [9] is plotted in Fig. C.7. The maximum value of the peak flux linkage is the same in all schemes. However, the flux-linkage pattern is different. As a result, the core losses would be different in each of the schemes, which is an important factor in determining the size and the efficiency of the CI, and it is discussed below.

The $\overrightarrow{V}_{ref}$ is sampled twice in a switching cycle, and the losses are evaluated for every half switching cycle. The flux density behavior in the half switching cycle can be described by the piecewise linear equations given in Table D.1 and D.3 for the SVM, and the DPWM1, respectively.

The Improved Generalized Steinmetz Equation (IGSE) [20, 21] is used to calculate the core losses, and the core losses per unit volume is given as

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{C.11}$$

where α, β and k_i are the constants determined by the material characteristics. The flux density pattern is identical over a quarter period of the fundamental cycle. Therefore, the core losses are evaluated for each half switching cycle over a quarter period of the fundamental cycle. The average core loss over this period is given as

$$P_v = \frac{2}{\left(\frac{f_{sw}}{f_0}\right)} \sum_{k=1}^{\left(\frac{f_{sw}}{2f_0}\right)} \frac{2}{T_s} \int_0^{\frac{T_s}{2}} k_i (4B_{max} f_{sw})^{\alpha} (\Delta B_k)^{\beta-\alpha} dt \tag{C.12}$$

where f_0 is the fundamental frequency and f_{sw} is the switching frequency. The amorphous metal cores are considered, where the Steinmetz constants

Table C.3: Parameters for simulation study

Parameters	Simulation study
Switching frequency	2.5 kHz
DC-link voltage	680 V
Maximum flux density B_{max}	1 T
Window utilization factor K_w	0.5
RMS current in winding $I_{A,1(rms)}$	8 A
Current density J	2 A/m^2
Core material	Amorphous metal AMCC40
Core cross-sectional area A_c	$3.7\times10^{-4}m^2$
No. of turns N	92

are $\alpha = 1.51$, $\beta = 1.74$ and $k_i = 0.622$.

To compare the PWM method independent of the design parameters, the volumetric losses in each of the DPWM schemes are normalized with respect to that of the SVM. From Fig. C.8, it is evident that the DPWM3 outperforms other schemes in terms of the core losses. All the DPWM schemes have lower core losses compared to SVM at low modulation indices. The switching sequences involved in the DPWM2 are the same as the switching sequences of the DPWM1 in subsector 1 ($0^\circ < \psi \leqslant 30^\circ$) and switching sequences of DPWM3 in subsector 2 ($30^\circ < \psi \leqslant 60^\circ$). Thus, the core losses of the DPWM2 is an average of the core losses of the DPWM1 and core losses of the DPWM3 as depicted in Fig. C.8. For high modulation indices, the DPWM1 has the highest core losses, followed by the DPWM2 and SVM.

4 Simulation and Experimental Results

The CI is designed using area a product approach and the design data are given in Table K.3. The area-product (A_p), which is the product of core cross-sectional area A_c and window area A_w, is given as

$$A_p = A_c \times A_w = \frac{V_{dc,max} I_{A,1(rms)}}{4K_w J B_{max} F_s} \tag{C.13}$$

where $V_{dc,max}$ is the maximum dc-link voltage, $I_{A,1(rms)}$ is the rms current flowing through each winding, K_w is the window utilization factor and B_{max} is the maximum flux density. The magnetic model is implemented in PLECS and the simulated flux density is depicted in Fig. C.9. The flux density pattern for all PWM schemes closely matches with the analysis presented in Section III. The flux density and the circulating current for the SVM is plotted

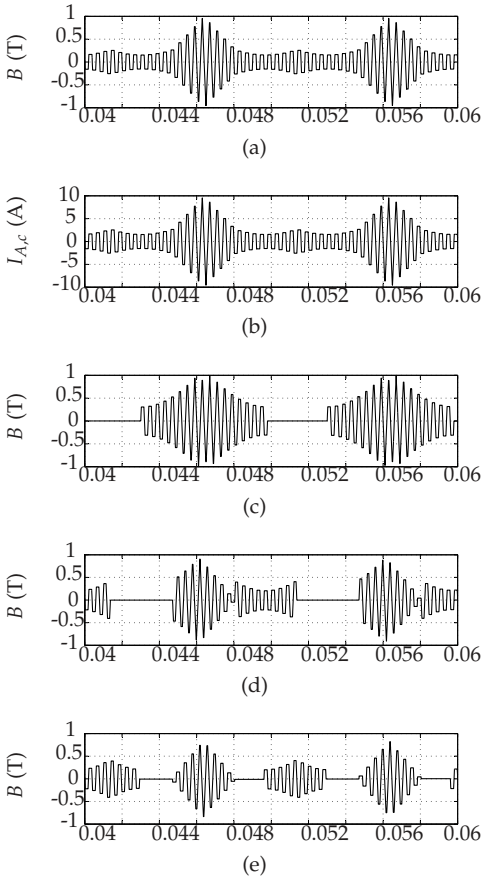
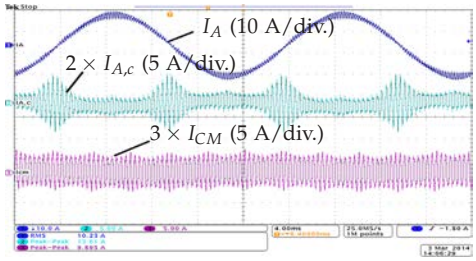
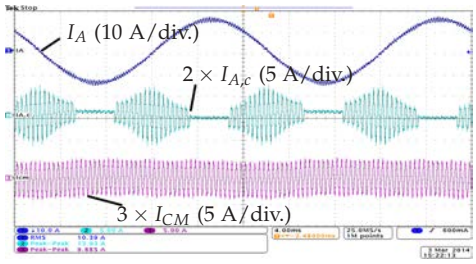


Fig. C.9: Simulated flux density in the CI and the circulating current. (a) SVM: flux density, (b) SVM: circulating current, (c) DPWM1: flux density, (d) DPWM2: flux density, (e) DPWM3: flux density.

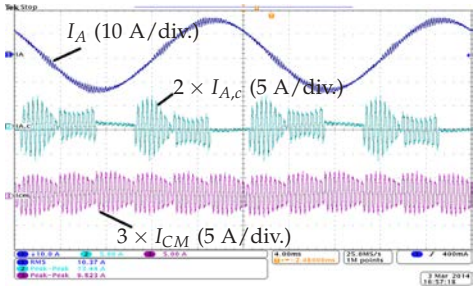
in Fig. C.9(a) and C.9(b), respectively. The simulation results are obtained with the modulation index of M=1. The core is excited only for two third period of the fundamental cycle for all DPWM schemes as evident from Fig. C.9. The maximum value of the peak flux density in the CI is the same in all the PWM schemes with M=1 except for the DPWM3. The DPWM3 has a low value of the maximum flux density for high modulation indices, as shown in Fig. C.7. The circulating current is proportional to the flux density in the core as it is evident from the Fig. C.9(a) and C.9(b), and thus the circulating current is measured and used for comparison of the PWM schemes in the experimental setup due to the ease of the measurement.



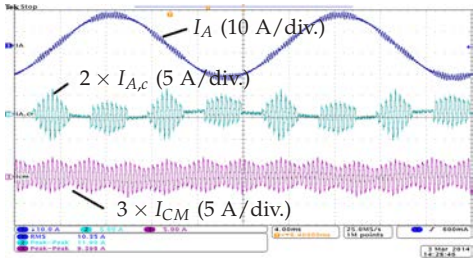
(a)



(b)



(c)



(d)

Fig. C.10: Performance comparison of the PWM schemes: The modulation index M=1. (a) SVM, (b) DPWM1, (c) DPWM2, (d) DPWM3.

Experimental measurements have been obtained to demonstrate the validity of the analysis presented in the paper. The schematic of the test setup is shown in Fig. F.1. The single phase inductors are used which will also introduce inductance in the circulating current path. This arrangement is adopted to simplify the measurement [9]. From Fig. F.1, the dynamic behavior of the circulating current is given as

$$I_{A,c} = \frac{1}{2L_f} \int (V_{A1O} - V_{A2O})\, dt \tag{C.14}$$

From (I.39) and (D.3), it is clear that the circulating current ($I_{A,c}$) is a replica of the flux linkage in the core. Therefore, the measurements of $I_{A1} - I_{A2}$, which is equal to $2 \times I_{A,c}$ are obtained.

The dc-link voltage is set to 600 V. The carrier frequency is taken to be 2.5 kHz and the interleaving angle of 180° is chosen. The dead-time of 2μ s is used. The line filter inductor of 6.8 mH is used, and a resistive load is set to 20 Ω. The inductance in the circulating current path is 2×6.8 mH. The results for modulation index of 1 for different PWM schemes are given in Fig. C.10.

The maximum value of the peak circulating current $I_{A,c}$ is measured for different the PWM schemes. The modulation index is varied in the full linear range. The peak value of circulating current is different in each half switching period and the highest value of the peak of $I_{A,c}$ is captured and given in Table C.4. The circulating current is a replica of the flux-linkage in the CI. The maximum value of the peak of the circulating current is the same for all of the PWM schemes. For SVM, a constant value of $I_{A,cmax}$ is observed over the entire modulation range, which is in agreement with the analysis presented in Section III. The DPWM schemes have smaller $I_{A,cmax}$ for lower modulation indices, and the $I_{A,cmax}$ variation with modulation index matches with the analysis.

5 Conclusion

The influence of the PWM schemes on the design of the CI, used for the circulating current reduction in the parallel interleaved VSCs, is discussed. The carrier interleaving improves the line current quality, thus the size of the line filter can be reduced. However, it requires additional circulating current filter. The design of this filter is strongly influenced by the PWM scheme used. The analytical model to evaluate the flux density in the CI is presented. The maximum value of the peak flux density for different PWM schemes is the same, however the flux density pattern is different. This would results in different core losses. The core losses, being an important factor for proper thermal design of the CI, it is also evaluated for each of the PWM schemes. The use of the SVM results in high core losses for low modulation indices.

Table C.4: Comparison: Maximum value of peak of $I_{A,c}$ (A)

M	$I_{A,cmax}$			
	SVM	DPWM1	DPWM2	DPWM3
0.1	3.55	0.79	0.81	0.84
0.2	3.52	1.46	1.47	1.47
0.3	3.50	2.09	2.07	2.02
0.4	3.55	2.68	2.67	2.63
0.5	3.50	3.23	3.19	3.20
0.6	3.48	3.72	3.72	3.79
0.7	3.48	3.63	3.63	3.71
0.8	3.42	3.55	3.42	3.27
0.9	3.40	3.50	3.42	2.82
1.0	3.40	3.48	3.36	2.97
1.1	3.36	3.48	3.36	3.24
1.15	3.38	3.39	3.37	3.37

The comparison also indicates that the use of DPWM3 results in the lowest core losses in the CI. Although the core is excited for two third period of the fundamental cycle in all DPWM schemes, the switching sequences involved in DPWM1 results in more flux linkage at high modulation indices and thus incurs the highest core losses for modulation indices higher than 0.6.

References

[1] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[2] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[3] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[4] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[5] T. Bhavsar and G. Narayanan, "Harmonic analysis of advanced bus-clamping PWM techniques," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2347–2352, 2009.

[6] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[7] R. Hausmann and I. Barbi, "Three-phase multilevel bidirectional DC-AC converter using three-phase coupled inductors," in *Proc. IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, Sept 2009, pp. 2160–2167.

[8] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[9] B. Cougo, T. Meynard, and G. Gateau, "Parallel Three-Phase Inverters: Optimal PWM Method for Flux Reduction in Intercell Transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[10] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, 2012.

[11] J. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a pwm converter system," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063–1075, 1991.

[12] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, May 1997.

[13] A. Hava, R. Kerkman, and T. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, 1998.

[14] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[15] M. Depenbrock, "Pulse width control of a 3-phase inverter with non-sinusoidal phase voltages," in *Conf. Rec. IEEE Int. Semiconductor Power Conversion Conference*, 1997, pp. 399–403.

[16] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based PWM-vsi drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan 1999.

[17] G. Ortiz, J. Biela, and J. Kolar, "Optimized design of medium frequency transformers with high isolation requirements," in *Proc. 36th Annual Conference on IEEE Industrial Electronics Society, IECON 2010*, Nov 2010, pp. 631–638.

[18] R. Wrobel and P. Mellor, "Thermal design of high-energy-density wound components," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4096–4104, Sept 2011.

[19] A. V. d. Bossche and V. C. Valchev, *Inductors and Transformers for Power Electronics*. Boca Raton, FL: CRC Press, 2004.

[20] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, 2002, pp. 36–41.

[21] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Thirty-Sixth IAS Annual Meeting, IEEE Industry Applications Conference.*, vol. 4, 2001, pp. 2203–2210 vol.4.

Paper D

Modified Discontinuous PWM for Size Reduction of the Circulating Current Filter in Parallel Interleaved Converters

Ghanshyamsinh Gohil,
RamKrishan Maheshwari,Lorand Bede,Tamas Kerekes,
Remus Teodorescu,Marco Liserre, and Frede Blaabjerg

The paper has been published in the
IEEE Transactions on Power Electronics Vol. 30, no. 7, pp. 3457-3470, July 2015.

The layout has been revised.

Abstract

Parallel Voltage Source Converters (VSCs) require an inductive filter to suppress the circulating current. The size of this filter can be minimized by reducing either the maximum value of the flux linkage or the core losses. This paper presents a modified Discontinuous Pulsewidth Modulation (DPWM) scheme to reduce the maximum value of the flux linkage and the core losses in the circulating current filter. In the proposed PWM scheme, the dwell time of an active vector is divided within a half-carrier cycle to ensure simultaneous occurrence of the same zero vectors in both VSCs. A function to decide the ratio of the dwell time of the divided active vector is also presented. The effect of the proposed PWM scheme on the maximum value of the flux linkage and the core losses is analyzed and compared with that of the space vector modulation and 60° clamped DPWM schemes. The analytical expressions for the maximum value of the flux linkage are derived for each of these PWM schemes. In addition, the effect of the proposed PWM scheme on the line current ripple and the switching losses is also analyzed and compared. To verify the analysis, experimental results are presented, which prove the effectiveness of the proposed PWM scheme.

1 Introduction

Three-phase voltage source converter (VSC) is widely used as a dc/ac converter in power electronics applications and often connected in parallel to meet the ever increasing demand for higher power rating converter [1, 2]. In grid-connected application, the total harmonic distortion (THD) in the line current should be low [3]. Due to limited switching frequency in the high power converters, large filters are required [4]. This leads to the increase in the size, weight, and cost of the overall converter system. For VSC fed variable speed machines, the harmonic distortion in the line current must be low for satisfactory operation of the drive [5]. The harmonic distortion depends primarily on the switching sequence, modulation index, and the switching frequency [5]. Several efforts have been made to improve the performance of the VSC in terms of the harmonic distortion and switching losses by using optimal switching sequences for modulation of the VSC legs [6–8].

The harmonic distortion in the line current can be reduced by increasing the switching frequency. However, the switching frequency of the semiconductor devices for high power applications is often limited. The effective switching frequency can be increased by using interleaved carriers in parallel-connected VSCs, and the line current quality can be improved [9]. The selection of the proper interleaving angle leads to the reduction in the line current ripple [9–15]. This implies that with interleaved parallel VSCs, the size of the line filter can be reduced, or the switching frequency can be reduced for a given set of filter components without violating the THD constraints.

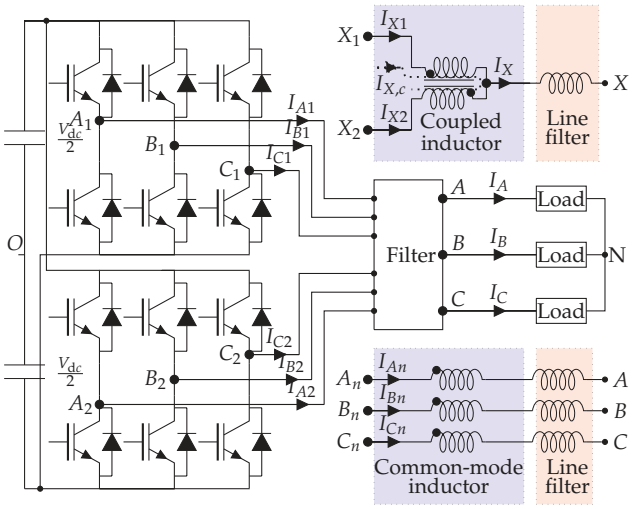


Fig. D.1: Two parallel interleaved VSCs with a common dc-link. The filter arrangement for circulating current suppression using the CI and the CM inductor is depicted, where $X = \{A, B, C\}$ and $n = \{1, 2\}$.

The circulating current is generated in the parallel VSCs due to hardware and control asymmetries [2]. When carrier interleaving is used, the pole voltages (measured with respect to the fictitious mid-point of the dc-link O, as shown in Fig. F.1) of the interleaved parallel legs are phase shifted. Therefore, there exists a potential difference that further increases the circulating current [16]. This is a high frequency circulating current with harmonic components concentrated around the odd multiples of the switching frequency [12]. This unwanted current increases stress on the semiconductor switches and causes additional losses. Therefore, it should be suppressed.

The circulating current is strongly influenced by the Pulsewidth Modulation (PWM) scheme. The conventional Space Vector Modulation (SVM) uses two adjacent active vectors and both of the zero vectors to synthesize a reference space vector. The zero vectors are applied at the beginning and at the end of a half-carrier cycle. Various other variants of the SVM scheme can be obtained by merely dividing the dwell time of the zero vectors unequally [17]. The Discontinuous PWM (DPWM) schemes use only one zero vector in each half-carrier cycle. The commutation of each phase leg is ceased for the one third period of the fundamental cycle [18, 19]. The PWM schemes, which modify the DPWM schemes by dividing one of the active vectors into two equal halves, are proposed in [20, 21]. These PWM schemes affect the line current ripple. A hybrid PWM scheme, which is a combination of the conventional SVM and different DPWM schemes, is proposed in [14] to mini-

mize the line current ripple for the parallel VSCs. However, separate dc-links are used and thus the circulating current filter is not present.

To avoid the circulating current, galvanic isolated transformer can be used for each VSC [22]. However, the use of the bulky transformer adds to the cost and increases the size. Therefore, it should be avoided. Instead of this, a coupled inductor (CI) [23–26] for each phase or a common-mode (CM) [27] inductor for each VSC can be used as a circulating current filter (Fig. F.1). Assuming strong magnetic coupling in the circulating current filter, the flux linkage in the core due to the line current can be neglected. Therefore, the flux linkage has only the high frequency components determined by the switching frequency. These high frequency components result in high core losses, and the circulating current filter requires larger surface area to dissipate the heat. Ewanchuk *et al.* [28] proposed a modified DPWM scheme that can make the CM voltage zero. This permits the use of a three limb inductor only. However, the number of commutations are increased. Therefore, it may not be feasible for medium/high power applications. Another PWM scheme is proposed in [29] to change the zero vector pattern by introducing an additional switching. This avoids the coexistence of the different zero vectors at a sector transition, and thus the jumping of the circulating current can be avoided.

The CI is used to provide magnetic coupling between the parallel interleaved legs [23–26]. A modified CI, which is proposed in [30], combines the functionality of both the line filter inductor and the circulating current filter. To reduce the flux linkage in the CI, a PWM scheme is proposed in [25]. This PWM scheme adds an optimal common-mode offset to the reference signals based on the modulation index. This can lead to the reduction of the maximum value of the flux linkage, but the discussion on the core losses is not given. However, the core losses are an important parameter to consider in the design of the circulating current filter. As discussed before, the high frequency components of the flux linkage increase the core losses. This may lead to a thermally limited design of the circulating current filter, where the maximum flux density in the core is limited by the heat dissipation capability and not by the magnetic saturation. In this case, the core losses can be reduced by reducing the peak flux density for a given switching frequency and core dimensions.

An active method to reduce the peak flux linkage as well as the core losses for the circulating current filter is proposed in this paper. The method divides the dwell time of an active vector within a half-carrier cycle to ensure simultaneous occurrence of the same zero vectors in both VSCs. A function to calculate the division of the dwell time are also proposed. This reduces both the maximum value of the flux linkage and the core losses in the circulating current filter.

The paper is organized as follows. Section II presents the basic theory of

the circulating current. In addition, the relationship between the flux linkage in the circulating current filter and the pole voltages is discussed for the interleaved VSCs. The effect of the different switching sequences on the flux linkage in the core is analyzed in Section III. Section IV presents the proposed DPWM scheme. The effect of the proposed PWM on the flux linkage in the CI and the CM inductor, the harmonic distortion in the line current, and the switching losses are also discussed and compared with that of the SVM and the 60° clamped DPWM. The experimental results are presented in Section V.

2 Parallel Interleaved VSCs

2.1 Circulating Current

The parallel-connected VSCs are operated with interleaved carrier signals. The circulating current ($I_{X,c}$) flows through the VSC legs in addition to the line current component $I_{X1,l}$, as shown in Fig. F.1. Therefore, the phase currents can be given by

$$\begin{aligned} I_{X1} &= I_{X1,l} + I_{X,c} \\ I_{X2} &= I_{X2,l} - I_{X,c} \end{aligned} \tag{D.1}$$

where $I_{X1,l}$ and $I_{X2,l}$ are the components of the phase currents contributing to the resultant line current I_X. $I_{X,c}$ is the circulating current, where $X = \{A, B, C\}$. Assuming ideal VSCs and neglecting the effect of the hardware/control asymmetries, the current component of each VSC, contributing to the grid current, are considered to be equal ($I_{X1,l} = I_{X2,l}$). Therefore,

$$I_{X,c} = \frac{I_{X1} - I_{X2}}{2} \tag{D.2}$$

The differential equation describing phase X circulating current can be given as

$$\frac{dI_{X,c}}{dt} = \frac{V_{X1O} - V_{X2O}}{L_c} \tag{D.3}$$

where L_c is the inductance offered to the circulating current. V_{X1O} and V_{X2O} are the pole voltages measured with respect to the fictitious dc-link mid point O.

2.2 Flux Linkage in Circulating Current Filter

To offer the desired inductance L_c to the circulating current, a CI and a CM inductor based solution is proposed in literature. To design the inductor, the maximum value of the flux linkage should be known. Therefore, the flux

linkage analysis for both the CI and the CM inductors is presented in this subsection.

2.2.1 Coupled Inductor

In case of the CI, the flux density in the core is given by

$$B_X(t) = \frac{1}{2NA_c}\int (V_{X1O} - V_{X2O})dt \tag{D.4}$$

and the flux linkage is

$$\lambda_X(t) = \lambda_{X1}(t) + \lambda_{X2}(t) = \int (V_{X1O} - V_{X2O})dt \tag{D.5}$$

where N is the number of turns, and A_c is the core cross-sectional area. The differential voltage across the filter ($V_{X1O} - V_{X2O}$) is responsible for the flux linkage, and in order to reduce the flux linkage, the time integral of this differential voltage should be reduced [26, 31].

Let L be the self inductance, and M be the mutual inductance of the CI. The pole voltage difference is given by

$$V_{X1O} - V_{X2O} = (L+M)\frac{dI_{X1}}{dt} - (L+M)\frac{dI_{X2}}{dt} \tag{D.6}$$

Using (F.3) and (D.6), the dynamic equation of the circulating current is given as

$$\frac{dI_{X,c}}{dt} = \frac{V_{X1O} - V_{X2O}}{2(L+M)} \tag{D.7}$$

If strong coupling is ensured ($L \approx M$), the inductance offered to the circulating current is $L_c = 4L$. From (I.39) and (D.7), the flux linkage in the CI is proportional to the circulating current $I_{X,c}$, which is half of the difference of the phase currents.

2.2.2 Common-mode Inductor

In the CM inductor, the magnetic coupling between the phases is used to suppress the circulating current. Since all three phases are wound on the same core, the flux linkage is proportional to the average of the phase currents, and the flux linkage is three times the CM flux linkage, where the CM flux linkage is given as

$$\lambda_{CM}(t) = \frac{\lambda_A(t) + \lambda_B(t) + \lambda_C(t)}{3} = \int (V_{CM1} - V_{CM2})\, dt \tag{D.8}$$

where V_{CMn} is the CM voltage of the nth VSC, and it is given by

$$V_{CMn} = \frac{V_{AnO} + V_{BnO} + V_{CnO}}{3} \tag{D.9}$$

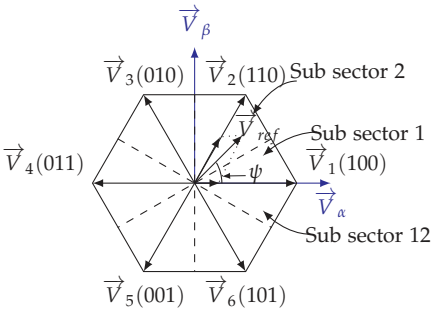


Fig. D.2: Basic space vector sectors and states in complex $\alpha\beta$ plane.

where $n = \{1, 2\}$.
The size of the CM inductor can be made smaller by reducing the peak flux linkage, which can be achieved by minimizing the time integral of the difference of the CM voltages. The difference depends on the interleaving angle, modulation index, and the PWM scheme used, and it is described in the following section.

3 Switching Sequences and their Effect on the Flux Linkage

The two-level VSC has eight voltage vectors defined by the combination of the switch states. These states generate six active vectors ($\overrightarrow{V}_1$- $\overrightarrow{V}_6$) and two zero vectors ($\overrightarrow{V}_0$, $\overrightarrow{V}_7$), as shown in Fig. D.2. The three-phase reference signals can be represented by a complex reference vector $\overrightarrow{V}_{ref}$. Based on the magnitude ($|\overrightarrow{V}_{ref}|$) and angle ($\psi$) of the sampled $\overrightarrow{V}_{ref}$, two adjacent active voltage vectors and zero vectors are commonly applied to synthesize the reference vector [19, 32, 33]. The respective dwell time of the active vectors is chosen to maintain the volt-sec balance. Let T_1, T_2, and T_z be the dwell time of $\overrightarrow{V}_1$, $\overrightarrow{V}_2$, and $\overrightarrow{V}_0$/ $\overrightarrow{V}_7$, respectively, and they are given by

$$T_1 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V}_{ref}|}{V_{dc}} T_s \sin(60^\circ - \psi) \tag{D.10a}$$

$$T_2 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V}_{ref}|}{V_{dc}} T_s \sin(\psi) \tag{D.10b}$$

$$T_z = T_s - T_1 - T_2 \tag{D.10c}$$

where T_s is the carrier interval. The dwell time of the zero voltage vectors $\overrightarrow{V}_0$ and $\overrightarrow{V}_7$ are given by $K_z T_z$ and $(1 - K_z)T_z$, respectively, where

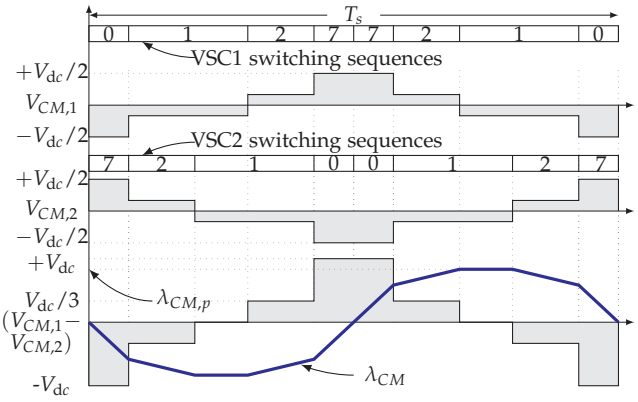


Fig. D.3: SVM: Common mode voltages of individual VSCs and their voltage difference when the carriers are interleaved by an angle of 180°.

$0 \leqslant K_z \leqslant 1$. Different modulation possibilities exist with variation in the parameter K_z [32]. For example, $K_z = 0.5$ results in the conventional SVM. By changing the value of K_z between zero and one with a frequency three times higher than the frequency of the reference signal, several DPWM schemes can be realized [32]. If the value of K_z is changed from zero to one in the middle of the sector 1, the reference signals for 60°clamped DPWM (DPWM1) is generated. Although the number of commutations is two-third of that of the SVM, the switching losses can be reduced up to 50% for unity power factor applications. However, the reduction in the switching losses strongly depend on the displacement power factor angle. For equal switching losses, the carrier frequency of the DPWM1 can be increased by a factor of K_f times than that of the SVM. The value of K_f varies in a wide range with the displacement power factor angle [19]. Therefore, the carrier frequency is taken to be the same in all of the cases for comparing the effect of the PWM schemes on the design of the circulating current filter. In addition, the switching losses are also compared for a fair evaluation. The effect of the switching sequences of the SVM and the DPWM1 on the CM flux linkage is analyzed. The interleaving angle is considered to be 180°.

3.1 Conventional Space Vector Modulation

In SVM, the opposite polarity zero vectors are applied at the same time and result in a maximum value of the CM voltage difference, as depicted in Fig. H.10. The simultaneous occurrence of $\overrightarrow{V}_7$ in VSC1 and $\overrightarrow{V}_0$ in VSC2 results in more flux linkage since the polarity of the CM voltage is opposite in this case. The same argument applies when both $\overrightarrow{V}_0$ in VSC1 and $\overrightarrow{V}_7$ in VSC2

coexist. Both of these undesirable voltage vectors appear when SVM is used with the interleaving angle of 180°. For low modulation indices, the dwell time of the zero vectors is dominant. This results in high flux linkage at lower modulation indices.

3.2 60°Clamped Discontinuous PWM (DPWM1)

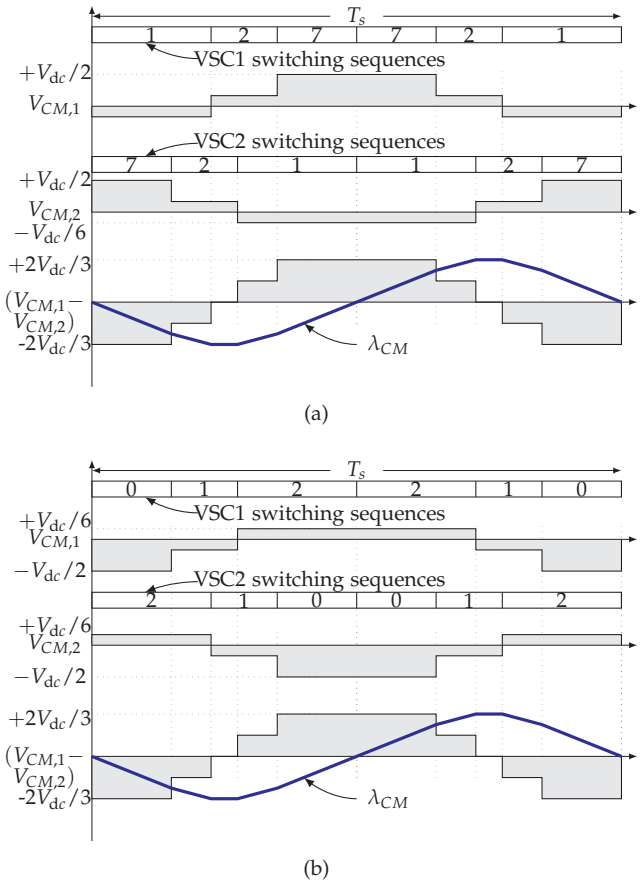


Fig. D.4: DPWM1: Switching sequences and common-mode voltages of both the VSCs. (a) sub-sector: 1, $0° \leq \psi < 30°$, (b) sub-sector: 2, $30° \leq \psi < 60°$.

The DPWM1 uses two different switching sequences in each sector. For $0° \leq \psi < 30°$ (sub-sector 1), the voltage vectors $\overrightarrow{V}_1$, $\overrightarrow{V}_2$, and $\overrightarrow{V}_7$ (127) are applied sequentially and vice-versa, as shown in Fig. D.4(a). Accordingly, $\overrightarrow{V}_0$, $\overrightarrow{V}_1$, and $\overrightarrow{V}_2$ (012) are applied for $30° \leq \psi < 60°$ (sub-sector 2), as

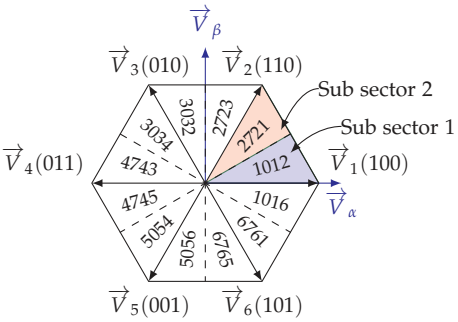


Fig. D.5: Switching sequences of the proposed scheme in each sub-sector.

shown in Fig. D.4(b). The CM voltages, their difference, and the CM flux linkage in both of the sub-sectors are depicted in Fig. D.4. The use of $\overrightarrow{V}_1$ and $\overrightarrow{V}_7$ results in opposite polarity CM voltages. Similarly, the polarities of the CM voltages are different when the voltage vectors $\overrightarrow{V}_0$ and $\overrightarrow{V}_2$ are used. The CM voltage difference increases if the polarities of the CM voltages are different in both VSCs. These undesirable vectors appear in both sub-sectors, when DPWM1 is used, as shown in Fig. D.4.

4 Modified DPWM for Circulating Current Reduction

It is evident that the PWM sequences determine the flux linkage pattern. Therefore, the design of the circulating current filter is strongly influenced by the PWM scheme used. Some vectors in a PWM scheme which may lead to high flux linkage are summarized below.

- The simultaneous application of $\overrightarrow{V}_7$ in VSC1 and $\overrightarrow{V}_0$ in VSC2 and vice-versa.
- The simultaneous occurrence of a zero vector in VSC1 and an active vector in VSC2 and vice-versa. For example, the simultaneous occurrence of $\overrightarrow{V}_7$ and $\overrightarrow{V}_1$ (vectors with opposite polarity CM voltage).

Since these vectors cause high flux linkage in the circulating current filter, they should be avoided. However, if the same zero vectors in both VSCs (e.g. $\overrightarrow{V}_7$ in both VSCs) are applied simultaneously, a significant reduction in the flux linkage can be achieved. Based on these observations, a PWM scheme is presented where the division of an active vector within a half-carrier cycle is

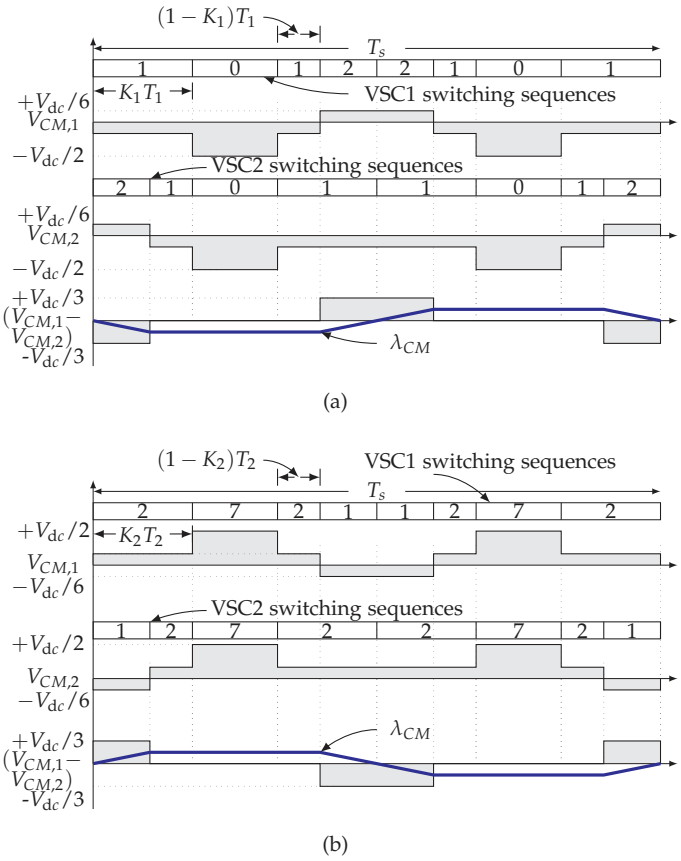


Fig. D.6: Proposed modulation scheme: Switching sequences and CM voltages of both the VSCs with an interleaving angle of 180°. (a) sub-sector 1: $0° \leq \psi < 30°$, (b) sub-sector 2: $30° \leq \psi < 60°$.

used to align the same zero vector in both VSCs.

The PWM schemes where the dwell time of the active vector are divided into two equal intervals in each half-carrier cycle is proposed in [5, 20, 21, 34, 35]. However, the dwell time of an active vector is not divided equally in this paper. It is divided in a manner to align the same zero vectors of both VSCs. The ratio, in which the dwell time is divided, varies with the reference space vector angle, and it is updated in each half-carrier cycle.

The sequences used in the proposed PWM scheme are depicted in Fig. D.5. The numbers shown in Fig. D.5 represent the sequence in which the voltage vectors are applied, e.g. 1012 represents that $\overrightarrow{V}_1$, $\overrightarrow{V}_0$, $\overrightarrow{V}_1$, and $\overrightarrow{V}_2$ are applied in sequence. The discussion is restricted to the first sector of

Table D.1: Flux density description in a half-carrier cycle using piecewise linear equations for SVM

Sub-sector	Peak flux density B_p	Flux density $B(t)$
$0^\circ \leq \psi \leq 60^\circ$	$B_p = \frac{V_{dc}(T_z)}{8NA_c}$	$B(t) = \frac{4B_p}{T_z}t$ for $0 \leq t \leq \frac{T_z}{4}$ $B(t) = B_p$ for $\frac{T_z}{4} \leq t \leq (\frac{T_s}{2} - \frac{T_z}{4})$ $B(t) = B_p - \frac{4B_p}{T_z}[t - (\frac{T_s}{2} - \frac{T_z}{4})]$ for $(\frac{T_s}{2} - \frac{T_z}{4}) \leq t \leq \frac{T_s}{2}$
$60^\circ \leq \psi \leq 90^\circ$	$B_p = \frac{V_{dc}(T_z+2T_3)}{8NA_c}$	$B(t) = \frac{4B_p}{T_z+2T_3}t$ for $0 \leq t \leq \frac{T_z+2T_3}{4}$ $B(t) = B_p$ for $\frac{T_z+2T_3}{4} \leq t \leq (\frac{T_s}{2} - \frac{T_z+2T_3}{4})$ $B(t) = B_p - \frac{4B_p}{T_z+2T_3}[t - (\frac{T_s}{2} - \frac{T_z+2T_3}{4})]$ for $(\frac{T_s}{2} - \frac{T_z+2T_3}{4}) \leq t \leq \frac{T_s}{2}$

Table D.2: Flux density description in CI for the proposed PWM scheme using piecewise linear equations

Sub-sector	Peak flux density B_p	Flux density $B(t)$
$0^\circ \leq \psi \leq 60^\circ$	$B_p = 0$	$B(t) = 0$
$60^\circ \leq \psi \leq 90^\circ$	$B_p = \frac{V_{dc}(T_3)}{4NA_c}$	$B(t) = \frac{2B_p}{T_3}t$ for $0 \leq t \leq \frac{T_3}{2}$ $B(t) = B_p$ for $\frac{T_3}{2} \leq t \leq \frac{T_s - T_3}{2}$ $B(t) = B_p - \frac{2B_p}{T_3}[t - (\frac{T_s - T_3}{2})]$ for $\frac{T_s - T_3}{2} \leq t \leq \frac{T_s}{2}$

Table D.3: DPWM1: Flux density description in a half switching cycle using piecewise linear equations

Sub-sector	$\overrightarrow{V}_{ref}$ position	Peak flux density B_p	Flux density $B(t)$
$0^\circ \leq \psi \leq 30^\circ$	-	$B_p = 0$	$B(t) = 0$
$30^\circ \leq \psi \leq 60^\circ$	$M\cos(30-\psi) \geqslant \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}T_z}{4NA_c}$	$B(t) = \frac{-2B_p}{T_z}t, \quad \text{for } 0 \leq t \leq \frac{T_z}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_z}{2} \leq t \leq \frac{T_s-T_z}{2}$ $B(t) = -B_p + \frac{2B_p}{T_z}[t - (\frac{T_s-T_z}{2})], \text{for} \frac{T_s-T_z}{2} \leq t \leq \frac{T_s}{2}$
	$M\cos(30-\psi) < \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}(T_1+T_2)}{4NA_c}$	$B(t) = \frac{-2B_p}{T_1+T_2}t, \quad \text{for } 0 \leq t \leq \frac{T_1+T_2}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_1+T_2}{2} \leq t \leq \frac{T_s-T_1+T_2}{2}$ $B(t) = -B_p + \frac{2B_p}{T_1+T_2}[t - (\frac{T_s-T_1-T_2}{2})], \text{for} \frac{T_s-T_1-T_2}{2} \leq t \leq \frac{T_s}{2}$
$60^\circ \leq \psi \leq 90^\circ$	$M\sin(60-\psi_s) \geqslant \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}(T_z+T_3)}{4NA_c}$	$B(t) = \frac{-2B_p}{T_z+T_3}t, \quad \text{for } 0 \leq t \leq \frac{T_z+T_3}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_z+T_3}{2} \leq t \leq \frac{T_s-T_z-T_3}{2}$ $B(t) = -B_p + \frac{2B_p}{T_z+T_3}[t - (\frac{T_s-T_z-T_3}{2})], \text{for} \frac{T_s-T_z-T_3}{2} \leq t \leq \frac{T_s}{2}$
	$M\sin(60-\psi_s) < \frac{1}{\sqrt{3}}$	$B_p = \frac{V_{dc}T_2}{4NA_c}$	$B(t) = \frac{-2B_p}{T_2}t, \quad \text{for } 0 \leq t \leq \frac{T_2}{2}$ $B(t) = -B_p, \quad \text{for } \frac{T_2}{2} \leq t \leq \frac{T_s-T_2}{2}$ $B(t) = -B_p + \frac{2B_p}{T_z+T_3}[t - (\frac{T_s-T_2}{2})], \text{for} \frac{T_s-T_2}{2} \leq t \leq \frac{T_s}{2}$

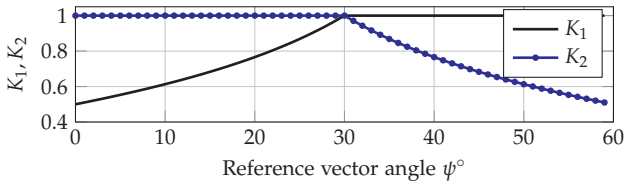


Fig. D.7: Variation in parameter K_1, K_2 with reference vector angle ψ. Due to the symmetry the plot is restricted to the first sector.

the space vector diagram. The same discussion applies to other sectors due to the symmetry. From Fig. D.5, it is evident that each phase discontinues switching for one third period of the fundamental cycle. For example, phase A is clamped twice to the positive dc-link for $30^\circ \leqslant \psi < 60^\circ$ and $300^\circ \leqslant \psi < 330^\circ$ and clamped twice to the negative dc-link for $120^\circ \leqslant \psi < 150^\circ$ and $210^\circ \leqslant \psi < 240^\circ$ in a fundamental period. The active voltage vector with the maximum dwell time is divided into two intervals and applied twice in a half-carrier cycle. Therefore, one of the phase legs is switched twice. In the proposed PWM scheme, one phase does not switch, whereas one of the phases is switched twice in a half-carrier cycle. Hence, it is referred to as the modified DPWM in this paper.

If the reference vector is in sub-sector 1, as shown in Fig. D.5, the dwell time of $\overrightarrow{V}_1$ is more than the dwell time of $\overrightarrow{V}_2$. Thus, the dwell time of $\overrightarrow{V}_1$ is divided, and $\overrightarrow{V}_0$ is applied in between to ensure simultaneous occurrence of the same zero vector in both VSCs. The reverse is true for sub-sector 2. Therefore, in sub-sector 1 ($0^\circ \leqslant \psi < 30^\circ$), T_1 is divided into two intervals and can be given as

$$T_1 = K_1 T_1 + (1 - K_1) T_1 \tag{D.11}$$

where $0 \leqslant K_1 \leqslant 1$. Similarly, in sub-sector 2 ($30^\circ \leqslant \psi < 60^\circ$), T_2 is divided into two intervals;

$$T_2 = K_2 T_2 + (1 - K_2) T_2 \tag{D.12}$$

where $0 \leqslant K_2 \leqslant 1$. The flexibility offered by the division of the active vectors is used to ensure simultaneous occurrence of the same zero vectors in both VSCs.

The switching sequences and the CM voltages in sub-sector 1 and sub-sector 2 for the proposed scheme are shown in Fig. D.6(a) and Fig. D.6(b), respectively for one switching cycle. In sub-sector 1, the value of K_1 is updated in each half-carrier cycle, while K_2 is equal to one. In sub-sector 2, K_2 is varied, and K_1 is equal to one. The careful observation of the switching

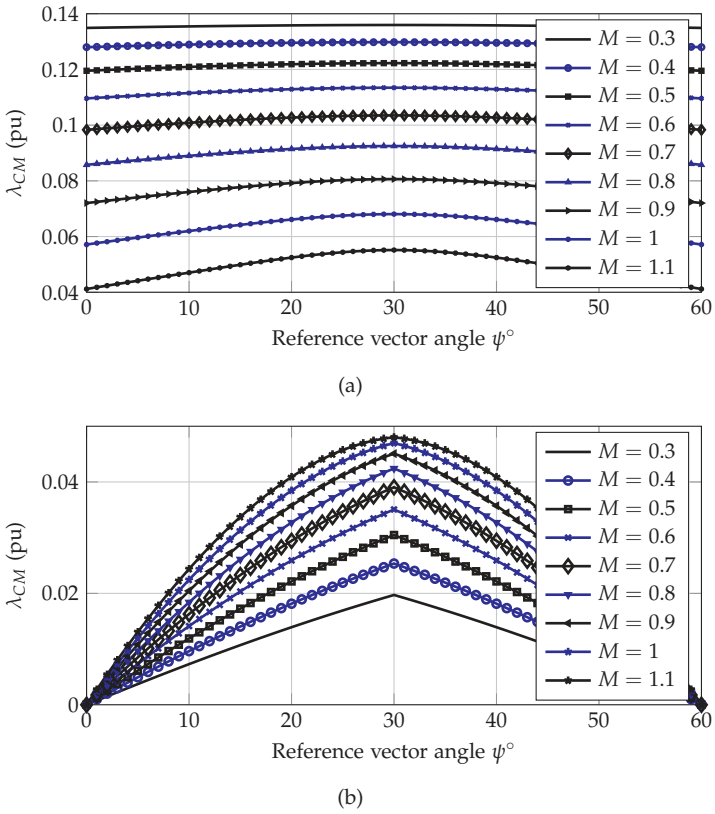


Fig. D.8: RMS value of the CM flux linkage λ_{CM} vs. reference space vector angle ψ in a switching cycle for (a) SVM and (b) the proposed PWM scheme. The flux linkage is normalized with respect to the $V_{\mathrm{dc}}T_s$.

sequence depicted in Fig. D.6 reveals that the same zero vector of both VSCs can coexist if

$$K_1 = \frac{T_1 + T_2}{2T_1}, K_2 = 1 \tag{D.13}$$

in sub-sector 1 and

$$K_1 = 1, K_2 = \frac{T_1 + T_2}{2T_2} \tag{D.14}$$

in sub-sector 2. The variation of K_1 and K_2 over a sector is depicted in Fig. D.7. The rms value of the CM flux linkage λ_{CM} in a switching cycle for the proposed scheme is shown in Fig. D.8 and compared with that of the SVM. A substantial reduction in λ_{CM} is achieved, especially at low values of the modulation indices.

As discussed in Section II, the PWM schemes strongly influence the flux

Table D.4: Maximum value of the peak flux linkage in a CI for different modulation schemes

Scheme	Max. value of peak flux linkage ($\lambda_{A,pmax}$)
SVM	$\lambda_{A,pmax} = \frac{1}{4} V_{dc} T_s$
DPWM1	$\lambda_{A,pmax} = \begin{cases} V_{dc} T_s (\frac{1}{\sqrt{3}} \frac{\lvert \overrightarrow{V}_{ref} \rvert}{V_{dc}}), & 0 \leq M < 1/\sqrt{3} \\ \frac{1}{4} V_{dc} T_s, & 1/\sqrt{3} \leq M < 2/\sqrt{3} \end{cases}$
Proposed	$\lambda_{A,pmax} = V_{dc} T_s (\frac{1}{2\sqrt{3}} \frac{\lvert \overrightarrow{V}_{ref} \rvert}{V_{dc}})$

linkage and the core losses in the circulating current filter. Therefore, the effects of the proposed PWM scheme on the filter design along with the line ripple current and the switching losses are discussed and compared with that of the SVM and the DPWM1 in the following subsections.

4.1 Effect of the Switching Sequences on the Circulating Current Filter Design

The circulating current is suppressed by introducing an impedance in the circulating current path. Typically, this impedance can be introduced by inserting CM inductor in series with the line filter inductors [27] or using CI for each phase group [23–25, 30]. Assuming a strong coupling between the windings, the effect of the leakage flux is neglected in the analysis. Therefore, the flux linkage in the core has only high frequency components, which result in more core losses. In addition to this, the maximum value of the flux linkage in the core also influences the core size. Therefore, both maximum value of the flux linkage and the core losses should be considered while designing both the CI and the CM inductor, and they are discussed below.

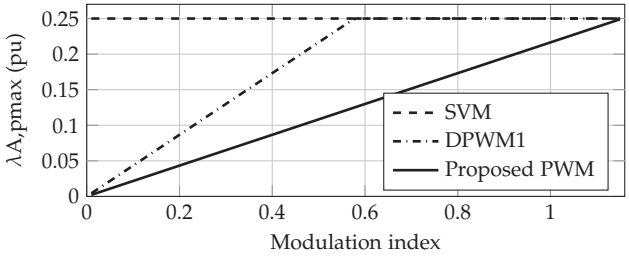


Fig. D.9: Comparison of the maximum value of the peak flux linkage as a function of the modulation index. The flux linkage is normalized with respect to the $V_{dc} T_s$.

4.1.1 Coupled Inductor

The CI provides magnetic coupling between the interleaved legs, and the schematic is shown in Fig. F.1. The flux linkage in the coupled inductor of phase A is evaluated using (I.39). Since the dwell time is updated in each half carrier cycle, the peak flux linkage is also different for each half-carrier cycle. The formulas describing the maximum value of the peak flux linkage as a function of the modulation index is given in Table. D.4, and plotted in Fig. D.9. The maximum value of the peak flux linkage is the same in all cases. However, the flux linkage pattern is different, which affects the core losses, and thus the design of the CI. Due to the quarter wave symmetry of the reference signal, the flux density pattern is the same in each quarter period of the fundamental cycle. Thus, it is sufficient to evaluate the core losses for that period (e.g. $0^\circ \leq \psi \leq 90^\circ$). The flux density behavior in a half-carrier cycle for the proposed PWM scheme is described by the piecewise linear equations given in Table D.2 and depicted in Fig. D.10(c). The piecewise linear equations, describing the flux density behavior in the CI, for the SVM and the DPWM1 are given in Table D.1 and Table D.3, respectively. The term T_3 in those tables is the dwell time of the voltage vector $\overrightarrow{V}_3$.

In case of SVM, the core is excited over an entire fundamental cycle. However, for the DPWM1, the core is excited for two third of the fundamental cycle, as shown in Fig. D.10. On the other hand, in the proposed PWM scheme, the core is excited only for one third of the fundamental cycle, as depicted in Fig. D.10(c).

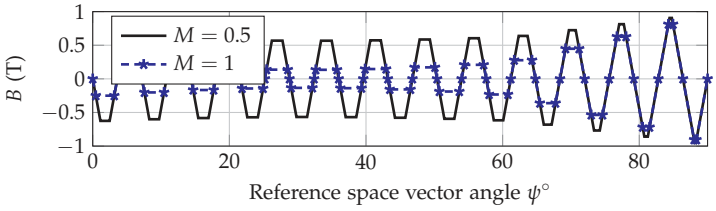
The core losses with the proposed PWM scheme are expected to reduce due to the reduction in both the peak flux linkage and the duration of the core excitation, and it is evaluated using the Improved Generalized Steinmetz Equation (IGSE) [36, 37] given as

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB(t)}{dt}\right|^\alpha (\Delta B)^{\beta-\alpha} dt \tag{D.15}$$

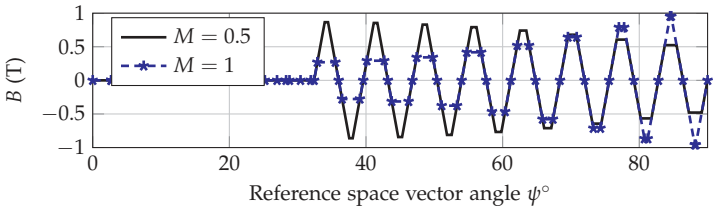
where α, β, and k_i are the constants determined by the material characteristics, and P_v is the core loss per unit volume. Using (K.62), the core losses averaged over a quarter of the fundamental cycle is given as

$$P_{v,avg} = \frac{2}{\left(\frac{f_{sw}}{f_0}\right)} \sum_{k=1}^{\left(\frac{f_{sw}}{2f_0}\right)} \frac{2}{T_s} \int_0^{\frac{T_s}{2}} k_i \left|\frac{dB_k(t)}{dt}\right|^\alpha (\Delta B_k)^{\beta-\alpha} dt \tag{D.16}$$

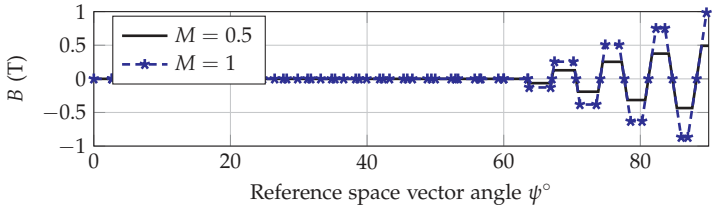
where f_0 is the fundamental frequency, and f_{sw} is the switching frequency. In order to make the core loss analysis more general (independent of the core



(a)



(b)



(c)

Fig. D.10: The flux density pattern in the CI core for modulation indices of 0.5 and 1. (a) SVM, (b) DPWM1, (c) Proposed scheme.

dimensions), the loss behavior is described in terms of B_{max} and T_s, as

$$P_{v,avg} = \frac{2}{(\frac{f_{sw}}{f_0})} \sum_{k=1}^{(\frac{f_{sw}}{2f_0})} \frac{2}{T_s} \int_0^{\frac{T_s}{2}} k_i (4B_{max} f_{sw})^{\alpha} (\Delta B_k)^{\beta-\alpha} dt \tag{D.17}$$

To make the core losses comparison independent of the design parameters, the analysis is presented in terms of the Core Loss Function (CLF), where CLF is given as the ratio of the average volumetric core loss for a PWM scheme to the average volumetric core loss for the SVM at a given modulation index M.

$$CLF = \frac{P_{v,avg}(M)}{P_{v,avg(SVM)}(M)} \tag{D.18}$$

The CLFs for all considered PWM schemes are depicted in Fig. D.11. Amor-

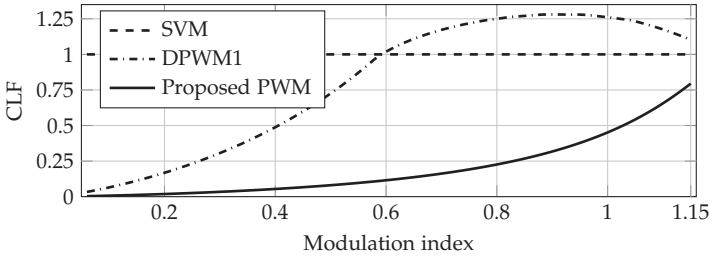


Fig. D.11: CLF as a function of the modulation index.

phous metal core is considered, where $\alpha = 1.51$, $\beta = 1.74$, and $k_i = 0.622$. Lower core losses over the entire modulation range are observed for the proposed method compared to the other considered schemes. The use of the SVM results in highest core losses in the CI for low modulation indices ($M < 0.6$), whereas the core losses are the highest in case of DPWM1 at high modulation indices.

The volume optimized design of the inductor often results in non-saturated thermally limited design, and the core losses primarily determine the size of the CI [38]. Due to the substantial reduction in the core losses with the proposed scheme, small size of the CI with minimal thermal management can be achieved with the proposed PWM scheme.

4.1.2 Common-mode Inductor

Asiminoaei *et al.* [27] proposed the use of a CM inductor to reduce the circulating current. This solution permits un-equal load sharing between the parallel interleaved VSCs and scalability, and may be a preferred solution when the modularity is the main design objective. The volume of the CM inductor can be minimized by reducing either the maximum value of the peak CM flux linkage or the core losses. The maximum value of the peak CM flux linkage as a function of the modulation index is given in Table F.1 and plotted in Fig. D.12 for the proposed PWM scheme along with that of the SVM and the DPWM1.

For SVM, the maximum value of the peak flux linkage increases as the modulation index decreases. Therefore, for applications demanding operation over the full modulation range, the CM inductor has to be designed for the maximum flux linkage, which occurs at low modulation indices. On the other hand, the CM is subjected to maximum flux linkage for a modulation index $M = 2/3$ if DPWM1 is employed. The proposed PWM scheme has the lowest peak flux linkage, compared to other PWM schemes, for the entire modulation range. The reduction in the maximum flux linkage in case of the CM filter is achieved by using the proposed DPWM scheme. As a result,

Table D.5: Maximum value of the peak CM flux linkage

PWM scheme	Max of the peak CM flux linkage ($\lambda_{CM,pmax}$)
SVM	$\lambda_{CM,pmax} = V_{dc}T_s(\frac{1}{4} - \frac{1}{3\sqrt{3}}\frac{\lvert\overrightarrow{V}_{ref}\rvert}{V_{dc}})$
DPWM1	$\lambda_{CM,pmax} = V_{dc}T_s(\frac{1}{3}\frac{\lvert\overrightarrow{V}_{ref}\rvert}{V_{dc}})$ for $(0 \leq \mathrm{M} \leq \frac{2}{3})$ $\lambda_{CM,pmax} = V_{dc}T_s\left(\frac{1}{3} - \frac{1}{3}\frac{\lvert\overrightarrow{V}_{ref}\rvert}{V_{dc}}\cos(60 - \arcsin\frac{\sqrt{3}V_{dc}}{4\lvert\overrightarrow{V}_{ref}\rvert})\right)$ for $(\frac{2}{3} \leq \mathrm{M} \leq \frac{2}{\sqrt{3}})$
Proposed PWM	$\lambda_{CM,pmax} = V_{dc}T_s(\frac{1}{6\sqrt{3}}\frac{\lvert\overrightarrow{V}_{ref}\rvert}{V_{dc}})$

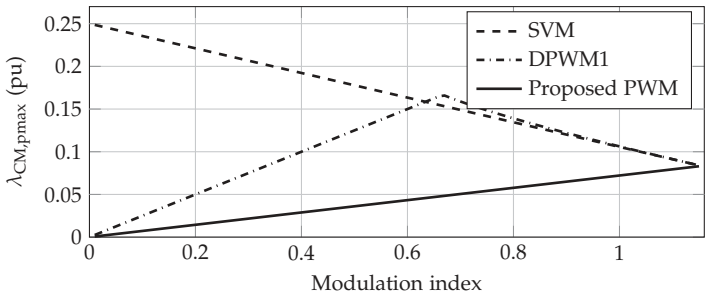


Fig. D.12: Comparison of the maximum values of the peak CM flux linkage as a function of the modulation index. The flux linkage is normalized with respect to $V_{dc}T_s$.

small CM inductor can be realized.

4.2 Ripple Current Analysis

The line current ripple of the proposed PWM scheme is analyzed and compared with that of the SVM and the DPWM1. The reference vector is synthesized using the discrete vectors. Thus, at any given instant, an error between the applied voltage vector and the reference vector exists. The error voltage vectors for a given sampling instance are shown in Fig. J.6. The time integral of the error vectors gives the harmonic flux vector, which is proportional to the ripple current [5, 20, 21].

In the synchronously rotating reference frame, the instantaneous error

voltage vectors depicted in Fig. J.6 are given as

$$\overrightarrow{V}_{err,1} = [\cos\psi - V_{ref}] - j\sin\psi \tag{D.19a}$$

$$\overrightarrow{V}_{err,2} = [\cos(60^\circ - \psi) - V_{ref}] + j\sin(60^\circ - \psi) \tag{D.19b}$$

$$\overrightarrow{V}_{err,z} = -V_{ref} \tag{D.19c}$$

In the proposed scheme, the time duration, for which an active vector is applied, is divided unequally, and the division of the active vector follows the rule given by (D.13) and (D.14).

For the proposed PWM scheme, the harmonic flux vector is given as

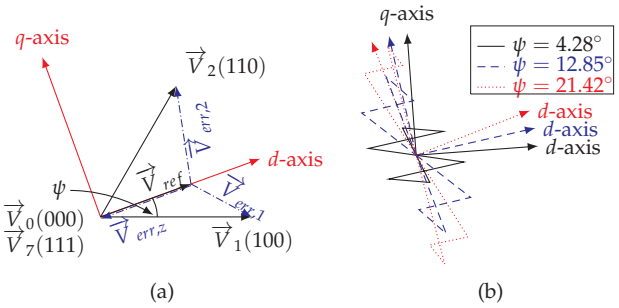


Fig. D.13: (a) The active and zero vectors to synthesize given reference vector and corresponding error voltage vectors, (b) Harmonic flux vector trajectory for different values of reference vector angle ψ for 1012 sequence in sub-sector 1.

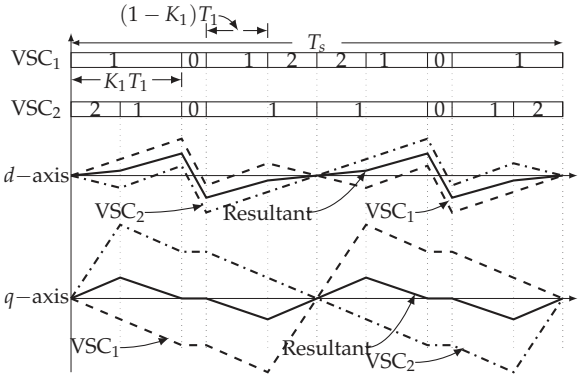


Fig. D.14: d-axis and q-axis ripple components of a harmonic flux vector over a switching cycle for two parallel VSCs and their resultant with an interleaving angle of 180° and reference vector angle $\psi = 12.8^\circ$.

$$\overrightarrow{V}_{err,1}K_1T_1 = [\cos\psi - V_{ref}]K_1T_1 - jK_1T_1\sin\psi \tag{D.20a}$$

$$\overrightarrow{V}_{err,1}(1-K_1)T_1 = [\cos\psi - V_{ref}](1-K_1)T_1 - j(1-K_1)T_1\sin\psi$$

$$\overrightarrow{V}_{err,2}T_2 = [\cos(60^\circ - \psi) - V_{ref}]T_2 + jT_2\sin(60^\circ - \psi) \tag{D.20b}$$

$$\overrightarrow{V}_{err,z}T_z = -V_{ref}T_z \tag{D.20c}$$

and it is plotted in Fig. D.13(b) for different values of the reference space vector angles. The harmonic flux vector is decomposed into d-axis and q-axis components, as shown in Fig. D.14. The resultant vector for an interleaving angle of 180° is also shown, and it is used to evaluate the ripple current/harmonic content in the line current.

The normalized rms value of the line current ripple over a half-carrier cycle [14] for different modulation indices for the proposed PWM scheme is plotted in Fig. D.15(c) as a function of the ψ. The variation in the rms value of the line current ripple for SVM and DPWM1 are also shown in Fig. D.15(a) and D.15(b), respectively. The variation of the total rms value of the line current ripple over the entire modulation range is also shown in Fig. D.16. DPWM1 demonstrates better line current quality over an entire modulation range. The total rms value of the line current ripple for the proposed PWM scheme closely matches that of the SVM. For SVM, the harmonic content for low modulation indices is slightly less compared to the proposed PWM scheme. On the other hand, the line current quality in the case of the proposed PWM scheme is marginally better than that of the SVM at higher modulation indices (M>0.9).

4.3 Semiconductor losses

Although one of the phase legs is clamped to dc-link for one third period of the fundamental cycle in the proposed scheme, an additional commutation is introduced in another leg as explained in the previous section. Thus, the switching losses are also evaluated in this paper. The switching loss function (SLF) [18] is used to compare the switching losses of the proposed PWM with other PWM schemes. The turn-on and turn-off characteristics of the semiconductor devices are assumed to be linear with respect to time. The contribution of the ripple current towards the switching losses is also neglected. Since the SLF normalizes the switching loss of the proposed method with respect to the switching loss of SVM, the relative error is small despite the simplified loss model [18] used. The SLF for the proposed method is given as

$$\text{SLF} = \begin{cases} 1 + (\frac{2-\sqrt{3}}{2})\cos\phi, & 0 \leqslant |\phi| < \frac{\pi}{6} \\ \cos\phi + \frac{1}{2}\sin\phi, & \frac{\pi}{6} \leqslant |\phi| < \frac{\pi}{3} \\ 2 - (\frac{2\sqrt{3}-1}{2})\sin\phi, & \frac{\pi}{3} \leqslant |\phi| \leqslant \frac{\pi}{2} \end{cases} \tag{D.21}$$

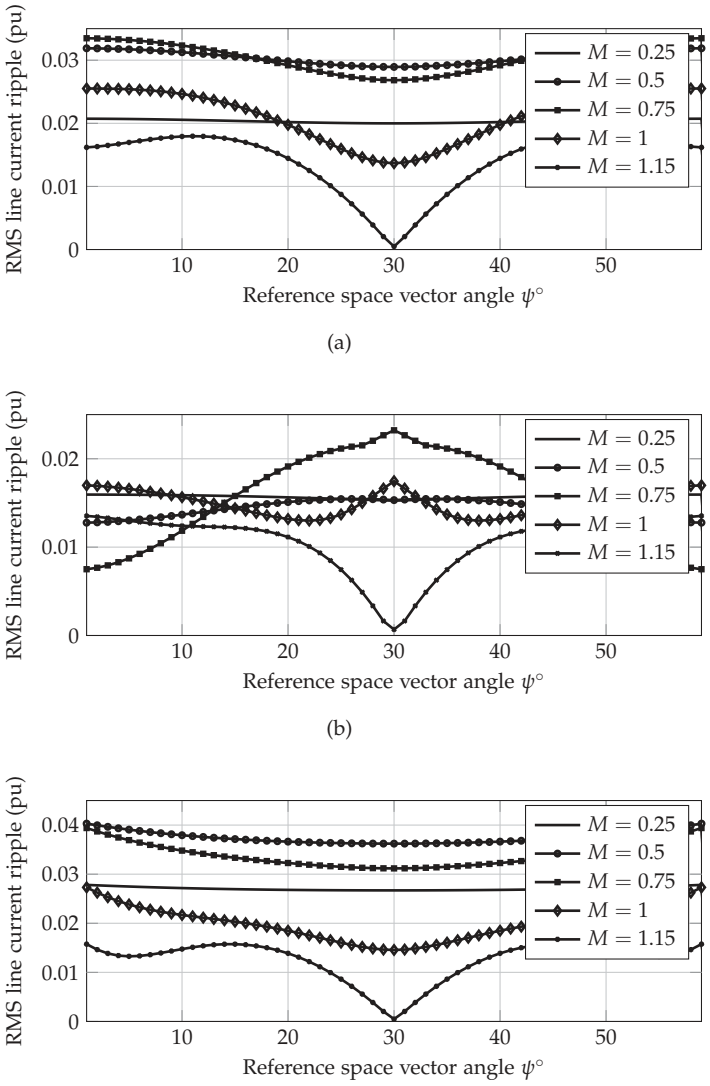


Fig. D.15: Space dependency of the rms value of the line current ripple (normalized) for different modulation indices. (a) SVM, (b) DPWM1, (c) Proposed scheme.

where ϕ is the displacement power factor angle. The SLFs for the proposed PWM scheme along with that of the SVM and DPWM1 are plotted in Fig. D.17. For the unity power factor applications, the switching losses are minimum if DPWM1 is used. For a displacement power factor angle higher than

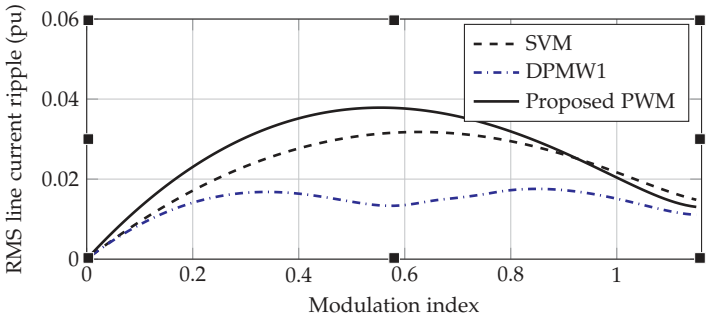


Fig. D.16: Total rms value of the line current ripple (normalized) as a function of modulation index.

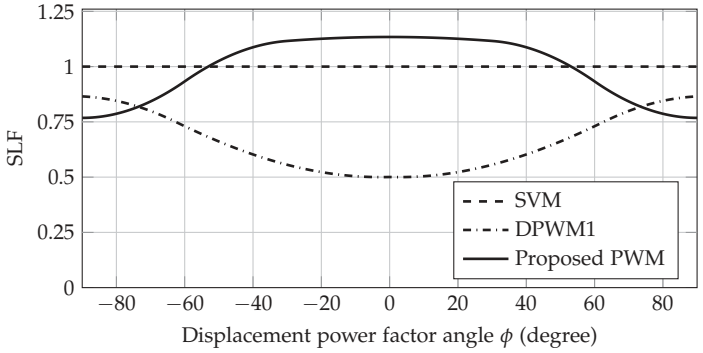


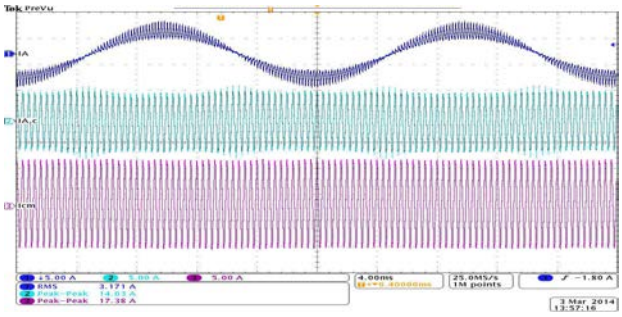
Fig. D.17: Comparison of the switching losses.

53°, the proposed method has lower switching losses compared to that of the SVM. However, for a displacement power factor angle in the vicinity of zero, the proposed method has high switching losses. For the reactive power compensation applications, the use of the proposed PWM scheme results in the lowest switching losses, as shown in Fig. D.17.

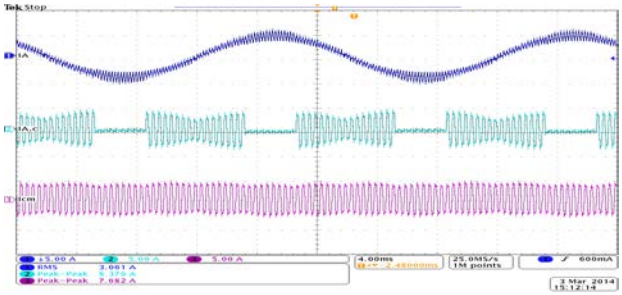
5 Experimental Results

The experiments have been performed using single-phase inductors, which act as both line filter inductor and the circulating current filter. This arrangement is used to simplify the measurement [39]. The results for $I_{A1} - I_{A2}$ are obtained, which is equal to $2 \times I_{A,c}$. As explained in Section II, the $I_{A,c}$ is proportional to the flux linkage in CI. Similarly, the sum of three-phase currents of each VSC is obtained. This current is equal to $3 \times I_{CM}$, and it is

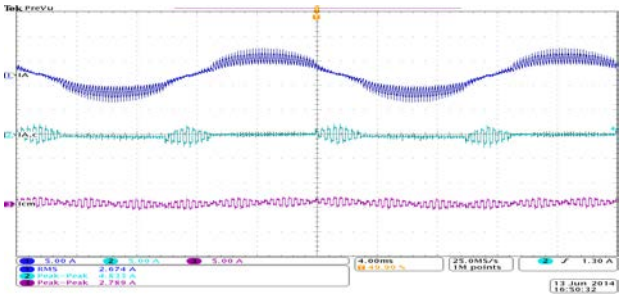
proportional to the CM flux linkage. The dc-link voltage of 600 V is used. The carrier frequency is taken to be 2.5 kHz and interleaving angle of 180°is chosen. The line filter inductor of 6.8 mH is used, and a resistive load is set to 20 Ω. The inductance in the circulating current path is $L_c = 2\times6.8$ mH.



(a)

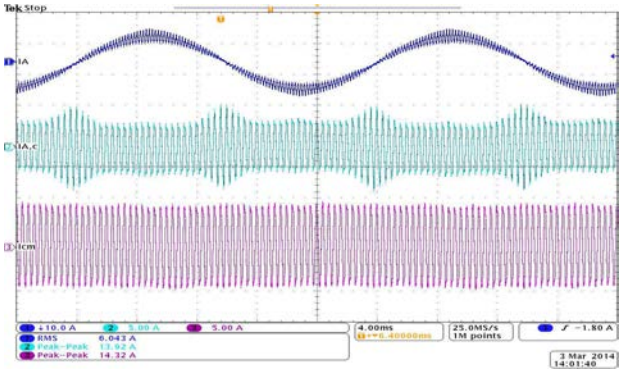


(b)

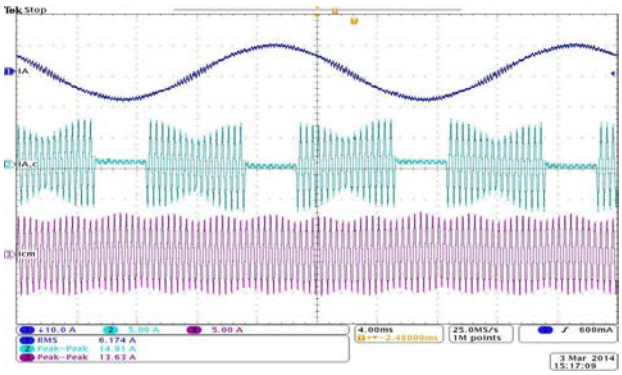


(c)

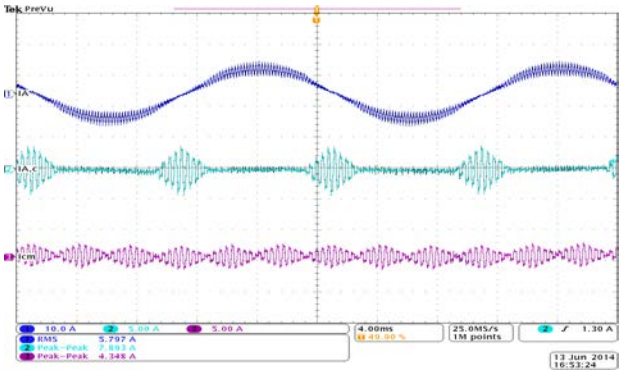
Fig. D.18: The performance comparison of the proposed PWM scheme. The modulation index M=0.3. Ch1: Phase A line current (5 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (5 A/div), Ch3: CM circulating current ($3 \times I_{CM}$) (5 A/div). (a) SVM, (b) DPWM1, (c) Proposed scheme.



(a)

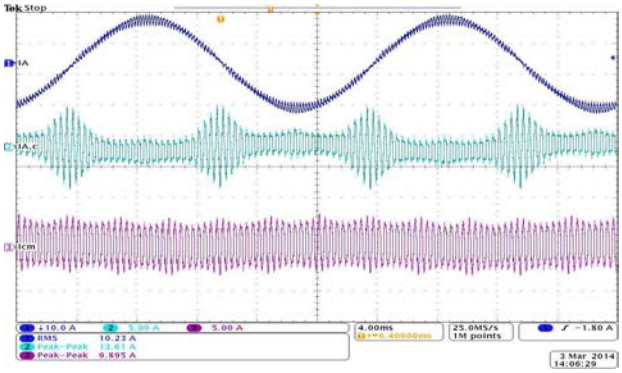


(b)

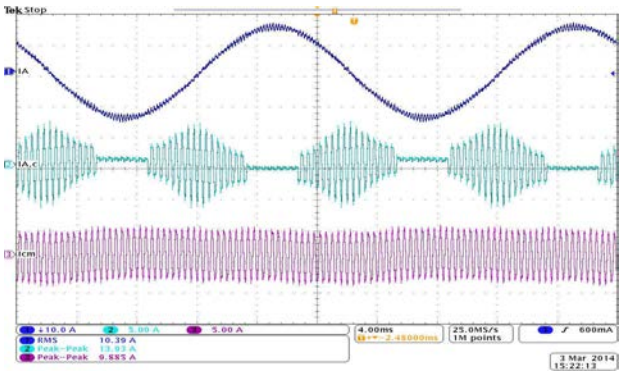


(c)

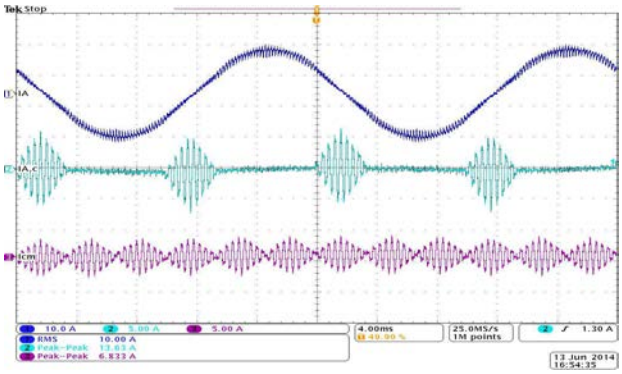
Fig. D.19: The performance comparison of the proposed PWM scheme. The modulation index M=0.6. Ch1: Phase A line current (10 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (5 A/div), Ch3: CM circulating current ($3 \times I_{CM}$) (5 A/div). (a) SVM, (b) DPWM1, (c) Proposed scheme.



(a)



(b)



(c)

Fig. D.20: The performance comparison of the proposed PWM scheme. The modulation index M=1. (a) SVM: Ch1: Phase A line current (10 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (5 A/div), Ch3: CM circulating current ($3 \times I_{CM}$) (5 A/div), (b) DPWM1, (c) Proposed scheme.

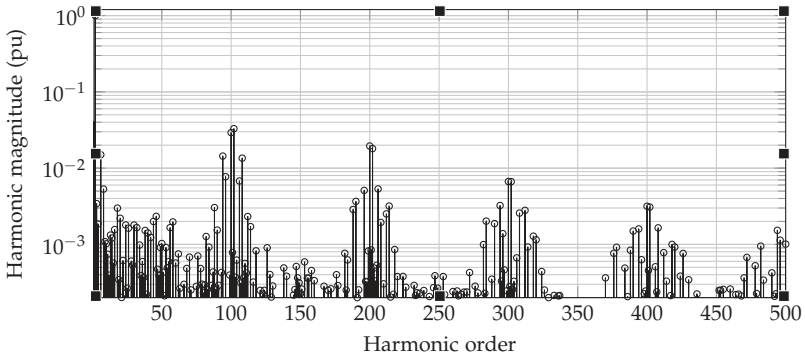


Fig. D.21: Proposed scheme: Experimental line current harmonic spectrum for a modulation index of 1. The harmonic magnitude is normalized to the magnitude of the fundamental component.

The line current of phase A (I_A), the circulating current of Phase A ($2\times I_{A,c}$), and the CM current ($3\times I_{CM}$) for modulation index of 0.3, 0.6, and 1 for SVM, DPWM1, and the proposed PWM scheme is depicted in Fig. D.18, D.19, and D.20, respectively. The experiments have been performed for the entire linear range of the modulation index and the results are given in Table D.6. The line current THD, the maximum value of the peak circulating current of phase A, and the maximum value of the peak CM circulating current of the proposed method are compared with that of the SVM and the DPWM1. The THD is calculated by performing discrete Fourier transform of the measured line current.

For the SVM, the maximum value of the peak circulating current of phase A remains almost constant over the entire modulation range. Since, the phase A circulating current is proportional to the flux linkage in the CI, it can be concluded that the maximum value of peak flux linkage in the CI over the full modulation range also remains constant. The use of SVM also results in more core losses in case of CI compared to the proposed PWM scheme, as the core is excited over the entire fundamental cycle. The I_{CM} is proportional to the flux linkage in the CM inductor and the experimental results of I_{CM} are also obtained. For the SVM, the maximum value of the peak CM circulating current decreases with the increase in the modulation index, which is in agreement with the analytical result presented in Section IV and illustrated in Fig. D.12. In the proposed scheme, the maximum value of the I_{CM} occurs at full modulation index, and it decreases with decrease in the modulation index. The maximum value of the peak CM current is 1.29 A at a modulation index of one in the proposed scheme, compared to 3.98 A at modulation index of 0.1 in case of the SVM and 2.39 A at a modulation index

Table D.6: Performance Comparison of the Proposed Method

M	Max. of $I_{A,c}$ (A)			Max. of $I_{CM}(A)$			Line current THD (%)		
	SVM	DPWM1	Proposed	SVM	DPWM1	Proposed	SVM	DPWM1	Proposed
0.1	3.55	0.79	0.59	3.98	0.52	0.32	24.15	26.14	28.62
0.2	3.52	1.46	0.85	3.12	0.93	0.33	22.30	19.29	25.31
0.3	3.50	2.09	1.15	2.89	1.28	0.46	19.60	15.21	22.06
0.4	3.55	2.68	1.42	2.71	1.62	0.52	17.63	11.56	19.68
0.5	3.50	3.23	1.76	2.57	1.94	0.61	15.86	7.95	16.49
0.6	3.48	3.72	2.03	2.38	2.27	0.73	13.85	6.03	14.38
0.7	3.48	3.63	2.28	2.20	2.39	0.82	11.88	5.92	12.38
0.8	3.42	3.55	2.53	2.03	2.10	0.91	10.03	5.85	10.26
0.9	3.40	3.50	2.81	1.85	1.86	0.98	8.25	5.28	8.09
1.0	3.40	3.48	3.03	1.64	1.64	1.14	6.37	4.49	6.17
1.1	3.36	3.48	3.19	1.46	1.49	1.27	4.71	3.66	4.47
1.15	3.38	3.39	3.37	1.39	1.28	1.29	4.05	3.31	3.87

of 0.7 for DPWM1. Thus, for applications demanding the operation over the full modulation range, the use of the proposed PWM scheme results in size reduction of CM inductor.

The undesirable effect of larger duration of T_z at lower modulation indices can be reduced by the same zero vector alignment in the proposed scheme. In case of CI, the core is excited only for the one third period of the fundamental cycle, as evident from the waveform of the $I_{A,c}$ in experimental results. If the design of CI is thermally limited, the reduced core losses result in more compact design. The harmonic analysis of the line current is shown in Fig. F.9. The major harmonic components are pushed close to the double of the switching frequency by the interleaving effect.

6 Conclusion

A PWM scheme to reduce the maximum value of the flux linkage and the core losses in the circulating current filter is presented in this paper. This PWM scheme uses the division of the active vectors within a half-carrier cycle to ensure simultaneous occurrence of the same zero vector in both of the VSCs. The effect of the proposed PWM scheme on the flux linkage and the core losses in the circulating current filter is analyzed. Both the maximum value of the flux linkage and the core losses are reduced substantially by the same zero vector alignment in the proposed PWM scheme. Thus, the size of the circulating current filter can be reduced. The switching losses are also analyzed for the proposed PWM scheme and compared with that of the SVM and 60°clamped DPWM. The proposed PWM scheme demonstrates superior efficiency for the reactive power compensation applications, as it is evident from the core losses and switching losses comparisons presented in this paper. However, for the applications, where the displacement power factor angle is in the vicinity of zero, the use of proposed method results in high switching losses. The line current ripple for the proposed scheme is also analyzed, which shows that the THD of the line current closely matches that of the SVM. The line current quality is superior in the case of the DPWM1, however the improvement is marginal at the higher modulation indices. The PWM scheme and the analysis presented in this paper are also supported by the experimental results.

References

[1] M. Baumann and J. Kolar, “Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link current balancing,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042–3053, 2007.

[2] Z. Xu, R. Li, H. Zhu, D. Xu, and C. Zhang, "Control of parallel multiple converters for direct-drive permanent-magnet wind power generation systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1259–1270, March 2012.

[3] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[4] A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, 2011.

[5] G. Narayanan, V. T. Ranganathan, D. Zhao, H. Krishnamurthy, and R. Ayyanar, "Space vector based hybrid PWM techniques for reduced current ripple," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1614–1627, 2008.

[6] D. Casadei, G. Serra, A. Tani, and L. Zarri, "Theoretical and experimental analysis for the rms current ripple minimization in induction motor drives controlled by svm technique," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1056–1065, Oct 2004.

[7] M. Meco-Gutierrez, F. Perez-Hidalgo, F. Vargas-Merino, and J. R. Heredia-Larrubia, "A new PWM technique frequency regulated carrier for induction motors supply," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1750–1754, Oct 2006.

[8] K. Taniguchi, M. Inoue, Y. Takeda, and S. Morimoto, "A PWM strategy for reducing torque-ripple in inverter-fed induction motor," *IEEE Trans. Ind. Appl.*, vol. 30, no. 1, pp. 71–77, Jan 1994.

[9] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[10] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[11] L. Asimmoaei, E. Aeloiza, J. Kim, P. Enjeti, F. Blaabjerg, L. Moran, and S. Sul, "An interleaved active power filter with reduced size of passive components," in *Proc. Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, 2006, pp. 1–7.

[12] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase

Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[13] T. Bhavsar and G. Narayanan, "Harmonic analysis of advanced bus-clamping PWM techniques," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2347–2352, 2009.

[14] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[15] M. Abusara and S. Sharkh, "Design and control of a grid-connected interleaved inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 748–764, Feb 2013.

[16] K. Xing, F. Lee, D. Borojevic, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, 1999.

[17] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[18] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based PWM-vsi drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan 1999.

[19] J. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a pwm converter system," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063–1075, 1991.

[20] G. Narayanan and V. T. Ranganathan, "Analytical evaluation of harmonic distortion in PWM AC drives using the notion of stator flux ripple," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 466–474, 2005.

[21] G. Narayanan, H. Krishnamurthy, D. Zhao, and R. Ayyanar, "Advanced bus-clamping PWM techniquesbased on space vector approach," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 974–984, 2006.

[22] H. Akagi, A. Nabae, and S. Atoh, "Control strategy of active power filters using multiple voltage-source PWM converters," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 3, pp. 460–465, 1986.

[23] R. Hausmann and I. Barbi, "Three-phase multilevel bidirectional DC-AC converter using three-phase coupled inductors," in *Proc. IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, Sept 2009, pp. 2160–2167.

[24] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[25] B. Cougo, T. Meynard, and G. Gateau, "Parallel Three-Phase Inverters: Optimal PWM Method for Flux Reduction in Intercell Transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[26] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, 2012.

[27] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[28] J. Ewanchuk and J. Salmon, "Three-limb coupled inductor operation for paralleled multi-level three-phase voltage sourced inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1979–1988, 2013.

[29] . Zhang, Di, F. Wang, R. Burgos, and D. Boroyevich, "Common-mode circulating current control of paralleled interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3925–3935, Dec 2011.

[30] D. Zhang, F. Wang, R. Burgos, and D. Boroyvich, "Total flux minimization control for integrated inter-phase inductors in paralleled, interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1679–1688, April 2012.

[31] F. Luo, S. Wang, F. Wang, D. Boroyevich, N. Gazel, Y. Kang, and A. Baisden, "Analysis of cm volt-second influence on cm inductor saturation and design for input emi filters in three-phase dc-fed motor drive systems," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1905–1914, 2010.

[32] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, May 1997.

[33] A. Hava, R. Kerkman, and T. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, 1998.

[34] H. Krishnamurthy, G. Narayanan, R. Ayyanar, and V. T. Ranganathan, "Design of space vector-based hybrid PWM techniques for reduced current ripple," in *Proc. Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03.*, vol. 1, 2003, pp. 583–588.

[35] A. C. Binojkumar, J. Prasad, and G. Narayanan, "Experimental investigation on the effect of advanced bus-clamping pulsewidth modulation on motor acoustic noise," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 433–439, Feb 2013.

[36] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, 2002, pp. 36–41.

[37] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Thirty-Sixth IAS Annual Meeting, IEEE Industry Applications Conference.*, vol. 4, 2001, pp. 2203–2210 vol.4.

[38] A. V. d. Bossche and V. C. Valchev, *Inductors and Transformers for Power Electronics*. Boca Raton, FL: CRC Press, 2004.

[39] B. Cougo, T. Meynard, and G. Gateau, "Parallel three-phase inverters: Optimal pwm method for flux reduction in intercell transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug 2011.

Paper E

Flux Balancing Scheme for PD Modulated Three Parallel Interleaved VSCs with Coupled Inductor

Ghanshyamsinh Gohil,
Lorand Bede,Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been submitted for the publication in the
IEEE Transactions on Power Electronics

The layout has been revised.

Abstract

The Two-Level Voltage Source Converters (2L-VSCs) are often connected in parallel to realize a high current rating in MW-level converter system. In such systems, multi-level waveform for the resultant voltages can be obtained by employing sequential switching. The harmonic performance of the multi-level voltage waveform can be further improved by using the Phase-Disposition carrier PWM (PD PWM). However, the conventional PD PWM implementation can not be used for the modulation of the parallel 2L-VSCs, as it causes dc flux injection and may saturate the Coupled Inductor (CI), which is needed to suppress the circulating current that flows between the parallel VSCs. A simple scheme to realize the PD PWM for three parallel 2L-VSCs is presented in this paper. The proposed implementation uses only a single carrier signal and can easily be implemented using a digital signal processor. The operation of the parallel VSCs with the CI, under the PD PWM is briefly discussed and the associated dc flux injection problem is investigated. The CI saturation issue during the band transition under the PD PWM scheme is also explored and the band strategy to avoid this problem is presented. In addition, the proposed band transition strategy also maintains a volt-sec balance to synthesize the reference space voltage vector during the band transition. As a result, a smooth transition from one modulation band to the other is ensured without causing disturbances in the line-to-line voltage. The switching losses and the harmonic performance of the proposed implementation are also compared with the commonly used Phase-Shifted carrier Pulse Width Modulation (PS PWM). The implementation issues are discussed and the experimental results are also presented.

1 Introduction

The three-phase Two-Level Voltage Source Converters (2L-VSC) are often connected in parallel to increase the current handling capability in MW-level converter system. The typical Silicon Insulated Gate Bipolar Transistors (Si-IGBT) that are used in such applications suffer from excessive losses if the switching frequency is increased beyond a few kHz. As a result, large passive filter components are generally employed to comply with the stringent power quality requirements, which lead to the increased cost, size and losses. Therefore the efforts are being made to reduce both the size of filter components and the switching frequency. One of the ways to achieve this contradictory requirements is to employ a multi-level VSC.

For the parallel connected 2L-VSCs, multi-level voltage waveforms can be achieved by a sequential switching of the parallel VSC legs. A four-level converter can be realized by the sequential switching of the three parallel 2L-VSCs, shown in Fig. E.1. One of the ways to achieve the sequential switching is to use the phase-shifted carrier signals [1–7]. Each of the 2L-VSC is inde-

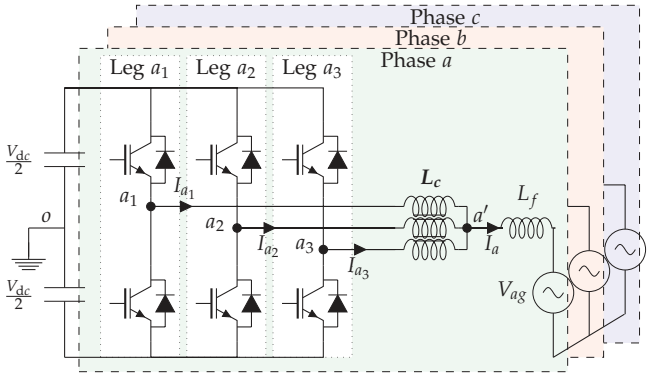


Fig. E.1: Four-level converter, realized using three parallel two-level voltage source converters. A Coupled Inductor (CI) is used for suppressing the circulating current.

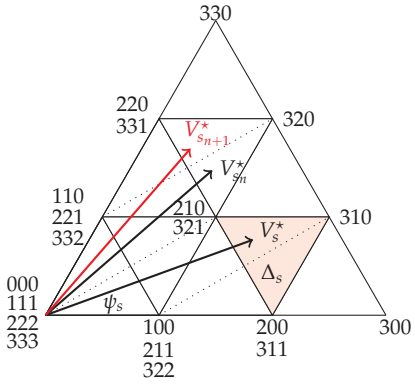


Fig. E.2: Projection of the reference space voltage vector $V_s^\star = 3\sqrt{3}/8\angle 20^\circ$ in the first sextant of the space vector diagram of the four-level converter.

pendently modulated to synthesize the reference space voltage vector having a magnitude $|V_s^\star|$ (normalized with respect to the dc-link voltage V_{dc}) and angle ψ_s (refer Fig. E.2). This scheme is commonly referred to as the Phase-Shifted Pulse Width Modulation (PS PWM) scheme.

The switched output voltages of phase a of each of the 2L-VSCs under the PS PWM (for $|V_s^\star| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$) are shown in Fig. E.3(a). The carrier signals of the three VSCs are symmetrical phase-shifted with an interleaving angle of 120°. The resultant switched output voltage is given as

$$V_{x'o} = \frac{1}{3}\sum_{k=1}^{3} V_{x_k o} \tag{E.1}$$

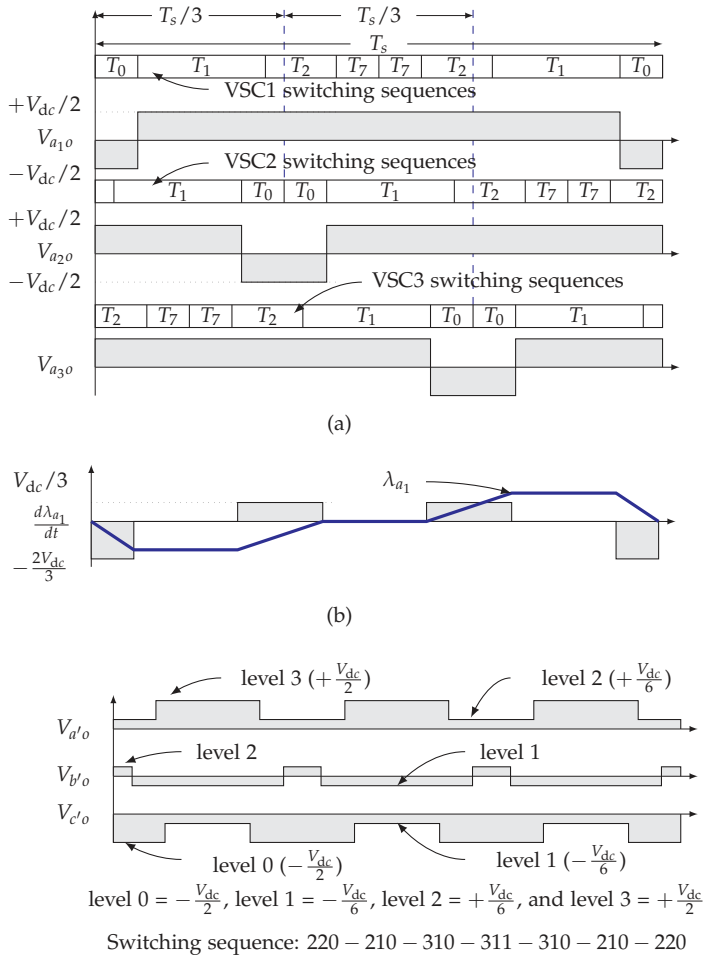


Fig. E.3: Switched output voltages for $|V_s^\star| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$. Each of the VSCs are modulated using two-level space vector modulation. (a) Switched output voltage of phase a of all three VSCs, (b) Flux linking with the coil a_1 of the CI, (c) Resultant switched output voltages of all three phases.

where subscript x represent phases a, b, and c and $V_{x_k o}$ is the switched output voltage of the phase x of kth VSC, where $k = \{1, 2, 3\}$. The resultant switched output voltages of all the phases are also shown in Fig. E.3(c), which demonstrate four-level voltage waveforms. The switching sequences $220 - 210 - 310 - 311 - 310 - 210 - 220$ are employed, where each of the digit represents the voltage level of the resultant output voltage of the phase a, b

and c, respectively (e.g. 210 represents that voltage levels of phase a, phase b, and phase c are level 2, level 1, and level 0, respectively).

As the three parallel 2L-VSC gives four-level voltage output, the $V_s^\star$ can be projected on the space vector diagram of the four-level converter, as shown in Fig. E.2, where the reference space voltage vector is located in the triangle Δ_s. The harmonic profile of the synthesized voltage can be improved by using the Nearest Three Vector (NTV) [8–10], which are located on the vertices of the triangle Δ_s (210-310-311). However, when the phase-shifted carrier signals are used, an additional voltage vector 220 is also employed, as shown in Fig. E.3(c). Therefore, it is evident that the PS PWM is not an optimal solution for the modulation of the parallel VSCs.

The optimal PWM scheme to improve the harmonic performance of the parallel 2L-VSCs under the PS PWM is presented in [3]. The effect of the combination of the several switching sequences and the phase-shift between the carrier signals on the harmonic quality is investigated and optimal combination has been identified for all possible values of the $|V_s^\star|$ and ψ_s. This information is then used to select the optimal combination of the switching sequences and the phase-shift during each sampling interval. Several combinations of the switching sequences and the phase-shift are used in one fundamental cycle of the reference space voltage vector. This would substantially increase the complexity and make it mere difficult to implement. Moreover, the CI could saturate during the transition from one combination to another.

For the multi-level converters, the use of the Phase Disposition carrier modulation (PD PWM) results in the lowest harmonic distortion [8, 11, 12] amongst other carrier modulation schemes. However, a conventional PD modulator can not be used for the parallel VSCs, as switching of all the parallel legs is not uniform and it could lead to the saturation of the CI. This issue is addressed in this paper. Moreover, a dc flux is injected during the transition from one modulation band to the other. The effect of the PD PWM on the operation of the CI is investigated and the band transition strategy to avoid the saturation of the CI is designed. A simple implementation using a Digital Signal Processor (DSP) is also proposed.

This paper is organized as follows. Section II describes the problems related to the use of the PD PWM in the three parallel interleaved VSCs with the CI. The proposed scheme is presented in Section III and a implementation using the DSP is discussed in Section IV. A comparative evaluation and performance verification through the experimental studies are included in Section V.

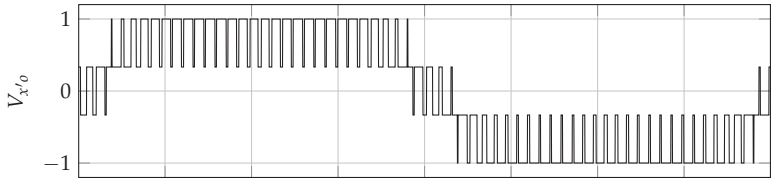


Fig. E.4: Resultant switched output voltage of three parallel interleaved two-level voltage source converters. The voltage is normalized to half of the dc-link voltage $V_{dc}/2$.

2 PD Modulation of the Parallel Interleaved VSCs and Associated Issues

In this section, the operating principle of the three parallel interleaved VSCs with the CI is briefly discussed and the issues related to the PD PWM of this converter is examined.

2.1 Operation of the Three Parallel Interleaved VSCs

Three parallel 2L-VSCs with a common dc-link is shown in Fig. E.1. The four level resultant switched output voltage waveforms $V_{x'k}$ can be achieved by sequential switching of these VSCs, as shown in Fig. E.4. The switched output voltages of the parallel legs of a given phase are shifted with respect to each other due to the sequential switching (cf. Fig. E.3(a)) and would drive large circulating current between the parallel legs. The flow of this unwanted circulating current increases losses and demands unnecessary oversizing of the components present in the circulating current path. Therefore, the circulating current should be suppressed to some acceptable value to realize the full potential of the parallel interleaved VSCs.

The circulating current suppression can be achieved by introducing impedance in the circulating current path. The use of the CI for this purpose is commonly reported in the literature [1, 13–15]. The CI provides magnetic coupling between the parallel interleaved legs of the corresponding phases and it offers high inductance to the circulating current component.

The magnetic structure of the CI is shown in Fig. E.5(a). It consists of three magnetic limbs around which the coils are placed. All the coils are wound in the same direction and the limbs are magnetically coupled to each other using the top and the bottom yokes. The start terminal of the three coils of the CI belonging to the phase x are connected to the corresponding output terminals of the VSC legs, whereas the other terminals are connected together to form the common point (x'), as shown in Fig. E.5(a), where the subscript x represents one of the phase in three phase system $x = \{a, b, c\}$.

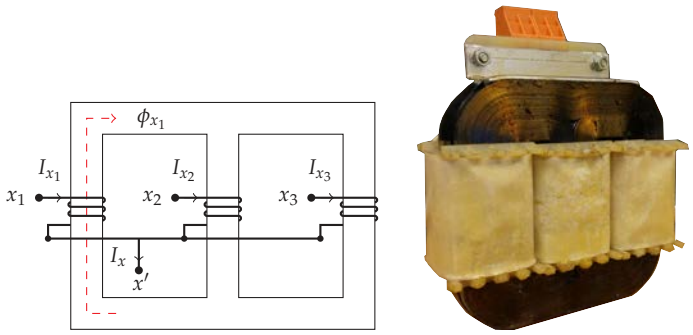


Fig. E.5: (a) Magnetic structure of the coupled inductor that is used to suppress the circulating current between the three parallel interleaved voltage source converters, (b) Photo of the realized coupled inductor for one of the phase.

The resultant line current of a particular phase is the sum of all leg currents of that phase and it is given as

$$I_x = \sum_{k=1}^{3} I_{x_k} \tag{E.2}$$

For the parallel interleaved VSCs, the leg current I_{x_k} can be split into two components:

1. Component contributing to the resultant line current $I_{x_k,l}$
2. The circulating current $I_{x_k,c}$

and it can be represented as

$$I_{x_k} = I_{x_k,l} + I_{x_k,c} \tag{E.3}$$

The circulating current components $I_{x_k,c}$ do not contribute to the resultant line current. Therefore, (H.9) can be re-written as

$$I_x = \sum_{k=1}^{3} I_{x_k,l} \tag{E.4}$$

Assuming an equal line current sharing between the parallel VSCs, the common component of the leg current is obtained as $I_{x_k,l} = I_x/3$. Considering equal current sharing and neglecting the leakage flux, the flux that links with kth coil can be given as

$$\phi_{x_k}(t) = \frac{1}{N}\Big(\frac{2}{3}\int V_{x_k o}\, dt - \frac{1}{3}\sum_{\substack{j=1 \\ j\neq k}}^{3}\int V_{x_j o}\, dt\Big) \tag{E.5}$$

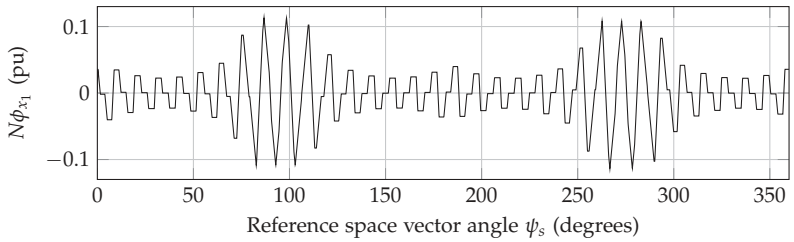


Fig. E.6: Flux linkage in a fundamental frequency cycle when the phase-shifted carrier modulation is used to synthesize $|V_s^\star| = 3\sqrt{3}/8$. The flux linkage is normalized with respect to $V_{\rm dc}T_s$.

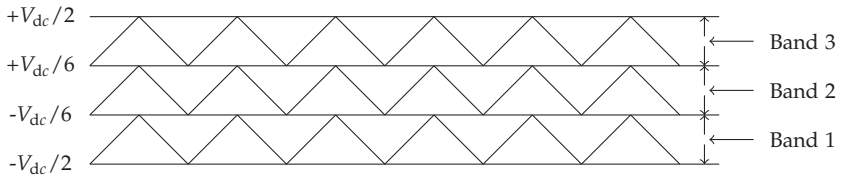


Fig. E.7: Arrangement of the carrier signals in the conventional phase disposition modulation scheme [8].

where N is the number of turns in each of the coils. The maximum value of the flux that links with the coil is found to be

$$N\phi_{a_{k,max}} = \frac{V_{\rm dc}}{9f_c} \tag{E.6}$$

The flux linking with the coil x_1 of the CI under PS PWM is shown in Fig. E.3(b). The CI is subjected to the switching frequency flux excitation and in order to prevent the oversizing (or to avoid the saturation) of the CI, the operation of the CI under flux balance condition, i.e. with zero dc voltage component (which would be translated into zero dc flux component) must be ensured. The natural flux balancing is obtained when PS PWM is used to modulate the parallel VSCs [6]. The associated flux linkage in half of the fundamental cycle is shown in Fig. H.11, which demonstrates that the dc flux component is absent. However, this is not the case when PD PWM is employed and the related issues are discussed in the following subsection.

2.2 Coupled Inductor Saturation Under PD PWM

The PD PWM of four-level converter is realized by arranging three carrier signals, which are in phase and level-shifted in order to occupy the linear modulation range, as shown in Fig. E.7. If the conventional PD PWM implemen-

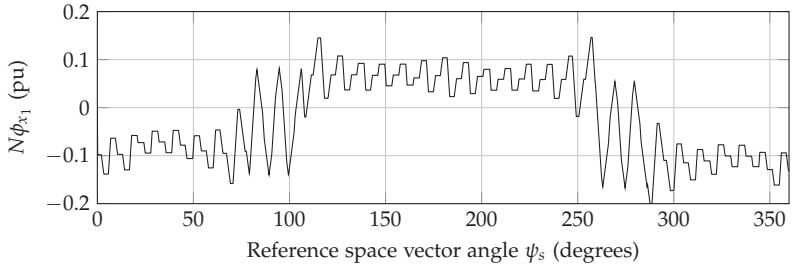


Fig. E.8: Flux linkage in a fundamental frequency cycle when the PD PWM with an even commutation distribution proposed in [16] is used to synthesize $|V_s^\star| = 3\sqrt{3}/8$. The flux linkage is normalized with respect to $V_{\text{dc}}T_s$.

tation is applied to parallel VSCs, each carrier would be responsible for the switching of one of the leg (i.e. carrier that spans in band k would be responsible for the commutation of the switches in leg k, shown in Fig. E.1). This would introduce a dc flux injection and would saturate the CI. The similar problem has been observed in the Flying Capacitor (FC) multi-level converter, where the conventional PD PWM implementation would lead to a capacitor voltage unbalance. Several strategies have been proposed to ensure natural voltage balancing of PD modulated FC multi-level converter [**?**, 16–18]. Even though these schemes can ensure even commutation distribution between the parallel VSCs, dc flux injection still happens during the band transition, as shown in Fig. E.8. Therefore, these schemes can not be readily applicable to the parallel VSCs.

The enhanced modulator for the parallel interleaved 2L-VSCs is proposed in [19]. It uses two sets of the evenly phase-shifted carrier signals that are dynamically allocated using multiplexer, which makes it difficult to implement. Moreover, this implementation is equivalent to the PD PWM, CI saturation during the band transition could still happen. The PD carrier modulation scheme for the two parallel VSCs is presented in [20]. It uses a state machine to select the switching states. However, the complexity in this case increases with the increase in the number of parallel VSCs. The strategy to avoid the CI saturation during the transition from the positive value of the command reference signal to the negative value of the command reference signal and vice-versa has been proposed for the two parallel VSCs. However, it does not ensure volt-sec balance to synthesize $V_s^\star$ during the band transition and introduces a disturbance in the line-to-line voltage of the three-phase system, which is highly undesirable.

A PWM scheme to ensure an even commutation distribution between the parallel VSCs is presented in this paper. The strategy ensures flux balancing in the CI and the volt-sec balance to synthesize the reference voltage space

vector $V_s^\star$, even during the band transition.

3 Modulation Algorithm

In the proposed implementation, a single carrier is used with the frequency of $f_c = 3 \times f_{sw}$, where f_{sw} is the switching frequency of each of the VSCs. The amplitude of the carrier signal is taken to be $+V_{\mathrm{dc}}/2$ (which occupies the region from 0 to $+V_{\mathrm{dc}}/2$). The appropriate processing and the scaling of the command reference signals ($V_a^\star$, $V_b^\star$, $V_c^\star$) is first performed to accommodate the modified reference signals in the carrier region spanning from 0 to $+V_{\mathrm{dc}}/2$. The modified reference signals can be achieved as

$$V_x^{\star\star} = \frac{3}{2}\mathrm{mod}\Big((V_x^\star + \frac{V_{\mathrm{dc}}}{2}), \frac{V_{\mathrm{dc}}}{3}\Big) \tag{E.7}$$

where mod is a function and it returns the remainder after a division. The band in which the reference signal is located can be obtained using the ceiling function as

$$B_x = \lceil \frac{V_x^\star + \frac{V_{\mathrm{dc}}}{2}}{\frac{V_{\mathrm{dc}}}{3}} \rceil \tag{E.8}$$

In a given sampling interval, the resultant output voltage should switch between the level $(B_x - 1)$ and level B_x.

3.1 Modulation Under Steady-state Conditions

The steady-state condition refers to the case when the band in which the reference signal is located is the same in the current (nth) sampling interval and previous $(n-1)$th sampling interval. The parallel VSCs are modulated to achieve the $(B_x - 1)$ and B_x voltage levels by taking into account the information of the band in which the command reference signal is located.

3.1.1 Modulation in Band 1

The carrier comparison scheme and the associated switched output voltages of all three parallel VSCs are shown in Fig. E.9. The VSCs are switched in a round-robin manner. During each sampling interval, the VSCs are categorized as:

1. Active VSC: which is being switched in a given sampling interval.
2. Passive VSCs: remaining two VSCs, which are latched to the previous switching state.

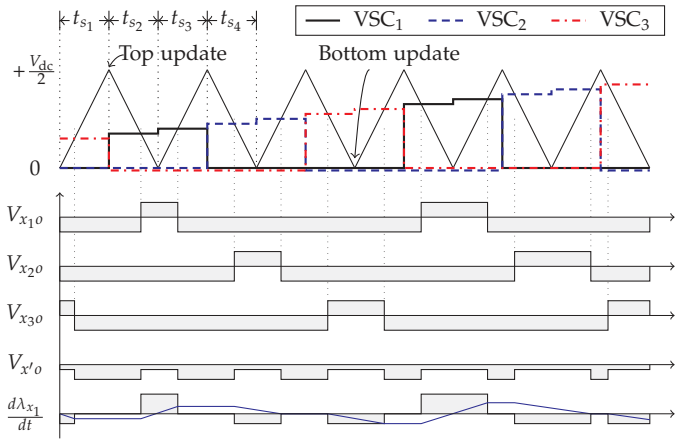


Fig. E.9: Phase disposition modulation using the carrier comparison and the associated switched voltages waveforms when the command reference signal lies in Band 1.

For example, in the sampling interval t_{s_1}, VSC$_3$ is an active VSC and VSC$_1$ and VSC$_2$ are the passive VSCs. Similarly in the interval t_{s_2} and t_{s_3}, VSC$_1$ is an active VSC and VSC$_2$ and VSC$_3$ are termed as the passive VSCs. The state of each of the VSCs remain active for two consecutive sampling intervals. The transition from the active state to the passive state for each of the VSCs happens at the top update, as shown in Fig. E.9. The modified reference $V_x^{\star\star}$ is used for the carrier comparison of the active VSCs, whereas the zero value is used for the passive VSCs.

The resultant switched output voltage $V_{x'o}$ has a transition from voltage level 0 to voltage level 1 and vice-versa during each switch transition, as shown in Fig. E.9. Even commutation distribution is ensured with each of the VSCs switching sequentially. Therefore, the dc flux component in the CI during the steady-state is avoided, which is evident from the flux linkage waveform of the coil x_1 (λ_{x_1}), shown in Fig. E.9.

3.1.2 Modulation in Band 2

The carrier comparison of the parallel VSCs in band 2 and the associated switched output voltages are shown in Fig. E.10. Each of the VSCs remains in an active state for only one sampling interval, followed by passive state in next two consecutive sampling intervals. In a given sampling interval, the modified reference $V_x^{\star\star}$ is used for the carrier comparison of the active VSCs, whereas zero and $+V_{dc}/2$ are used for the carrier comparison of the passive VSCs, as shown in Fig. E.10. For example, in the sampling interval t_{s_1}, $V_x^{\star\star}$ is used for the carrier comparison for VSC$_2$ (active VSC), whereas zero and

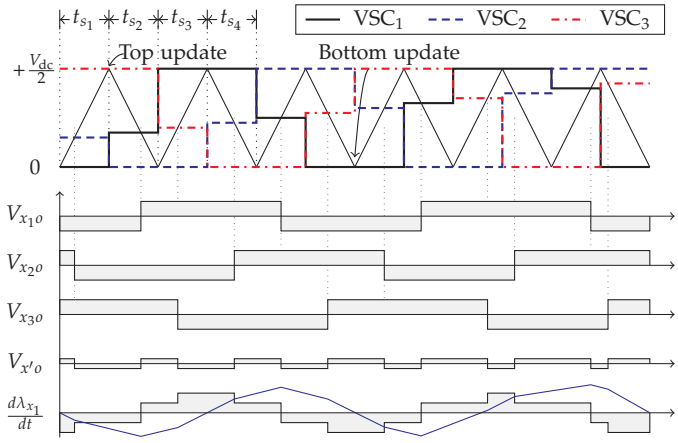


Fig. E.10: Carrier comparison and the associated switched voltages waveforms when the command reference signal is located in Band 2.

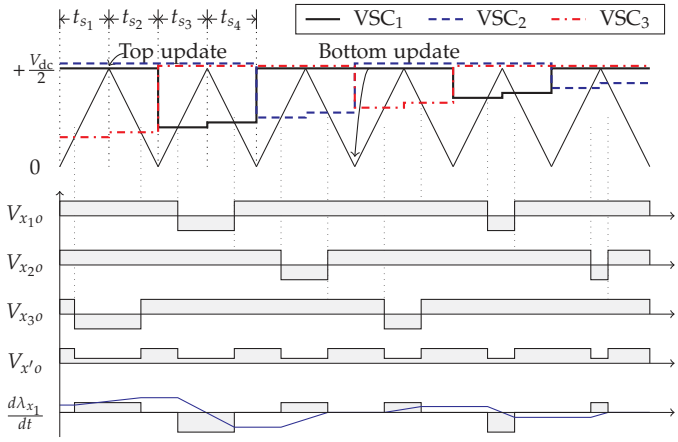


Fig. E.11: Carrier comparison and the associated switched voltages waveforms when the command reference signal is located in band 3.

$+V_{dc}/2$ are used for the VSC$_1$ and VSC$_3$, respectively. During the top update, the state of the passive VSC with the zero compare value is changed to active state (and vice-versa), whereas the state of the passive VSC with the $+V_{dc}/2$ compare value is changed to the active state (and vice-versa) at the bottom update.

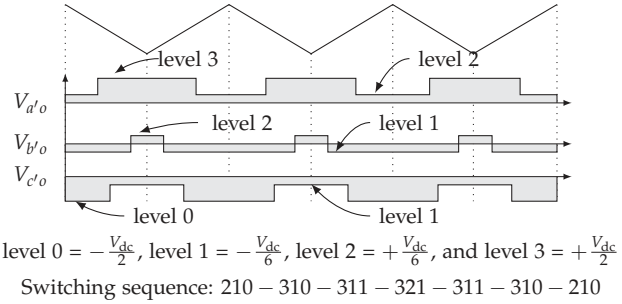


Fig. E.12: Resultant switched output voltages for $|V_s^\star| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$ with the proposed implementation.

3.1.3 Modulation in Band 3

The operation in band 3 is similar to the operation in band 1. The only difference is the values assigned to the passive VSCs for the carrier comparison is $+V_{dc}/2$ (whereas it was zero in band 1) and the transition from active state to passive state for each of the VSCs happens at the bottom update, as shown in Fig. E.11.

The resultant switched output voltages of all the three phases when $V_s^\star = 3\sqrt{3}/8\angle 20^\circ$ is synthesized using the proposed implementation is shown in Fig. E.12. The switching sequences 210-310-311-321 are used, which are the nearest three vectors, as shown in Fig. E.2. As a result, compared to PS PWM, significant improvement in the harmonic quality of the voltage waveforms can be achieved. However, dc flux component is injected during the band transition in the proposed implementation, as shown in Fig. E.13. The case in which the command reference signal $V_x^\star$ has gone through a transition from the band 2 to the band 3 is illustrated. The dc voltage is injected during the first sampling interval following the band transition. This could lead to the saturation or unnecessary oversizing of the CI. The flux balancing scheme to avoid this problem is discussed in the following subsection.

3.2 Flux Balancing During Band Transition

In every fundamental cycle, four band transition instances are encountered (barring the operation with the low modulation index when the reference signal only lies in the band 2):

1. Transition from band 1 to band 2 and vice-versa.

2. Transition from band 2 to band 3 and vice-versa.

The flux balancing scheme is illustrated for the case in which the transition

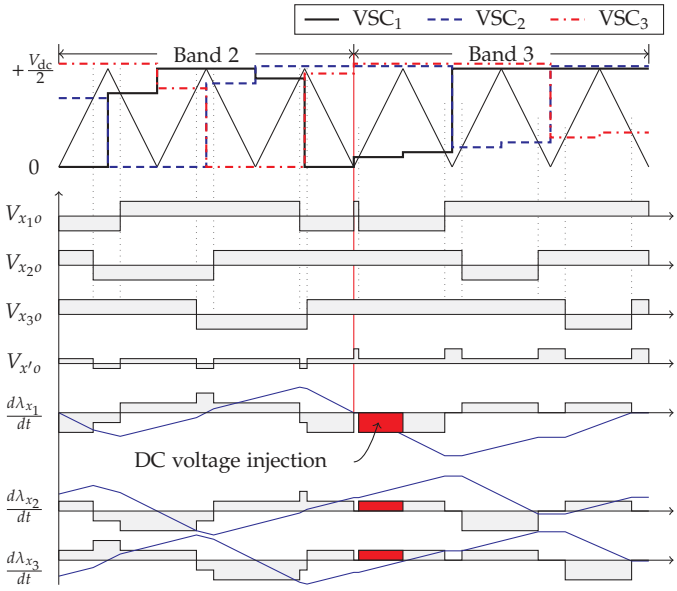


Fig. E.13: DC voltage injection during the transition from the band 2 to the band 3.

happens from band 2 to band 3. However, the same strategy can be applied to the remaining cases as well. As shown in Fig. E.13, the dc voltage is injected during the first sampling interval, followed by the band transition. The flux balancing can be achieved by ensuring a zero dc voltage injection during that sampling interval. In addition, the volt-sec balance to synthesize $V_s^\star$ should also be maintained.

The switching sequences that should be used to synthesize $V_s^\star$ are different for the sampling interval followed by the Top Update (TU) and the sampling interval followed by the Bottom Update (BU), as shown in Fig. E.12. Therefore the band transition strategy also takes into account the TU and BU. For example, in order to synthesize $|V_s^\star| = 3\sqrt{3}/8$ and $\psi_s = 20^\circ$, the voltage level of the phase a should be 2 at the top update (to realize 210-310-311-321) and it should be 3 at the bottom update (to realize 321-311-310-210) (refer Fig. E.12 and Fig. E.13).

3.2.1 Band Transition at Bottom Update

The instant when the transition from the band 2 to the band 3 occurs for the phase b is shown in Fig. E.14, where $V_{s_n}^\star$ represents the sampled reference space vector just before the transition and $V_{s_{n+1}}^\star$ is the sampled reference space vector for the next sampling interval, which occurs just after the transition (the reference space vectors are shown in Fig. E.2). The pivot vector

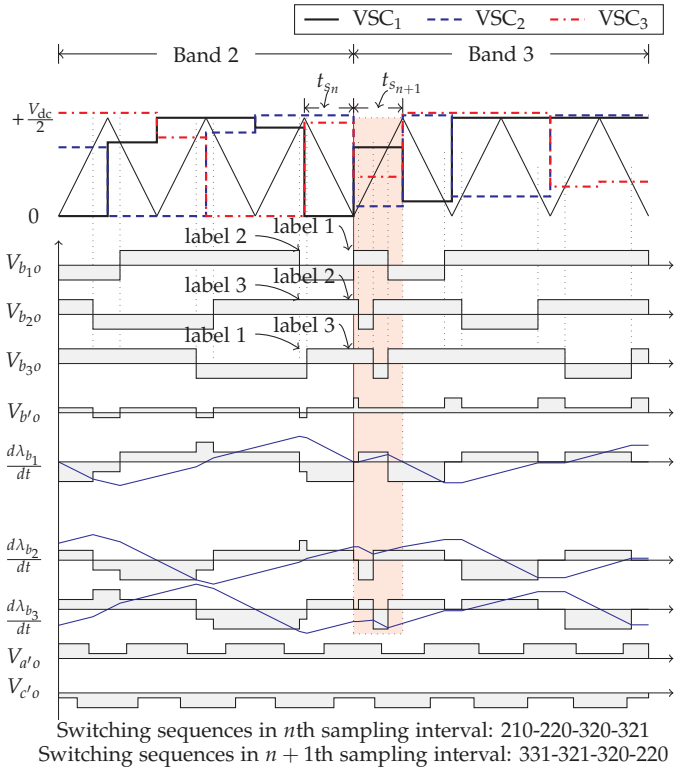


Fig. E.14: Flux balancing strategy for the band transition that occurs at the bottom update.

Table E.1: Transition from band 2 to band 3 at bottom update (BU): values used for the carrier comparison in the $_{n+1}$th sampling interval.

Leg	Leg b_1	Leg b_2		Leg b_3	
	OFF	ON	OFF	ON	OFF
Values	$\frac{V_{dc}+V_b^{\star\star}}{3}$	$\frac{V_{dc}+4V_b^{\star\star}}{6}$	$V_b^{\star\star}$	$\frac{V_{dc}+4V_b^{\star\star}}{6}$	$\frac{V_{dc}+V_b^{\star\star}}{3}$

changes from 210/321 to 220/331 during band transition. So if the transition occurs at the bottom update, the switching sequence in the $n+1$th sampling interval (first sampling interval after the transition) should be 331-321-320-220.

The strategy for the band transition occurring at the bottom update is shown in Fig. E.14. The dc flux injection in the $(n+1)$th sampling interval is avoided by introducing an extra commutation in two legs (leg b_2 and leg b_3 as shown in Fig. E.14). The turn-off interval of all legs is ensured to be the same

Table E.2: Transition from band 2 to band 3 at top update (TU): values used for the carrier comparison in the $_{n+1}$st sampling interval.

Leg	Leg b_1	Leg b_2		Leg b_3	
	ON	ON	OFF	ON	OFF
Values	$\frac{V_{\rm dc}+V_b^{\star\star}}{3}$	$V_b^{\star\star}$	$\frac{V_{\rm dc}+4V_b^{\star\star}}{6}$	$\frac{V_{\rm dc}+4V_b^{\star\star}}{6}$	$\frac{V_{\rm dc}+V_b^{\star\star}}{3}$

and it is taken to be $(\frac{V_{\rm dc}}{2} - V_x^{\star\star})/6f_c$. The values for the carrier comparison and the switching logic are given in Table E.1. This ensures that the volt-sec balance is maintained while synthesizing the reference space vector $V_s^{\star}$.

All three legs are turned on at the start of the sampling interval for the duration of $V_b^{\star\star}/(V_{\rm dc}f_c)$ to achieve the voltage level 3, whereas for the remaining duration of $(V_{\rm dc} - 2V_b^{\star\star})/2V_b^{\star\star}V_{\rm dc}$, the legs are sequentially turned off in order to achieve the voltage level 2. The resultant switched output voltages of the phase *a* and phase *c* are also shown in Fig. E.14, which demonstrates that the nearest three vectors are used during the $(n+1)$th sampling interval. As a result, a disturbance in the line-to-line voltage is avoided.

The flux linkage associated with each of the coils of the phase *b* is also shown in Fig. E.14. During the $(n+1)$th sampling interval, positive dc voltage of $V_{\rm dc}/3$ appears for the interval $(\frac{V_{\rm dc}}{2} - V_x^{\star\star})/6f_c$, which has been balanced by the negative voltage of $2V_{\rm dc}/3$ with duration $(\frac{V_{\rm dc}}{2} - V_x^{\star\star})/3f_c$. As a result, the dc flux injection in the $(n+1)$th sampling interval is assured to be zero. From the $(n+2)$nd sampling interval onwards, all the VSCs operate in steady-state in modulation band 3. The sequences in which VSC legs are switched in band 3 ($(n+2)$nd sampling interval onwards) is decided based on the information of the active and passive VSCs in the nth sampling interval.

3.2.2 Band Transition at Top Update

In this case, all the VSC legs corresponding to phase *b* are switched to obtain the voltage level 2 at the start of the $(n+1)$th sampling interval, whereas level 3 is obtained at the end, as shown in Fig. E.15. The values that are used for the carrier comparison in order to achieve the desired switching sequences are given in Table E.2. The flux balancing is maintained and the nearest three vectors are used to synthesize the reference space voltage vector.

3.3 Transition in Other Cases

The strategy that is used for the transition from band 2 to band 3 is also applied to other cases as well. The values used for the carrier comparison in $(n+1)$th sampling interval in case of the transition from the band 3 to the

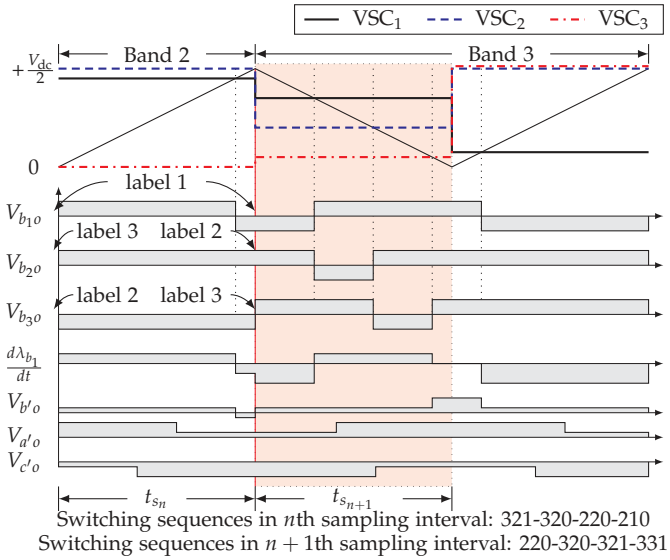


Fig. E.15: Flux balancing strategy for the band transition occurring at the top update.

Table E.3: Transition from band 3 to band 2: values used for the carrier comparison in the $_{n+1}$th sampling interval.

Leg	Leg b_1	Leg b_2		Leg b_3	
	OFF/ON	ON	OFF	ON	OFF
BU	$\frac{V_{dc}+2V_x^{\star\star}}{3}$	$\frac{V_{dc}+2V_x^{\star\star}}{3}$	$\frac{4V_x^{\star\star}-V_{dc}}{6}$	$\frac{4V_x^{\star\star}-V_{dc}}{6}$	$V_x^{\star\star}$
TU	$\frac{V_{dc}+2V_x^{\star\star}}{3}$	$\frac{4V_x^{\star\star}-V_{dc}}{6}$	$\frac{V_{dc}+2V_x^{\star\star}}{3}$	$V_x^{\star\star}$	$\frac{4V_x^{\star\star}-V_{dc}}{6}$

Table E.4: Transition from band 2 to band 1: values used for the carrier comparison in the $_{n+1}$th sampling interval.

Leg	Leg b_1	Leg b_2		Leg b_3	
	OFF/ON	ON	OFF	ON	OFF
BU	$\frac{V_x^{\star\star}}{3}$	$\frac{V_x^{\star\star}}{3}$	$\frac{2V_x^{\star\star}}{3}$	$\frac{2V_x^{\star\star}}{3}$	$V_x^{\star\star}$
TU	$\frac{V_x^{\star\star}}{3}$	$\frac{2V_x^{\star\star}}{3}$	$\frac{V_x^{\star\star}}{3}$	$V_x^{\star\star}$	$\frac{2V_x^{\star\star}}{3}$

band 2, from the band 2 to the band 1, and from band 1 to the band 2 are given in Table E.3, Table E.4, and Table E.5, respectively.

Table E.5: Transition from band 2 to band 1: values used for the carrier comparison in the $_{n+1}$th sampling interval.

Leg	Leg b_1	Leg b_2		Leg b_3	
	OFF/ON	ON	OFF	ON	OFF
BU	$\frac{V_{\rm dc}+2V_x^{\star\star}}{6}$	$\frac{V_{\rm dc}+2V_x^{\star\star}}{6}$	$\frac{V_{\rm dc}+2V_x^{\star\star}}{3}$	$\frac{V_{\rm dc}+2V_x^{\star\star}}{3}$	$V_x^{\star\star}$
TU	$\frac{V_{\rm dc}+2V_x^{\star\star}}{6}$	$\frac{V_{\rm dc}+2V_x^{\star\star}}{3}$	$\frac{V_{\rm dc}+2V_x^{\star\star}}{6}$	$V_x^{\star\star}$	$\frac{V_{\rm dc}+2V_x^{\star\star}}{3}$

4 Implementation of the Proposed Modulation

Fig. E.16 shows the flow chart of the proposed modulation scheme. The operation under the steady-state condition is described. Each of the VSC leg is labeled using the variable $\text{VSC}_{xk_{\rm L}}$, where subscript x represents one of the phases ($x = \{a, b, c\}$) and subscript k represents VSC ($k = \{1, 2, 3\}$). The VSC label $\text{VSC}_{xk_{\rm L}}$ takes any integer value from one to three. This label is used to determine the sequence in which the VSC legs are switched. i.e. VSC leg with label 1 ($\text{VSC}_{xk_{\rm L}} = 1$) is termed as an active VSC and it is always switched in a given sampling interval, whereas the VSC legs with label 2 and label 3 are clamped to either positive dc bus or the negative dc bus. The VSC leg is clamped to the positive dc bus by setting the value used for the carrier comparison to the $V_{\rm dc}/2$ ($\text{CMPR}_{xk} = V_{\rm dc}/2$), whereas zero value is used to clamp the VSC leg to the negative dc bus ($\text{CMPR}_{xk} = 0$). During the steady-state operation, the active VSC, i.e. the VSC leg with the label equal to one ($\text{VSC}_{xk_{\rm L}} = 1$) is assigned $V_x^{\star\star}$ for the carrier comparison ($\text{CMPR}_{xk} = V_x^{\star\star}$). For example, during the steady-state operation in band 3, the label of each of the VSC leg is incremented in the Interrupt Service Routine (ISR) occurring at the top update, whereas labels are kept as it is during the ISR occurring at the bottom update. This VSC label information is then used to determine the values for the carrier comparison for the modulation of the corresponding VSC legs, as shown in Fig. E.16.

The flow chart, explaining the flux balancing scheme during the band transition is shown in Fig. E.17. Only the case in which the transition happens from band 2 to band 3 is shown. However, the same procedure is followed in other cases as well. The switching logic and the values for the carrier comparison in the $(n + 1)$th sampling interval is determined based on the following:

1. Whether the transition happens at the top update or at the bottom update.

2. Label of each of the before the start of the nth sampling interval.

The carrier comparison logic, which is reversed for some of the VSCs during

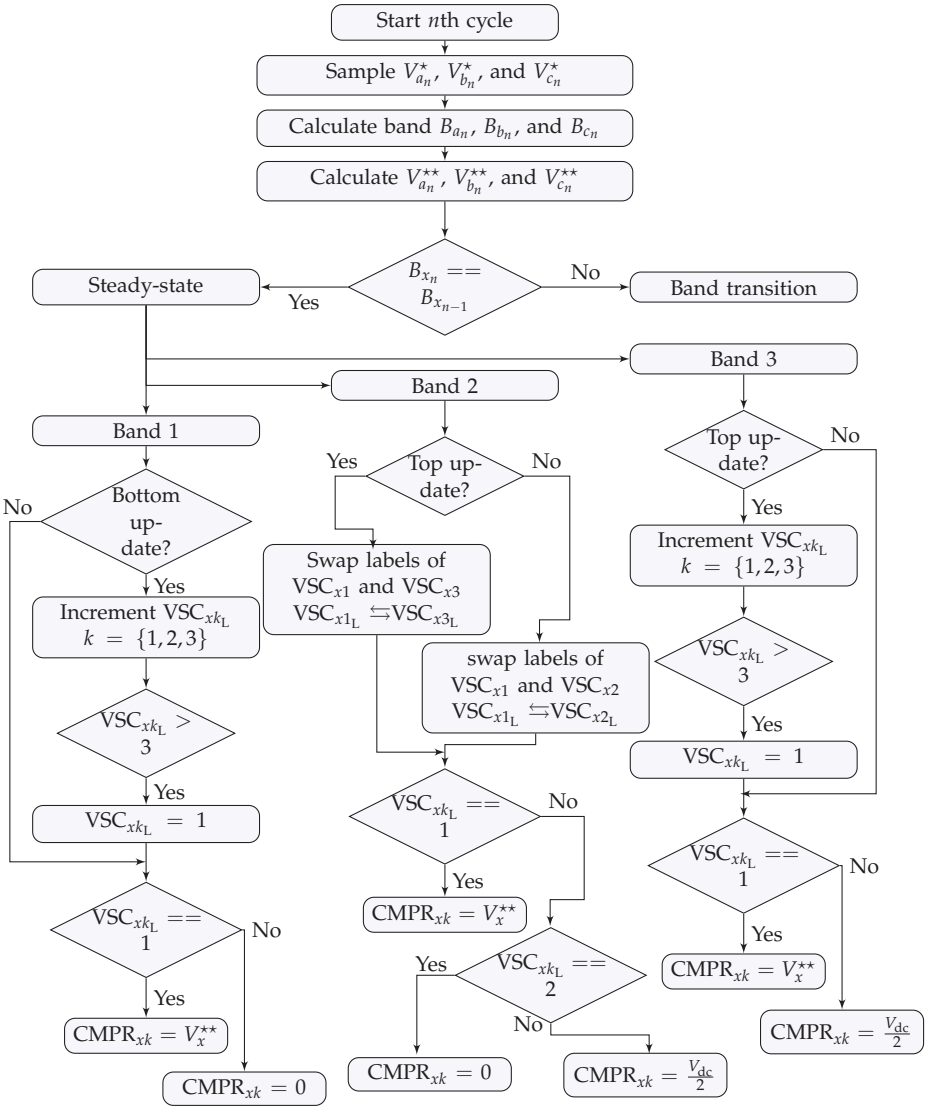


Fig. E.16: Flow chart of the proposed modulation scheme. The operation under steady-state is described. Subscript k represents the voltage source converter number ($k = \{1,2,3\}$). Subscript x represents the phases a, b, and c ($x = \{a,b,c\}$). The sequence in which the legs are switched is represented by label VSC_{xk_L}, where VSC_{xk_L} is the label of the kth leg of the phase x. VSC leg with label 1 ($\text{VSC}_{xk_\text{L}} = 1$) is switched, whereas VSC legs with label 2 and label 3 are clamped to either positive dc bus or negative dc bus. CMPR_{xk} represents the value that is used for the carrier comparison for the kth leg of the phase x.

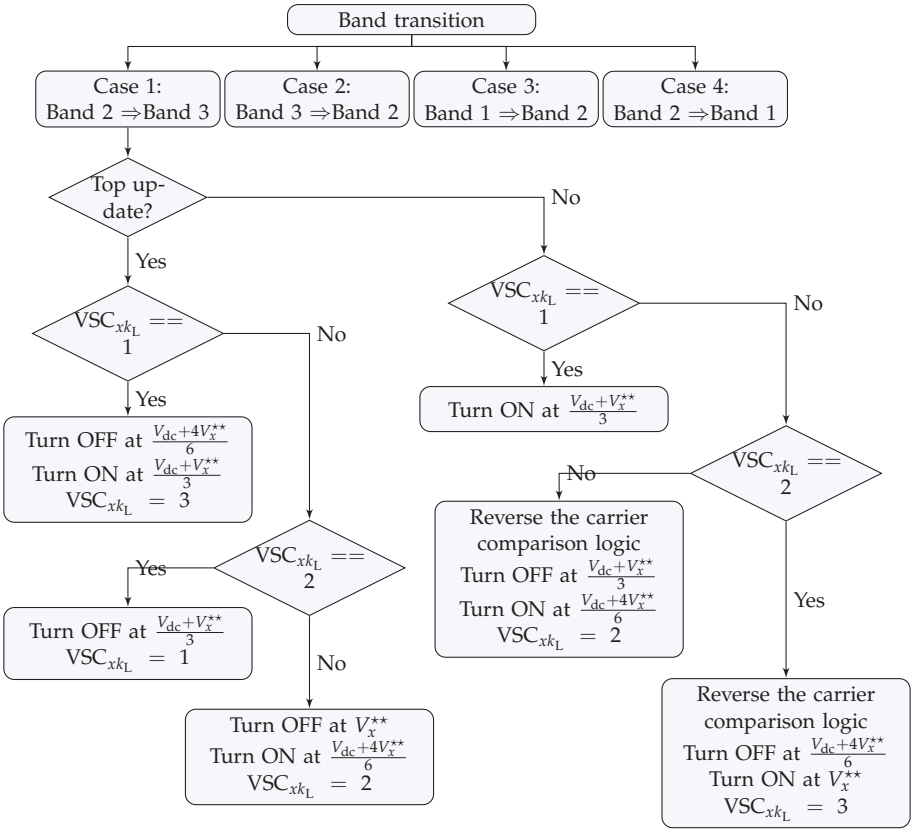


Fig. E.17: Flow chart for the proposed flux balancing scheme during the band transition. The scheme for the transition from band 2 to band 3 is only discussed. Refer Fig. E.14 and Fig. E.15 for the graphical explanation.

the nth sampling interval, is restored back to the original during the $(n+1)$st sampling interval. The label information of each of the VSCs is used to ensure a proper transition from one band to the other, as shown in Fig. E.17 (refer Fig. E.14 and Fig. E.15 for the graphical explanation).

5 Comparative Evaluation and Results

The proposed scheme implements PD PWM of the parallel VSCs. The use of the PD PWM results in a superior harmonic performance compared to the PS PWM. However, additional commutations are introduced in the proposed implementation to ensure the flux balancing during the band transition. As a result, for the same carrier frequency, the switching losses in the proposed

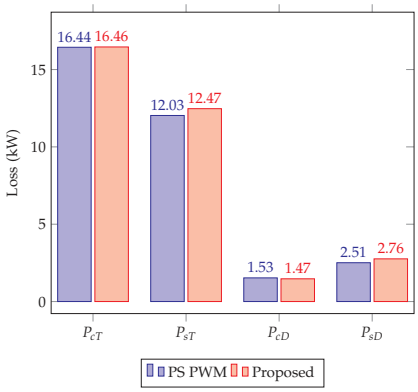


Fig. E.18: Total semiconductor losses in the case of the PS PWM and the proposed scheme evaluated at the full load condition with the power factor of one. Switching frequency is 1.65 kHz in both cases. P_{cT}, P_{sT}, P_{cD}, and P_{sD} are the IGBT conduction losses, IGBT switching losses, diode conduction losses, and diode switching losses, respectively.

implementation would be more compared to that in the case of the PS PWM. Therefore, the harmonic performances of both the proposed scheme and PS PWM are evaluated under a constant loss condition.

5.1 Simulation Results

Time domain simulations have been carried out uing PLECS to calculate the semiconductor losses. A 3.45 MW, 690 V converter system with three parallel VSCs is considered as an example system. The VSCs are assumed to be operated to share the equal current. The 1700 V, 1000 A IGBT with anti-parallel diode from Infineon (FF1000R17IE4) is considered. The conduction losses of the IGBT and the diodes, the turn-on and turn-off losses of the IGBTs and the recovery losses of the diodes are calculated using the parameters given in the datasheet. The dc-link voltage is set to be 1100 V. The effects of the junction temperature on the losses is also considered, where the junction-to-case thermal behavior of the IGBTs and the diodes is modeled using the Foster network representation of the thermal equivalent circuit. The case temperature is assumed to be constant at 60°C.

The semiconductor losses are evaluated at full load conditions with a displacement power factor of one. The carrier frequency is taken to be $f_c = 3 \times 1650$ Hz for the proposed scheme. Three 120° phase-shifted carrier signals with the carrier frequency of 1650 Hz are used for the PS PWM. The total semiconductor losses (of all three VSCs) in both the cases are shown in Fig. E.18. The conduction losses in both the cases are almost the same, whereas the switching losses in the case of the proposed scheme is slightly higher

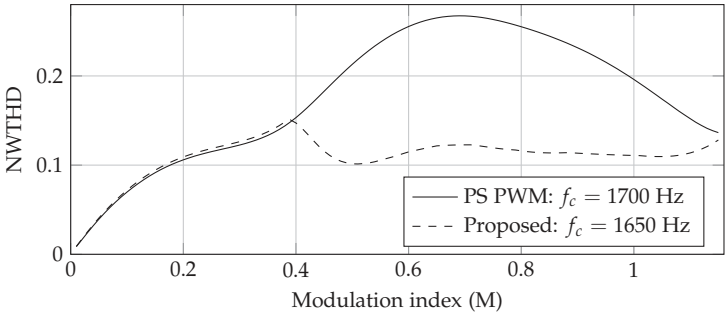


Fig. E.19: Harmonic performance of the PS PWM and the proposed scheme, evaluated under the constant loss condition for the full load unity power factor application.

than that of the PS PWM, as expected due to the additional commutations during the band transition. The switching losses in the IGBTs are higher by 0.47 kW, whereas the switching losses in the diodes are higher by 0.25 kW.

In order to evaluate the harmonic performance under the constant loss conditions, the carrier frequency in the case of the PS PWM is increased to 1700 Hz. The command reference signals for the phase voltages ($V_x^\star$) are obtained by adding common mode offset in the sinusoidal phase voltages (V_a, V_b, and V_c) and it is given as

$$V_x^\star = V_x - 0.5[\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)] \tag{E.9}$$

The harmonic performances of both schemes are compared by evaluating the Normalized Weighted Total Harmonic Distortion (NWTHD) of the line-to-line voltage, which is defined as

$$\text{NWTHD} = \frac{M}{V_f}\sqrt{\sum_{h=2}^{1000}(V_h/h)^2} \tag{E.10}$$

where M is the modulation index and it is defined as the ratio of the amplitude of the reference phase voltage (V_x) to the half of the dc-link voltage. V_f is the fundamental component of the line-to-line voltage, whereas V_h is the magnitude of the hth harmonic component of the line-to-line voltage.

The NWTHD over the full modulation range is shown in Fig. E.19. As the proposed scheme realizes the PD PWM, it demonstrates a better harmonic performance over a wide modulation indices region ($0.4 \leq M \leq 2/\sqrt{3}$). For the grid connected applications, where the converters typically operates with a modulation index in vicinity to one, the use of the proposed scheme results in the 44% reduction in the NWTHD compared to the PS PWM (at $M = 1$). The PS PWM is marginally better than the proposed scheme at lower modulation index due to the higher carrier frequency (constant loss condition).

Table E.6: System parameters.

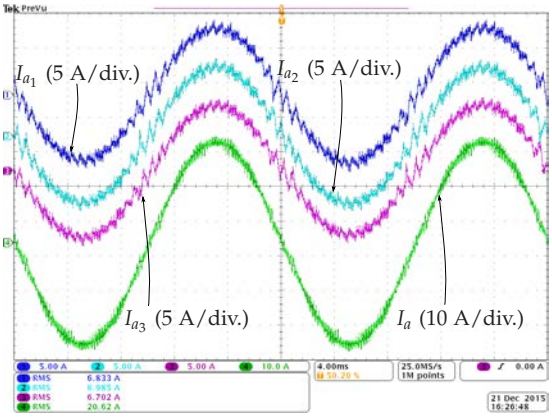
Parameters	Values
Power	15 kW
No. of parallel VSCs	Three (5 kW each)
DC link voltage	700 V
Line filter inductor L_f	0.6 mH
Circulating current inductance L_c	30 mH

5.2 Hardware Results

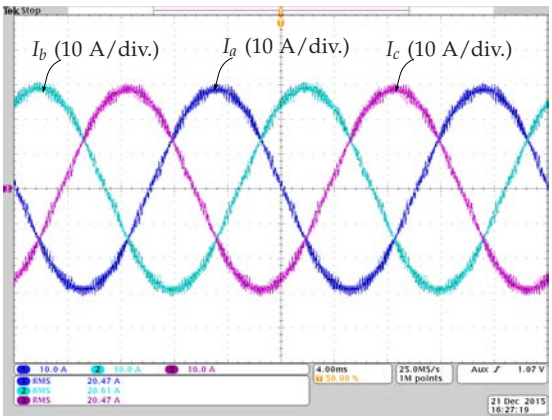
To verify the proposed modulation scheme, a small scale prototype was developed. The specifications of this prototype are given in Table I.1. The CI was build using the three-phase E-core, made from the amorphous alloy 2605SA1. The effective cross-section area of each of the limb is 5.78×10^{-4} m^2 and number of turns in each of the coils are 78. The photograph of the CI is shown in Fig. E.5(b). The proposed modulation scheme has been implemented using the TMS320F28377D Micro-controller. The system was connected to the resistive load of 11.5 Ω. The carrier frequency is taken to be 3×1650 Hz.

The leg currents of phase a of all the VSCs along with the resultant current of phase a for the modulation index of $M = 1$ are shown in Fig. E.20(a). All three VSCs have equal current sharing. The resultant line currents of all the phases are shown in Fig. E.20(b). The resultant currents are sinusoidal, which show that the disturbance in the line-to-line voltage during the band transition due to the extra commutations is avoided in the proposed modulation scheme. The circulating current components of the phase a of all three VSCs along with the resultant switched line-to-line voltage $V_{a'b'}$ are shown in Fig. E.21(a). These circulating current component is proportional to the flux in the CI and it is evident that the flux balancing is achieved by the proposed modulation scheme (as against the dc flux injection shown in Fig. E.8 for the PD PWM implementation). The switched line-to-line voltage has a transition between the two nearest voltage levels during each commutation, as shown in Fig. E.21(a). However, this is not the case when PS PWM is used, as shown in Fig. E.21(b). As a result, substantial improvement in the harmonic performance can be achieved by the proposed modulation scheme, which is evident from the Fig. E.20(b) and Fig. E.22, where the resultant line currents for both cases are shown for the comparison.

Several experimental results with the different values of the modulation index for both cases are obtained. The total harmonic distortion of the resul-



(a)



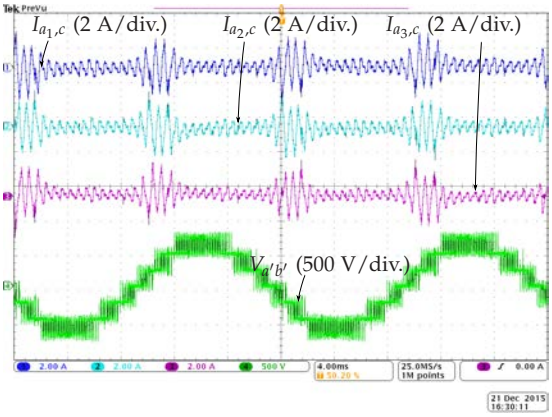
(b)

Fig. E.20: The experimental current waveforms for the proposed modulation scheme. The carrier frequency is 3×1650 Hz. (a) Ch1: VSC1 phase a current (I_{a_1}), Ch2: VSC2 phase a current (I_{a_2}), Ch3: VSC3 phase a current (I_{a_3}), Ch4: Resultant current of phase a (I_a), (b) Ch1: Resultant current of phase a (I_a), Ch2: Resultant current of phase b (I_b), Ch3: Resultant current of phase c (I_c).

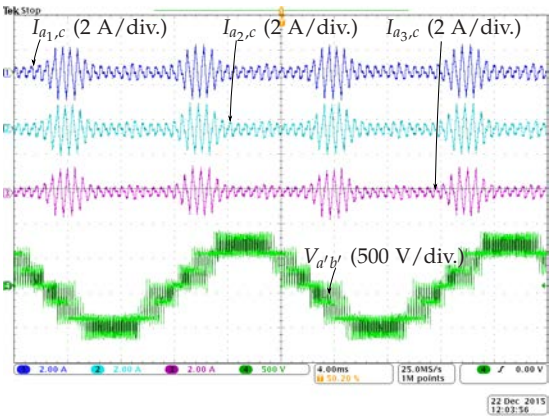
tant line current is obtained as

$$I_{\text{THD}} = \frac{1}{I_{x,f}} \sqrt{\sum_{h=2}^{1000} (I_{x,h})^2} \tag{E.11}$$

The variation of the total harmonic distortion of the resultant line current as a function of the modulation index is shown in Fig. F.18. The proposed modulation scheme demonstrates superior harmonic performance over wide



(a)



(b)

Fig. E.21: Circulating currents of phase a of all three VSCs and the resultant line-to-line voltage $V_{a'b'}$. (a) Proposed modulation scheme with the carrier frequency of 3×1650 Hz, (b) Phase-shifted PWM with three 120° phase-shifted carrier with the frequency of 1700 Hz.

modulation index range.

6 Conclusion

A modulation scheme using the single carrier to realize PD PWM for the three parallel 2L-VSCs is presented. The proposed scheme can easily be implemented using a DSP and the complexity is substantially reduced compared to other implementations, which require several trapezoidal carriers. The operation of the parallel VSCs with the coupled inductor is discussed and the

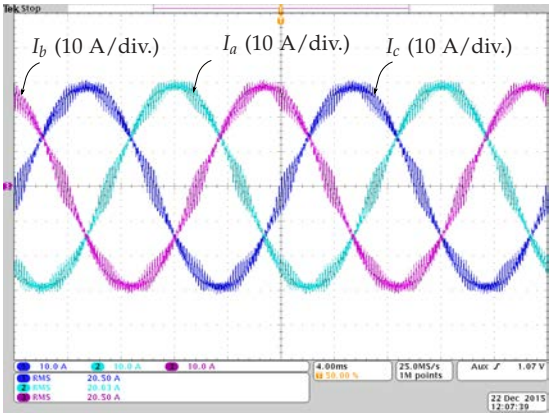


Fig. E.22: Resultant line currents for the phase-shifted PWM with three 120° phase-shifted carrier with the frequency of 1700 Hz.

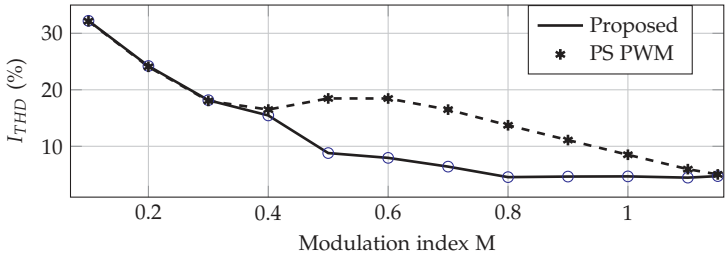


Fig. E.23: Measured total harmonic distortion of the resultant line current as a function of the modulation index.

dc flux injection issue in the case of the PD PWM is investigated. Flux balancing during the transition from one band to the other is ensured. The band transition scheme also ensures the volt-sec balance to synthesize the reference space voltage vector even during a band transition. As a result, any disturbance in the line-to-line voltage is avoided. The harmonic performance of the proposed scheme is compared with the PS PWM by evaluating the NWTHD under constant loss condition. The carrier frequency in the proposed scheme is reduced to account for the effect of the additional commutations introduced during the band transition. As a result, the harmonic performance of the proposed implementation is slightly inferior compared to the PS PWM for the low modulation indices ($M < 0.4$), whereas it is harmonically superior in the remaining modulation range. For the grid connected applications, where the converter operates with the modulation index in the vicinity to one, the proposed implementation results in 44% reduction in the NWTHD.

References

[1] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[2] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[3] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[4] K. Xing, F. Lee, D. Borojevic, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, 1999.

[5] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[6] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved three-phase voltage source converters," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3400–3414, May 2016.

[7] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved vscs and pwm schemes for flux minimization," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7534–7546, Dec 2015.

[8] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[9] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar 2001.

[10] J. H. Seo, C. H. Choi, and D.-S. Hyun, "A new simplified space-vector pwm method for three-level inverters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul 2001.

[11] V. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier pwm techniques," in *Proc. 29th Annual IEEE*

Power Electronics Specialists Conference, vol. 1, May 1998, pp. 172–178 vol.1.

[12] B. McGrath, D. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov 2003.

[13] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[14] F. Forest, T. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire, "Optimization of the supply voltage system in interleaved converters using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 934–942, 2007.

[15] R. Hausmann and I. Barbi, "Three-phase DC-AC converter using four-state switching cell," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1857–1867, July 2011.

[16] B. McGrath, T. Meynard, G. Gateau, and D. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, March 2007.

[17] A. Shukla, A. Ghosh, and A. Joshi, "Natural balancing of flying capacitor voltages in multicell inverter under pd carrier-based pwm," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1682–1693, June 2011.

[18] A. Ghias, J. Pou, G. Capella, V. Agelidis, R. Aguilera, and T. Meynard, "Single-carrier phase-disposition pwm implementation for multilevel flying capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5376–5380, Oct 2015.

[19] G. Capella, J. Pou, S. Ceballos, G. Konstantinou, J. Zaragoza, and V. Agelidis, "Enhanced phase-shifted pwm carrier disposition for interleaved voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1121–1125, March 2015.

[20] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, 2012.

Paper F

An Integrated Inductor for Parallel Interleaved VSCs and PWM Schemes for Flux Minimization

Ghanshyamsinh Gohil,
Lorand Bede,Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been published in the
IEEE Transactions on Industrial Electronics Vol. 62, no. 12, pp. 7534-7546, Dec 2015.

The layout has been revised.

Abstract

The interleaving of the carrier signals of the parallel Voltage Source Converters (VSCs) can reduce the harmonic content in the resultant switched output voltages. As a result, the size of the line filter inductor can be reduced. However, in addition to the line filter, an inductive filter is often required to suppress the circulating current. The size of the system can be reduced by integrating these two inductors in a single magnetic component. A integrated inductor, which combines the functionality of both the line filter inductor and the circulating current filter inductor is presented. The PulseWidth Modulation (PWM) schemes to reduce the flux in some parts of the integrated inductor are also analyzed. The flux reduction achieved by using these schemes is demonstrated by comparing these schemes with the conventional space vector modulation and the 60° clamped discontinuous PWM scheme. The impact of these PWM schemes on the harmonic performance is also discussed. Simulation and experimental results are presented to validate the analysis.

1 Introduction

Voltage Source Converters (VSCs) are often connected in parallel in many high power applications. The harmonic quality of the resultant voltage waveforms in such systems can be improved by interleaving the carrier signals of the parallel connected VSCs [1–3]. This leads to size reduction of the line filter inductor through the improvement in the output voltage quality. However, when VSCs are connected in parallel, the circulating current flows through the closed path due to the control asymmetry and the impedance mismatch. When the carriers are interleaved, the pole voltages (switched output voltage of the VSC leg, measured with respect to the dc-linl mid-point O) of the interleaved parallel legs are phase shifted. This instantaneous potential difference further increases the circulating current, which would result in increased losses and unnecessary over-sizing of the components present in the circulating current path. Therefore, the circulating current should be suppressed to realize the full potential of the interleaved carriers in parallel connected VSCs.

The formation of the circulating current path can be avoided by using the line frequency isolation transformer [4]. However, it increases the overall size of the system and should be avoided. The use of the Common-Mode (CM) inductor in series with the line filter inductor for each of the VSCs is proposed in [2], as shown in Fig. F.1. Another approach proposes the use of the Coupled Inductor (CI) to suppress the circulating current by providing magnetic coupling between the parallel interleaved legs of the corresponding phases [1, 5] is also shown in Fig. F.1. A Pulse Width Modulation (PWM) scheme to reduce the peak value of the flux density in the CI is presented

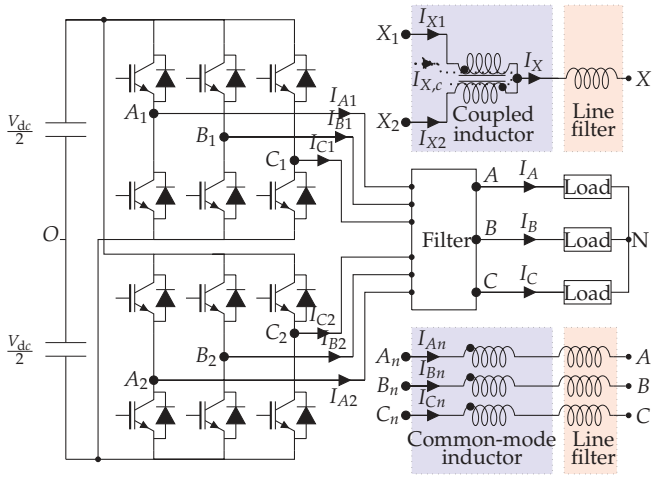


Fig. F.1: Two parallel interleaved VSCs with a common dc-link. The filter arrangement for circulating current suppression using the CI and the CM inductor is depicted, where $X = \{A, B, C\}$ and $n = \{1, 2\}$.

in [6], where the common mode signal, which is added to the reference voltage waveforms, has been optimized. Ewanchuk *et al.* [7] proposed the integration of three different CIs into one three-limb core. However, in order to suppress the circulating current using the three-limb core, the CM voltage difference between the two parallel VSCs should be made zero. This was achieved by employing a modified Discontinuous PulseWidth Modulation (DPWM) scheme, which has more number of commutations than the conventional (both the continuous and the discontinuous) modulation schemes. Therefore, this scheme may not be feasible for medium/high power applications.

In all of the above discussed approaches, two distinct magnetic components are involved:

1. Line filter inductor (commonly referred as a boost inductor) for improving the line current quality.

2. Additional inductive components (CI / CM inductor) for suppressing the circulating current.

The improvement in the power density can be achieved by integrating both of these inductors in a single magnetic structure.

This paper presents an integrated three-phase inductor for the parallel interleaved VSCs, which integrates three CIs and a three phase line filter inductor in a single magnetic structure. The analysis of the integrated three-phase inductor is given in Section II. Optimized PWM schemes to reduce the

flux in some parts of the proposed inductor are discussed in Section III and their impact on the line current quality is evaluated in Section IV. A design example of an integrated inductor is presented in Section V. Finally, Section VI summarizes simulations and experimental results.

2 Integrated Inductor

The magnetic structure of the proposed integrated inductor, which combines the functionality of three separate CIs and the three-phase line filter inductor, is shown in Fig. H.2(a). The core is composed of three inner legs (referred as a phase leg), two outer common legs and two bridge legs which facilitate the magnetic coupling between the phases. The coils of a particular phase of both of the parallel VSCs are wound on the same phase leg with opposite winding directions. A high permeability material is used for the phase legs and the common legs, whereas the bridge legs are realized using laminated iron core. Necessary air gaps have been inserted in between the bridge leg and the phase legs.

2.1 Simplified Reluctance Model

A simplified reluctance model of the integrated inductor is shown in Fig. F.2(b). The reluctance of half of the phase leg is taken to be $\Re_L$ and the reluctance of each of the air gap is termed as $2\Re_g$. The equivalent reluctance of each bridge leg is the addition of the reluctance of the air gap

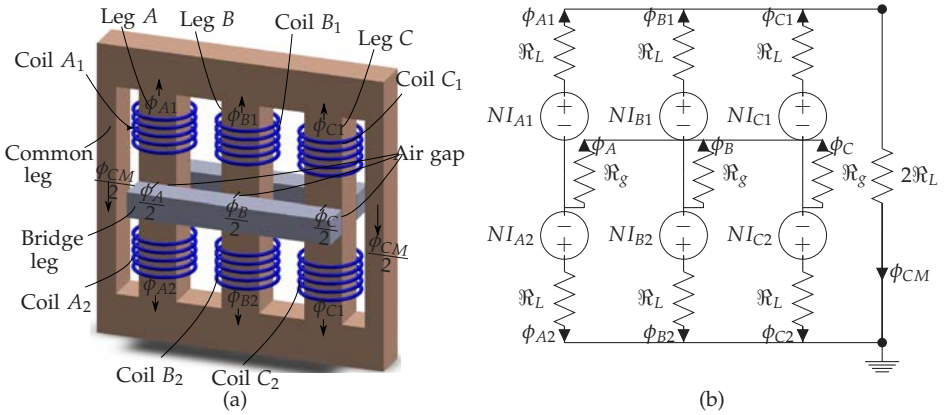


Fig. F.2: Magnetic structure of the proposed integrated three-phase inductor. (a) Physical arrangement, (b) Simplified reluctance model of the proposed integrated three-phase inductor.

($\Re_g = 2\Re_g \parallel 2\Re_g$) and the reluctance of the laminated iron core of that bridge. However, the reluctance of the laminated steel core is very small compared to the equivalent reluctance of the air gap $\Re_g$. Therefore, the reluctance of each bridge leg is approximated as $\Re_g$, as shown in Fig. F.2(b). In addition, the magnetic asymmetry introduced by the yokes of the high permeability magnetic material is also neglected.

The coils are represented by the equivalent Magneto-Motive Forces (MMFs) in the simplified reluctance model. The MMF of each coil is proportional to the current flowing through that coil. Therefore, the involved current quantities are first defined and then the reluctance network is solved in order to obtain the flux linkage associated with each of the coils.

In parallel interleaved VSCs, the current flowing through the coil has a circulating current component ($I_{x,c}$) and a line current component $I_{x,l}$. Assuming ideal VSCs and neglecting the effect of the hardware/control asymmetries, the line current component of each of the VSCs are considered to be equal and it is given as

$$I_{x,l} = \frac{I_x}{2} \tag{F.1}$$

where $x = \{A, B, C\}$ and I_x is the resultant line current. Therefore, the coil currents can be expressed as

$$I_{x1} = \frac{I_x}{2} + I_{x,c} \text{ and } I_{x2} = \frac{I_x}{2} - I_{x,c} \tag{F.2}$$

where $I_{x,c}$ is the circulating current. Using (F.2), the circulating current is obtained as

$$I_{x,c} = \frac{I_{x1} - I_{x2}}{2} \tag{F.3}$$

The CM current is defined as

$$I_{CM,n} = \frac{I_{An} + I_{Bn} + I_{Cn}}{3} \tag{F.4}$$

where n={1,2}. Using (F.3) and (F.4), the CM circulating current $I_{CM,c}$ is given by

$$I_{CM,c} = \frac{I_{CM,1} - I_{CM,2}}{2} = \frac{I_{A,c} + I_{B,c} + I_{C,c}}{3} \tag{F.5}$$

By solving the simplified reluctance network, the flux in the phase legs are

$$\begin{aligned} \phi_{x1} &\approx \frac{1}{2(\Re_L + 2\Re_g)} NI_x + \frac{1}{\Re} NI_{x,c} - \frac{3}{4\Re} NI_{CM,c} \\ \phi_{x2} &\approx \frac{1}{2(\Re_L + 2\Re_g)} NI_x - \frac{1}{\Re} NI_{x,c} + \frac{3}{4\Re} NI_{CM,c} \end{aligned} \tag{F.6}$$

The CM flux component is given as

$$\phi_{CM} \approx \frac{3}{4\Re_L} N I_{CM,c} \tag{F.7}$$

and the flux in the common leg is half of the CM flux $\phi_{CM}/2$. The flux in the air gaps is given as

$$\phi_x \approx -\frac{1}{\Re_L + 2\Re_g} N I_x \tag{F.8}$$

2.2 Line Filter Inductance L_f

Using (F.6), the voltage across the coil $x1$ can be obtained as

$$\int V_{x1x}\, dt = \frac{N^2}{2(\Re_L + 2\Re_g)} I_x + \frac{N^2}{\Re} I_{x,c} - \frac{3N^2}{4\Re} I_{CM,c} \tag{F.9}$$

Similarly, the voltage across across the coil $x2$ is given as

$$\int V_{x2x}\, dt = \frac{N^2}{2(\Re_L + 2\Re_g)} I_x - \frac{N^2}{\Re} I_{x,c} + \frac{3N^2}{4\Re} I_{CM,c} \tag{F.10}$$

Averaging the voltages across the coils of the respective phases

$$\boldsymbol{V_{avg}} = \boldsymbol{L_f} \frac{d}{dt} \boldsymbol{I} + \boldsymbol{V_g} \tag{F.11}$$

where

$$\boldsymbol{V_{avg}} = \begin{bmatrix} \frac{V_{A1O}+V_{A2O}}{2} & \frac{V_{B1O}+V_{B2O}}{2} & \frac{V_{C1O}+V_{C2O}}{2} \end{bmatrix}^T \tag{F.12}$$

$$\boldsymbol{V_g} = \begin{bmatrix} V_{A_g} & V_{B_g} & V_{C_g} \end{bmatrix}^T, \ \boldsymbol{I} = \begin{bmatrix} I_A & I_B & I_C \end{bmatrix}^T \tag{F.13}$$

$$\boldsymbol{L_f} = \frac{N^2}{6(\Re_L + 2\Re_g)} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{F.14}$$

Differential equation (H.19) describes the dynamics of the resultant line current. For a three-phase balance system

$$I_A + I_B + I_C = 0 \tag{F.15}$$

Using (H.19) and (F.15), the average value of the flux linkage of the respective phase is given as

$$\int \left(\frac{V_{x1O} + V_{x2O}}{2} \right) dt = \frac{N^2}{2(\Re_L + 2\Re_g)} I_x + V_{x_g} \tag{F.16}$$

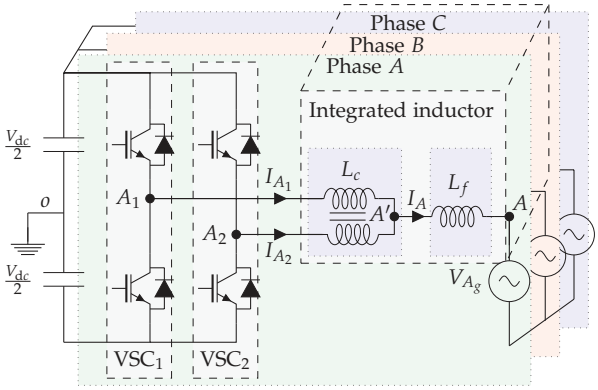


Fig. F.3: Parallel interleaved VSCs with the proposed integrated inductor.

and the inductance offered to the line current is given as

$$L_f \approx \frac{N^2}{2(\Re_L + 2\Re_g)} \approx \frac{N^2}{4\Re_g} \tag{F.17}$$

Let, the length of each of the air gap be l_g and the effective cross-sectional area of the gap is A_g. Then (K.34) can be rewritten as

$$L_f \approx \frac{\mu_0 N^2 A_g}{2l_g} \tag{F.18}$$

2.3 Circulating Current Filter Inductance L_c

The circulating current is proportional to the time integral of the difference of the pole voltages of the parallel legs. For the proposed integrated inductor, the differential equations that describe the behavior of the circulating current is obtained from (F.9) and (F.10) and it is given as

$$\boldsymbol{\Delta V} = \boldsymbol{L_c} \frac{d}{dt} \boldsymbol{I_c} \tag{F.19}$$

$$\text{where } \boldsymbol{\Delta V} = \begin{bmatrix} \Delta V_A & \Delta V_B & \Delta V_C \end{bmatrix}^T \tag{F.20}$$

$$\boldsymbol{I_c} = \begin{bmatrix} I_{A,c} & I_{B,c} & I_{C,c} \end{bmatrix}^T \tag{F.21}$$

$$\boldsymbol{L_c} = \frac{N^2}{2\Re_L} \begin{bmatrix} 3 & -1 & -1 \\ -1 & 3 & -1 \\ -1 & -1 & 3 \end{bmatrix} \tag{F.22}$$

where $\Delta V_x = V_{x1O} - V_{x2O}$ and $x = \{A, B, C\}$. As given in (H.21), the value of the $\boldsymbol{L_c}$ is independent of the air gap geometry and depends only on the values of the reluctance of the phase legs and the common legs. The circulating current can effectively be suppressed by reducing the reluctance of the phase legs and the common legs.

Using (H.19) and (H.21), electrical equivalent circuit of the parallel interleaved VSCs with the proposed integrated inductor is derived, as shown in Fig. F.3.

2.4 Flux Linkage in the Common Legs

The common legs in the proposed integrated inductor are required to provide the return path for the common flux components of the circulating flux of all three phases. The size of the proposed integrated inductor can be further reduced by reducing the peak value of the flux in the common legs. The flux in the common leg depends on the reluctance of the common leg, the number of turns, and the CM circulating current $I_{CM,c}$, as shown in (F.7). The CM circulating current $I_{CM,c}$ is proportional to the time integral of the CM voltage difference of the parallel VSCs.

In order to present a general analysis (independent of the number of turns N), the CM flux linkage is analyzed. Using (F.6) and (F.7), the CM flux linkage is derived, and it is given as

$$\lambda_{CM}(t) = \frac{3}{2} \int \Delta V_{CM}\, dt \tag{F.23}$$

where ΔV_{CM} is the CM voltage difference of both the VSCs ($V_{CM,1} - V_{CM,2}$). Therefore, the flux density in the common leg can be reduced by decreasing the $\int \Delta V_{CM} dt$.

3 PWM Schemes

The size reduction of the proposed integrated inductor can be achieved by reducing the peak value of the λ_{CM}. PWM schemes to reduce the peak value of the λ_{CM} are discussed in this Section. The improvement achieved by using these schemes is demonstrated by comparing the peak value of the λ_{CM} of these schemes with that of the center aligned Space Vector Modulation (SVM) and the 60° clamped discontinuous modulation (DPWM1) [8]. The analysis is carried for the interleaving angle of 180°, as it results in optimal harmonic performance at high modulation indices.

3.1 Conventional PWM Schemes

In a conventional SVM, VSC cycles through four switch states in each switching cycle. Based on the position of the reference space vector ($\overrightarrow{V}_{ref}$), two adjacent active voltage vectors and both of the zero voltage vectors ($\overrightarrow{V}_0$, $\overrightarrow{V}_7$) are applied to synthesize $\overrightarrow{V}_{ref}$. Out of the two zero voltage vectors, one is redundant and can be omitted. As a result, several DPWM schemes have emerged. In both the SVM and the DPWM, at least one zero voltage vector is used in each switching cycle. The use of the zero vector would lead to the maximum value of the CM voltage of $\pm V_{\mathrm{dc}}/2$. For the parallel interleaved VSCs with an interleaving angle of 180°, the use of the SVM would result in maximum value of the ΔV_{CM} to be $\pm V_{\mathrm{dc}}$, whereas for DPWM schemes, this value is $\pm 2V_{\mathrm{dc}}/3$ [9]. From (F.23), it is evident that the flux in the common leg can be reduced by reducing the time integral of the ΔV_{CM}. This can be achieved by avoiding the use of zero voltage vectors.

3.2 Reduced CM Voltage PWM Schemes

Several PWM schemes, which do not use zero vectors to synthesize the $\overrightarrow{V}_{ref}$, are reported in the literature [10]. Out of these reported schemes, the most suitable schemes for parallel interleaved VSCs with the proposed integrated inductor are identified and their effect on the λ_{CM} is discussed.

An Active Zero State PWM (AZSPWM) scheme uses two adjacent active voltage vectors and two near opposing active vectors [11–14]. The active voltage vectors that are 120° apart are used in a Remote State PWM (RSPWM) scheme [15]. However, the number of commutations in a switching cycle is increased compared to that of the SVM and may not be feasible in high power applications due to the high switching losses. A Near State PWM (NSPWM) employs three nearest active voltage vectors to synthesize the $\overrightarrow{V}_{ref}$ [16, 17]. Out of these PWM schemes, the AZSPWM and the NSPWM are adopted to modulate the parallel interleaved VSCs because of their superior harmonic performance, as discussed in Section IV.

3.2.1 Near State PWM

The NSPWM scheme employs three nearest active voltage vectors to synthesize the reference voltage vector $\overrightarrow{V}_{ref}$. Fig. F.4(a), shows the switching sequences used in the different sectors of the space vector diagram, where the number represents the sequence in which the corresponding voltage vectors are applied. Depending on the switching sequences involved, the space vector diagram is divided into six regions. The switching sequence 612 is used in both sub-sector 1 ($0° \leq \psi < 30°$) and sub-sector 12 ($330° \leq \psi < 360°$) and these two sub-sector together constitute region 1.

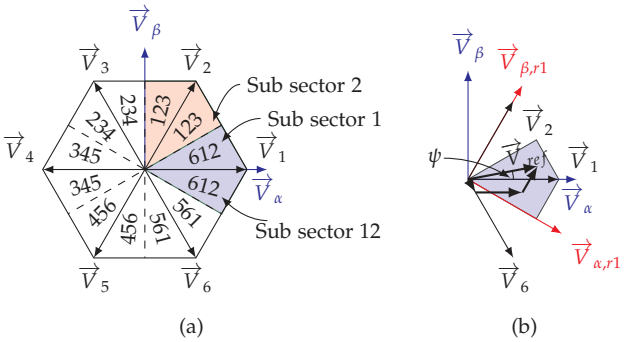


Fig. F.4: NSPWM. (a) Switching sequences involved in the near state PWM. Numbers represents the switching sequence, (b) Formation of a reference space vector V_{ref} by the geometrical summation of the three nearest voltage vectors in the region 1.

The geometrical formation of the $\overrightarrow{V}_{ref}$ in region 1 is depicted in Fig. F.4(b). The active voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_6}$ are used and their respective dwell times are given as

$$T_1 = (\sqrt{3}\frac{V_{\alpha,r}}{V_{\text{dc}}} + \frac{V_{\beta,r}}{V_{dc}} - 1)T_s \tag{F.24a}$$

$$T_2 = (1 - \frac{2}{\sqrt{3}}\frac{V_{\alpha,r}}{V_{\text{dc}}})T_s \tag{F.24b}$$

$$T_6 = (1 - \frac{1}{\sqrt{3}}\frac{V_{\alpha,r}}{V_{\text{dc}}} - \frac{V_{\beta,r}}{V_{\text{dc}}})T_s \tag{F.24c}$$

where $V_{\alpha,r}$ and $V_{\beta,r}$ are the α and β components at the start of the region. For the region 1, these components are given as

$$V_{\alpha,r1} = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta\,,\; V_{\beta,r1} = \frac{1}{2}V_\alpha + \frac{\sqrt{3}}{2}V_\beta \tag{F.25}$$

Let the modulation index M be the ratio of the amplitude of the reference phase voltage to the half of the dc-link voltage. In NSPWM, the value of M should not fall below 0.769 in order to ensure positive dwell times of the active voltage vectors. Therefore, the modulation index M should be restricted within a range of 0.769 to 1.154, which is sufficient for most grid-connected applications in a normal operating mode. However, the VSC is required to operate in a low modulation index region during the low voltage ride through and AZSPWM is used in this region.

3.2.2 AZSPWM Scheme

The adjacent active voltage vectors and the two near opposing active voltage vectors are used to formulate the reference voltage vector $\overrightarrow{V}_{ref}$ [11–13]. The

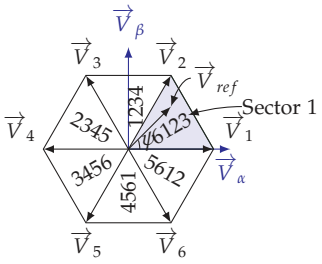


Fig. F.5: Switching sequences involved in the active zero state PWM.

switching sequences involved in the AZSPWM are shown in Fig. F.5. The discussion is only restricted to sector 1 ($0^\circ \leq \psi < 60^\circ$) due to the symmetry. The active voltage vectors $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_3}$, and $\overrightarrow{V_6}$ are used in sector 1, and their respective dwell times are given as

$$T_1 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V_{ref}}|}{V_{\mathrm{dc}}} T_s \sin(60^\circ - \psi) \tag{F.26a}$$

$$T_2 = \frac{2}{\sqrt{3}} \frac{|\overrightarrow{V_{ref}}|}{V_{\mathrm{dc}}} T_s \sin(\psi) \tag{F.26b}$$

$$T_3 = T_6 = (T_s - T_1 - T_2)/2 \tag{F.26c}$$

The dwell time of the adjacent active vectors (T_1, T_2) is the same as that of the conventional SVM. However, instead of using the zero vectors, two near opposing active voltage vectors ($\overrightarrow{V_3}, \overrightarrow{V_6}$) are used. As a result, the linear operation over the entire modulation range ($0 \leq M < 2/\sqrt{3}$) is achieved.

3.3 Flux Linkage

3.3.1 NSPWM

The CM voltage of the individual VSC ($V_{CM,1}$ and $V_{CM,2}$) and their difference ΔV_{CM} are shown in Fig. F.6. Due to the use of only active vectors, the maximum CM voltage of the individual VSCs is limited to $\pm V_{\mathrm{dc}}/6$. The application of voltage vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ results in the equal and opposite polarity CM voltages. Due to the opposite polarity of the individual CM voltages, the simultaneous application of $\overrightarrow{V_1}$ in VSC1 and $\overrightarrow{V_2}$ in VSC2 and vice-versa in sub sector 1 forces the difference in CM voltages ΔV_{CM} to take the value of $\pm V_{\mathrm{dc}}/3$. Therefore, for a given dc-link voltage, the peak value of the flux linkage in a switching cycle ($\lambda_{CM,p}$) depends on the overlap time of the voltage vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$, as shown in Fig. F.6. Similarly, when the $\overrightarrow{V}_{ref}$ is in sub sector 12, the overlap time of the voltage vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_6}$

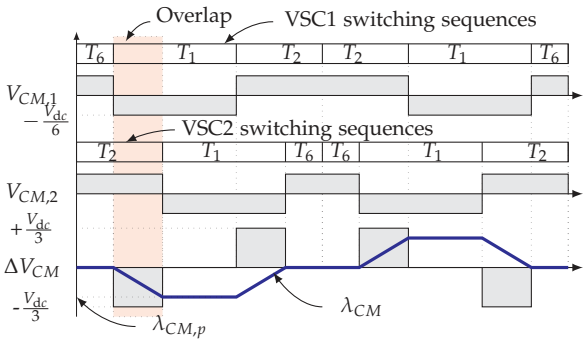


Fig. F.6: Switching sequences and CM voltages of both the VSCs with an interleaving angle of 180°in sub-sector 1 ($30° \leq \psi < 60°$) for the NSPWM.

Table F.1: Maximum value of the peak CM flux linkage

PWM	Max of the peak CM flux linkage ($\lambda_{CM,pmax}$)
NSPWM	$\lambda_{CM,pmax} = \frac{V_{dc}T_s}{16}\left(3M\sin\left[\arccos\left(\frac{1}{\sqrt{3}M}\right)\right]-1\right)$ for $(0.769 \leq M \leq \frac{2}{\sqrt{3}})$
AZSPWM	$\lambda_{CM,pmax} = \frac{V_{dc}T_s}{12}\left(1-\frac{3}{4}M\right)$ for $\left(0 \leq M \leq \frac{8}{3+4\sqrt{3}}\right)$ $\lambda_{CM,pmax} = \frac{V_{dc}T_s}{12}\left(\sqrt{3}M-1\right)$ for $\left(\frac{8}{3+4\sqrt{3}} \leq M \leq \frac{2}{\sqrt{3}}\right)$

decides the value of the $\lambda_{CM,p}$.

The value of the $\lambda_{CM,p}$ changes with every update of the reference voltage vector $\overrightarrow{V}_{ref}$ (varies with the space vector angle ψ, and therefore has different values in each switching cycle). The maximum value out of the $\lambda_{CM,p}$ values over a 60° region of the space diagram is denoted as $\lambda_{CM,pmax}$ and it is given in Table F.1.

3.3.2 AZSPWM

The variation of the $\lambda_{CM,pmax}$ over a 60° region of the space diagram for the AZSPWM is also given in Table F.1.

The variation in the $\lambda_{CM,pmax}$ with respect to the modulation index M for both the NSPWM and the AZSPWM is plotted in Fig. F.7 and compared

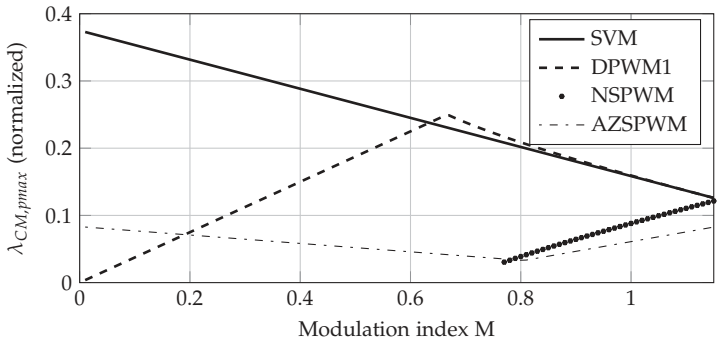


Fig. F.7: The variation of the maximum value of the flux linkage in the common leg as a function of the modulation index. The $\lambda_{CM,pmax}$ is normalized with respect to the $V_{\mathrm{dc}}T_s$. For the NSPWM, the $\lambda_{CM,pmax}$ is plotted only for the linear modulation range of $0.769 \leqslant M \leqslant 1.154$.

Table F.2: Maximum value of the CM flux linkage over the entire linear modulation range

PWM	Maximum flux-linkage (normalized)	Reduction
SVM	0.37 ($M = 0$)	100%
DPWM1	0.25 ($M = 2/3$)	67%
NSPWM	0.12 ($M = \frac{2}{\sqrt{3}}$)	32%
AZSPWM	0.082 ($M = 0$, $M = \frac{2}{\sqrt{3}}$)	22%

with that of the SVM and the 60° clamped DPWM (commonly referred as a DPWM1) schemes. The equations for $\lambda_{CM,pmax}$ as a function of modulation index M for the SVM and the DPWM1 are derived in [9] and the variation of the $\lambda_{CM,pmax}$ is plotted in Fig. F.7 for the sake of comparison. The maximum values of the CM flux linkage for the entire linear modulation range for each of the PWM schemes are shown in Table F.2. The CM flux linkage values are normalized with respect to the $V_{\mathrm{dc}}T_s$. Considering the maximum value of the CM flux linkage of the SVM as a base value, the reduction achieved by other PWM schemes is given in Table F.2. A considerable reduction in the maximum CM flux-linkage is achieved using the AZSPWM (78% reduction compared to SVM and 66% reduction compared to the DPWM1). The use of the NSPWM also results in substantial reduction in the maximum value of the CM flux-linkage.

Table F.3: The polarity of the carrier signals of each of the phases of the individual VSCs in sector 1 ($0^\circ \leq \psi < 60^\circ$) for the SVM and the AZSPWM and in region 1 for the DPWM1 and the NSPWM

Carrier	SVM / DPWM1		AZSPWM		NSPWM	
Phase	VSC1	VSC2	VSC1	VSC2	VSC1	VSC2
A	$+ve$	$-ve$	$-ve$	$+ve$	$+ve$	$-ve$
B	$+ve$	$-ve$	$+ve$	$-ve$	$+ve$	$-ve$
C	$+ve$	$-ve$	$-ve$	$+ve$	$-ve$	$+ve$

4 Assessment of the Line Current Quality

The impact of the switching sequences of the NSPWM and the AZSPWM on the line current quality is analyzed in this section.

4.1 Pulse Patterns

The use of NSPWM and AZSPWM is limited in a single VSC system as the line-to-line voltage pulses exhibits bipolar pattern and results in more ripple in the line current [17]. However, in the case of the parallel interleaved VSCs, the pulse pattern of the resultant line-to-line voltage can be significantly improved by using an interleaving angle of 180°, as explained in this subsection.

The scalar implementation of the AZSPWM requires two opposite polarity carrier signals. The modulation waveforms are the same as that of the SVM and the carrier waveforms are selected based on the reference space vector angles [18]. For the parallel interleaved VSCs, the selection of the carrier signals to modulate each of the phases in sector 1 ($0^\circ \leq \psi < 60^\circ$) for the SVM and the AZSPWM scheme are shown in Table F.3. The use of the same modulation signal and the same carrier signals for phase B in both the PWM schemes yields the same pole voltages of phase B. However, the carrier signals of phase A and phase C in AZSPWM have opposite polarity than the SVM. As a result, the pole voltages of phase A and phase C of the individual VSCs are different in the SVM and the AZSPWM. For the parallel VSCs, the resultant pole voltage is an average of the pole voltages of the individual VSCs. The pole voltages of the individual VSCs and the resultant pole voltage for phase A for the SVM and the AZSPWM are shown in Fig. F.8 and it is evident that the resultant pole voltages are the same in both the cases. Therefore, for the parallel interleaved VSCs with an interleaving angle 180°, the resultant pole voltages of all the phases are the same for both the SVM and the AZSPWM. As a result, the harmonic performance of the parallel interleaved VSCs modulated using the AZSPWM is also the same as that of the SVM.

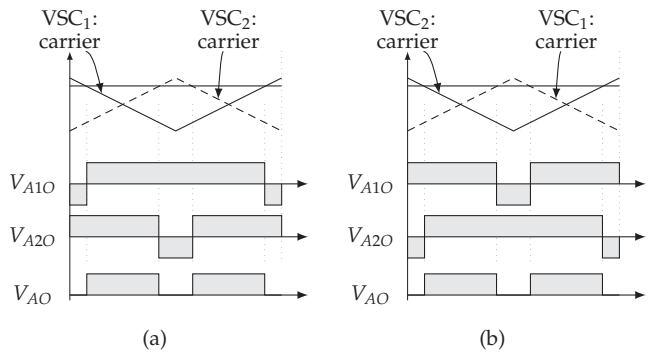


Fig. F.8: Pole voltages of phase A of individual VSCs and their average with $M = 1$ and $\psi = 20^\circ$. (a) SVM, (b) AZSPWM.

Similarly, the NSPWM scheme can be realized by using the modulation waveforms of the DPWM1 and by using two carrier signals with opposite polarities [18]. For an interleaving angle of 180°, the polarity of the carrier signals of each of the phases of the individual VSCs in region 1 ($330^\circ \leq \psi < 360^\circ$ and $0^\circ \leq \psi < 30^\circ$) for the NSPWM and the DPWM1 schemes are given in Table F.3. Due to the use of the same modulation waveform and the same carrier signals in region 1, the pole voltages of phase A and phase B are the same for both the PWM schemes. In NSPWM, phase C is modulated using the opposite polarity carrier than that of the DPWM1 and therefore the pole voltages of phase C of the individual VSCs are different in both the schemes. However, the average of the pole voltages of phase C is the same for both of the PWM schemes. As a result, the harmonic performance of the parallel interleaved VSCs, modulated using the NSPWM, is also the same as that of the DPWM1.

4.2 Harmonic Performance

As a result of the modulation, the pole voltages have undesirable harmonic components in addition to the required fundamental component. These harmonic components can be represented as the summation series of sinusoids, characterized by the carrier index variable m and the baseband index variable

n [8] and it is given as

$$\begin{aligned} f(t) =& \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n}\cos(n[\omega_0 t + \theta_0]) + B_{0n}\sin(n[\omega_0 t + \theta_0])] \\ &+ \sum_{m=1}^{\infty} [A_{m0}\cos(m[\omega_c t + \theta_c]) + B_{m0}\sin(m[\omega_c t + \theta_c])] \\ &+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} [A_{mn}\cos(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0]) \\ &\quad + B_{mn}\sin(m[\omega_c t + \theta_c] + n[\omega_0 t + \theta_0])] \end{aligned} \tag{F.27}$$

The h*th* harmonic component is defined in terms of m and n, and it is given as

$$h = m\left(\frac{\omega_c}{\omega_0}\right) + n \tag{F.28}$$

where ω_0 is the fundamental frequency and ω_c is the carrier frequency.

The harmonic coefficients A_{mn} and B_{mn} in (F.27) are evaluated for each 60° sextant using the double Fourier integral and they are given as

$$Amn_{AZS} = \frac{4V_{\mathrm{dc}}}{q\pi^2} \times \left(\begin{array}{l} \frac{\pi}{6}\cos(m\frac{\pi}{2})\sin(n\frac{\pi}{2})[1-\cos(2n\frac{\pi}{3})] \\ \qquad \times \{J_n(q\frac{3\pi}{4}M) + 2\cos(\frac{n\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)\} \\ + \sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n+k]\frac{\pi}{2}\right)\sin\left([n+k]\frac{\pi}{6}\right) \\ \qquad \times \left\{J_k(q\frac{3\pi}{4}M)\left[1-\cos([n+3k]\frac{\pi}{3})\right]\right\} \\ \qquad + 2\left[\cos\left([2n+3k]\frac{\pi}{6}\right) - \cos\left([n-3k]\frac{\pi}{6}\right)\cos(n\frac{\pi}{6})\right]\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\} \\ + \sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n-k]\frac{\pi}{2}\right)\sin\left([n-k]\frac{\pi}{6}\right) \\ \qquad \times \left\{J_k(q\frac{3\pi}{4}M)\left[1-\cos([n-3k]\frac{\pi}{3})\right]\right\} \\ \qquad + 2\left[\cos\left([2n-3k]\frac{\pi}{6}\right) - \cos\left([n+3k]\frac{\pi}{6}\right)\cos(n\frac{\pi}{6})\right]\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\} \end{array} \right) \tag{F.29}$$

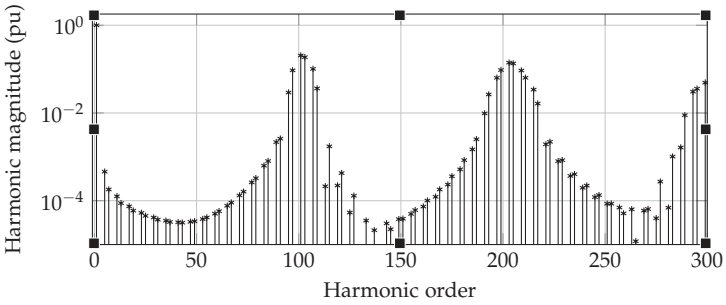


Fig. F.9: Theoretical harmonic spectra of the line-to-line output voltage of the parallel interleaved VSCs with interleaving angle of 180°, modulated using AZSPWM with modulation index of $M = 1$ and the carrier ratio (ω_c/ω_0)=51.

$$
Bmn_{AZS} = \frac{4V_{\mathrm{dc}}}{q\pi^2} \times \left(\begin{array}{l}
\frac{\pi}{6}\cos(m\frac{\pi}{2})\sin(n\frac{\pi}{2})\sin(2n\frac{pi}{3}) \\
\qquad \times \{J_n(q\frac{3\pi}{4}M) + 2\cos(\frac{n\pi}{6})J_n(q\frac{\sqrt{3}\pi}{4}M)\} \\
+ \sum\limits_{\substack{k=1 \\ k\neq -n}}^{\infty} \frac{1}{n+k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n+k]\frac{\pi}{2}\right)\sin\left([n+k]\frac{\pi}{6}\right) \\
\qquad \times \left\{J_k(q\frac{3\pi}{4}M)\sin\left([n+3k]\frac{\pi}{3}\right)\right. \\
\qquad \left. - 2\cos(n\frac{\pi}{6})\sin\left([n-3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right. \\
+ \sum\limits_{\substack{k=1 \\ k\neq n}}^{\infty} \frac{1}{n-k}\cos(m\frac{\pi}{2})\sin(k\frac{\pi}{2})\cos\left([n-k]\frac{\pi}{2}\right)\sin\left([n-k]\frac{\pi}{6}\right) \\
\qquad \times \left\{J_k(q\frac{3\pi}{4}M)\sin\left([n-3k]\frac{\pi}{3}\right)\right. \\
\qquad \left. - 2\cos(n\frac{\pi}{6})\sin\left([n+3k]\frac{\pi}{6}\right)\left\{J_k(q\frac{\sqrt{3}\pi}{4}M)\right\}\right.
\end{array} \right)
$$

(F.30)

where V_{dc} is the dc-link voltage, M is the modulation index, and $q = m + n(\omega_0/\omega_c)$. The harmonic coefficients for this case are given in (F.29) and (F.30). The expressions contain $J_y(z)$, which represents the Bessel functions of the first kind of the order y and argument z. The double summation term in (F.27) is the ensemble of all possible frequencies, formed by taking the sum and the difference between the carrier harmonics, the fundamental waveform and its associated baseband harmonics.

The theoretical closed form harmonic solution of the line-to-line voltage for the AZSPWM is obtained by using (F.29) and (F.30) and the harmonic

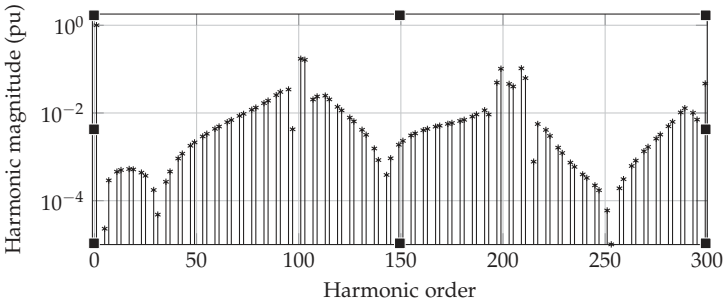


Fig. F.10: Theoretical harmonic spectra of the line-to-line output voltage of the parallel interleaved VSCs with interleaving angle of 180°, modulated using NSPWM with modulation index of $M = 1$ and the carrier ratio (ω_c/ω_0)=51.

spectrum is shown in Fig. F.9. The magnitude of the odd multiple of the carrier harmonics and the associated sideband harmonic components are very small. The major harmonic components appear at the even multiple of the carrier harmonics and its odd sideband harmonics.

The harmonic coefficients of NSPWM are also evaluated in a similar manner and the theoretical harmonic spectrum for $M = 1$ is shown in Fig. F.10. In contrast to the AZSPWM, the magnitude of the even multiple of the carrier harmonic components and its sidebands is reduced considerably. However, the roll-off in magnitude of the sideband harmonic components is slower than for the AZSPWM. The harmonic performance of both of the PWM schemes is compared by evaluating the Normalized Weighted Total Harmonic Distortion (NWTHD), which is defined as

$$\text{NWTHD} = \frac{M\sqrt{\sum_{h=2}^{\infty}(V_h/h)^2}}{V_f} \tag{F.31}$$

where V_f is the fundamental component and V_h is the magnitude of the hth harmonic component.

The NWTHD for all of the PWM schemes are shown in Fig. F.11. The resultant pole voltages of the two parallel interleaved VSCs with an interleaving angle of 180° are the same in SVM and in AZSPWM. Therefore, the NWTHD of SVM is the same as that of the AZSPWM. Similarly, the NWTHD in the case of the NSPWM in the linear modulation range ($0.769 \leq M < 2/\sqrt{3}$) is the same as the DPWM1. Although NSPWM is a discontinuous PWM scheme, it demonstrates better harmonic performance compared to the AZSPWM. Therefore, the use of the NSPWM results in a improved harmonic performance and reduced switching losses. In order to operate the

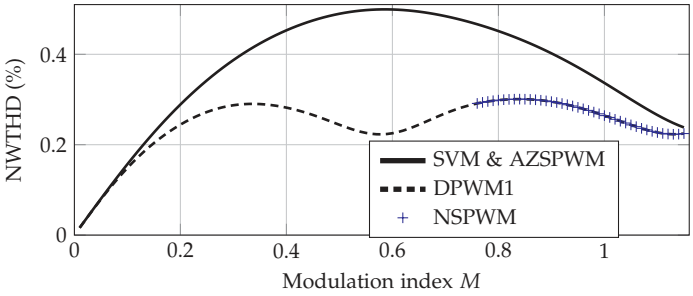


Fig. F.11: Theoretical variation of the NWTHD with a modulation index M of the parallel interleaved VSCs with an interleaving angle of 180°.

VSCs in the full modulation range, AZSPWM in the low modulation index range ($0 \leq M < 0.769$) and NSPWM in the high modulation index range ($0.769 \leq M < 2/\sqrt{3}$) can be used.

5 Design of Integrated Inductor

Design steps are illustrated by deriving design equations of an integrated inductor for an active three-phase rectifier.

5.1 Design Procedure

Design steps of an integrated inductor for an active three-phase rectifier are illustrated. The flux in the integrated inductor is highly influenced by the PWM scheme used. For the active rectifier applications, the modulation index varies in close vicinity to one. Therefore, the use of the NSPWM is considered due to its superior harmonic performance and lower switching losses. The relevant design equations are derived hereafter.

5.1.1 Value of the Line Filter Inductor

The value of a line filter inductor L_f is generally chosen to limit the peak-to-peak value of the ripple component of the resultant line current to an acceptable value. Let

$$k = \frac{\Delta I_{x,m}}{I_{x,p}} \tag{F.32}$$

where $\Delta I_{x,m}$ is the maximum value of the peak-to-peak ripple current component of the resultant line current and $I_{x,p}$ is the amplitude of the fundamental component of the resultant line current. For the NSPWM, the peak-to-peak value of the ripple current component is maximum for the modulation index

of $M = 1$ and at the reference voltage space vector angle of $\psi = 0^\circ$ [19] (and $\psi = 180^\circ$) and it is given as

$$\Delta I_{x,m} = \frac{V_{\mathrm{dc}}}{24 f_c L_f} \tag{F.33}$$

Using (F.32) and (F.33), the value of the line filter inductor can be obtained as

$$L_f = \frac{V_{\mathrm{dc}}}{24 f_c k I_{x,p}} \tag{F.34}$$

5.1.2 Maximum Flux Density in Bridge Legs

The flux density in the bridge legs is obtained using (F.8), (K.34), and (I.25) and it is given as

$$B_{bl}(t) = \frac{V_{\mathrm{dc}}(2+k)}{48 N f_c k A_{c,bl}} \cos(\psi + \gamma) \tag{F.35}$$

where $A_{c,bl}$ is the cross-section area of the bridge leg and γ is the power factor angle. For the active rectifier, γ is considered to be zero. Therefore, the flux density in the bridge leg is maximum at $\psi = 0^\circ$ and it is obtained as

$$B_{bl,m} = \frac{V_{\mathrm{dc}}(2+k)}{48 N f_c k A_{c,bl}} \tag{F.36}$$

5.1.3 Maximum Flux Density in Common Legs

Obtaining the value of the $I_{CM,c}$ form (H.21) and substituting in (F.7) yields

$$B_{cl} = \frac{\lambda_{CM}}{2 N A_{c,cl}} \tag{F.37}$$

where $A_{c,cl}$ is the cross-section area of the Common leg. Substituting the value of λ_{CM} from Table F.1 into (F.37) yields

$$B_{cl} = \frac{V_{\mathrm{dc}}}{32 N f_c A_{c,cl}} \left(3M \sin[\arccos(\frac{1}{\sqrt{3}M})] - 1 \right) \tag{F.38}$$

The flux density in the common leg is maximum for the modulation index $M = M_{max}$ and it is given as

$$B_{cl,m} = B_{cl} \mid_{M=M_{max}} \tag{F.39}$$

where M_{max} is the maximum value of the modulation index in the given operating range.

5.1.4 Maximum Flux Density in Phase Legs

Obtaining the values of the $I_{x,c}$ and $I_{CM,c}$ form (H.21) and substituting in (F.6) yields

$$\phi_{x1}(t) = \frac{1}{N} L_f I_x(t) + \frac{1}{2N} \int \Delta V_x dt \tag{F.40}$$

As evident from (K.4), the flux in the phase leg has two distinct component:

1. Resultant flux component ϕ_x.
2. Circulating flux component $\phi_{x,c}$.

The resultant flux component ϕ_x is equal to the flux through the bridge leg. ϕ_x attains its maximum value for reference voltage space vector angle $\psi = 0^\circ$ and can be readily obtained from (F.36). The circulating flux component $\phi_{x,c}$ is proportional to the $\int \Delta V_x dt$. The peak value of the $\int \Delta V_x dt$ is different in each sampling interval due to the change in the dwell times of the corresponding voltage vectors. For the NSPWM, the circulating flux component attains maximum value at the reference voltage space vector angle ψ_m and it is given as

$$\phi_{x,c_{max}} = \phi_{x,c}(t) \mid_{\psi=\psi_m} = \frac{V_{\mathrm{dc}}}{8Nf_c} \tag{F.41}$$

$$\psi_m = 120^\circ - \arcsin\left(\frac{1}{\sqrt{3}M_{min}}\right) \tag{F.42}$$

where M_{min} is the minimum value of the modulation index in the given operating range. Flux in the phase leg

$$\phi_{x1}(t) = \phi_x(t) + \phi_{x,c}(t) \tag{F.43}$$

and for the phase A, it could attain its maximum value at $\psi = 0^\circ$, $\psi = \psi_m$, or $\psi = 30^\circ$. The flux density in the phase leg at these values of the reference voltage space vector angle is given as

$$\begin{aligned} B_{A1}(t) \mid_{\psi=0^\circ} &= \tfrac{V_{\mathrm{dc}}(2+k)}{48Nf_c k A_{c,pl}} \\ B_{A1}(t) \mid_{\psi=30^\circ} &= \tfrac{V_{\mathrm{dc}}}{4Nf_c A_{c,pl}}\left(1 + \tfrac{\sqrt{3}}{2}\left[\tfrac{2+k}{12k} - M_{min}\right]\right) \\ B_{A1}(t) \mid_{\psi=\psi_m} &= \tfrac{V_{\mathrm{dc}}}{8Nf_c A_{c,pl}}\left(1 + \tfrac{2+k}{6k}\cos\psi_m\right) \end{aligned} \tag{F.44}$$

where $A_{c,pl}$ is the cross-section area of the phase leg. The maximum value of the flux density in the phase leg is obtained from (K.44) and it is given as

$$B_{pl,m} = \max(B_{A1} \mid_{\psi=0^\circ}, B_{A1} \mid_{\psi=30^\circ}, B_{A1} \mid_{\psi=\psi_m}) \tag{F.45}$$

5.1.5 Number of Turns and Cross-section Area of the Cores

Once the material for the magnetic core is chosen, value of the $B_{pl,m}$ is selected such that $B_{pl,m} < B_{sat}$, where B_{sat} is the saturation flux density. The value of the $N \times A_{c,pl}$ can be obtained using (K.44) and (F.45) and the number of turns and the cross-section area of the core is selected using this value. Once the value of the number of turns N is known, the cross-section area of the bridge legs and the common legs can be obtained using (F.36) and (F.39), respectively. The air gap cross-section can be obtained from the dimensions of the phase leg and the bridge leg. Using the value of the air gap cross-section and (G.11), the length of the air gap can be obtained.

5.2 Comparative Evaluation

The size reduction is achieved by using the integrated inductor and it is demonstrated by comparing the volume of the integrated inductor with the volume of the magnetic component of a system, which uses two separate inductors, one for the circulating current suppression and another for reducing the ripple in the line current for each of the phases, as shown in Fig. F.1.

5.2.1 Coupled Inductor

The maximum value of the product of the number of turns and the cross-section area of the core is given as

$$N_{CI} A_{c,CI} = \frac{V_{\mathrm{dc}}}{8 f_c B_{CI,m}} \tag{F.46}$$

where N_{CI} is the number of turns of each coil of the CI, $B_{CI,m}$ is the maximum permissible value of the flux density, and $A_{c,CI}$ is the cross-section area of the central leg of the CI. The cross-section area of the side legs is half than that of the central leg.

5.2.2 Line Filter Inductor

The maximum value of the product of the number of turns and the cross-section area is

$$N_{L_f} A_{c,L_f} = \frac{V_{\mathrm{dc}}(2+k)}{48 f_c k B_{L_f,m}} \tag{F.47}$$

where N_{L_f} is the number of turns in the line filter inductor, $B_{L_f,m}$ is the maximum flux density, and A_{c,L_f} is the cross-section area of the central leg of the line filter inductor.

5.2.3 Comparison

The number of turns N and the cross-section area of the phase leg $A_{c,pl}$ of the integrated inductor is taken as base values for the comparison.

For the specified modulation range (the modulation index is assumed to be $0.9(M_{min}) \leq M \leq 1.1(M_{max})$), $\psi_m = 80^\circ$ and $B_{pl,m} = B_{A1}\mid_{\psi=\psi_m}$. The maximum value of the $N \times A_{c,pl}$ is given as

$$NA_{c,pl} = \frac{V_{\text{dc}}}{8 f_c B_{pl,m}}(1 + \frac{2+k}{35k}) \tag{F.48}$$

Assuming $A_{c,pl} = A_{c,CI}$ and taking $k = 0.35$, the relationship between N and N_{CI} is obtained using (F.46) and (F.48) as it is given by

$$N = 1.19 N_{CI} \tag{F.49}$$

As coils in both the cases should be designed to carry the same current, it is evident from (F.49) that for the $A_{c,pl} = A_{c,CI}$, the volume of the winding material in the integrated inductor is 19% higher than that of the CI. However, the separate inductor based solution requires additional coils for the line filter inductor, which should be designed to carry the rated current.

Assuming $B_{L_f,m} = B_{pl,m}$ and using (F.47) and (F.48), the relationship between the parameters of the separate line filter inductor and the integrated inductor is derived as

$$\frac{N_{L_f} A_{c,L_f}}{N A_{c,pl}} = 0.94 \tag{F.50}$$

Taking $N_{L_f} = 0.67N$ gives

$$A_{c,L_f} = 1.4 A_{c,pl} \tag{F.51}$$

For the given value of the M_{max}, the maximum value of the $N \times A_{c,cl}$ can be obtained using (F.38) and (F.39) and it is given as

$$NA_{c,cl} = \frac{1.8 V_{\text{dc}}}{32 f_c B_{cl,m}} \tag{F.52}$$

Assuming $B_{cl,m} = B_{pl,m}$ and using (F.48) and (F.52), the relationship between the cross-section area of the common leg and the cross-section area of the phase leg is obtained as

$$A_{c,cl} = 0.4 A_{c,pl} \tag{F.53}$$

Therefore, the total cross-section area of both of the common legs is 80% of the cross-section area of a phase leg. Using (F.36) and (F.48), the relationship between the $A_{c,bl}$ and the $A_{c,pl}$ is obtained as

$$A_{c,bl} = 0.94 A_{c,pl} \tag{F.54}$$

Table F.4: Parameters for the simulations and the experimental studies

Parameters	Values
Power	3 KVA
DC-link voltage V_{dc}	650 V
Switching frequency f_c	4.95 kHz
Line filter inductance L_f	2.4 mH
Circulating current inductance L_c	94 mH
Interleaving angle	180°

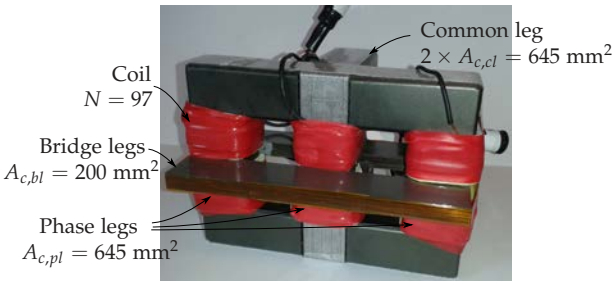


Fig. F.12: Image of the implemented integrated inductor.

Using these derivations, the volume of the proposed integrated inductor is compared with the state-of-the-art filter arrangement. The maximum value of the flux density of the magnetic cores and the current density are taken to be the same in both the cases. In this scenario, the integrated inductor results in 39% saving in copper and 35% reduction in the magnetic material.

6 Simulation and Experimental Results

6.1 Simulation Study

The system parameters that are used for the simulations and the experimental studies are listed in Table K.3. The phase legs and the common legs of the integrated inductor are realized using three U shape (0R49925UC) and one I shape (0R49925IC) ferrite cores from Magnetics, as shown in Fig. F.12. Instead of using two common legs with the cross-section area of $A_{c,cl}$, single common leg having the cross-section area of $2 \times A_{c,cl}$ is used. The bridge legs are realized using the laminated steel block. The implemented inductor and the inductor shown in Fig. H.2(a) are magnetically equivalent and the use of the inductor shown in Fig. F.12 does not impair the significance of the analysis and the obtained experimental results.

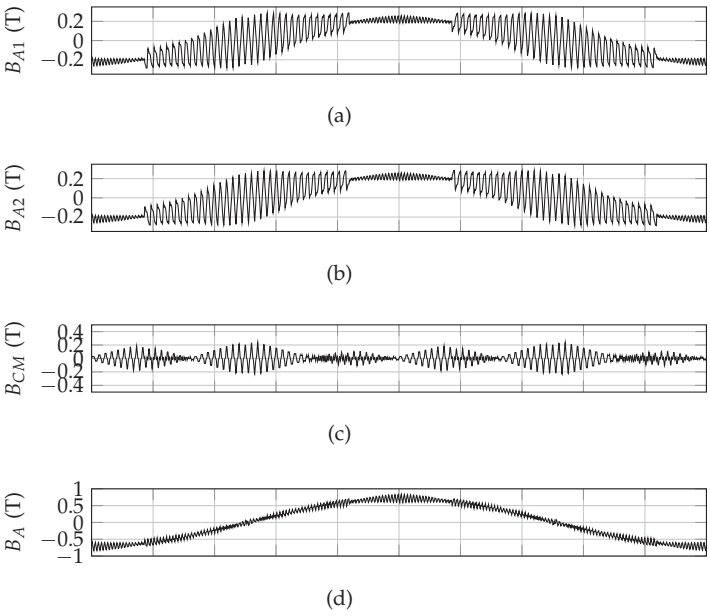


Fig. F.13: NSPWM: Flux density waveforms for modulation index of $M = 1$. (a) Flux density in the upper part of the phase leg, (a) Flux density in the lower part of the phase leg, (c) Flux density in the common leg, (d) Air gap flux density.

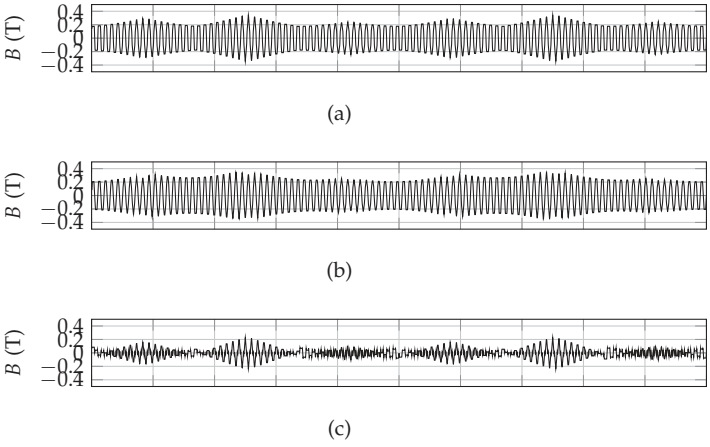
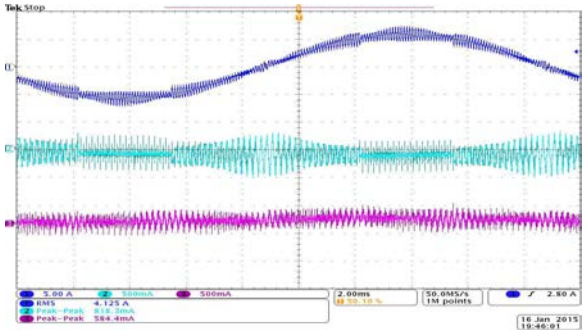
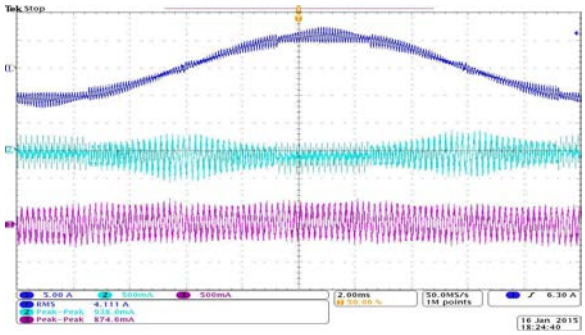


Fig. F.14: Flux density in the common leg for $M = 1$. (a) SVM, (b) DPWM1, (c) AZSPWM.

Time domain simulations have been carried out using PLECS. The flux



(a)

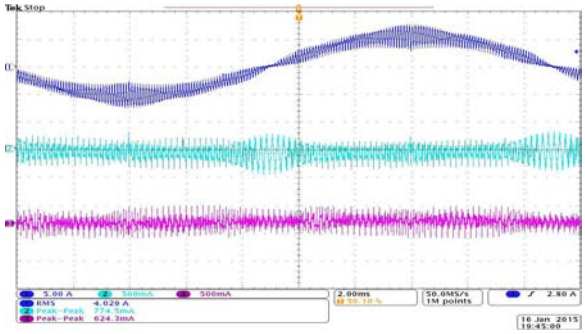


(b)

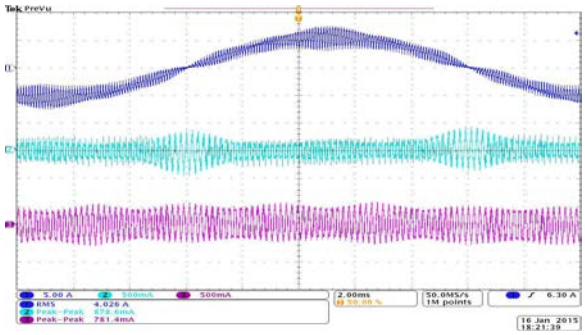
Fig. F.15: Measured currents at modulation index of $M = 1$. Ch1: Phase A line current (5 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (0.5 A/div), Ch3: CM circulating current ($I_{A1} + I_{B1} + I_{C1} = 3 \times I_{CM,c}$) (0.5 A/div). (a) NSPWM, (b) DPWM1.

density in the various parts of the integrated inductor in the case of the NSPWM, are shown in Fig. F.13. The fundamental frequency component of the flux density in both the upper and the lower part of the phase legs is the same. Whereas, the circulating flux component has the same magnitude but opposite polarity, as shown in Fig. F.13(a) and F.13(b). The flux density in the air gap (which is the same as the flux density in the bridge leg) has predominant fundamental frequency component, as shown in Fig. F.13(d).

The flux density waveform in the common leg for the different PWM schemes is shown in Fig. F.14 for the modulation index $M = 1$. The use of both the SVM and the DPWM1 results in the maximum value of the B_{CM} close to 0.35 T. On the other hand, the maximum value of the B_{CM} is 0.25 T in the case of the NSPWM. The use of the AZSPWM results in a maximum value of the B_{CM} to be 0.22 T.



(a)



(b)

Fig. F.16: Measured currents at modulation index of $M = 1$. Ch1: Phase A line current (5 A/div), Ch2: Phase A circulating current ($2 \times I_{A,c}$) (0.5 A/div), Ch3: CM circulating current ($I_{A1} + I_{B1} + I_{C1} = 3 \times I_{CM,c}$) (0.5 A/div). (a) AZSPWM, (b) SVM.

6.2 Hardware Results

The PWM schemes are realized by the scalar implementation using TMS320F28346 floating-point digital signal processor. The output terminals are connected to a three-phase resistive load of 53 Ω. The line current I_x, the circulating current $I_{x,c}$, and the CM circulating current $I_{CM,c}$ for the NSPWM and the AZSPWM are shown in Fig. F.15(a), and F.16(a), respectively. It is evident from these results that the integrated inductor offers the desired inductance to the line current and also suppresses the circulating current. The current waveforms for the DPWM1 is shown in Fig. F.15(b). From Fig. F.15, it is clear that the resultant line current I_x and the circulating current $I_{x,c}$ are similar in case of the NSPWM and the DPWM1. However, the CM circulating current $I_{CM,c}$ in the case of the NSPWM is very small compared to that of the DPWM1. Similarly, the line current quality in the case of the AZSPWM and

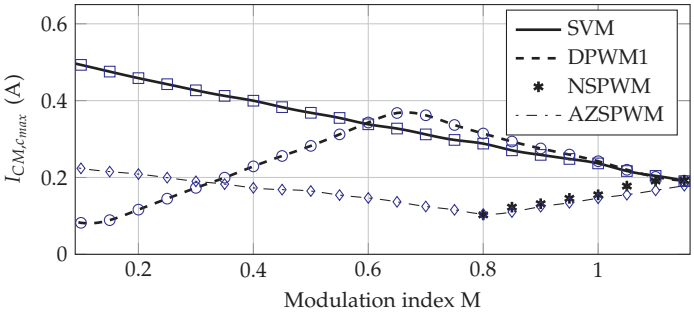


Fig. F.17: Measured maximum values of the CM circulating current over a fundamental cycle as a function of the modulation index. For the NSPWM, the values are plotted only for the linear modulation range of $0.769 \leqslant M \leqslant 1.154$.

the SVM is the same, as it is evident form Fig. F.16. However, the use of the AZSPWM would result in less CM circulating current compared to that of the SVM.

It has been analytically shown that the peak value of the CM flux can be reduced by using the NSPWM and the AZSPWM. This has been verified by measuring the sum of the currents of all the three phases of the first VSC. As defined in (F.4), the sum of the currents of all the three phases of the first VSC is equal to the $3I_{CM,1}$. Since $I_{CM,2} = -I_{CM,1}$, substituting this in (G.2) yields

$$I_{A1} + I_{B1} + I_{C1} = 3I_{CM,1} = 3I_{CM,c} \tag{F.55}$$

Using (F.22), (F.23), and (F.55) the sum of the currents of all the three phases of the first VSC is obtained as

$$I_{A1} + I_{B1} + I_{C1} = \frac{4\Re_L}{N^2}\lambda_{CM} \tag{F.56}$$

As the sum of the current of all the three phases of the first VSC is proportional to the CM flux, set of readings of this value were obtained with the dc-link voltage of 325 V and a resistive load of 27 Ω. The dc-link voltage value is reduced to half to obtain these sets of readings, as the use of the SVM at the low modulation indices with the rated dc-link voltage causes the saturation of the designed integrated inductor due high CM flux (as analyzed in this paper and shown in Fig. F.7). The variation of the maximum value of the CM circulating current with the modulation index is shown in Fig. F.17, which is in a good agreement with the analysis presented in a section III.

It has been analytically shown in section IV that the AZSPWM is harmonically equivalent to the SVM. Similarly, it is also established that the harmonic performance of the NSPWM is same as that of the DPWM1. This has been demonstrated by evaluating the NWTHD of the resultant line-to-line voltage

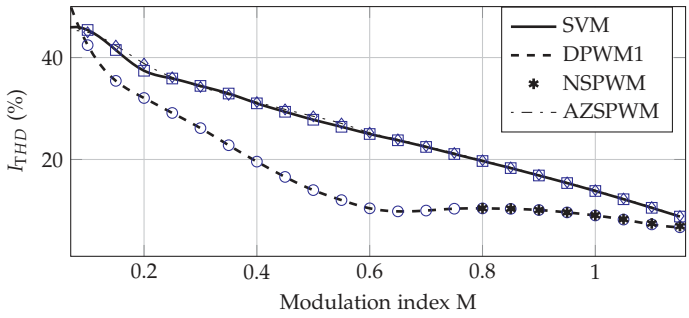


Fig. F.18: Measured total harmonic distortion of the resultant line current as a function of the modulation index. For the NSPWM, the values are plotted only for the linear modulation range of $0.769 \leqslant M \leqslant 1.154$.

($V_{A'B'}$) using the analytical expressions of the harmonic coefficients A_{mn} and B_{mn}. However, A' and B' are the fictitious terminals and not available for measurement (refer Fig. F.3). Therefore, the harmonic performance of the PWM scheme has been indirectly verified by measuring the total harmonic distortion of the resultant line current. The variation of the total harmonic distortion of the resultant line current as a function of the modulation index is shown in Fig. F.18. For any given modulation index, the I_{THD} values for the AZSPWM closely matched with that of the SVM. Similarly, the harmonic performance of NSPWM in its linear modulation range is the same as that of the DPWM1. It is also clear from Fig. F.18 that the NSPWM and the DPWM1 are harmonically superior than the AZSPWM and the SVM, which is in agreement with the NWTHD results shown in Fig. F.11.

7 Conclusion

In this paper, the integrated inductor for the parallel interleaved VSCs is presented. The proposed inductor combines the functionality of both the line filter inductor and the circulating current filter inductor. A five leg magnetic structure is proposed, where the outer two legs provide low reluctance path for the CM flux. A PWM scheme, which employs AZSPWM in the low modulation index range ($0 \leq M < 0.769$) and NSPWM in the high modulation index range ($0.769 \leq M < 2/\sqrt{3}$) is analyzed for the parallel interleaved VSCs. It reduces the maximum value of the CM flux-linkage by 68 % compared to that of the SVM and 52 % compared to that of the DPWM1. The harmonic performance of the NSPWM and the AZSPWM for the parallel interleaved VSCs is also analyzed and it is established that the magnitude of the harmonic frequency components in the NSPWM is the same as that of

the DPWM1 for an interleaving angle of 180°. Similarly, the harmonic performance of the AZSPWM is the same as that of the SVM. Therefore, the use of the NSPWM and the AZSPWM result in flux reduction in the common legs of the integrated inductor, without compromising the harmonic performance.

Procedure for designing the integrated inductor is also presented. The design equations are derived for the active three-phase rectifier application. The volume of the magnetic core and the copper of the proposed integrated inductor is compared with the converter system, having separate CI and the line filter inductor for each of the phases. When used with the NSPWM, the integrated leads to 35% reduction in magnetic core and 39% saving in copper.

References

[1] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[2] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[3] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[4] H. Akagi, A. Nabae, and S. Atoh, "Control strategy of active power filters using multiple voltage-source PWM converters," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 3, pp. 460–465, 1986.

[5] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[6] B. Cougo, T. Meynard, and G. Gateau, "Parallel three-phase inverters: Optimal pwm method for flux reduction in intercell transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug 2011.

[7] J. Ewanchuk and J. Salmon, "Three-limb coupled inductor operation for paralleled multi-level three-phase voltage sourced inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1979–1988, 2013.

[8] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[9] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Modified discontinuous pwm for size reduction of the circulating current filter in parallel interleaved converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3457–3470, July 2015.

[10] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, April 2013.

[11] G. Oriti, A. Julian, and T. Lipo, "A new space vector modulation strategy for common mode voltage reduction," in *Proc. of 28th Annual IEEE Power Electronics Specialists Conference*, vol. 2, Jun 1997, pp. 1541–1546 vol.2.

[12] Y.-S. Lai and F.-S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part i: basic development," *IEEE Trans. Ind. Appl.*, vol. 40, no. 6, pp. 1605–1612, 2004.

[13] Y.-S. Lai, P.-S. Chen, H.-K. Lee, and J. Chou, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part ii: applications to im drives with diode front end," *Ind. Appl., IEEE Trans. on*, vol. 40, no. 6, pp. 1613–1620, 2004.

[14] W. Hofmann and J. Zitzelsberger, "PWM-control methods for common mode voltage minimization - a survey," in *Proc. International Symposium on Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006.*, 2006, pp. 1162–1167.

[15] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 469–476, 1999.

[16] A. Hava and E. Un, "A high-performance PWM algorithm for common-mode voltage reduction in three-phase voltage source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1998–2008, 2011.

[17] E. Un and A. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 782–793, 2009.

[18] A. Hava and N. Cetin, "A generalized scalar pwm approach with easy implementation features for three-phase, three-wire voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1385–1395, May 2011.

[19] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

Paper G

Integrated Inductor for Interleaved Operation of Two Parallel Three-phase Voltage Source Converters

Ghanshyamsinh Gohil,
Lorand Bede, Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been published in the
in Proc. 17th European Conference on Power Electronics and Applications, EPE'15
ECCE-Europe, pp. 1-10, Sept 2015.

The layout has been revised.

Abstract

This paper presents an integrated inductor for two parallel interleaved Voltage Source Converters (VSCs). Interleaving of the carrier signals leads to improvement in the harmonic quality of the resultant output voltage and the line current filtering requirements can then be reduced. However, the instantaneous potential difference, caused by the interleaved carriers, may drive large circulating current between the parallel VSCs and an additional inductor is often placed in the circulating current path to suppress the current to an acceptable limit. Integration of both line filter inductor and circulating current filter inductor is proposed. The flux in the magnetic structure is analyzed and the values of the line filter inductance and circulating current filter inductance are derived. Steady-state and the transient performance of the system has been verified by means of simulation and experimental results.

1 Introduction

Three-phase two-level pulsewidth modulated Voltage Source Converter (VSC) is widely used in many industrial and renewable energy applications. This converter is often realized using a Si Insulated Gate Bipolar Transistor (IGBT). The VSC, with an IGBT as a switching device, suffers from excessive losses if the switching frequency is increased beyond few kHz. Due to the limited switching frequency, large line filter components are generally employed to comply with the power quality requirements. In many high power applications, several VSCs are connected in parallel to achieve the desired power/current level [1]. These parallel connected VSCs can be operated with interleaved carrier signals and multi-level voltage waveforms can be achieved.

As a result of the interleaved carriers, the switched output voltages (referred as a pole voltage hereafter) of the parallel VSC legs are phase shifted. As a result, some of the harmonic frequency components that are present in the individual pole voltages of the parallel VSC legs are also phase shifted and their contribution in the resultant output voltage is fully/partly canceled [2–5]. The improvement in the harmonic quality of the resultant output voltage leads to reduction in the line current filtering requirements. However, the difference of the phase shifted harmonic components of the pole voltages appears across the closed path and drives the circulating current between the parallel VSCs.

The flow of the circulating current between parallel VSCs increases the losses and leads to unnecessary over-sizing of the components present in the circulating current path. Therefore, it should be suppressed to an acceptable limits. An inductive component is often used, which offers high impedance to the phase shifted harmonic component of the pole voltages and thereby suppressing the circulating current. One of the ways to achieve this is to

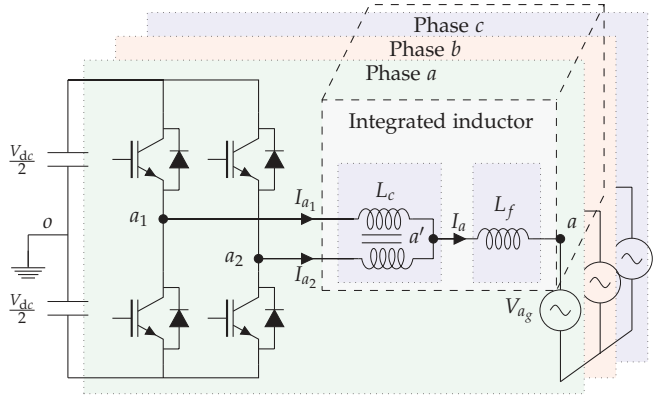


Fig. G.1: Two parallel interleaved voltage source converters with a common dc-link. Circulating current is suppressed by inductor L_c and the line filter inductor L_f provides desired inductance for line current filtering. Proposed integrated inductor combines the functionalities of both the L_c and L_f of all three phases.

provide a strong magnetic coupling between the parallel VSC legs [3, 6–9], as shown in Fig. G.1. The system with parallel interleaved VSCs uses two distinct inductive components:

1. Line filter inductor (L_f) for improving the injected line current quality.
2. An inductor (L_c) for suppressing the circulating current.

The advantage offered in terms of the size reduction of the line filter component is somewhat offset by the introduction of the additional circulating current inductor. The volume of these inductive components can be reduced by integrating the functionalities of both the line filter inductor and the circulating current inductor. Moreover, the size of the magnetic component can be further reduced by integrating the inductors of all three phases in a single magnetic structure.This paper proposes such integrated inductor for two parallel connected VSCs.

2 Parallel Interleaved Voltage Source Converters

Two parallel VSCs with the common dc-link is shown in Fig. G.1. The carrier signals of these parallel VSCs are interleaved by an interleaving angle of 180°. The harmonic performance of the switched output voltage and the behavior of the circulating current is significantly influenced by the Pulse Width Modulation (PWM) scheme used [10, 11]. Therefore, the PWM scheme is briefly discussed hereafter.

A 60° discontinuous modulation (commonly referred to as a DPWM1) is

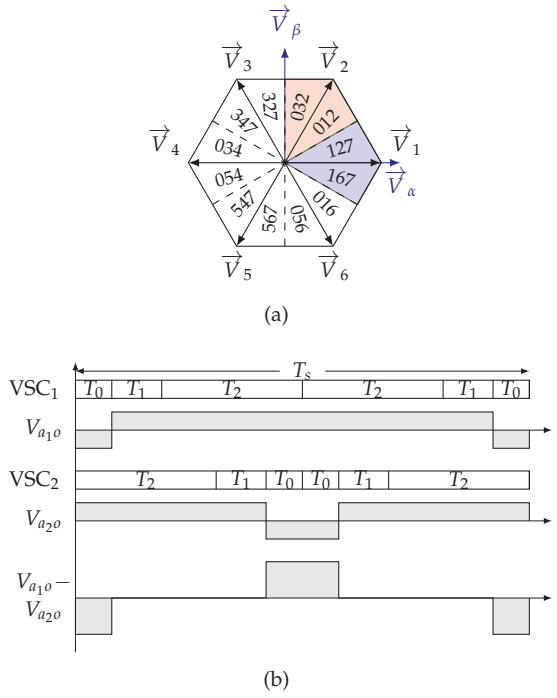


Fig. G.2: Pulse width modulation scheme and the pole voltages of the parallel voltage source converters. (a) Switching sequences used in the DPWM1. The numbers represent the corresponding voltage vectors, (b) Pole voltages of phase a of both the parallel voltage source converters for the modulation index $M = 1$ and voltage space vector angle $\psi = 45^\circ$. The interleaving angle is 180°.

used to modulate the parallel VSCs. Each VSC leg remains clamped to the dc bus for one third period (120°) of the fundamental cycle. This clamping interval is divided into two sub-intervals of 60° each and the voltage vectors are selected to arrange these sub-intervals around the positive and the negative peak of the reference voltage waveform, as shown in Fig. G.2(a). For the unity power factor applications, the switching of the semiconductor device is avoided when the current through that device is near its peak value. In this manner, the switching losses can be reduced up to 50% compared to that of the continuous space vector modulation scheme. In addition, for the symmetrical interleaving, the use of the DPWM1 results in a better harmonic performance compared to the continuous space vector modulation scheme [5, 10].

The pole voltages of both the VSCs are shown in Fig. G.2(b). These pole voltages have the same average value. However, due to the interleaved car-

riers, these pole voltages are phase shifted. Therefore, there exist an instantaneous potential difference, which appears across the closed path formed due to the interleaved carriers and the parallel connection. The potential difference of the pole voltages for a particular switching interval is also shown in Fig. G.2(b). This potential difference drives a circulating current and the integrated inductor is used to suppress this current.

3 Integrated Inductor

A magnetic structure and the analysis of the integrated inductor is presented in this section.

3.1 Magnetic Structure

An integrated three-phase inductor, which combines the functionalities of the circulating current filter inductor and the three-phase line filter inductor, is proposed. The magnetic structure of the proposed inductor is shown in Fig. G.3(a). The flux components corresponding to each of the phases can be made balance by using the symmetrical magnetic structure. The magnetic core is composed of three outer legs (referred to as a phase leg), a common leg and three bridge legs between the phases (referred to as a bridge leg). The phase leg receives both the coils of that phase. The number of turns are the same in all the coils. However, the coils corresponding to VSC_2 are wound in opposite direction than the coils of the VSC_1. The starting terminals of both the coils of a particular phase are connected to the respective output terminals of the corresponding parallel VSC legs (starting terminals of the coils of phase a are connected to the a_1 and a_2), whereas ending terminals of both the coils are connected to the common connection point (a). A high permeability material is used for the phase legs and the common leg, whereas the bridge legs are realized using the laminated iron core and the necessary air gap has been inserted in each of the bridge legs.

3.2 Simplified Reluctance Model

A simplified reluctance model of the integrated inductor is shown in Fig. G.3(b). The permeability of the magnetic material is assumed to be constant and the flux is assumed to be confined to the magnetic core (flux leakage is neglected). Each of the coils is represented by an equivalent magneto-motive force, which is equal to the product of the number of turns N and the current flowing through that coil. Each phase leg comprises a limb and two yokes. The reluctance of half of the limb is taken as $\Re_L$. The reluctance of each yoke is termed as $\Re_Y$. The series connection of the reluctance of the half of the limb ($\Re_L$) and the reluctance of the yoke ($\Re_Y$) is represented by the equivalent

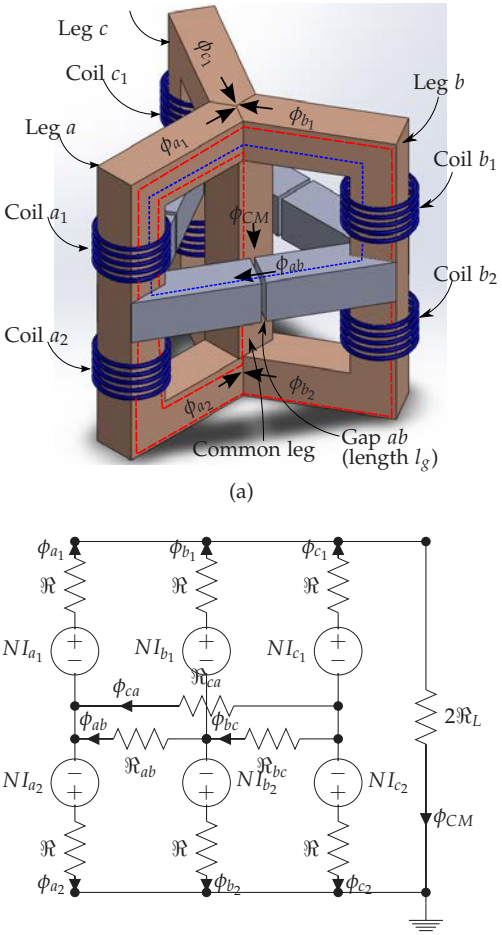


Fig. G.3: Three phase integrated inductor. (a) Magnetic structure, (b) Simplified reluctance model.

reluctance $\Re$ ($\Re = \Re_L + \Re_Y$). The equivalent reluctance of each of the bridge leg is the sum of the reluctance of the magnetic material of that bridge leg and the effective reluctance of an air gap ($\Re_{ab} = \Re_{ab_s} + \Re_{g'}$). The reluctance of the laminated steel core is very small compared to the reluctance of the air gap $\Re_{g'}$. Therefore, the reluctance of each bridge leg is approximated as $\Re_{g'}$.

By solving the reluctance network, the flux linking with the respective

coils of the phase x is given as

$$\begin{aligned}\phi_{x_1} &= \frac{3}{2(3\Re + 2\Re_{g'})}N(I_{x_1} + I_{x_2}) + \frac{1}{2\Re}N(I_{x_1} - I_{x_2}) - \frac{3}{8\Re}N(I_{CM,1} - I_{CM,2}) \\ \phi_{x_2} &= \frac{3}{2(3\Re + 2\Re_{g'})}N(I_{x_1} + I_{x_2}) - \frac{1}{2\Re}N(I_{x_1} - I_{x_2}) + \frac{3}{8\Re}N(I_{CM,1} - I_{CM,2})\end{aligned} \tag{G.1}$$

where x is a subscript, which represents phases a, b, and c and $I_{CM,n}$ is the the Common Mode (CM) current of the nth VSC and it is defined as

$$I_{CM,n} = \frac{I_{a_n} + I_{b_n} + I_{c_n}}{3} \tag{G.2}$$

The flux in the common leg and the bridge leg between the phase leg a and the phase b are given as

$$\phi_{CM} = \frac{3}{8\Re_L}N(I_{CM,1} - I_{CM,2}) \text{ and } \phi_{ab} = \frac{1}{3\Re + 2\Re_{g'}}N(I_a - I_b) \tag{G.3}$$

For the parallel interleaved VSCs, the leg current can be decomposed into two distinct components

1. Resultant line current component .
2. Circulating current component.

Assuming equal current sharing between the VSCs, the leg current can be given as

$$I_{x_1} = \frac{I_x}{2} + I_{x,c} \text{ and } I_{x_2} = \frac{I_x}{2} - I_{x,c} \tag{G.4}$$

where, I_x is the resultant line current and $I_{x,c}$ is the circulating current component. Using (J.2), the circulating current can be obtained as

$$I_{x,c} = \frac{I_{x_1} - I_{x_2}}{2} \tag{G.5}$$

Using (G.2) and (H.27), the difference of the CM currents of the VSCs can be obtained. Since, $I_a + I_b + I_c = 0$, the CM circulating current is given as

$$I_{CM,c} = \frac{I_{CM,1} - I_{CM,2}}{2} = \frac{I_{a,c} + I_{b,c} + I_{c,c}}{3} \text{ where } n = 1, 2 \tag{G.6}$$

Using (G.1), (H.27), and (G.6) the voltage across the coils are given as

$$\begin{aligned}V_{a_1a} &= V_{a_1o} - V_{ao} = -N\frac{d\phi_{x_1}}{dt} \\ &= -\frac{3N^2}{2(3\Re + 2\Re_{g'})}\frac{dI_x}{dt} - \frac{N^2}{\Re}\frac{dI_{x,c}}{dt} + \frac{3N^2}{4\Re}\frac{dI_{CM,c}}{dt}\end{aligned} \tag{G.7}$$

$$\begin{aligned}V_{a_2a} &= V_{a_2o} - V_{ao} = -N\frac{d\phi_{x_2}}{dt} \\ &= -\frac{3N^2}{2(3\Re + 2\Re_{g'})}\frac{dI_x}{dt} + \frac{N^2}{\Re}\frac{dI_{x,c}}{dt} - \frac{3N^2}{4\Re}\frac{dI_{CM,c}}{dt}\end{aligned} \tag{G.8}$$

3.3 Line Filter Inductor L_f

Averaging of the (G.7) and (G.8) yields

$$V_{a'o} - V_{ao} = -\frac{3N^2}{2(3\Re + 2\Re_{g'})}\frac{dI_x}{dt}, \text{ where } V_{a'o} = \frac{V_{a_1o} + V_{a_2o}}{2} \tag{G.9}$$

As shown in Fig. G.1, voltage $V_{a'o} - V_{ao}$ appears across the line filter inductor L_f. Therefore, from (G.9) the value of the line filter inductor is obtained as

$$L_f = \frac{3N^2}{4\Re_{g'} + 6\Re} \approx \frac{3N^2}{4\Re_{g'}} \tag{G.10}$$

Let the length of the air gap be l_g and the effective cross-sectional area of the air gap after considering the effects of the fringing flux be $A_{g'}$. The effective cross-sectional area of the air gap $A_{g'}$ is obtained by evaluating the cross-section area of the air gap after adding l_g to each dimension in the cross-section. Then (K.34) can be rewritten as

$$L_f \approx \frac{3\mu_0 N^2 A_{g'}}{4l_g} \tag{G.11}$$

3.4 Circulating Current Inductor L_c

The difference in the pole voltages of the corresponding phase drives the circulating current between the parallel VSC legs (VSC_1 and VSC_2) of that phase. This current is suppressed by inserting the inductance L_c in the circulating current path. For the proposed integrated inductor, the circulating current is described as

$$\begin{bmatrix} \Delta V_a \\ \Delta V_b \\ \Delta V_c \end{bmatrix} = \frac{N^2}{2\Re}\begin{bmatrix} 3 & -1 & -1 \\ -1 & 3 & -1 \\ -1 & -1 & 3 \end{bmatrix} \times \frac{d}{dt}\begin{bmatrix} I_{a,c} \\ I_{b,c} \\ I_{c,c} \end{bmatrix} \tag{G.12}$$

where $\Delta V_x = V_{x_1o} - V_{x_2o}$. As given in (H.21), the value of the L_c is independent of the air gap geometry and only depends on the value of the reluctance of the half of the limb ($\Re_L$) and the reluctance of the yoke ($\Re_Y$). The inductance offered to the circulating current can be increased by reducing the value of the $\Re$, which can be realized using a high permeability material for the phase legs and the common leg.

4 Design and Performance Comparison

The maximum value of the flux density in various parts of the integrated inductor is derived in this sub section.

4.1 Maximum Flux Density in Bridge Legs

Using (G.3) and (K.34), the flux in the bridge leg is given as

$$\phi_{ab} = \frac{2L_f}{3N}(I_a - I_b) \tag{G.13}$$

Normally the value of the L_f is chosen to limit the switch current ripple to the desired value. Let β be the ratio of the maximum switch current ripple to the rms value of the line current ($\beta = \Delta I_{x,max}/I_{x,rms}$). For the parallel interleaved VSCs with the interleaving angle of 180° and modulated using the DPWM1, the switch current ripple is maximum for $M = 1$ and for voltage space vector angle of $\psi = 0°$ [2]. The maximum switch current ripple is given as

$$\Delta I_{x,max} = \beta I_{x,rms} = \frac{V_{\mathrm{dc}}}{24 f_c L_f} \tag{G.14}$$

Substituting the value of L_f and $I_a - I_b$ in (G.13) yields

$$\phi_{ab} = \frac{\sqrt{6}V_{\mathrm{dc}}}{36 N f_c \beta}\cos(\psi + \theta + 30°) \tag{G.15}$$

where θ is the displacement power factor angle. Let, $A_{c,bl}$ be the cross section area of the bridge leg, the maximum value of the flux density in the bridge leg is given as

$$B_{bl,max} = \frac{V_{\mathrm{dc}}}{6\sqrt{6} N f_c \beta A_{c,bl}} \tag{G.16}$$

4.2 Maximum Flux Density in Common Leg

Obtaining the circulating current values from (H.21) and substituting in (G.3) yields

$$\phi_{CM} = \frac{3\Re}{2\Re_l N}\int (V_{CM,1} - V_{CM,2})dt \tag{G.17}$$

The flux in the common leg is proportional to the time integral of the CM voltage difference. The peak value of the $\int (V_{CM,1} - V_{CM,2})dt$ is different in every switching intervals. The maximum value out of these peak values for a given modulation index is given as

$$\int (V_{CM,1} - V_{CM,2})dt = \begin{cases} \frac{MV_{\mathrm{dc}}}{4f_c}, & 0 \leqslant M < \frac{2}{3} \\ \frac{V_{\mathrm{dc}}}{f_c}\left[\frac{1}{3} - \frac{M}{4}\cos\left(60° - \arcsin(\frac{1}{\sqrt{3}M})\right)\right], & \frac{2}{3} \leqslant M < \frac{2}{\sqrt{3}} \end{cases} \tag{G.18}$$

Over the entire modulation range, $\int (V_{CM,1} - V_{CM,2})dt$ achieves maximum value at $M = 2/3$ and the maximum value of the flux density in the common

leg is given as

$$B_{CM,max} = (1 + \frac{L_y}{L_l}) \frac{V_{\mathrm{dc}}}{4Nf_c A_{c,cl}} \tag{G.19}$$

where $A_{c,cl}$ is the cross section area of the common leg. L_y and L_l are the mean magnetic length of the yoke and the half of the limb, respectively. It should be noted that the flux density in the common leg is maximum for $M = 2/3$. However, in many grid connected applications, the grid voltage could vary over a range of 1 ± 0.1 pu. This results in modulation index range as $0.9 \leq M \leq 1.1$. For such systems, the flux density in the common leg is maximum for $M = 0.9$ and it is given as

$$B_{CM,max} \mid_{M=0.9} = (1 + \frac{L_y}{L_l}) \frac{V_{\mathrm{dc}}}{5.466Nf_c A_{c,cl}} \tag{G.20}$$

4.3 Maximum Flux Density in Phase Leg

Obtaining the circulating current values from (H.21) and substituting it in (G.1) yields

$$\phi_{a_1}(t) = \frac{3N}{6\Re + 4\Re_{g'}} I_a(t) + \frac{1}{2N} \int \Delta V_a dt \tag{G.21}$$

Substituting the values of the $\Re_{g'}$ and I_a into (G.17)

$$\phi_{a_1}(t) = \frac{(\sqrt{2} + \frac{\beta}{2}) V_{\mathrm{dc}}}{24Nf_c\beta} \cos(\psi + \theta) + \frac{1}{2N} \int \Delta V_a dt \tag{G.22}$$

As it is evident from (G.22), the flux in the phase leg has two distinct components:

1. Resultant flux component $\phi_{x,r}$.
2. Circulating flux component $\phi_{x,c}$.

The displacement power factor angle is zero ($\theta = 0$) for the unity power factor applications. In this case, the resultant flux component $\phi_{x,r}$ attains its maximum value at $\psi = 0^\circ$ and it is given as

$$\phi_{a,r_{max}} = \phi_{a,r}(t) \mid_{\psi=0^\circ} = \frac{(\sqrt{2} + \frac{\beta}{2}) V_{\mathrm{dc}}}{24Nf_c\beta} \tag{G.23}$$

The circulating flux component $\phi_{x,c}$ is proportional to the $\int \Delta V_a dt$ and the peak value of the $\int \Delta V_a dt$ is different in every sampling interval due to the change in the dwell times of the voltage vector. Let the maximum value out of these peak values be λ_{max} and it is given as

$$\lambda_{max} = \begin{cases} \frac{\sqrt{3}M}{4f_c} V_{\mathrm{dc}}, & 0 \leq M < 1/\sqrt{3} \\ \frac{1}{4f_c} V_{\mathrm{dc}}, & 1/\sqrt{3} \leq M < 2/\sqrt{3} \end{cases} \tag{G.24}$$

For the grid connected applications ($0.9 \leq M \leq 1.1$), the circulating flux component $\phi_{x,c}$ is maximum for the space vector angle ψ_{max} and it is given as

$$\phi_{a,c_{max}} = \phi_{a,c}(t) \mid_{\psi=\psi_{max}} = \frac{V_{\mathrm{dc}}}{8Nf_c} \tag{G.25}$$

and the voltage space vector angle at which this value is achieved is given as

$$\psi_{max} = 120^\circ - \arcsin(\frac{1}{\sqrt{3}M}) \tag{G.26}$$

The flux in the phase leg is the addition of the $\phi_{a,r}(t)$ and $\phi_{a,c}(t)$ and the $\phi_{a_1}(t)$ could attain its maximum value at $\psi = 0^\circ$, $\psi = 30^\circ$, or $\psi = \psi_{max}$. The values of the flux density in the phase leg at those voltage space vector angles are given in Table K.2. The maximum value out of these values is used for choosing the cross section area of the phase leg.

Table G.1: Values of the flux density in the phase leg for different voltage space vector angles

Value	Condition
$B_{a_1}(t) \mid_{\psi=0^\circ} = \frac{(\sqrt{2}+\frac{\beta}{2})V_{\mathrm{dc}}}{24Nf_c\beta A_{c,pl}}$	$\psi = 0^\circ$
$B_{a_1}(t) \mid_{\psi=30^\circ} = \frac{\sqrt{3}(\sqrt{2}+\frac{\beta}{2})V_{\mathrm{dc}}}{48Nf_c\beta A_{c,pl}} + \frac{V_{\mathrm{dc}}}{4Nf_cA_{c,pl}}(1 - \frac{\sqrt{3}}{2}M_{min})$	$\psi = 30^\circ$
$B_{a_1}(t) \mid_{\psi=\psi_{max}} = \frac{(\sqrt{2}+\frac{\beta}{2})V_{\mathrm{dc}}}{24Nf_c\beta A_{c,pl}} \cos\psi_{max} + \frac{V_{\mathrm{dc}}}{8NA_{c,pl}f_c}$	$\psi = \psi_{max}$

5 Simulation and Experimental Results

Time domain simulations and experimental studies have been carried out for the two parallel interleaved VSCs with an interleaving angle of 180°. The total power rating of the system is 3.3 kVA. The switching frequency is taken to be 4.95 kHz. The converter system is connected to the 400V grid and the dc-link voltage is set to 650 V. The fundamental component of the line current is shared equally between the two VSCs. The integrated inductor is designed using the area-product approach to offer the line filter inductance $L_f = 3.8$ mH ($\beta = 0.3$) and the parameters of the inductor are given in Table G.2. The phase legs and the common leg are made up from ferrite, whereas laminated steel is used for the bridge legs.

5.1 Simulation Results

Simulation results for both the steady-state and the transient conditions are discussed in this sub section.

Table G.2: Design parameters of the Integrated Inductor

Parameters	Values
Cross-section area of the phase leg $A_{c,pl}$	6.45×10^{-4} m^2
Cross-section area of the common leg $A_{c,cl}$	6.45×10^{-4} m^2
Cross-section area of the bridge leg $A_{c,bl}$	2×10^{-4} m^2
Length of the air gap l_g	5×10^{-4} m
Number of turns N	97

5.1.1 Steady-state Considerations

Simulated flux density waveforms in the various parts of the magnetic structure of the integrated inductor are shown in Fig. I.14.

Fig. G.4(a) shows the flux density waveform in the upper limb of one

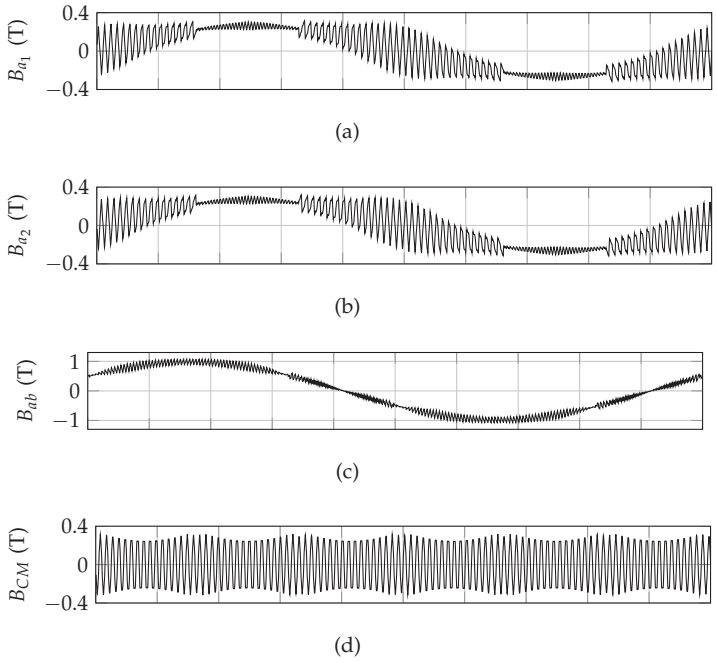


Fig. G.4: Simulated flux density waveforms. (a) Flux density in the upper limb, (b) Flux density in the lower limb, (c) Flux density in the bridge leg, (d) Flux density in the common leg.

of the phase leg. The flux linking with the coils has the resultant flux component and the circulating flux component. The resultant flux component has a dominant harmonic component at the fundamental frequency. It also

contains the even multiple of the carrier harmonic components and their side bands. On the other hand, odd multiple of the carrier harmonic frequency components and their side band harmonic components synthesize the circulating flux. The resultant flux component completes its path through the bridge legs, as shown in Fig. G.4(c). Fig. G.4(d) shows the flux in the common leg, which has dominant harmonic component at the carrier harmonic frequency.

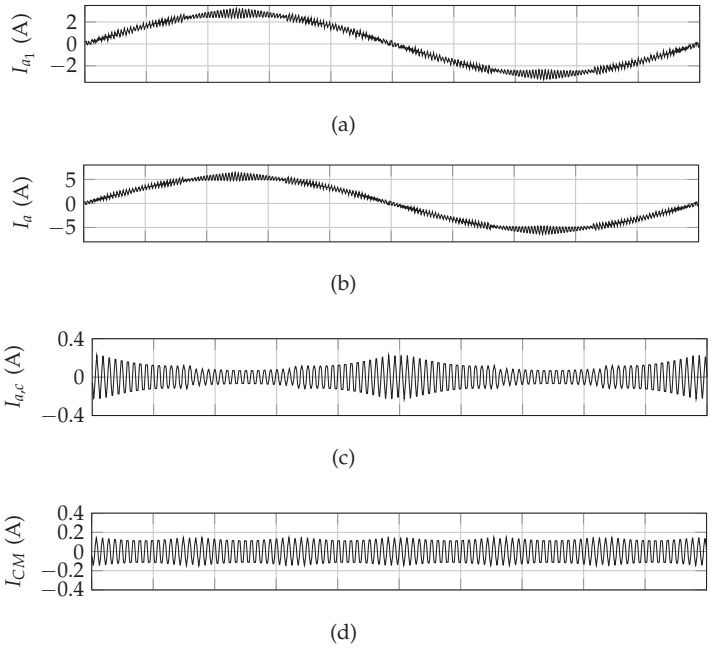


Fig. G.5: Simulated current waveforms of phase a. (a) Phase a current of VSC_1 I_{a_1}, (b) Resultant line current I_a, (c) Phase a circulating current $I_{a,c}$, (d) Common mode circulating current $I_{CM,c}$.

The simulated current waveforms are shown in Fig. G.5. The circulating current between the parallel interleaved legs of the phase A is shown in Fig. G.5(c) and it is evident that it is effectively suppressed by the proposed integrated inductor. The resultant line current of phase A is also shown in Fig. G.5(b) and the ripple content in the line current is limited to the desired value. In the steady state, the resultant line current is shared equally between the parallel VSCs and current waveform of one of the VSC_1 as shown in Fig. G.5(a).

5.1.2 Transient Considerations

There is no controlled air gap in the phase legs and the common leg. Therefore, the control scheme should be designed to prevent saturation of the integrated inductor. Asymmetrical regular sampling is used. The feedback signals are sampled and the reference signals are updated at the peak and the valley of the carrier signals, as shown in Fig. G.6. For the interleaving angle of 180°, both the VSCs are sampled at the same instant. The strong magnetic coupling between the parallel legs helps in maintaining the equal current sharing in steady-state and sampling the feedback samples at the same instant would ensure voltage second balance. As a result, saturation free operation can be achieved during the transient operation.

Individual VSC currents are controlled using the Proportional-Integral

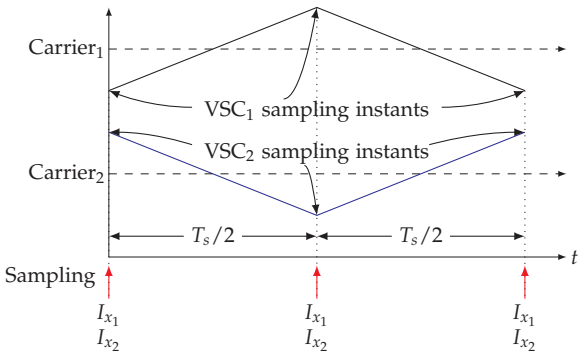


Fig. G.6: Carrier signals and the sampling instances of both the VSCs with the interleaving angle of 180°.

(PI) controller. The control variables are transformed in a synchronously rotating frame, which rotates at the fundamental frequency of the grid voltage. The transfer function of the PI controller is given by

$$G_{\mathrm{PI}}(s) = K_p + \frac{K_i}{s} \tag{G.27}$$

where K_i is the integral gain and the K_p is the proportional gain of the PI controller. The parameters of the PI controller are $K_p = 0.32$ and $K_i = 134.6$. The reference for the active component of the resultant line current has been changed from 50% of the rated value to the 100% of the rated value. The transient response of the d-axis current controller of the VSC_1 is shown in Fig. G.7(a). The individual VSC leg current and the resultant line current are shown in Fig. G.7(b) and Fig. G.7(c), respectively. The flux density in the phase leg and the common leg are also shown in Fig. G.7. As a result of the simultaneous sampling for both the VSCs, a dc component is avoided in

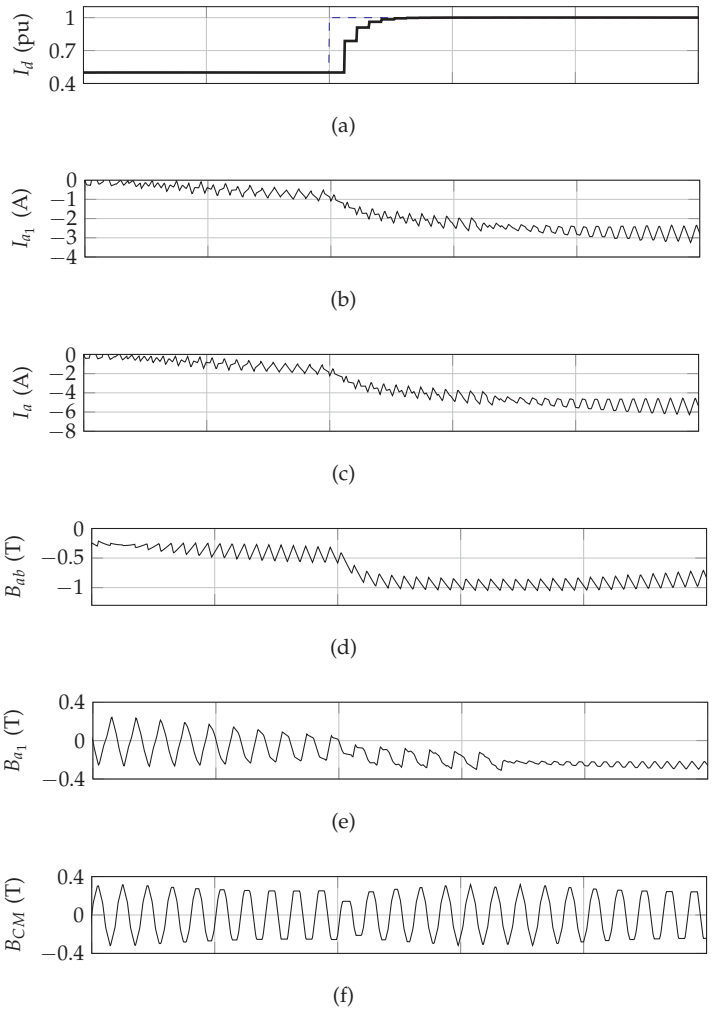
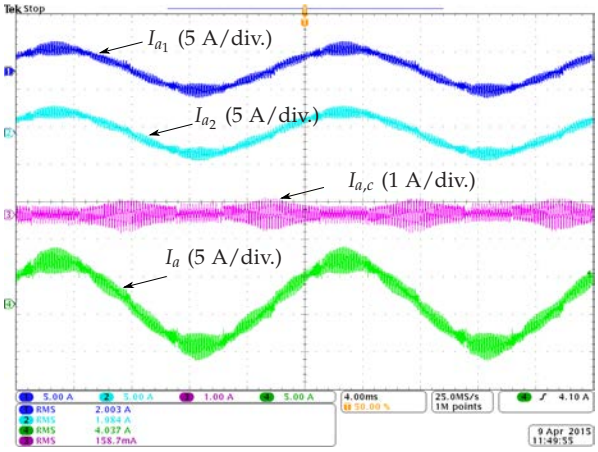
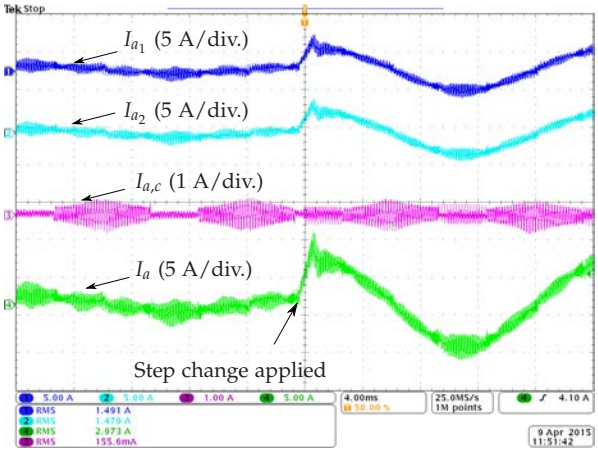


Fig. G.7: Simulation results during the transient condition, when the reference for the active component of the resultant line current has been changed from 50% of the rated value to 100% of the rated value. (a) Controller performance, (b) Phase a leg current of VSC$_1$ (I_{a_1}), (c) Resultant line current I_a, (d) Flud density in the bridge leg B_{ab}, (e) Flux density in the upper limb of the phase leg B_{a_1}, (f) Flux density in the common leg B_{CM}.

the B_{CM} and the integrated inductor operation in the linear part of the B-H curve is ensured. However, inaccuracy in the current measurement sensor (typically $<$ 1% of the rated current) could lead to an erroneous feedback signal and may introduce dc component in the circulating flux component and the CM flux component. However, the influence of the inaccuracy in the



(a)



(b)

Fig. G.8: Experimental results. (a) Steady-state: VSCs are controlled to inject the rated current, (b) Transient considerations: The reference for the injected current is changed from 25% of the rated current to 100% of the rated current.

measurement sensor is small and can be neglected for the design purpose.

5.2 Experimental Results

An integrated inductor prototype was built with the parameters given in Table G.2. Both the VSCs were connected to the same dc-link and the AC side of these VSCs were connected to the AC power source MX-35 from California

Instruments. The control was implemented using TMS320F28346 floating-point digital signal processor.

The experimental waveforms are shown in Fig. G.8. Fig. G.8(a) shows the individual currents of each of the inverter, the circulating current between the parallel interleaved VSC legs of that phase and the resultant line current in a steady-state operating conditions. The VSCs were controlled to supply the rated current. As it is evident from Fig. G.8(a), the ripple in the resultant line current is limited to the desired value and the circulating current between the parallel VSCs is also suppressed effectively by the integrated inductor. The relevant current waveforms during the transient conditions, when the reference current is changed from 25% of the rated value to the 100% of the rated value is shown in Fig. G.8(b). The circulating current is proportional to the circulating flux component in the integrated inductor. As shown in Fig. G.8(b), the change in the individual converter current does not influence the circulating current (and therefore the circulating flux component and the CM flux component are also remains unaffected) due to the simultaneous sampling of both the VSCs. As a result of this, the integrated inductor without any controlled air gap in the phase leg and the common leg can be used.

6 Conclusion

An integrated inductor for two parallel interleaved VSCs is proposed. A four leg magnetic structure is used. The integrated inductor combines the functionalities of both the line filter inductor and the circulating current inductor. Both the parallel VSCs are modulated using the 60° discontinuous modulation scheme. For the unity power factor applications, the resultant flux component achieves its maximum value when the value of the circulating flux component is very small and vice-versa. As a result, substantial size reduction can be achieved. A sampling scheme for both the VSCs along with the controller design has been also discussed. The steady-state and the transient performance of the system are also verified by the simulations and the experimental results.

References

[1] R. Jones and P. Waite, "Optimised power converter for multi-MW direct drive permanent magnet wind turbines," in *Proc. European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–10.

[2] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conver-

sion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[3] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[4] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[5] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[6] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[7] R. Hausmann and I. Barbi, "Three-phase multilevel bidirectional DC-AC converter using three-phase coupled inductors," in *Proc. IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, Sept 2009, pp. 2160–2167.

[8] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[9] J. Salmon, J. Ewanchuk, and A. Knight, "PWM inverters using split-wound coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2001–2009, 2009.

[10] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Modified discontinuous pwm for size reduction of the circulating current filter in parallel interleaved converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3457–3470, July 2015.

[11] G. Gohil, L. Bede, R. Maheshwari, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Parallel interleaved VSCs: influence of the PWM scheme on the design of the coupled inductor," in *Proc. 40th Annual Conference on IEEE Industrial Electronics Society, IECON 2014*, Oct 2014, pp. 1693–1699.

Paper H

An integrated inductor for parallel interleaved three-phase voltage source converter

Ghanshyamsinh Gohil,
Lorand Bede,Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been published in the
IEEE Transactions on Power Electronics [Online early access], DOI:
10.1109/TPEL.2015.2459134, 2015.

The layout has been revised.

Abstract

Three phase Voltage Source Converters (VSCs) are often connected in parallel to realize high current output converter system. The harmonic quality of the resultant switched output voltage can be improved by interleaving the carrier signals of these parallel connected VSCs. As a result, the line current filtering requirement can be reduced. However, an additional inductive filter is required to suppress the circulating current. The integrated inductive component, which combines the functionality of the line filter inductor and the circulating current inductor is presented in this paper. An analysis of the flux density distribution in the integrated inductor is presented and design procedure is described. The analysis has been also verified by performing finite element analysis. The advantage offered by the use of the integrated inductor is demonstrated by comparing its volume with the volume of the state-of-the-art filtering solution. The performance of the integrated inductor is also verified by the experimental measurements.

Nomenclature: Paper H

A_g Cross section area of the air gap.

A_w Area of each of the windows in the cell structure.

$A_{c,CI}$ Cross section area of the core of the Coupled Inductor (CI).

$A_{c,bl}$ Cross section area of the bridge leg.

$A_{c,l}$ Cross section area of the limb.

A_{cu} Cross section area of the coil.

$A_{w,CI}$ Window area of the CI.

$B_{m,bl}$ Maximum allowable value of the flux density in the bridge leg.

$B_{m,c}$ Maximum allowable value of the flux density in the cell.

I_x Resultant line current of phase x.

$I_{x,f}$ Fundamental frequency component of the resultant line current.

$I_{x,p}$ Peak value of the fundamental frequency component I_x, f.

$I_{x_k,c}$ Circulating current component of the leg current I_{x_k}.

$I_{x_k,l}$ Common component of the leg current I_{x_k}.

I_{x_k} Leg current of phase x of the kth VSC.

J Current density.

K_s Stacking factor.

K_w Window utilization factor.

L_c Circulating current filter inductor.

L_f Line filter inductor.

M Modulation index.

N Number of turns in each coil.

P Rated power of the parallel VSCs.

V_{dc} DC-link voltage.

V_{ph} RMS value of the rated phase voltage.

$V_{x_k o}$ Switched output voltage of phase x of the kth VSC with respect to the dc-link mid-point o.

$V_{x_v o}$ Averaged switched output voltage of phase x with respect to the common reference point o.

V_{xg} RMS value of the grid voltage of phase x.

ΔI_x Ripple component of the resultant line current.

$\Delta I_{x,p_{max}}$ Worst case ripple component of the resultant line current.

$\Delta I_{x,p}$ Peak value of the ripple component of the resultant line current.

$\Re_g$ Reluctance of the air gap.

$\Re_l$ Reluctance of each of the limb.

$\Re_y$ Reluctance of the yoke.

$\Re_{by}$ Reluctance of the bridge yoke.

α Ratio of the maximum current ripple to the peak value of the fundamental frequency component of the current.

$\mathbf{I_{x,c}}$ Circulating current vector.

$\mathbf{I}$ Leg current vector.

$\mathbf{L}$ Inductance matrix.

$\mathbf{V_S}$ Switched output voltage vector.

$\mathbf{V_{ref}}$ Reference space voltage vector.

$\mathbf{V}$ Output voltage vector.

λ_{x_k} Flux linkage with kth coil of phase x.

λ_x Average value of the flux linkages of coils of phase x.

μ_0 Permeability of the air.

ϕ_x Common flux.

$\phi_{x,c_{max}}$ Maximum value of the circulating flux component.

$\phi_{x,c}$ Circulating flux component.

$\phi_{x_k,c}$ Circulating flux component that links with the kth coil of phase x.

$\phi_{x_k,f}$ Fundamental frequency component of the flux.

$\phi_{x_k,l_{max}}$ Worst case value of the common flux component.

$\phi_{x_k,l}$ Common flux component that links with the kth coil of the phase x.

$\phi_{x_k,r}$ Ripple component of the common flux.

$\phi_{x_{k_{max}}}$ Maximum value of the flux in the limbs.

ψ Reference voltage space vector angle (typically the grid voltage vector).

σ Interleaving angle.

θ Displacement power factor angle.

f_c Carrier frequency.

l_g Length of the air gap.

n Total number of the parallel connected VSCs.

x Subscript, which represents phases a, b, and c.

x_c Common (output) terminal of the of phase x.

x_k Input terminal of the kth coil of phase x.

1 Introduction

Three-Phase Voltage Source Converter (VSC) is commonly used in many power electronics applications and often connected in parallel to realize medium/high power converter systems [1, 2]. The switching frequency of the semiconductor devices, used in medium/high power applications, is often limited [3]. Therefore, such systems may require large filter components to meet the stringent power quality requirements imposed by the utility [4]. The use of the large filter components occupy significant amount of space [5] and increase the cost of the overall converter system [6].

The size of the line filter components can be reduced by improving the output voltage waveform quality. In a system with parallel connected VSCs, this can be achieved by interleaving the carrier signals [7–12]. For a system

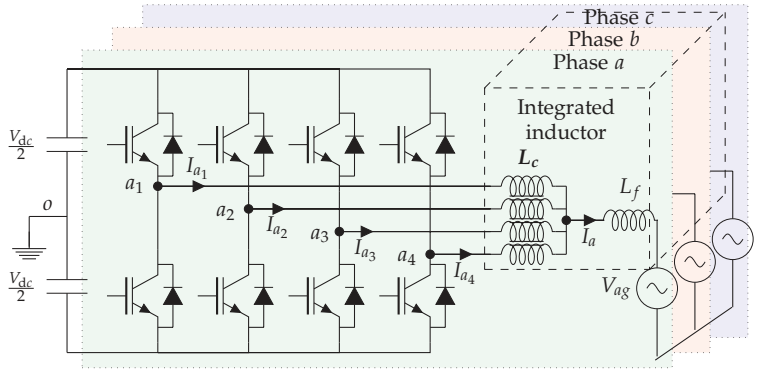


Fig. H.1: Parallel interleaved voltage source converters with common dc-link (n = 4 in this illustration). Coupled inductor (CI) is used for suppressing the circulating current.

with parallel connected VSCs, the resultant voltage of a given phase is the average of the switched output voltages of that phase of the individual VSCs. As a result of the interleaving of the carrier signals, the switched output voltages of the corresponding phase are shifted with respect to each other by an interleaving angle. Therefore, some of the harmonic frequency components present in the individual switched output voltages are either completely canceled or significantly reduced in the resultant output voltage. This helps to achieve the desired line current quality with relatively small line filter components. However, when connected to the common dc link, the circulating current flows between the parallel VSCs due to hardware and control asymmetries [13] and increases significantly when the carriers are interleaved [12]. This unwanted circulating current increases the stress on the semiconductor switches and causes additional losses. Therefore, it should be suppressed to some acceptable limits.

The circulating current can be avoided by providing galvanic isolation between the parallel VSCs using the multiple winding line frequency transformer [14]. However, the use of the bulky line frequency transformer adds to the cost and increases the size. Another approach is to suppress the circulating current to some acceptable limit by introducing impedance in the circulating current path. This can be achieved by

1. Using Common-Mode (CM) inductor in series with the line filter inductor for each of the VSCs [8].

2. Using the Coupled Inductor (CI) to suppress the circulating current by providing magnetic coupling between the parallel interleaved legs of the corresponding phases [15–20] (refer Fig. H.1).

In both of the above mentioned approaches, two distinct magnetic compo-

nents are used:

1. Circulating current inductor L_c (CI / CM inductor).
2. Line filter inductor L_f (commonly referred to as a boost inductor) for improving the line current quality.

The volume of the inductive components can be reduced by integrating both of these functionalities into a single magnetic component. A single phase integrated inductor for the two parallel interleaved VSCs is proposed in [21]. The magnetic structure of this inductor has two side limbs and a central limb. Air gaps are introduced in all the three legs, out of which the length of the air gaps in both the side limbs are equal. The coils are placed around the side limbs and have equal number of turns. The flux in the magnetic core has two distinct components:

1. Flux component corresponding to the line filter inductor L_f (referred to as the common flux ϕ_x).
2. Flux component corresponding to the CI (referred to as the circulating flux $\phi_{x,c}$, which mainly confines to the side limbs).

The circulating flux component $\phi_{x,c}$ is given as

$$\phi_{x,c} = \frac{1}{2N} \int (V_{x_1o} - V_{x_2o})\, dt \tag{H.1}$$

The maximum value of the circulating flux component is given as [22]

$$\phi_{x,c_{max}} = \frac{V_{\mathrm{dc}}}{8Nf_c} \tag{H.2}$$

The $\phi_{x,c_{max}}$ depends only on the dc-link voltage V_{dc}, the number of turns N, and the switching frequency f_c. Therefore, the introduction of the two air gaps in the magnetic path of the $\phi_{x,c}$ does not bring any advantage in terms of the size reduction (However depending upon the control scheme employed, small air gap may be needed to avoid the saturation). In addition, it is difficult to realize the inductor using the standard cores, when the length of the air gaps in the side limbs and the central limbs are different. Moreover, the solution presented in [21] is only applicable to two parallel interleaved VSCs. The circulating current suppression for three parallel VSCs is presented in [20]. Three limb magnetic core is used for the CIs and single phase inductors are employed for the line current filtering of each of the phases. The magnetic integration of all these components in a single magnetic structure can further reduce the volume of the overall system.

A three-phase integrated inductor for arbitrary number of parallel interleaved VSCs is proposed in this paper. The proposed integrated inductor

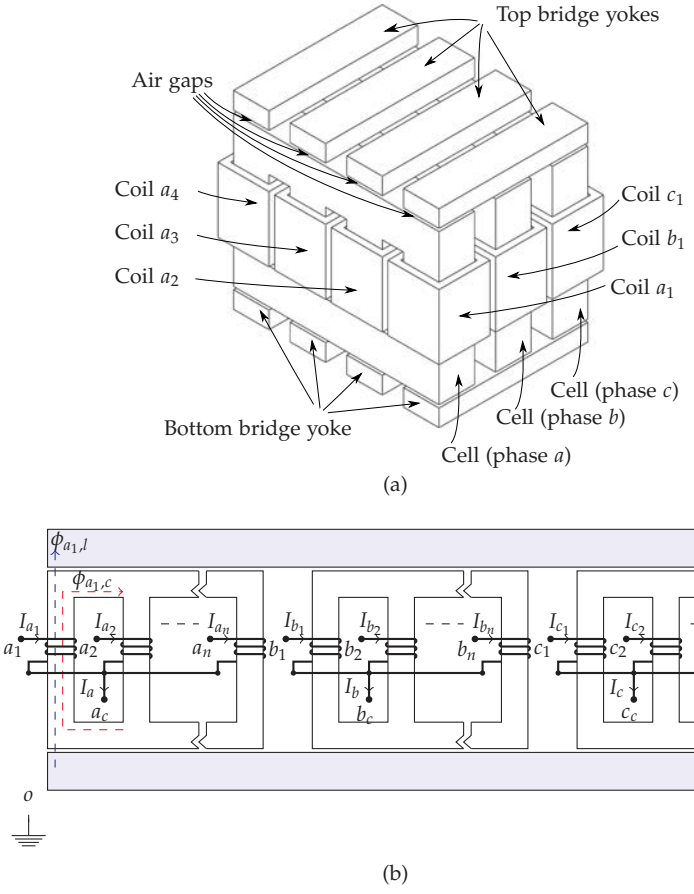


Fig. H.2: Magnetic structure. (a) Magnetic structure of the proposed integrated three-phase inductor for n number of parallel connected VSCs (n = 4 in this illustration), (b) Alternative simplified arrangement.

combines the functionality of both the line filter inductor L_f and the circulating current inductor L_c. The magnetic structure and the detailed analysis of the proposed three-phase integrated inductor is presented in Section II. Section III, summarizes the design methodology of the integrated inductor. A comparison between the proposed inductor and the state-of-the-art solution, which uses a separate CIs for each of the phases and a three phase line filter inductor L_f, is also presented. Simulations and experimental results are given in Section IV.

2 Integrated Inductor

The magnetic structure, modeling and analysis of the proposed integrated inductor for n number of parallel interleaved VSCs is presented in this section.

2.1 Magnetic Structure

The magnetic structure of the proposed three-phase integrated inductor for n number of parallel VSCs is shown in Fig. H.2(a) (n = 4 in the illustration). The simplified arrangement of the integrated inductor is also shown in Fig. H.2(b). The magnetic core is composed of three identical magnetic structure belonging to each of the phases of the three-phase system. Such magnetic structure is referred to as a cell. Each cell contains n limbs, magnetically coupled to each other using the yokes, as shown in Fig. H.2(a). Small inherent air gap exists when the limbs and the yokes are arranged together to form the cell structure. Therefore an intentional air gap is avoided (which otherwise may be needed to avoid saturation) to achieve high circulating current filter inductance L_c. Each limb carries a coil having N turns and all the coils are wound in the same direction. For a three phase system, three such cell are used, as shown in Fig. H.2(a). The cells of all the three phases are magnetically coupled using the top and bottom bridge yokes. The necessary air gaps are inserted between the cells and the bridge yokes. The magnetic structure shown in Fig. H.2(a) has six ventilation channels that can be used for guiding the air flow from bottom to top for better cooling.

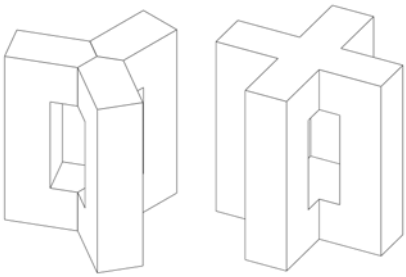
The start terminal of the coils of a cell belonging to phase x is connected to the output terminal of the respective VSC leg x_k of the corresponding phase and the end terminal is connected to a common connection point of that phase x_c, as shown in Fig. H.2(b). The magnetic structure, as shown in Fig. H.2(a), is asymmetrical for $n > 2$. However, symmetrical cells can be realized using alternative cell structures, as shown in Fig. H.3. In the interest of brevity, the analysis is presented for the symmetrical cell structure.

2.2 System Description

$$\overrightarrow{V}_S = \begin{bmatrix} V_{a_1o} & V_{a_2o} \cdots & V_{a_no} & V_{b_1o} & V_{b_2o} \cdots & V_{bno} & V_{c_1o} & V_{c_2o} \cdots & V_{c_no} \end{bmatrix}^T \tag{H.3}$$

$$\overrightarrow{I} = \begin{bmatrix} I_{a_1} & I_{a_2} \cdots I_{a_n} & I_{b_1} & I_{b_2} \cdots I_{b_n} & I_{c_1} & I_{c_2} \cdots I_{c_n} \end{bmatrix}^T \tag{H.4}$$

$$\overrightarrow{V} = \begin{bmatrix} V_{a_co} & V_{a_co} \cdots & V_{a_co} & V_{b_co} & V_{b_co} \cdots & V_{b_co} & V_{c_co} & V_{c_co} \cdots & V_{c_co} \end{bmatrix}^T \tag{H.5}$$



(a) (b)

Fig. H.3: Symmetrical magnetic cell structures for different number of parallel connected VSCs. (a) Three VSC case, (b) Four VSC case.

$$\boldsymbol{L} = \left[\begin{array}{ccccccccc}
L_{a_1a_1} & L_{a_1a_2}\cdots & L_{a_1a_n} & L_{a_1b_1} & L_{a_1b_2}\cdots & L_{a_1b_n} & L_{a_1c_1} & L_{a_1c_2}\cdots & L_{a_1c_n} \\
L_{a_2a_1} & L_{a_2a_2}\cdots & L_{a_2a_n} & L_{a_2b_1} & L_{a_2b_2}\cdots & L_{a_2b_n} & L_{a_2c_1} & L_{a_2c_2}\cdots & L_{a_2c_n} \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\
L_{a_na_1} & L_{a_na_2}\cdots & L_{a_na_n} & L_{a_nb_1} & L_{a_nb_2}\cdots & L_{a_nb_n} & L_{a_nc_1} & L_{a_nc_2}\cdots & L_{a_nc_n} \\
\hline
L_{b_1a_1} & L_{b_1a_2}\cdots & L_{b_1a_n} & L_{b_1b_1} & L_{b_1b_2}\cdots & L_{b_1b_n} & L_{b_1c_1} & L_{b_1c_2}\cdots & L_{b_1c_n} \\
L_{b_2a_1} & L_{b_2a_2}\cdots & L_{b_2a_n} & L_{b_2b_1} & L_{b_2b_2}\cdots & L_{b_2b_n} & L_{b_2c_1} & L_{b_2c_2}\cdots & L_{b_2c_n} \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\
L_{b_na_1} & L_{b_na_2}\cdots & L_{b_na_n} & L_{b_nb_1} & L_{b_nb_2}\cdots & L_{b_nb_n} & L_{b_nc_1} & L_{b_nc_2}\cdots & L_{b_nc_n} \\
\hline
L_{c_1a_1} & L_{c_1a_2}\cdots & L_{c_1a_n} & L_{c_1b_1} & L_{c_1b_2}\cdots & L_{c_1b_n} & L_{c_1c_1} & L_{c_1c_2}\cdots & L_{c_1c_n} \\
L_{c_2a_1} & L_{c_2a_2}\cdots & L_{c_2a_n} & L_{c_2b_1} & L_{c_2b_2}\cdots & L_{c_2b_n} & L_{c_2c_1} & L_{c_2c_2}\cdots & L_{c_2c_n} \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\
L_{c_na_1} & L_{c_na_2}\cdots & L_{c_na_n} & L_{c_nb_1} & L_{c_nb_2}\cdots & L_{c_nb_n} & L_{c_nc_1} & L_{c_nc_2}\cdots & L_{c_nc_n}
\end{array}\right] \tag{H.6}$$

Referring to Fig. H.2(b) and by neglecting the resistance of the coils, the switched output voltages (with respect to the fictitious mid-point of the dc-link o) are given as

$$\boldsymbol{V_S} = \boldsymbol{L}\frac{d}{dt}\boldsymbol{I} + \boldsymbol{V} \tag{H.7}$$

where the corresponding current and voltage vectors and the inductance matrix $\boldsymbol{L}$ are given in (H.3), (K.20), (H.5), and (H.6) at the top of the next page.

Let the average of the switched output voltages of phase x be V_{x_vo} and it is represented as

$$V_{x_vo} = \frac{1}{n}\sum_{k=1}^{n} V_{x_ko}; \text{ where } 1 < k \leq n \tag{H.8}$$

The resultant line current of a particular phase is the sum of all leg currents of that phase and it is given as

$$I_x = \sum_{k=1}^{n} I_{x_k}; \text{ where } 1 \leq k \leq n \tag{H.9}$$

For the parallel interleaved VSCs, the leg current I_{x_k} can be split into two components:

1. The component contributing to the resultant line current $I_{x_k,l}$
2. The circulating current $I_{x_k,c}$

and it can be represented as

$$I_{x_k} = I_{x_k,l} + I_{x_k,c} \tag{H.10}$$

The circulating current components $I_{x_k,c}$ do not contribute to the resultant line current. Therefore, (H.9) can be re-written as

$$I_x = \sum_{k=1}^{n} I_{x_k,l}; \text{ where } 1 \leq k \leq n \tag{H.11}$$

Assuming an equal line current sharing between the parallel VSCs, the common component of the leg current is obtained as

$$I_{x_k,l} = \frac{I_x}{n} \tag{H.12}$$

Once the current quantities are defined, the qualitative analysis of the magnetic couplings is presented by performing the finite element analysis and the inductances values of the matrix $\boldsymbol{L}$ are obtained by solving the reluctance network, which is discussed in following sub sections.

2.3 Finite Element Analysis

Due to the Pulse Width Modulation (PWM), the switched output voltage $V_{x_k o}$ has undesirable harmonic frequency components in addition to the required fundamental frequency component. When the carrier signals are interleaved, some of the harmonic frequency components of the switched output voltages of the parallel interleaved legs are phase shifted with respect to each other, whereas the rest of the harmonic frequency components are in-phase [23, 24]. The effects of these two distinct voltage components on the flux density distribution in the integrated inductor is evaluated by performing finite element analysis of an integrated inductor for the three parallel interleaved VSCs. The magnetic structure of the integrated inductor is shown in Fig. H.4.

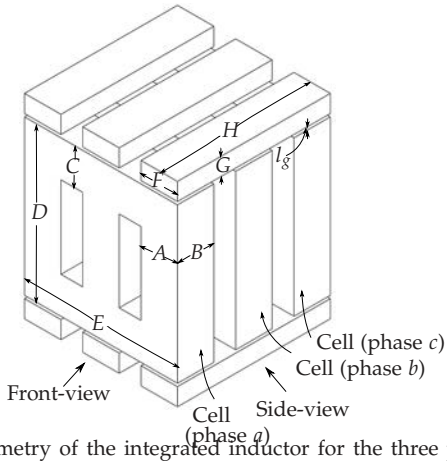


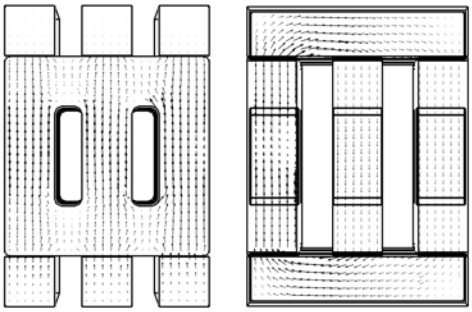
Fig. H.4: Magnetic core geometry of the integrated inductor for the three parallel interleaved voltage source converters. The cross section area of the limb $A_{c,l} = A \times B \times K_s$. The cross section area of the bridge leg $A_{c,bl} = F \times G \times K_s$. The air gap area $A_g = B \times F$.

2.3.1 Effect of the In-phase Harmonic Frequency Components

All three coils of the phase a are excited by equal and in-phase fundamental frequency currents. The flux density vector distribution in this case is shown in Fig. H.5, where the flux direction is indicated by the arrows. The flux density distribution in all three limbs of the cell is almost symmetrical and the flux linkage between the coils of the same phase is zero, as shown in Fig. H.5(a). The flux due to the flow of the in-phase current in the kth coil of phase a, couples with the kth coils of the phase b and the phase c. For example, the induced flux due to the fundamental frequency component of I_{a_1} only links with coil b_1 and coil c_1 and completes its path through two air gaps and the corresponding top and bottom bridge yokes, as shown in Fig. H.5(b). Therefore, the magnetic coupling coefficient between the kth coil of one of the phase and the jth coil of the other phase (where $k \neq j$) can be considered to be zero.

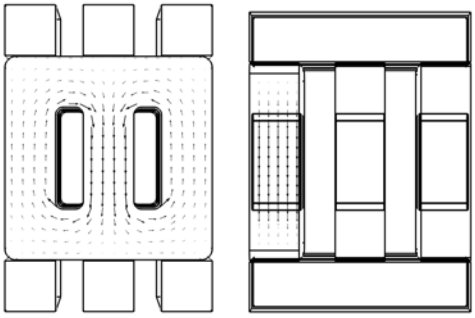
2.3.2 Effect of the Phase Shifted Harmonic Frequency Components

Assuming symmetrical VSC legs, the magnitude of the harmonic frequency components in the switched output voltages of each of the interleaved legs is considered to be equal. If the interleaving angle σ between the successive carrier signals is taken to be the same $\sigma = 2\pi/n$ (symmetrical interleaving), then the effect of the phase shifted harmonic components is canceled in the resultant voltage [23, 24]. Therefore, the phase shifted harmonic frequency components only appears across the corresponding coils and does not influence the resultant output. The flux density vector distribution, when



(a) (b)

Fig. H.5: Flux density vector distribution when the equal and in-phase fundamental frequency component of the current flows through the all three coils of phase A. (a) Cross-sectional view (front), (b) Cross-sectional view (side).



(a) (b)

Fig. H.6: Flux density vector distribution when the equal and symmetrically phase-shifted switching frequency component of the voltage applied across the all three coils of phase A. (a) Cross-sectional view (front), (b) Cross-sectional view (side).

the switching frequency component with equal magnitude and symmetrical phase shift is applied across the coils of phase a, is shown in Fig. H.6. The induced flux is mainly confined to the cell. For example, the induced flux due to the phase shifted component of the voltage across coil a_1 links with coil a_2 and coil a_3 and does not link with the coils of phase b and phase c. Similar argument applies to the phase b and the phase c.

Neglecting the leakage, the flux that links with each of the coils can be divided into two distinct components:

1. The flux component, which links with the corresponding coils of the other two phases (referred to as the common flux component $\phi_{x_k,l}$).

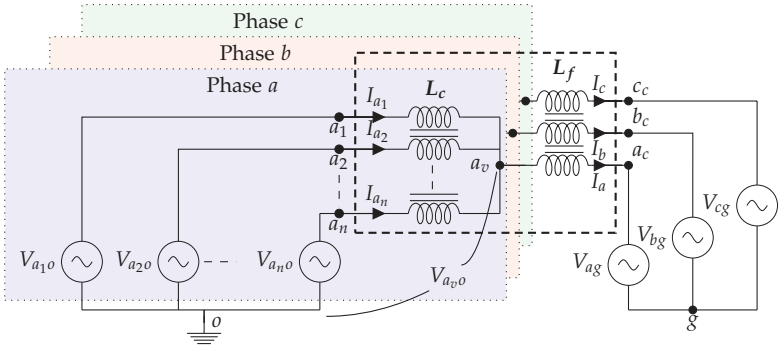


Fig. H.7: Equivalent electrical circuit of the parallel interleaved VSCs with the proposed integrated inductor.

2. The flux component, which links with the remaining coils of the cell belonging to the same phase (referred to as a circulating flux component $\phi_{x_k,c}$).

Considering symmetrical cell structure, the inductances can be represented as

$$L_{a_jb_j} = L_{b_jc_j} = L_{c_ja_j} = -L_m \text{ for all } 1 \leq j \leq n \tag{H.13}$$

$$\begin{aligned} L_{a_jb_k} = L_{b_jc_k} = L_{c_ja_k} \cong 0 \\ \text{for all } 1 \leq j \leq n, 1 \leq k \leq n, \text{ and } j \neq k \end{aligned} \tag{H.14}$$

$$L_{x_jx_k} = -L_{m_1} \text{ for all } 1 \leq j \leq n, 1 \leq k \leq n, \text{ and } j \neq k \tag{H.15}$$

The $-ve$ sign is used to represent the L_m and L_{m_1} and the same convention has been followed through out the paper. Neglecting the leakage flux, the self-inductance of each of the coils is given as

$$\begin{aligned} L_{a_ja_j} = L_{b_jb_j} = L_{c_jc_j} = (n-1)L_{m_1} + 2L_m \\ \text{for all } 1 \leq j \leq n \end{aligned} \tag{H.16}$$

2.4 Equivalent Electrical Circuit

By substituting these inductance values in (H.6) and averaging the pole voltages of each of the phase gives

$$\begin{bmatrix} V_{a_vo} - V_{a_co} \\ V_{b_vo} - V_{b_co} \\ V_{c_vo} - V_{c_co} \end{bmatrix} = \frac{1}{n} \begin{bmatrix} 2L_m & -L_m & -L_m \\ -L_m & 2L_m & -L_m \\ -L_m & -L_m & 2L_m \end{bmatrix} \frac{d}{dt} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{H.17}$$

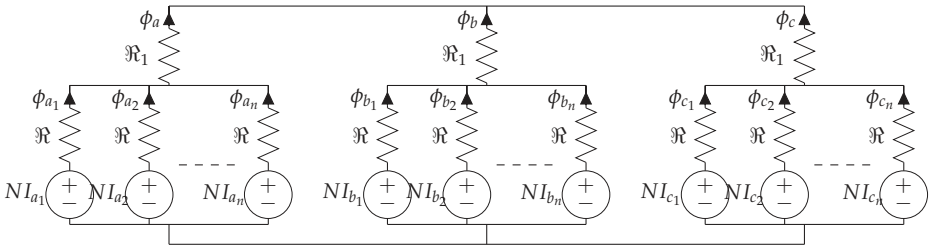


Fig. H.8: Simplified reluctance model of the three-phase inductor with symmetrical cells.

For the three-phase three-wire system, $I_a + I_b + I_c = 0$ and the inductance offered to the resultant line current is given as

$$L_f = \frac{V_{x_v o} - V_{x_c o}}{dI_x/dt} = \frac{3}{n} L_m \tag{H.18}$$

The behavior of the circulating current can be described by subtracting the averaged pole voltage from the pole voltages of the corresponding phases and further simplification of those equations give

$$\boldsymbol{V_{S_x}} = \boldsymbol{L_c} \frac{d}{dt} \boldsymbol{I_{x,c}} + V_{x_v o} \tag{H.19}$$

where

$$\boldsymbol{V_{S_x}} = \begin{bmatrix} V_{x_1 o} & V_{x_2 o} & \dots & V_{x_n o} \end{bmatrix}^T \tag{H.20}$$

$$\boldsymbol{I_{x,c}} = \begin{bmatrix} I_{x_1,c} & I_{x_2,c} & \dots & I_{x_n,c} \end{bmatrix}^T \tag{H.21}$$

$$\boldsymbol{L_c} = \begin{bmatrix} (n-1)L_{m_1} & -L_{m_1} & \cdots & -L_{m_1} \\ -L_{m_1} & (n-1)L_{m_1} & \cdots & -L_{m_1} \\ \vdots & \vdots & \vdots & \vdots \\ -L_{m_1} & -L_{m_1} & \cdots & (n-1)L_{m_1} \end{bmatrix} \tag{H.22}$$

Using (H.18) and (H.19), the electrical equivalent circuit is obtained and it is shown in Fig. H.7. Here x_v is the virtual common point and the potential of this point with respect to the mid-point of the dc-link is the averaged pole voltage $V_{x_v o}$. The potential difference of $V_{x_v o} - V_{x_c o}$ appears across the line filter inductor L_f, as shown in Fig. H.7.

2.5 Reluctance Network

The relationship between the inductance values and the physical parameters of the integrated inductor is obtained by solving the reluctance network and

presented in this sub section.

The simplified reluctance model of the three-phase integrated inductor with the symmetrical cells is shown in Fig. H.8. The reluctance of each of the leg is $\Re$ and it is given as

$$\Re = \Re_l + \Re_y \tag{H.23}$$

The equivalent reluctance of the air gaps ($\Re_g$) and the bridge yoke ($\Re_{by}$) is represented by $\Re_1$ and can be written as

$$\Re_1 = \frac{2}{n}(\Re_g + \Re_{by}) \tag{H.24}$$

The reluctance of the air gaps is generally large compared to the reluctance of the bridge yoke. Therefore, $\Re_1$ can be approximated to be $\frac{2}{n}\Re_g$. By solving the reluctance network, the flux linking with each of the coils is given as

$$\begin{aligned}\lambda_{x_k}(t) &= \int \Big(V_{x_k o} - V_{x_c o}\Big)dt \\ &= \frac{N^2}{\Re + n\Re_1}\frac{I_x(t)}{n} + \frac{N^2}{\Re} I_{x_k,c}(t)\end{aligned} \tag{H.25}$$

Averaging the flux linkages of each of the phase group gives

$$\begin{aligned}\lambda_x(t) &= \frac{1}{n}\sum_{k=1}^{n}\lambda_{x_k} = \int \Big(V_{x_v o} - V_{x_c o}\Big)dt \\ &= \frac{N^2}{\Re + n\Re_1}\frac{I_x(t)}{n} + \frac{N^2}{\Re}\frac{1}{n}\sum_{k=1}^{n} I_{x_k,c}(t)\end{aligned} \tag{H.26}$$

As per the definition of the circulating current

$$\sum_{k=1}^{n} I_{x_k,c} = 0 \tag{H.27}$$

Using (H.18), (I.39), and (H.26), the inductance offered to the resultant line current is given as

$$L_f = \frac{N^2}{n(\Re + n\Re_1)} \tag{H.28}$$

since, $n\Re_1 >> \Re$, the line inductance can be given as

$$L_f \approx \frac{N^2}{n^2\Re_1} = \frac{N^2}{2n\Re_g} = \frac{\mu_0 N^2 A_g}{2nl_g} \tag{H.29}$$

As it is evident from (H.29), the line inductance value mainly depends on the geometry of the air gap.

The values of the circulating current inductance can be obtained by subtracting (H.26) from (I.39) as

$$\int \left(V_{x_k o} - V_{x_v o}\right) dt = \frac{(n-1)}{n} \frac{N^2}{\Re} I_{x_k,c}(t) - \frac{1}{n} \frac{N^2}{\Re} \left(\sum_{\substack{j=1 \\ j \neq k}}^{n} I_{x_j,c}(t) \right) \tag{H.30}$$

Using (H.19) and (H.30), the expression for L_{m_1} is obtained as

$$L_{m_1} = \frac{1}{n} \frac{N^2}{\Re} = \frac{1}{n} \frac{N^2}{\Re_l + \Re_y} \tag{H.31}$$

It is evident that L_{m_1} is independent of the air gap geometry and depends only on the reluctances of the limb and yokes (and the reluctance of the inherent air gaps). The value of the L_{m_1} and therefore the inductance offered to the circulating current can be increased by using high permeability magnetic material for the cells.

3 Design and Volumetric Comparison

The design methodology of the integrated inductor for grid-connected unity power factor application is presented in this section and the results are compared with the state-of-the-art solution of using three separate CIs and one three-phase line filter inductor. Design equations for three parallel interleaved VSCs are presented for the core geometry shown in Fig. H.4. However, the design methodology presented in this paper is applicable to any number of parallel interleaved VSCs.

3.1 Pulse Width Modulation Scheme

The flux in the core is strongly influenced by the PWM scheme used [25]. The use of the center aligned Space Vector Modulation (SVM) is considered in this paper. Each of the VSCs cycles through four switch states in each switching cycle. Based on the position of the reference space vector ($\overrightarrow{V}_{ref}$), two adjacent active voltage vectors and both of the zero voltage vectors are applied to synthesize $\overrightarrow{V}_{ref}$. The carrier signals of the parallel VSCs are phase shifted with respect to each other by an interleaving angle $\sigma = 120^\circ$.

3.2 Maximum Flux Values

The flux waveforms in various parts of the integrated inductor are shown in Fig. H.9. The flux components can be classified into three categories:

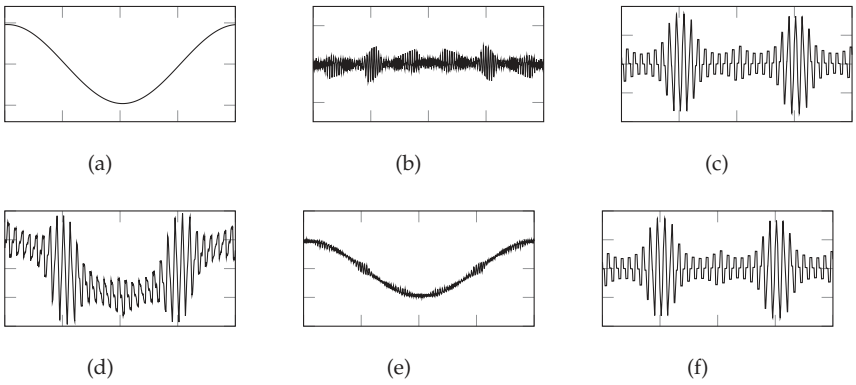


Fig. H.9: Flux waveforms. (a) Fundamental component of the common flux $\phi_{x_k,f}$, (b) Ripple component of the common flux $\phi_{x_k,r}$, (c) Circulating flux component $\phi_{x_k,c}$, (d) Flux in the limbs $\phi_{x_k}(t) = \big(\phi_{x_k,f}(t) + \phi_{x_k,r}(t) + \phi_{x_k,c}(t)\big)$, (e) Flux in the bridge legs $\phi_{x_k,l}(t) = \big(\phi_{x_k,f}(t) + \phi_{x_k,r}(t)\big)$, (f) Flux in the yokes $\phi_{x_k,c}$.

1. Fundamental flux component $\phi_{x_k,f}$.
2. Ripple component of the flux $\phi_{x_k,r}$ with predominant harmonic frequency component of $3 \times f_c$.
3. Circulating flux component $\phi_{x_k,c}$ with predominant harmonic frequency component of f_c and $2 \times f_c$.

The flux in each limb is the vector addition of the $\phi_{x_k,l}$ and $\phi_{x_k,c}$, whereas the bridge yokes only experiences the flux of $\phi_{x_k,l}$. For the proper design of an integrated inductor, maximum value of these flux components are required and derived hereafter.

3.2.1 Common Flux Component

The common flux component can be obtained from (I.39) and it is given as

$$\phi_{x_k,l}(t) \approx \frac{\mu_0 N A_g}{2n l_g} I_x(t) \tag{H.32}$$

The resultant line current I_x is a combination of a fundamental frequency component I_x, f and a ripple component ΔI_x. Therefore, (H.32) can be re-written as

$$\phi_{x_k,l}(t) = \frac{\mu_0 N A_g}{2n l_g} \Big(I_{x,p} \cos(\psi - \theta) + \Delta I_x(t) \Big) \tag{H.33}$$

The maximum value of ΔI_x depends on the pulse-width modulation scheme, the modulation index M, the dc-link voltage V_{dc}, the switching frequency

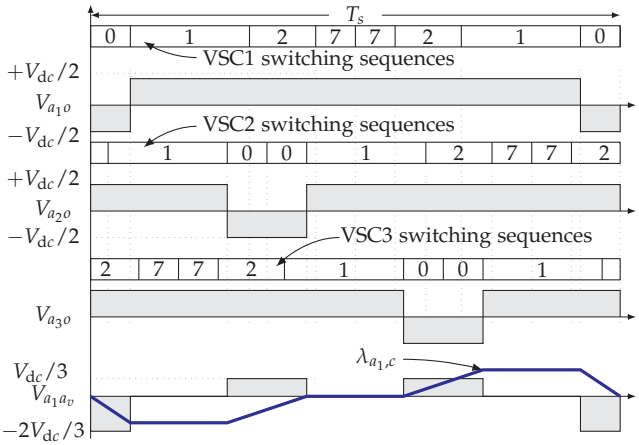


Fig. H.10: Space vector modulation: Switched output voltage of phase a of each of the individual VSCs and the voltage across coil a_1 when the carriers are interleaved by an interleaving angle of 120°. The modulation index $M = \sqrt{3}/2$ and a space vector angle $\psi = 20°$.

f_c [25], and the line filter inductor L_f. Considering the balanced three-phase system, the design equations for only phase a are derived. For the unity power factor applications, the fundamental component of the resultant line current is maximum for full load condition at $\psi = 0°$. The ripple component of the line current for $M > \frac{4}{9}$ at $\psi = 0°$ is given as

$$\Delta I_{a,p} \mid_{\psi=0°} = \frac{V_{\mathrm{dc}}}{3L_f f_c}\left(\frac{5M}{8} - \frac{9M^2}{32} - \frac{1}{3}\right) \tag{H.34}$$

where the modulation index M is defined as

$$M = \frac{2\sqrt{2}V_{xg}}{V_{\mathrm{dc}}} \tag{H.35}$$

The worst case value of the common flux component $\phi_{a_k,l_{max}}$ is

$$\begin{aligned}\phi_{a_k,l_{max}} &= \frac{\mu_0 N A_g}{2nl_g}\left(I_{x,p_{max}} + \Delta I_{x,p} \mid_{\psi=0°}\right) \\ &= \frac{\sqrt{2}L_f P}{3NV_{ph}} + \frac{V_{\mathrm{dc}}}{3Nf_c}\left(\frac{5M}{8} - \frac{9M^2}{32} - \frac{1}{3}\right)\end{aligned} \tag{H.36}$$

3.2.2 Circulating Flux Component

Using (H.30), the circulating flux component in each limb $\phi_{x_k,c}$ is given as

$$\phi_{x_k,c}(t) = \frac{1}{N}\Big(\frac{n-1}{n}\int V_{x_k o}\,dt - \frac{1}{n}\sum_{\substack{j=1\\ j\neq k}}^{n}\int V_{x_j o}\,dt\Big) \tag{H.37}$$

For $n = 3$, the flux linkage of coil a_1 due to the circulating flux component is given as

$$N\phi_{a_1,c}(t) = \frac{2}{3}\int V_{a_1 o}\,dt - \frac{1}{3}\int (V_{a_2 o} + V_{a_3 o})\,dt \tag{H.38}$$

The switching sequences and the switched output voltages of the phase a of all three VSCs are shown in Fig. H.10. T_1, T_2, T_0 and T_7 are the dwell times of the voltage vectors $\overrightarrow{V}_1$, $\overrightarrow{V}_2$, $\overrightarrow{V}_0$, and $\overrightarrow{V}_7$, respectively. The flux linkage due to the circulating flux component in a given switching cycle is shown in Fig. H.10 for the modulation index $M = \sqrt{3}/2$ and the space vector angle $\psi = 20^\circ$. The peak value of the flux linkage is different in each switching cycle due to the change in the dwell times of the voltage vectors, as shown in Fig. H.11. The flux linkage due to the circulating flux component is independent of the load and depends only on the modulation scheme, the dc-link voltage, and the switching frequency. The maximum value of the peak flux linkage occurs at the $\psi = 90^\circ, 270^\circ$ (refer Appendix) and it is given as

$$N\phi_{a_k,c_{max}} = \frac{V_{\mathrm{dc}}}{9f_c} \tag{H.39}$$

Let the common-mode flux be

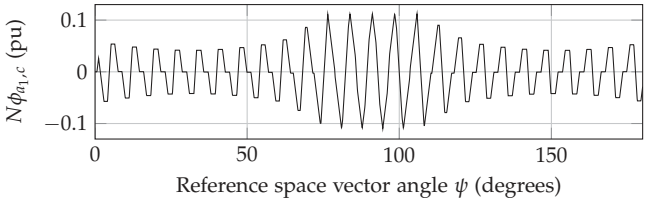


Fig. H.11: Flux linkage due to the circulating flux component in a half fundamental frequency cycle for $m = \sqrt{3}/2$. The flux linkage is normalized with respect to $V_{\mathrm{dc}}T_s$.

$$\phi_{CM_1} = \frac{\phi_{a_1} + \phi_{b_1} + \phi_{c_1}}{3} \tag{H.40}$$

After some mathematical manipulation, this can be represented as

$$\phi_{CM_1} = \frac{\phi_{a_1,c} + \phi_{b_1,c} + \phi_{c_1,c}}{3} \tag{H.41}$$

From (H.41), it is clear that the common-mode flux component ϕ_{CM_1} of VSC1 is composed of the circulating flux component of all the phases of that VSC. As the low reluctance path for the circulating flux component of each of the phase exists in the proposed structure, high value of the inductance for the common-mode circulating current is also achieved.

3.2.3 Maximum Flux in Various Parts of the Integrated Inductor

For the unity power factor applications considered in this paper, the resultant flux component $\phi_{a_k,l}$ reaches the maximum value at $\psi = 0^\circ$, whereas $\phi_{a_k,c}$ attains maximum value at $\psi = 90^\circ$. The total flux in the limbs of the integrated inductor is a vector sum of the $\phi_{a_k,l}$ and the $\phi_{a_k,c}$. Therefore, the maximum value of the flux in the limbs is given as

$$\phi_{a_{k_{max}}} = \max\Big(\phi_{a_k}\mid_{\psi=0^\circ}, \phi_{a_k}\mid_{\psi=90^\circ}\Big) \tag{H.42}$$

The circulating flux component at $\psi = 0^\circ$ is given as (refer Appendix)

$$\phi_{a_k,c}\mid_{\psi=0^\circ} = \begin{cases} \frac{V_{\rm dc}}{9Nf_c}, & 0 \leqslant M < \frac{4}{9} \\ \frac{(4-3M)V_{\rm dc}}{24Nf_c}, & \frac{4}{9} \leqslant M < \frac{2}{\sqrt{3}} \end{cases} \tag{H.43}$$

In most grid connected applications, the modulation index varies in a small range around 1. Once the range of the modulation index is defined, the maximum value of $\phi_{a_k,c}\mid_{\psi=0^\circ}$ can be obtained using (H.43). The flux in the limb at $\psi = 0^\circ$ can be obtained using (H.36) and (H.43) and it is given as

$$\phi_{a_k}\mid_{\psi=0^\circ} = \phi_{a_k,l_{max}} + \phi_{a_k,c}\mid_{\psi=0^\circ} \tag{H.44}$$

Similarly, the flux in the limb at $\psi = 90^\circ$ is given as

$$\phi_{a_k}\mid_{\psi=90^\circ} = \phi_{a_k,c_{max}} + \phi_{a_k,l}\mid_{\psi=90^\circ} \tag{H.45}$$

The value of the common component of the flux at $\psi = 90^\circ$ is

$$\phi_{a_k,l}\mid_{\psi=90^\circ} = \frac{V_{\rm dc}}{18Nf_c}\Big(\frac{2}{3} - \frac{\sqrt{3}M}{4}\Big) \tag{H.46}$$

Using (H.39), (H.45), and (H.46), the flux in the limb at $\psi = 90^\circ$ is given as

$$\phi_{a_k}\mid_{\psi=90^\circ} = \frac{V_{\rm dc}}{18Nf_c}\Big(\frac{8}{3} - \frac{\sqrt{3}M}{4}\Big) \tag{H.47}$$

Values of the $\phi_{a_k}\mid_{\psi=0^\circ}$ and $\phi_{a_k}\mid_{\psi=90^\circ}$ are calculated using (H.44) and (H.47), respectively. From these values, $\phi_{a_{k_{max}}}$ can be obtained using (H.42). The common flux component completes its path through the bridge yokes and corresponding legs of the other two phases. Therefore, the maximum value of the flux component in the bridge yokes is $\phi_{a_k,l_{max}}$ and can be obtained by using (H.36).

3.3 Design Methodology

The steps toward the design of the integrated inductor are described in this sub section.

3.3.1 Calculation of the Line Filter Inductance L_f

The required value of the line filter inductance L_f can be calculated based on the permissible value of the ripple component of the resultant line current and it is given as

$$L_f = \frac{V_{\mathrm{dc}}}{18\Delta I_{x,p_{max}} f_c}\left(\frac{2}{3} - \frac{\sqrt{3}M}{4}\right) \tag{H.48}$$

Let α be the ratio of the maximum current ripple to the peak value of the fundamental frequency component of the current and it can be written as

$$\alpha = \frac{\Delta I_{x,p_{max}}}{I_{x,p}} \tag{H.49}$$

Substituting (H.35) and (H.49) in (H.48), the inductance value at rated grid voltage can be obtained as

$$L_f = \frac{V_{\mathrm{dc}}}{18\alpha I_{x,p} f_c}\left(\frac{2}{3} - \frac{2\sqrt{6}V_{ph}}{4V_{\mathrm{dc}}}\right) \tag{H.50}$$

3.3.2 Area Product Requirement

The product of the cross section area of the limb $A_{c,l}$ and the window area A_w is referred to as an area product in this paper and it is used for the design of the integrated inductor.

The ripple component in the common flux component is very small compared to the ripple of the circulating flux component and its effect in the total flux can be neglected. In this case, the magnetic flux density in the limb at $\psi = 0^\circ$ and $\psi = 90^\circ$ can be obtained from (H.44) and (H.47), respectively. The values of the flux densities are

$$B_{a_k}\,|_{\psi=0^\circ} = \frac{2V_{\mathrm{dc}}(2+9\alpha) - 3\sqrt{6}V_{ph}(1+3\sqrt{3}\alpha)}{108N\alpha A_{c,l} f_c} \tag{H.51a}$$

$$B_{a_k}\,|_{\psi=90^\circ} = \frac{16V_{\mathrm{dc}} - 3\sqrt{6}V_{ph}}{108NA_{c,l} f_c} \tag{H.51b}$$

The values of the $B_{a_k}\,|_{\psi=0^\circ}$ and $B_{a_k}\,|_{\psi=90^\circ}$ should be less than the maximum allowable value of the flux density $B_{m,c}$. Each window in the integrated inductor receives two coils with the same number of turns. The circulating current is suppressed effectively and its contribution in the rms value of the

total current can be neglected. In this case, the number of turns can be expressed as

$$N = \frac{3K_w A_w J}{2I_x} \tag{H.52}$$

Using (H.51) and (K.54), the area product requirements to ensure that the maximum value of the flux density remains within the maximum allowable value $B_{m,c}$. These values can be expressed as

$$(A_{c,l}A_w)\mid_{\psi=0^\circ} = \frac{I_x\left[2V_{\mathrm{dc}}(2+9\alpha)-3\sqrt{6}V_{ph}(1+3\sqrt{3}\alpha)\right]}{162\alpha B_{m,c}K_w J f_c} \tag{H.53a}$$

$$(A_{c,l}A_w)\mid_{\psi=90^\circ} = \frac{I_x[16V_{\mathrm{dc}}-3\sqrt{6}V_{ph}]}{162B_{m,c}K_w J f_c} \tag{H.53b}$$

The area product requirement is given as

$$A_{c,l}A_w = \max\left((A_{c,l}A_w)\mid_{\psi=0^\circ}, (A_{c,l}A_w)\mid_{\psi=90^\circ}\right) \tag{H.54}$$

3.3.3 Core Selection for the Cell and Number of turns

Based on the computed value of the area product $A_{c,l}A_w$, the suitable core should be selected. Once the cross section area of the limb $A_{c,l}$ is know, the number of turns can be obtained from (H.51) and it can be given as

$$N = \frac{2V_{\mathrm{dc}}(2+9\alpha) - 3\sqrt{6}V_{ph}(1+3\sqrt{3}\alpha)}{108B_{m,c}\alpha A_{c,l} f_c} \tag{H.55}$$
$$\text{for } B_{a_k}\mid_{\psi=0^\circ} > B_{a_k}\mid_{\psi=90^\circ}$$

or

$$N = \frac{16V_{\mathrm{dc}} - 3\sqrt{6}V_{ph}}{108B_{m,c}A_{c,l} f_c} \tag{H.56}$$
$$\text{for } B_{a_k}\mid_{\psi=90^\circ} > B_{a_k}\mid_{\psi=0^\circ}$$

3.3.4 Core Selection for the Bridge Legs

The cross section area of the bridge leg is obtained from the (H.36) and it can be given as

$$A_{c,bl} = \frac{\phi_{a_k,l_{max}}}{B_{m,bl}} \tag{H.57}$$

3.3.5 Air Gap Geometry

The geometry of the air gap is obtained form (H.29) as

$$\frac{A_g}{l_g} = \frac{6L_f}{\mu_0 N^2} \tag{H.58}$$

Table H.1: System Specifications

Parameters	Values
No. of parallel VSCs n	3
Power P	15 kW
Switching frequency f_s	1.65 kHz
AC voltage (line-to-line)	400 V
DC-link voltage V_{dc}	650 V
Line filter inductor L_f	0.85 mH

Table H.2: Constants used for the design of the integrated inductor

Constants	α	$B_{m,c}$	$B_{m,bl}$	J	K_w	K_s
Values	0.2	0.9 T	1 T	2 A/mm^2	0.5	0.89

Table H.3: Parameters of the designed inductor. All dimensions are in mm. Unit of the area is mm^2. See Fig. H.4 for definitions.

Parameters	A, C, F	B	D	E	G	H	l_g	A_{cu}
Values	30	25	135	120	12	105	1.2	3.3

The air gap area A_g depends on the dimensions of the cell and the bridge legs, as shown in Fig. H.4. Once A_g is known, the value of l_g can be obtained using (H.58). In case of the requirement of the large air gap, several discrete air gaps can be realized using the core blocks that can be placed between the cells and the bridge yokes.

3.4 Design Example

An integrated inductor is designed for the three parallel interleaved VSCs. The system specifications are given in Table H.1. A laminated steel with 0.35 mm lamination thickness is used for the bridge yokes, whereas the cells are made up of amorphous metal alloy. Each of the coils has 81 number of turns ($N = 81$). Various constants, that are used in the design, are specified in Table H.2. The geometrical parameters of the designed integrated inductor, defined in Fig. H.4, are listed in Table H.3. The cell structure is realized using the rectangular blocks of the amorphous alloy and six inherent air gap exists in the cell structure. This would influence the value of the circulating current inductance $\boldsymbol{L_c}$. For the brevity, the analysis presented in section II assumes symmetrical cell structure, whereas the cell structure is asymmetrical in the realized integrated inductor. The circulating current inductance $\boldsymbol{L_c}$ of the

realized inductor is calculated using the finite element analysis and it is found to be

$$\boldsymbol{L_c} = \begin{bmatrix} 11.48 & -5.97 & -5.03 \\ -5.97 & 12.32 & -5.92 \\ -5.03 & -5.92 & 11.48 \end{bmatrix} \text{mH} \tag{H.59}$$

The inherent air gap is taken to be 0.15 mm for this finite element analysis.

3.5 Volumetric Comparison

The advantages offered by the proposed integrated inductor is demonstrated by comparing it with the system with three separate CIs and a three phase line filter inductor L_f. Such system is shown in Fig. H.1. Separate CI is used for each of the phases. For $n = 3$, three limb magnetic structure is required. Similarly, three limb magnetic structure is used for the line filter inductor. The area product approach is used to design these components as well. The maximum value of the flux density B_m and the current density J are assumed to be the same in both the cases.

3.5.1 Three Limb Coupled Inductor

Using (H.39) and (H.56), the area product of the CI is obtained as

$$(A_{c,CI} A_{w,CI}) = \frac{2 I_x V_{\text{dc}}}{27 B_{m,c} K_w J f_c} \tag{H.60}$$

For the integrated inductor, where $(A_{c,l} A_w) \mid_{\psi=0^\circ} < (A_{c,l} A_w) \mid_{\psi=90^\circ}$, the ratio of the area product of the integrated inductor to the area product of the CI can be obtained from (H.53) and (H.60) and it can be written as

$$\frac{(A_{c,l} A_w) \mid_{\psi=90^\circ}}{(A_{c,CI} A_{w,CI})} = 1 + \frac{4 - 3\sqrt{6}\frac{V_{ph}}{V_{\text{dc}}}}{12} \tag{H.61}$$

For the system parameters specified in Table H.1, the area product of the integrated inductor is 11.6% higher than that of the CI. However, the state-of-the-art solution requires line filter inductor L_f and the area product requirement of the L_f is discussed in the subsequent text.

3.5.2 Three Phase Line Filter Inductor L_f

The area product of the three phase line filter inductor L_f is given as

$$(A_{c,L_f} A_{w,L_f}) = \frac{I_x (4 V_{\text{dc}} - 3\sqrt{6} V_{ph})}{54 B_{m,bl} \alpha K_w J f_c} \tag{H.62}$$

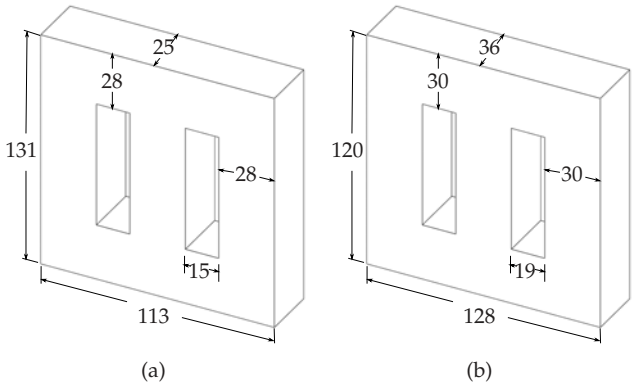


Fig. H.12: Dimensions of the magnetic cores in millimeter. (a) Coupled inductor, (b) Line filter inductor.

Table H.4: Coil parameters of the CI and L_f

Parameters	CI	L_f
No. of turns N	78	27
Required copper area A_{cu}	3.3 mm^2	10.52 mm^2

Table H.5: Volume comparison of integrated inductor with a combination of three CIs and L_f

Volume (in ltr.)	Integrated inductor	Three CIs + L_f	% Change
Copper	0.322	0.44	73%
Amorphous alloys	1.046	0.947	110%
Laminated steel	0.226	0.470	48%
Total	1.594	1.857	85%

Both the CI and three phase line filter inductor are designed using the area product approach. The dimensions of the magnetic cores are shown in Fig. H.12. The number of turns and the cross section area of the coil for both the CI and the three phase inductor L_f are given in Table H.4.

The volume of the different materials in case of both the solutions are calculated and the results are presented in Table I.5. For the system parameters considered in this paper, the use of integrated inductor results in a volume reduction of the copper by 27% and a volume reduction of the laminated steel by 52%. However, the volume of the amorphous alloys increases by 10%. The total volume the integrated inductor is 15% less than that of the

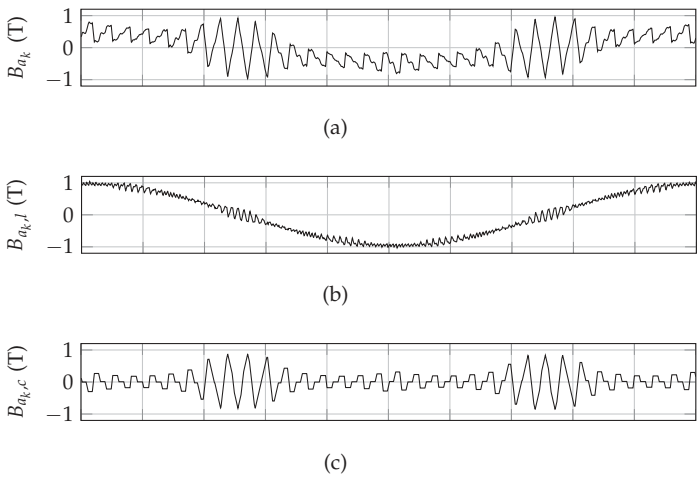


Fig. H.13: Flux density waveforms in various parts of the integrated inductor. (a) Flux density in the limb, (b) Flux density in the bridge leg, (c) Flux density in the yoke.

state-of-the-art solution.

4 Simulations and Experimental Results

4.1 Simulation Study

Time domain simulations have been carried out using the PLECS for the system parameters specified in Table H.1 and Table H.3. The flux density waveforms in various parts of the integrated inductor are shown in Fig. H.13. The flux in the limb of the integrated inductor is ensemble of the of the fundamental frequency flux component, the circulating flux component (with dominant frequency components at f_c and $2 \times f_c$), and the ripple component of the common flux (with dominant frequency component at $3 \times f_c$), as shown in Fig. H.13(a). Out of these, the common flux components flow through the bridge yokes, as shown in Fig. J.16, whereas the circulating flux component is mainly confined in the cell and flows through the yokes, as shown in Fig. H.13(c). The peak values of the flux density in various parts of the integrated inductor matches with the analysis presented in this paper. The simulated current waveforms are shown in Fig. H.14. The integrated inductor suppresses the circulating current and offers the desired inductance to the resultant line current as shown in Fig. H.14(b) and Fig. H.14(c), respectively.

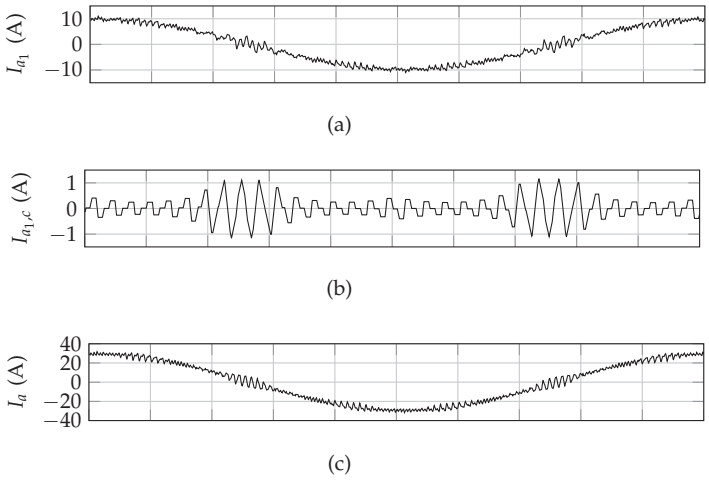


Fig. H.14: Current waveforms of phase a. (a) Leg current of VSC1, (b) Circulating current of VSC1, (c) Resultant line current.

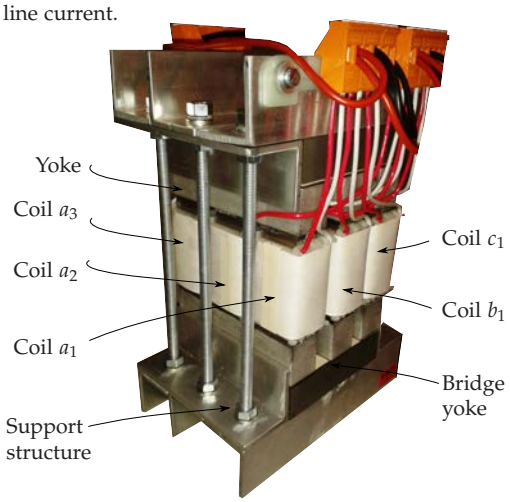
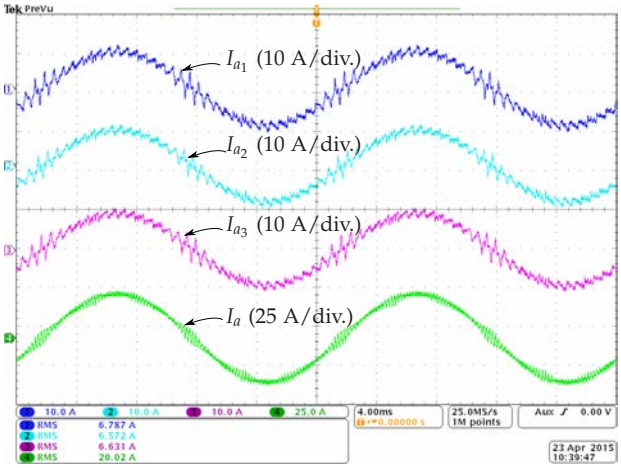


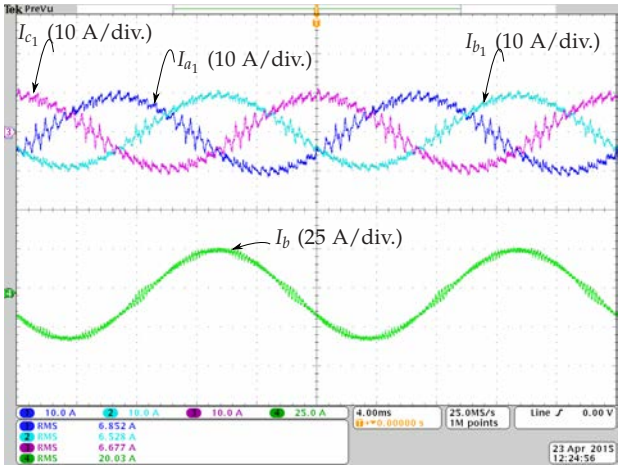
Fig. H.15: Photograph of the implemented integrated inductor.

4.2 Hardware Results

The integrated inductor was designed and built for the system specified in Table H.1 and the photograph of the implemented inductor is shown in Fig. I.12. The parameters of the integrated inductor are given in Table H.3. The cells were made from amorphous alloys, whereas laminated steel was used for the bridge legs. The coils are wound using the AWG 12 copper wire. The dc side of the three parallel VSCs were connected to the common dc sup-



(a)



(b)

Fig. H.16: Experimental waveforms. (a) Ch1: phase a current of VSC1 I_{a_1}, Ch2: phase a current of VSC2 I_{a_2}, Ch3: phase a current of VSC3 I_{a_3}, Ch4: Resultant line current of phase a I_a, (b) Ch1: phase a current of VSC1 I_{a_1}, Ch2: phase b current of VSC1 I_{b_1}, Ch3: phase c current of VSC3 I_{c_1}, Ch4: Resultant line current of phase b I_b.

ply of 650 V. The control was implemented using the TMS320F28346 floating point digital signal processor. The carrier signals of the three VSCs were interleaved by 120° and the line currents are sampled and the control loop is executed on every top and bottom update of each of the carrier signals.

The VSCs were operated to inject rated line current. The phase a cur-

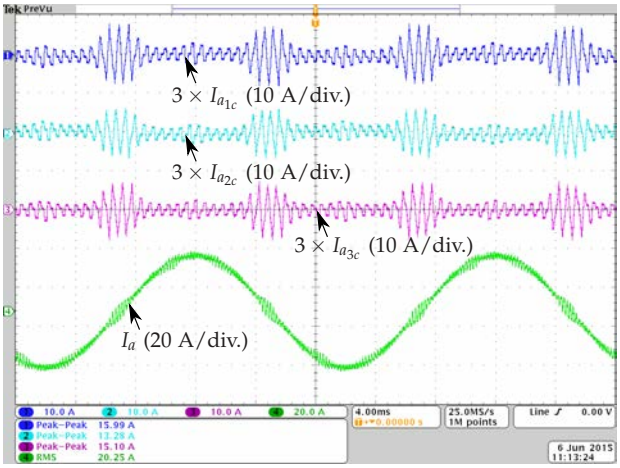


Fig. H.17: Experimental waveforms of the scaled circulating currents of phase a. The captured circulating current waveforms are $3 \times I_{a_{kc}}$. (a) Ch1: Scaled version of the circulating current of VSC1 ($3 \times I_{a_{1c}}$), Ch2: Scaled version of the circulating current of VSC2 ($3 \times I_{a_{1c}}$), Ch3: Scaled version of the circulating current of VSC3 ($3 \times I_{a_{1c}}$), Ch4: Resultant line current of phase a I_a.

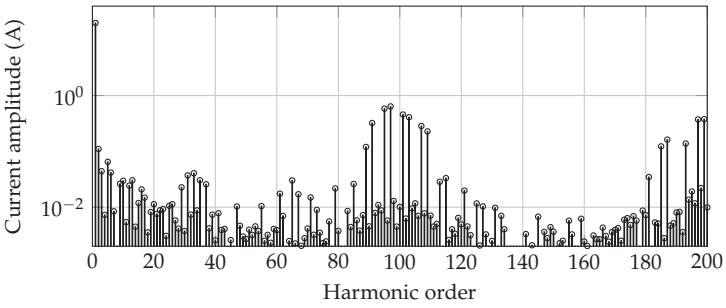


Fig. H.18: Harmonic spectra of the resultant line current I_a. Total harmonic distortion of the I_a is 4.85%.

rents of all the VSCs along with the resultant line current are shown in Fig. H.16(a). The integrated inductor offers desired line filtering to the resultant current, which is evident from Fig. H.16(a). The current waveforms of all three phases of the VSC1 are also shown in Fig. H.16(b). The circulating current component is defined as the $I_{a_{kc}} = I_{a_k} - (I_a/3)$. As it is difficult to measure these quantities, the scaled version is measured, which is three times more than the actual circulating current and it is measured by passing three turns of the conductor carrying I_{a_k} and one turn of the conductor carrying current I_a through the current probe. The difference of these two currents is

obtained by arranging these conductors in such a manner that the current in them flows in opposite direction to each other. The scaled version of the circulating current components of each of the VSCs ($3 \times I_{a_{kc}}$) are shown in Fig. H.17, which demonstrates that the integrated inductor effectively suppresses the circulating current. Peak value of the circulating current is restricted to 20% of the amplitude of the fundamental component of the rated value of the individual VSC current.

The harmonic spectra of the resultant line current I_a is shown in Fig. H.18. The major harmonic component appears at the $3 \times f_c$ and the magnitude of the harmonic components in the resultant line current is significantly small due to the inductance L_f offered by the integrated inductor. The total harmonic distortion of the I_a is measured to be 4.85 %, which proves the effectiveness of the integrated inductor.

5 Conclusion

An integrated inductor for parallel interleaved VSCs is presented in this paper. The proposed inductor integrates the functionality of three CIs and a three phase line filter inductor. The detailed analysis of the flux density distribution in various parts of the integrated inductor is presented and the analysis has been verified by the finite element analysis and the time domain simulations. The design methodology has been illustrated and the integrated inductor for the three parallel interleaved VSCs has been designed. The advantage offered by the integrated inductor in terms of the size reduction is demonstrated by comparing the volume of the integrated inductor with the state-of-the-art solution of using three CIs and the three phase line filter inductor. For the system considered in this paper, the total volume of the material is reduced by 15% by using the integrated inductor. The performance of the integrated inductor is also verified by carrying out the experimental measurements.

A Appendix

A.1 Derivation of Circulating Flux Component

For $n = 3$, the flux linkage of coil a_1 due to the circulating flux component is given by (H.38). The switched output voltages of phase a of individual VSCs (after multiplying the appropriate coefficients given in (H.38)) at the $\psi = 90^\circ$ are shown in Fig. H.19. The voltage that is responsible for the circulating flux component that links with the coil a_1 ($\frac{2}{3}V_{a_1o} - \frac{1}{3}V_{a_2o} - \frac{1}{3}V_{a_3o}$) is also shown. The time integral of this voltage gives the flux linkage and it is shown by the dashed line in Fig. H.19. The flux linkage achieves maximum value at time

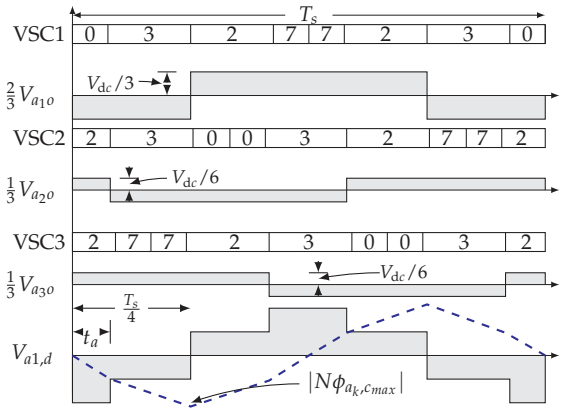


Fig. H.19: Switching sequences of all three VSCs and their pole voltages for the interleaving angle of 120° and space vector angle of $psi = 90°$. The voltage that is responsible for the circulating flux component that links with the coil a_1 ($V_{a1,d} = \frac{2}{3}V_{a_1o} - \frac{1}{3}V_{a_2o} - \frac{1}{3}V_{a_3o}$) is also shown. The numbers represent the time during which the corresponding voltage vectors are applied.

$t = T_s/4$. In this interval, the flux linkage can be described by the Piece-Wise Linear Equations (PWLE) and it is given as

$$\begin{aligned} N\phi_{a_1,c}(t)\mid_{\psi=90^\circ} &= N\phi_{a_1,c}(t_0) - \frac{2}{3}V_{\rm dc}t\,;\, 0 \le t < t_a \\ &= N\phi_{a_1,c}(t_a) - \frac{1}{3}V_{\rm dc}(t-t_a)\,;\, t_a \le t < \frac{T_s}{4} \end{aligned} \tag{H.63}$$

where $t_a = \frac{T_7}{2} + \frac{T_2}{2} - \frac{T_s}{6}$ and T_2 and T_7 are the dwell time of the voltage vectors $\overrightarrow{V}_2$ and $\overrightarrow{V}_7$, respectively. For the space vector angle $\psi = 0°$, $\frac{T_7}{2} + \frac{T_2}{2} = \frac{T_s}{4}$. Therefore, $t_a = \frac{T_s}{12}$. Substituting this value of t_a in (H.63) yields

$$\begin{aligned} N\phi_{a_1,c}(t_a)\mid_{\psi=90^\circ} &= -\frac{V_{\rm dc}T_s}{18} \\ N\phi_{a_1,c}(\frac{T_s}{4})\mid_{\psi=90^\circ} &= -\frac{V_{\rm dc}T_s}{9} \end{aligned} \tag{H.64}$$

Since the $N\phi_{a_1,c}(t)$ is maximum at $t = T_s/4$ for $\psi = 0°$, the maximum value of the peak flux linkage is given as

$$N\phi_{a_k,c_{max}} = \frac{V_{\rm dc}}{9f_c} \tag{H.65}$$

Similarly, the voltage that is responsible for the circulating flux component that links with the coil a_1 ($\frac{2}{3}V_{a_1o} - \frac{1}{3}V_{a_2o} - \frac{1}{3}V_{a_3o}$) for voltage space vector angle $\psi = 0°$ can be obtained. However, this voltage waveforms are different

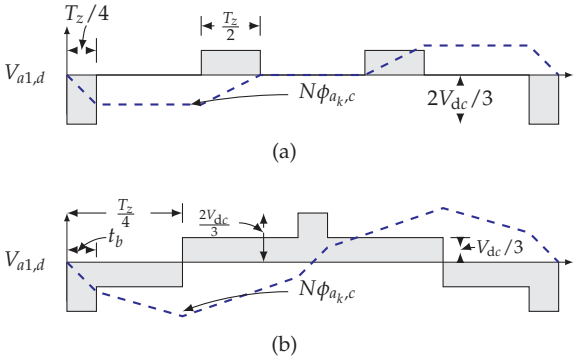


Fig. H.20: voltage that is responsible for the circulating flux component that links with the coil a_1 ($V_{a1,d} = \frac{2}{3}V_{a_1o} - \frac{1}{3}V_{a_2o} - \frac{1}{3}V_{a_3o}$) at voltage space vector angle $\psi = 0°$. T_z is the dwell time of the zero voltage vector. (a) $T_1 > T_s/3$, (b) $T_1 < T_s/3$.

for the $T_1 < T_s/3$ ($0 \leqslant M < \frac{4}{9}$) and for the $T_1 > T_s/3$ ($\frac{4}{9} \leqslant M < \frac{2}{\sqrt{3}}$). The voltage waveforms for both of these conditions are shown in Fig. H.20.

For the $T_1 > T_s/3$ ($\frac{4}{9} \leqslant M < \frac{2}{\sqrt{3}}$), the flux linkage is maximum at $t = T_z/4$ and its value is given as

$$N\phi_{a_1,c}(\frac{T_z}{4}) \mid_{\psi=0°} = \frac{1}{6}V_{\rm dc}T_z \tag{H.66}$$

where T_z is the dwell time of the zero voltage vector. For the space vector angle $\psi = 0°$, $T_z = T_s - T_1$ and $T_1 = \frac{3}{4}MT_s$. Substituting this values in (H.66), yields

$$\phi_{a_1,c} \mid_{\psi=0°} = \frac{(4-3M)V_{\rm dc}}{24Nf_c}\,,\ \frac{4}{9} \leqslant M < \frac{2}{\sqrt{3}} \tag{H.67}$$

For the $T_1 < T_s/3$ ($0 \leqslant M < \frac{4}{9}$), the flux linkage is maximum at $t = T_z/4$, as shown in Fig. H.20(b). The flux linkage can be described by the PWLE and it is given as

$$\begin{aligned} N\phi_{a_1,c}(t) \mid_{\psi=0°} &= N\phi_{a_1,c}(t_0) - \frac{2}{3}V_{\rm dc}t\,;\ 0 \leq t < t_b \\ &= N\phi_{a_1,c}(t_b) - \frac{1}{3}V_{\rm dc}(t-t_b)\,;\ t_b \leq t < \frac{T_z}{4} \end{aligned} \tag{H.68}$$

where t_b is given as

$$t_b = (\frac{1}{3} + \frac{3M}{4})\frac{T_s}{4} \tag{H.69}$$

and T_z is given as

$$T_z = (1 - \frac{3M}{4})T_s \tag{H.70}$$

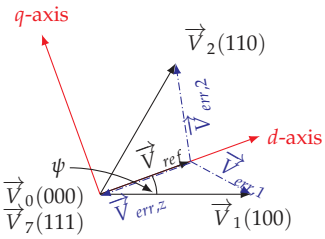


Fig. H.21: Active and zero vectors that are used to synthesize the reference voltage space vector of one of the VSCs and corresponding error voltage vectors.

substituting the values of t_b and T_z in (H.68) yields

$$\begin{aligned} N\phi_{a_1,c}(t_b)\mid_{\psi=0^\circ} &= -(\frac{1}{3}+\frac{3M}{4})\frac{V_{\rm dc}}{6f_c} \\ N\phi_{a_1,c}(\frac{T_z}{4})\mid_{\psi=0^\circ} &= -\frac{V_{\rm dc}}{9f_c}\,,\ 0 \leqslant M < \frac{4}{9} \end{aligned} \tag{H.71}$$

A.2 Derivation of Common Component of Flux

The VSC synthesize the reference voltage space vector using the discrete voltage vectors. Therefore at any given instant, an error between the applied voltage vector and the reference voltage vector exists. The error voltage vectors for a given sampling instance for one of the VSCs are shown in Fig. H.21. The time integral of the error voltage vectors gives the flux linkage of the line filter inductor. For the parallel interleaved VSCs, the flux linkage due to the ripple component of the common flux is the average of the time integral of the error voltage vectors of all three VSCs, as given in (H.26).

In the reference frame, rotating synchronously at the fundamental frequency, the instantaneous error voltage vectors can be decomposed into d-axis and the q-axis components and the decomposed error voltage vectors corresponding the active and zero vectors are given as

$$\begin{aligned} \overrightarrow{V}_{err,1} &= \frac{2}{3}V_{dc}\{(\cos\psi-\frac{3}{4}M)-j\sin\psi\} \\ \overrightarrow{V}_{err,2} &= \frac{2}{3}V_{dc}\{\cos(60^\circ-\psi)-\frac{3}{4}M+j\sin(60^\circ-\psi)\} \\ \overrightarrow{V}_{err,z} &= -\frac{1}{2}V_{dc}M \end{aligned} \tag{H.72}$$

where the real part represents the d-axis component of the error voltage vector and the q-axis component is represented by an imaginary part. The average of the time integration of the error voltage vectors gives the ripple component of the common flux linkage $\Delta\lambda_d$ and $\Delta\lambda_q$. The fundamental component

of the common flux appears as a dc component in the frame, rotating synchronously at the fundamental frequency. The dc components of both d-axis and q-axis (λ_D, λ_Q) flux are assumed to be constant during each sampling interval. Therefore, the d-axis and q-axis flux components in the rotating reference frame can be represented as

$$\lambda_d = \lambda_D + \Delta\lambda_d \text{ and } \lambda_q = \lambda_Q + \Delta\lambda_q \tag{H.73}$$

For the unity power factor applications, the dc components of both d-axis and q-axis fluxes are given as

$$\lambda_D = \lambda_p \text{ and } \lambda_Q = 0 \tag{H.74}$$

where λ_p is the peak value of the fundamental frequency flux component. Considering the three-phase symmetry, the flux linkage due to the common component of flux of phase a is only analyzes and it is given as

$$\lambda_a = \lambda_d \cos\psi - \lambda_q \sin\psi \tag{H.75}$$

In order to obtain the common component of the flux linkage with kth coil at $\psi = 90^\circ$, it is sufficient to only evaluate the q-axis flux components. Evaluating the q-axis flux components of individual VSCs and taking their average [11, 22] gives

$$N\phi_{a_k,l}\mid_{\psi=90^\circ} = \Delta\lambda_{q,avg}\mid_{\psi=90^\circ} = \frac{V_{\text{dc}}}{18f_c}\left(\frac{2}{3} - \frac{\sqrt{3}M}{4}\right) \tag{H.76}$$

similarly, the ripple component of the common flux component at $\psi = 0^\circ$ is obtained by evaluating only the d-axis flux component of individual VSCs and taking the average. For $M > 4/9$, it is given as

$$\Delta\lambda_{d,avg}\mid_{\psi=0^\circ} = \frac{V_{\text{dc}}}{3f_c}\left(\frac{5M}{8} - \frac{9M^2}{32} - \frac{1}{3}\right) \tag{H.77}$$

Using (H.77), the worst case value of the common flux component $\phi_{a_k,l_{max}}$ is evaluated.

References

[1] M. Baumann and J. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link current balancing," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042–3053, 2007.

[2] B. Andresen and J. Birk, "A high power density converter system for the gamesa G10x 4,5 MW wind turbine," in *Proc. European Conference on Power Electronics and Applications, 2007*, Sept 2007, pp. 1–8.

[3] H. Zhang and L. Tolbert, "Efficiency impact of silicon carbide power electronics for modern wind turbine full scale frequency converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 21–28, Jan 2011.

[4] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[5] J. Muhlethaler, M. Schweizer, R. Blattmann, J. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, 2013.

[6] M. Liserre, R. Cardenas, M. Molinas, and J. Rodriguez, "Overview of multi-MW wind turbines and wind parks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1081–1095, April 2011.

[7] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[8] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[9] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[10] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[11] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[12] K. Xing, F. Lee, D. Borojevic, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, 1999.

[13] Z. Xu, R. Li, H. Zhu, D. Xu, and C. Zhang, "Control of parallel multiple converters for direct-drive permanent-magnet wind power generation systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1259–1270, March 2012.

[14] H. Akagi, A. Nabae, and S. Atoh, "Control strategy of active power filters using multiple voltage-source PWM converters," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 3, pp. 460–465, 1986.

[15] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[16] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[17] F. Forest, T. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire, "Optimization of the supply voltage system in interleaved converters using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 934–942, 2007.

[18] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[19] J. Salmon, J. Ewanchuk, and A. Knight, "PWM inverters using split-wound coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2001–2009, 2009.

[20] R. Hausmann and I. Barbi, "Three-phase DC-AC converter using four-state switching cell," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1857–1867, July 2011.

[21] D. Zhang, F. Wang, R. Burgos, and D. Boroyevich, "Total flux minimization control for integrated inter-phase inductors in paralleled, interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1679–1688, 2012.

[22] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Modified discontinuous pwm for size reduction of the circulating current filter in parallel interleaved converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3457–3470, July 2015.

[23] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Design of the trap filter for the high power converters with parallel interleaved VSCs," in *Proc. 40th Annual Conference on IEEE Industrial Electronics Society, IECON 2014*, Oct 2014, pp. 2030–2036.

[24] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[25] G. Gohil, L. Bede, R. Maheshwari, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Parallel interleaved VSCs: influence of the PWM scheme on the design of the coupled inductor," in *Proc. 40th Annual Conference on IEEE Industrial Electronics Society, IECON 2014*, Oct 2014, pp. 1693–1699.

Paper I

Magnetic Integration for Parallel Interleaved VSCs Connected in a Whiffletree Configuration

Ghanshyamsinh Gohil,
Lorand Bede,Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been published in the
IEEE Transactions on Power Electronics [Online early access], DOI:
10.1109/TPEL.2015.2514182, 2016.

The layout has been revised.

Abstract

The Voltage Source Converters (VSCs) are often connected in parallel to realize a high current rating. In such systems, the harmonic quality of the output voltage can be improved by interleaving the carrier signals of the parallel VSCs. However, an additional inductive filter is often required to suppress the circulating current that flows between the parallel interleaved VSCs. One of the ways to deal with the circulating current problem is to use the coupled inductors in a whiffletree configuration. This paper proposes the integration of the line filter inductor and the circulating current filter inductor in a single magnetic component for such systems. The fundamental frequency component of the flux is mostly confined to the limbs around which the coils are placed, whereas other parts of the magnetic structure only experiences high frequency flux excitation. As a result, the integrated inductor can be made smaller and the power density of the overall converter system can be increased. The magnetic structure of the integrated inductor is analyzed and performance is verified by simulation and experimental studies.

1 Introduction

In many high power applications, the two-level Voltage Source Converters (VSCs) are normally connected in parallel to meet the high current requirement and often share the common dc-link, as shown in Fig. I.1. The Silicon Insulated Gate Bipolar Transistors (IGBTs) are normally used in high power applications and they suffer from excessive losses if the switching frequency is increased beyond a few kHz. Due to the this limitation, large passive filter components are generally employed to comply with the stringent power quality requirements. This lead to the increased cost, size and losses. Therefore the efforts are being made to reduce the size of these components. For a given switching frequency, one of the ways to reduce the filtering requirement is to employ a multi-level VSC.

For the parallel connected two-level VSCs, multi-level voltage waveforms can be achieved by interleaving the carrier signals. As a result of the interleaved carriers, some of the harmonic frequency components present in the switched output voltage of the parallel interleaved legs are phase shifted with respect to each other [1–7]. For the parallel connected VSCs, the output voltage of a given phase is the average of the switched output voltages of all parallel VSC legs of that phase. As a result of the averaging, the contribution of the phase shifted harmonic frequency components of the individual switched output voltages is fully or partially canceled in the resultant voltage [8], which leads to the reduction in the value of the filter components [9].

When connected to a common dc-link, the circulating current flows between the parallel VSCs due to the hardware and control asymmetries [10], as

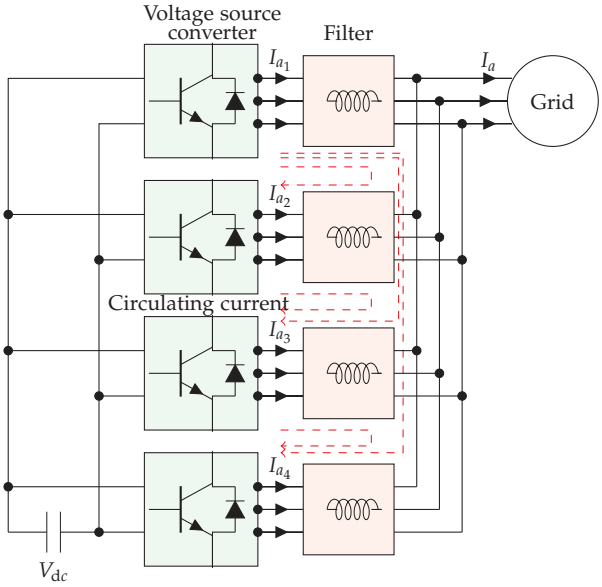


Fig. I.1: Parallel voltage source converters with a common dc-link and output filters.

shown in Fig. I.1, where four VSCs are connected in parallel and shares the same dc-link. Five-level resultant voltage waveforms for each of the phases can be achieved by interleaving the carrier signals of these four parallel VSCs. However, the interleaving of the carrier signals further aggravates the already existing problem of the circulating current [7]. This unwanted circulating current increases the losses in both the semiconductor devices and in the passive components and it should be suppressed. An additional inductive filter is often required for this purpose. One of the solutions is to use a Coupled Inductor (CI). The CI can be designed to provide magnetic coupling between the parallel interleaved legs of the corresponding phases [1, 11–16]. By choosing a proper value of the magnetic coupling coefficient, desired value of the inductance can be offered to the circulating current component. In the case of the four parallel VSCs, the CIs are often connected in a whiffletree configurations, as proposed in [1] and reproduced in Fig. I.2(b). Such arrangement requires two distinct inductive component:

1. Line filter inductor (L_f) for improving the injected line current quality.
2. CIs for suppressing the circulating current.

Although the interleaved carrier signals leads to the reduction in the value of the line filter inductor L_f, additional filter components (CIs) are often required, as shown in Fig. I.2(b). The volume of these inductive components

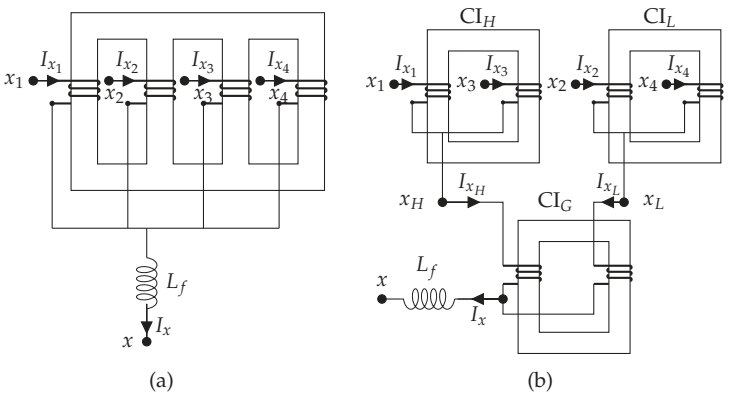


Fig. I.2: Various arrangements of the filters for four parallel interleaved VSCs. (a) CI with four limb core structure, (b) Whiffletree configuration using the two limb CIs. The subscript x represents phases $x = \{a, b, c\}$.

can be reduced by integrating both of these functionalities into a single magnetic component. This paper proposes the magnetic integration of the line filter inductor L_f and the circulating current filters (which mainly experiences the switching frequency flux excitation) for a four parallel interleaved VSCs. The VSCs are divided into two converter groups and the carrier signals of the VSCs within each group are shifted by 180°. In addition, the carrier signals of the VSCs of both the converter groups are also phase-shifted with respect to each other. Therefore, the circulating current flows between the VSCs of each of the converter group as well as between the two converter groups. The proposed integrated inductor offers desired line filter inductance L_f and also suppresses the circulating current between the VSCs within each of the converter groups. The circulating current between the converter groups is suppressed using an additional CI (referred to as a CI_G).

The paper is organized as follow: The issue of the circulating current and the overview of the existing filtering solutions are briefly discussed in Section II. The proposed integrated inductor is analyzed in Section III. The design equations of the coupled inductor that are used for circulating current suppression between the two converter groups are discussed in Section IV. The volume reduction achieved by the proposed solution is demonstrated in Section V, by comparing its volume with that of the state-of-the-art solution. The functionality of the integrated inductor is verified by performing simulation and experimental studies and the results are presented in Section VI.

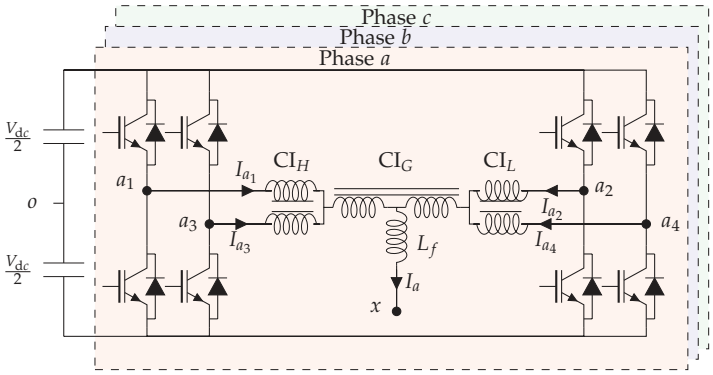


Fig. I.3: Whiffletree configuration for parallel interleaved voltage source converters [1].

2 Circulating Current in a Parallel Interleaved VSCs

The switched output voltages of the parallel legs are phase shifted with respect to each other due to the interleaved carriers. When VSCs are connected to the common dc-link, this instantaneous potential difference appears across the closed path and gives rise to the circulating current. In order to reduce the losses, the circulating should be suppressed to some acceptable limit. The reduction in the circulating current can be achieved by introducing sufficiently high inductance in the circulating current path. The CI is typically used for this purpose [1, 11–16]. It provides magnetic coupling between the interleaved legs of a particular phase and offers high inductance to the circulating current, while its effect on the line current is minimal (considering negligible flux leakage).

The various possible arrangements of the CI for four parallel VSCs are shown in Fig. I.2. Fig. I.2(a) shows the magnetic structure of the CI with four parallel limbs. This magnetic structure is asymmetrical (for more than two limbs). The symmetry can be achieved by using a whiffletree configuration, as shown in Fig. I.2(b). Two limb CI is used as a basic building block and the system arrangement, such as shown in Fig. I.3, can be realized using it. Two interleaved VSC legs of a respective phase are magnetically coupled using the CI_H, whereas CI_L used to couple remaining two VSC legs (refer Fig. I.3). The magnetic coupling between these two groups is achieved using the third CI (CI_G). One of the main advantages of the whiffletree configuration is the magnetically symmetrical structure of all CIs. However, it can only be only used for the even number of parallel VSCs. The integrated inductor is proposed for four parallel VSCs, which combines the functionality of the line filter inductor L_f and the CI_H and the CI_L (refer Fig. I.2(b)) and it is

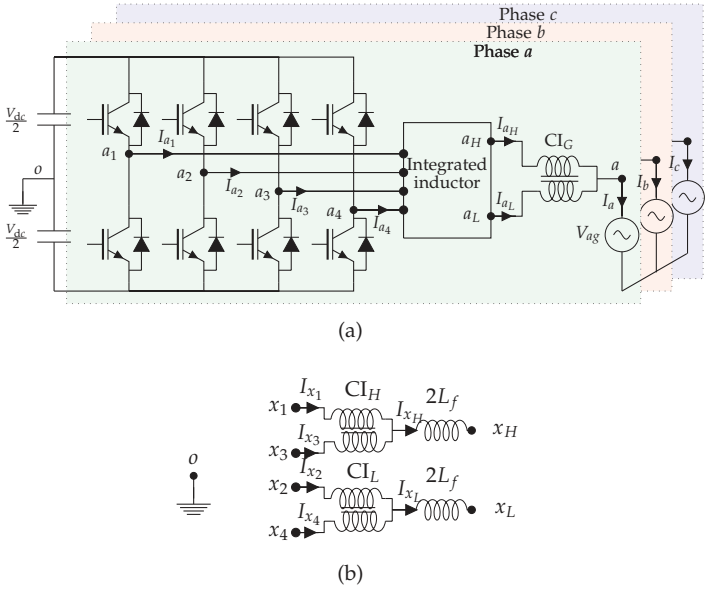


Fig. I.4: Four parallel interleaved VSCs with the proposed integrated inductor. (a) System schematic, (b) Equivalent electrical model of the integrated inductor. The subscript x represents phases $x = \{a, b, c\}$

presented in the following Section.

3 Integrated Inductor

The system comprises of four parallel VSCs with the proposed integrated inductor is shown in Fig. I.4(a). All four VSCs share a common dc-link and the carrier signals are symmetrically interleaved, i.e. the carrier signals are phase shifted from each other by 90°. The carrier signals of the VSC1 and VSC3 are phase shifted by 180° from each other and these two VSCs form the High-Side Converter Group (HSCG). Similarly, VSC2 and VSC4 forms the Low-Side Converter Group (LSCG), and use the carrier signals that are phase shifted from each other by 180°.

The proposed integrated inductor for such systems is shown in Fig. I.5, where two different core geometries are shown. The magnetic structure comprises of two cells. The cell is a two limb CI structure and each limb carries a coil with N number of turns. Both of these coils in the given cell are wound in the same direction. The limbs are magnetically coupled to each other using the top and the bottom yokes.

Out of these two cells, one of the cells magnetically couples the interleaved

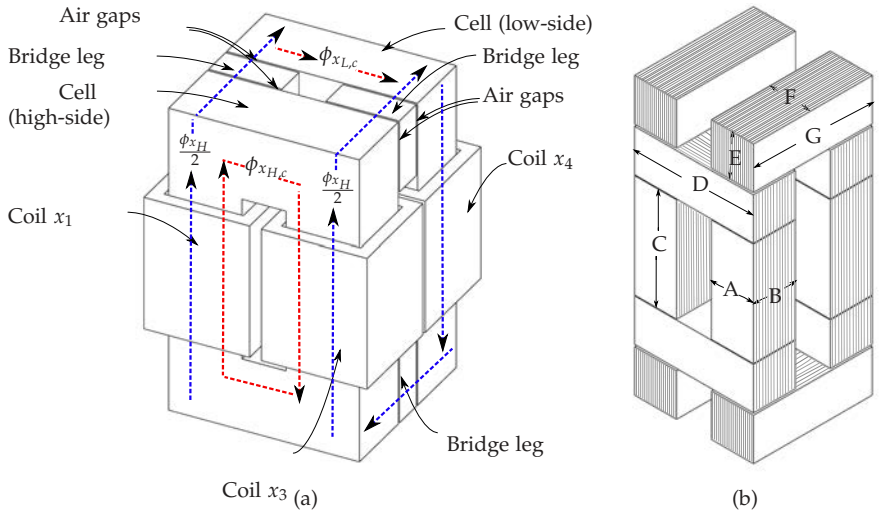


Fig. I.5: Magnetic structures of the proposed integrated inductor. Two different arrangements of the bridge legs are shown. Based on the direction of the laminations, one of the arrangement can be used. The subscript x represents the phase, $x = \{a, b, c\}$ (a) Suitable for the ferrite cores. It can be also used when the cells are made from the tape wound core, (b) Suitable for the laminated cores.

legs of the respective phases of the HSCG, whereas the other cell belongs to the LSCG. The input terminals of the coils of the high-side cell are connected to the output of VSC1 (x_1) and VSC3 (x_3) and the output terminals of these coils are connected together to form the common output x_H. Similarly, the output of VSC2 (x_2) and VSC4 (x_4) are connected to the input terminal of the coils of the low-side cell. Whereas, the other end of the coils are connected together to form the common output terminal x_L. The winding direction of the coils of the high-side cell is opposite to that of the coils of the low-side cell. The high-side and the low-side cells are magnetically coupled to each other using the bridge legs, as shown in Fig. I.5(a). The necessary air gaps have been inserted between the cells and the bridge legs. The output terminals of the HSCG and the LSCG are connected to another CI (CI_G), as shown in Fig. I.4(a).

3.1 Magnetic Circuit Analysis

The integrated inductor is analyzed in this sub section. Due to the phase symmetry, the analysis is presented for one of the phases, which is denoted by the subscript x. For the brevity, the permeability of the magnetic material is assumed to be constant and the leakage flux is neglected. For the system

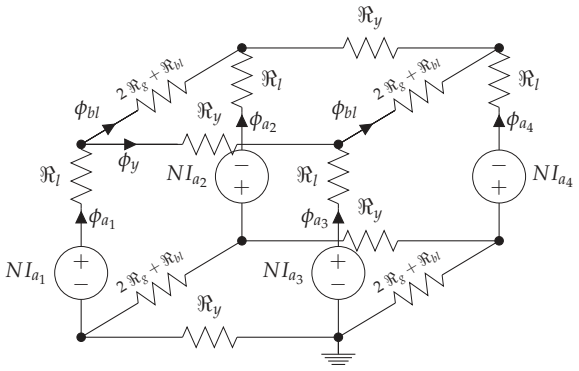


Fig. I.6: Simplified reluctance model of the proposed integrated inductor.

shown in Fig. I.4(a), the voltage across the coil x_1 is given as

$$V_{x_1x_H} = L_{x_1x_1}\frac{dI_{x_1}}{dt} + L_{x_1x_2}\frac{dI_{x_2}}{dt} + L_{x_1x_3}\frac{dI_{x_3}}{dt} + L_{x_1x_4}\frac{dI_{x_4}}{dt} \tag{I.1}$$

where $L_{x_jx_k}$ is the inductance between the jth and the kth coil of the integrated inductor of phase x and I_{x_n} is the current flowing through the nth coil of phase x. The simplified reluctance model of the integrated inductor is shown in Fig. I.6. The reluctance of each of the limbs and the yoke of the cell are represented by $\Re_l$ and $\Re_y$, respectively. The reluctance of the bridge leg is $\Re_{bl}$, whereas the reluctance of each of the air gaps is denoted by $\Re_g$. The magneto-motive force of the coil is represented as NI_{x_n}, where N is the number of turns.

By solving the reluctance network, the flux in each limb can be obtained as

$$\overrightarrow{\boldsymbol{\phi}} = \frac{1}{\Re_l}\boldsymbol{R}\left(\frac{1}{\Re_l}\boldsymbol{A} + \boldsymbol{R^{-1}}\right)\overrightarrow{\boldsymbol{M}} \tag{I.2}$$

where $\boldsymbol{A}$ is the unit matrix,

$$\overrightarrow{\boldsymbol{\phi}} = \begin{bmatrix}\phi_{x_1} & \phi_{x_2} & \phi_{x_3} & \phi_{x_4}\end{bmatrix}^T \tag{I.3}$$

$$\overrightarrow{\boldsymbol{M}} = \begin{bmatrix}NI_{x_1} & -NI_{x_2} & NI_{x_3} & -NI_{x_4}\end{bmatrix}^T \tag{I.4}$$

$$\boldsymbol{R} = \begin{bmatrix} \frac{1}{\Re_{eq}} & -\frac{1}{\Re_2} & -\frac{1}{\Re_1} & 0 \\ -\frac{1}{\Re_2} & \frac{1}{\Re_{eq}} & 0 & -\frac{1}{\Re_1} \\ -\frac{1}{\Re_1} & 0 & \frac{1}{\Re_{eq}} & -\frac{1}{\Re_2} \\ 0 & -\frac{1}{\Re_1} & -\frac{1}{\Re_2} & \frac{1}{\Re_{eq}} \end{bmatrix} \tag{I.5}$$

where $\Re_1 = 2\Re_y$, $\Re_2 = 4\Re_g + 2\Re_{bl}$, and $\frac{1}{\Re_{eq}} = \frac{1}{\Re_1} + \frac{1}{\Re_2}$. The reluctance of the air gap is very large compared to the reluctance of the bridge legs

($\Re_g >> \Re_{bl}$). Therefore $\Re_2 \approx 4\Re_g$. The limbs and the yokes of the cell are made from the same magnetic material and let $\Re_1$ to be equal to $\alpha\Re_l$. The flux linking with each of the coils is obtained by solving (I.2) and the inductances between the coils are obtained from the associated flux linkages. For most of the commercially available cell structures, the ratio of the window height to window width varies from 2 to 3. In this case, α can be safely assumed to be equal to 1. With $\alpha = 1$, the inductance values are obtained as

$$\begin{aligned}
L_{x_1x_1} &= L_S = \frac{N^2(2\Re_1^2 + 13\Re_1\Re_g + 12\Re_g^2)}{3\Re_1(\Re_1 + 2\Re_g)(\Re_1 + 6\Re_g)} \\
L_{x_1x_2} &= L_{M_1} = \frac{N^2(\Re_1 + 5\Re_g)}{3(\Re_1 + 2\Re_g)(\Re_1 + 6\Re_g)} \\
L_{x_1x_3} &= L_{M_2} = -\frac{N^2(\Re_1^2 + 8\Re_1\Re_g + 24\Re_g^2)}{6\Re_1(\Re_1 + 2\Re_g)(\Re_1 + 6\Re_g)} \\
L_{x_1x_4} &= L_{M_3} = \frac{N^2(\Re_1 + 8\Re_g)}{6(\Re_1 + 2\Re_g)(\Re_1 + 6\Re_g)}
\end{aligned} \tag{I.6}$$

Substituting these inductance values in (I.1) yields

$$\begin{aligned}
V_{x_1x_H} &= V_{x_1o} - V_{x_Ho} \\
&= L_S\frac{dI_{x_1}}{dt} + L_{M_1}\frac{dI_{x_2}}{dt} + L_{M_2}\frac{dI_{x_3}}{dt} + L_{M_3}\frac{dI_{x_4}}{dt}
\end{aligned} \tag{I.7}$$

Using the same procedure for the remaining coils, the voltage across each of the coils are obtained as

$$\overrightarrow{\boldsymbol{V_c}} = \boldsymbol{L}\frac{d\,\overrightarrow{\boldsymbol{I_c}}}{dt} \tag{I.8}$$

where

$$\begin{aligned}
\overrightarrow{\boldsymbol{V_c}} &= \begin{bmatrix} V_{x_1x_H} & V_{x_2x_L} & V_{x_3x_H} & V_{x_4x_L} \end{bmatrix}^T \\
&= \begin{bmatrix} V_{x_1o} - V_{x_Ho} & V_{x_2o} - V_{x_Lo} & V_{x_3o} - V_{x_Ho} & V_{x_4o} - V_{x_Lo} \end{bmatrix}^T
\end{aligned} \tag{I.9}$$

$$\overrightarrow{\boldsymbol{I_c}} = \begin{bmatrix} I_{x_1} & I_{x_2} & I_{x_3} & I_{x_4} \end{bmatrix}^T \tag{I.10}$$

and

$$\boldsymbol{L} = \begin{bmatrix} L_S & L_{M_1} & L_{M_2} & L_{M_3} \\ L_{M_1} & L_S & L_{M_3} & L_{M_2} \\ L_{M_2} & L_{M_3} & L_S & L_{M_1} \\ L_{M_3} & L_{M_2} & L_{M_1} & L_S \end{bmatrix} \tag{I.11}$$

Each of the coil currents has two distinct components

1. Common current component that contributes to the output current

2. Circulating current component

The sum of the common current component of each of the VSCs withing the converter group constitutes the output current of the corresponding converter group. Therefore, the output currents of the HSCG and the LSCG are

$$\begin{aligned} I_{x_H} &= I_{x_1} + I_{x_3} \\ I_{x_L} &= I_{x_2} + I_{x_4} \end{aligned} \tag{I.12}$$

Assuming equal current sharing between the VSCs, the common component of each of the VSCs is taken to be the same. Therefore, the output current of the individual VSCs are given as

$$\begin{aligned} I_{x_1} &= \frac{I_{x_H}}{2} + I_{x_{H,c}} \\ I_{x_3} &= \frac{I_{x_H}}{2} - I_{x_{H,c}} \\ I_{x_2} &= \frac{I_{x_L}}{2} + I_{x_{L,c}} \\ I_{x_4} &= \frac{I_{x_L}}{2} - I_{x_{L,c}} \end{aligned} \tag{I.13}$$

where $I_{x_{H,c}}$ and $I_{x_{L,c}}$ are the circulating current between the VSCs of the HSCG and the LSCG, respectively and given as

$$I_{x_{H,c}} = \frac{I_{x_1} - I_{x_3}}{2} \tag{I.14}$$

similarly

$$I_{x_{L,c}} = \frac{I_{x_2} - I_{x_4}}{2} \tag{I.15}$$

The sum of the output currents of the HSCG and the LSCG constitutes the resultant line current and it is given as

$$I_x = I_{x_L} + I_{x_H} \tag{I.16}$$

and the circulating current between the high-side and the low-side converter groups is given as

$$I_{x,c} = \frac{I_{x_H} - I_{x_L}}{2} \tag{I.17}$$

The circulating current between the HSCG and the LSCG ($I_{x,c}$) is suppressed using the CI_G.

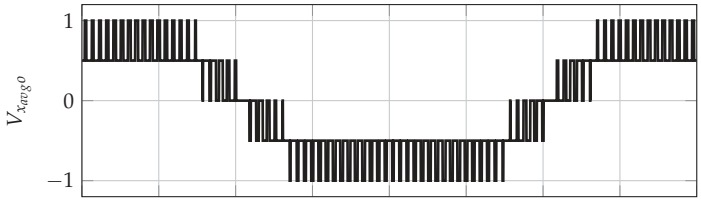


Fig. I.7: Voltage waveform of an average voltage $V_{x_{avg}o}$, which exhibits five-level voltage waveforms. The VSCs are modulated using the space vector modulation with the modulation index $m = 0.8$. The average voltage is normalized to half of the dc-link voltage $\frac{V_{dc}}{2}$.

3.2 Inductance Offered by the Integrated Inductor

Using the induced voltages given in (I.8) and averaging the switched output voltages of the VSCs of the HSCG gives

$$\left(\frac{V_{x_1o} + V_{x_3o}}{2}\right) - V_{x_Ho} = \left(\frac{L_S + L_{M_2}}{2}\right)\frac{d(I_{x_1} + I_{x_3})}{dt} + \left(\frac{L_{M_1} + L_{M_3}}{2}\right)\frac{d(I_{x_2} + I_{x_4})}{dt} \tag{I.18}$$

similarly, averaging the switched output voltages of the VSCs of the LSCG yields

$$\left(\frac{V_{x_2o} + V_{x_4o}}{2}\right) - V_{x_Lo} = \left(\frac{L_{M_1} + L_{M_3}}{2}\right)\frac{d(I_{x_1} + I_{x_3})}{dt} + \left(\frac{L_S + L_{M_2}}{2}\right)\frac{d(I_{x_2} + I_{x_4})}{dt} \tag{I.19}$$

Using (I.12) and averaging (I.18) and (I.19) yields

$$V_{x_{avg}o} - V_{xo} = \left(\frac{L_S + L_{M_1} + L_{M_2} + L_{M_3}}{4}\right)\frac{d(I_{x_H} + I_{x_L})}{dt} \tag{I.20}$$

where

$$V_{x_{avg}o} = \frac{1}{4}\sum_{k=1}^{4} V_{x_ko} \tag{I.21}$$

and

$$V_{xo} = \frac{V_{x_Ho} + V_{x_Lo}}{2} \tag{I.22}$$

The waveform of the average voltage $V_{x_{avg}o}$ is shown in Fig. I.7. The $V_{x_{avg}o}$ exhibits five-level voltage waveforms and the voltage difference of $V_{x_{avg}o} - V_{xo}$ appears across the integrated inductor. The integrated inductor offers desired value of the inductance L_f to the line current I_x and it the the voltage $V_{x_{avg}o} - V_{xo}$ along with the L_f determines the ripple content in the I_x. The dynamic behavior of the I_x can be represented as

$$V_{x_{avg}o} - V_{xo} = L_f\frac{dI_x}{dt} \tag{I.23}$$

Using (I.16) and (I.20), the line filter inductance can be obtained as

$$L_f = \frac{L_S + L_{M_1} + L_{M_2} + L_{M_3}}{4} = \frac{N^2}{4(\Re_1 + 2\Re_g)} = \frac{N^2}{8\Re_g(1 + \frac{\Re_1}{2\Re_g})} \tag{I.24}$$

As $\Re_g >> \Re_1$, the line filter inductance can be approximated as

$$L_f = \frac{\mu_0 N^2 A_g^{'}}{8 l_g} \tag{I.25}$$

where μ_0 is the permeability of the free space, l_g is the length of the air gap, and $A_g^{'}$ is the effective cross-section area of the air gap. The effective cross-sectional area of the air gap $A_{g'}$ is obtained by evaluating the cross-section area of the air gap after adding l_g to each dimension in the cross-section.

The switched output voltage difference of VSC1 and VSC3 ($V_{x_1o} - V_{x_3o}$) drives the $I_{a_H,c}$. Similarly, the behavior of the $I_{a_L,c}$ depends on the difference of the switched output voltages of VSC2 and VSC4 ($V_{x_2o} - V_{x_4o}$). Using (I.8), the difference of the switched output voltages of the VSC1 and VSC3 ($V_{x_1o} - V_{x_3o}$) is obtained as

$$V_{x_1o} - V_{x_30} = (L_s - L_{M_2})\frac{d(I_{x_1} - I_{x_3})}{dt} + (L_{M_1} - L_{M_3})\frac{d(I_{x_2} - I_{x_4})}{dt} \tag{I.26}$$

Using (I.6), (I.26), (I.14), and (I.15), the inductance offered to the circulating currents is given as

$$\begin{bmatrix} V_{x_1o} - V_{x_30} \\ V_{x_2o} - V_{x_40} \end{bmatrix} = \boldsymbol{L_c}\frac{d}{dt}\begin{bmatrix} I_{x_{H,c}} \\ I_{x_{L,c}} \end{bmatrix} \tag{I.27}$$

where the circulating current inductance matrix $\boldsymbol{L_c}$ is given as

$$\boldsymbol{L_c} = 2\begin{bmatrix} L_s - L_{M_2} & L_{M_1} - L_{M_3} \\ L_{M_1} - L_{M_3} & L_s - L_{M_2} \end{bmatrix} \tag{I.28}$$

where $L_s - L_{M_2} = \frac{2N^2}{3\Re_1}$ and $L_{M_1} - L_{M_3} = \frac{N^2}{36\Re_g}$. As $\Re_g >> \Re_1$, the circulating current inductance matrix can be approximated as

$$\boldsymbol{L_c} \approx 2\begin{bmatrix} \frac{2N^2}{3\Re_1} & 0 \\ 0 & \frac{2N^2}{3\Re_1} \end{bmatrix} \tag{I.29}$$

3.3 Flux Density Analysis

The integrated inductor combines the functionalities of two CIs (CI_H and CI_L) and the line filter inductor L_f. Therefore, the flux in the magnetic core has distinct components corresponding to these inductances and it is analyzed in this sub section.

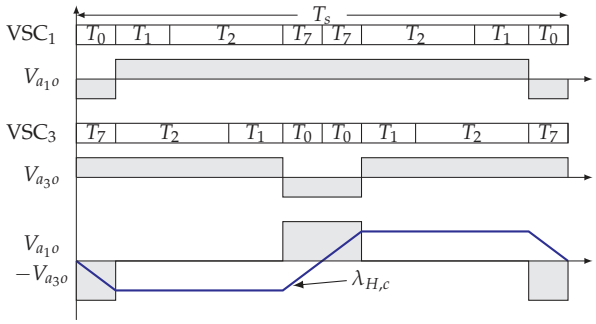


Fig. I.8: Pole voltages of phase a of VSC1 and VSC3 and their difference for space vector modulation. The modulation index $M = 1$ and voltage space vector angle $\psi = 45°$. Time T_o, T_1, T_2, and T_7 are the dwell times of the corresponding voltage vectors.

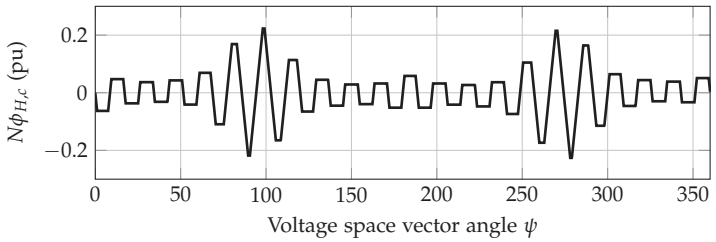


Fig. I.9: Circulating flux component $\lambda_{H,c}$ over a complete fundamental period. The flux linkage is normalized to $V_{\mathrm{dc}} T_s$.

3.3.1 Circulating Flux Component

The circulating flux linkage in the HSCG cell can be obtained as [17, 18]

$$\lambda_{x_{H,c}} = N\phi_{x_{H,c}} = \frac{1}{2}\int (V_{x_1o} - V_{x_3o})\, dt \tag{I.30}$$

where $\phi_{x_{H,c}}$ is the circulating flux component in the high-side cell of the integrated inductor. The carrier signals of the VSC1 and VSC3 are interleaved by 180° and the corresponding voltages for a particular switching cycle is shown in Fig. I.8. The VSCs are modulated using the space vector modulation [19]. Due to the change in the dwell time of the voltage vectors in each sampling interval, the peak value of the $\lambda_{x_{H,c}}$ also attains different values in each of the sampling intervals, as shown in Fig. I.9. The $\lambda_{x_{H,c}}$ achieves the maximum value for the voltage space vector angle $\psi = 90°$ (and $\psi = 270°$), as shown in Fig. I.9 and it is obtained as

$$\lambda_{x_{H,cmax}} = N\phi_{x_{H,cmax}} = \frac{V_{\mathrm{dc}}}{8 f_s} \tag{I.31}$$

where V_{dc} is the dc-link voltage, f_s is the switching frequency, and $\phi_{H,c_{max}}$ is the maximum value of the circulating flux component.

For the LSCG, the carrier signals of the VSC2 and the VSC4 are also interleaved by 180° and the same analysis can be applied. The maximum value of the circulating flux component is also $N\phi_{x_{L,c_{max}}} = V_{\mathrm{dc}}/8f_s$.

From the reluctance model, it is evident that the flux in the yokes of the cell is equal to the resultant component of the circulating flux component $\phi_y = \phi_{x_{H,c}} = \phi_{x_{L,c}}$. Therefore, the maximum value of the flux density in the yokes is

$$B_{y_{max}} = \frac{V_{\mathrm{dc}}}{8NA_{c_y}f_s} \tag{I.32}$$

where A_{c_y} is the cross section area of the yoke.

3.3.2 Common Flux Component

The common current component of each of the VSCs can be decomposed into:

1. Fundamental frequency component.
2. Major harmonic components at the $4kf_s$, where $k = 1, 2, .. \infty$.

As the common flux component is replica of the common current component, the common flux component is also comprised of a fundamental frequency component and a ripple component. The fundamental component of the common flux component is given as

$$\phi_r(t) = \frac{\mu_0 N A_g^{'}}{8l_g} I_{x_{max}} \cos(\psi + \theta) \tag{I.33}$$

Normally the line filter inductance value is selected to limit the peak-to-peak value of the ripple component of the line current to the desired value. Let the ratio of the peak-to-peak value of the ripple component of the line current to the amplitude of the fundamental component of the line current be ε. For the space vector modulation, the ripple component attains its maximum value at the space vector angle of $\psi = 0°$. For unity power factor applications, the fundamental component is also maximum at the $\psi = 0°$. Therefore, the common flux component also attains its maximum value at the space vector angle of $\psi = 0°$ and it is given as

$$\phi_{r_{max}} = (1 + \frac{\varepsilon}{2}) \frac{\mu_0 N A_g^{'}}{8l_g} I_{x_{max}} \tag{I.34}$$

where $I_{x_{max}}$ is the amplitude of the rated current. The common component of the flux ϕ_r completes its path through the bridge legs, air gaps and legs of

the cells. Therefore, the maximum value of the flux density in the bridge leg is given as

$$B_{bl_{max}} = (1 + \frac{\varepsilon}{2}) \frac{\mu_0 N A_g^{'}}{8 l_g A_{c_{bl}}} I_{x_{max}} \tag{I.35}$$

where $A_{c_{bl}}$ is the cross section area of the bridge leg.

3.3.3 Flux in the limbs of the cells

The flux in the limbs is the addition of the circulating flux component and the resultant flux component and it is given as

$$\phi_l(t) = \phi_r(t) + \phi_{x_{H,c}}(t) \tag{I.36}$$

for the unity power factor applications ($\theta = 0$), the common component of the flux is maximum for $\psi = 0^\circ$, whereas the circulating flux component $\phi_{x_{H,c}}$ is minimum at this voltage space vector angle. Similarly, the $\phi_{x_{H,c}}$ is maximum at $\psi = 90^\circ$ and the common flux component is zero. Therefore, for the unity power factor applications

$$\phi_{l_{max}} = \max(\phi_{x_{H,c_{max}}}, \phi_{r_{max}} + \phi_{x_{H,c_{|\psi=0^\circ}}}) \tag{I.37}$$

4 Circulating Current Suppression Between the Two Converter Groups

The resultant output voltages of both the HSCG and LSCG are also phase-shifted with respect to each other and the circulating current flows between them due to these phase-shifted voltages. Additional CI (CI_G) is used to suppress this current.

The flux linkage in the CI_G is given as

$$N\phi_{x_{CI_G}} = \frac{1}{2} \int \left((\frac{V_{x_1o} + V_{x_3o}}{2}) - (\frac{V_{x_2o} + V_{x_4o}}{2}) \right) dt \tag{I.38}$$

The pole voltages of the individual VSCs and their average voltage for both the HSCG and the LSCG are shown in Fig. I.10(a) and I.10(b), respectively. The difference in the average voltages of both the converter groups and flux linkage of the CI_G is shown in Fig. I.10(c). The flux linkage behavior over a fundamental period is also shown in Fig. I.11. The flux reversal in the CI_G is $2 \times f_s$ and subjected to the half of the dc-link voltage, which is also evident in Fig. I.10(c). The maximum value of the flux linkage in the CI_G is given as

$$N_{CI_G} \phi_{CI_{G,max}} = \frac{V_{dc}}{32 f_s} \tag{I.39}$$

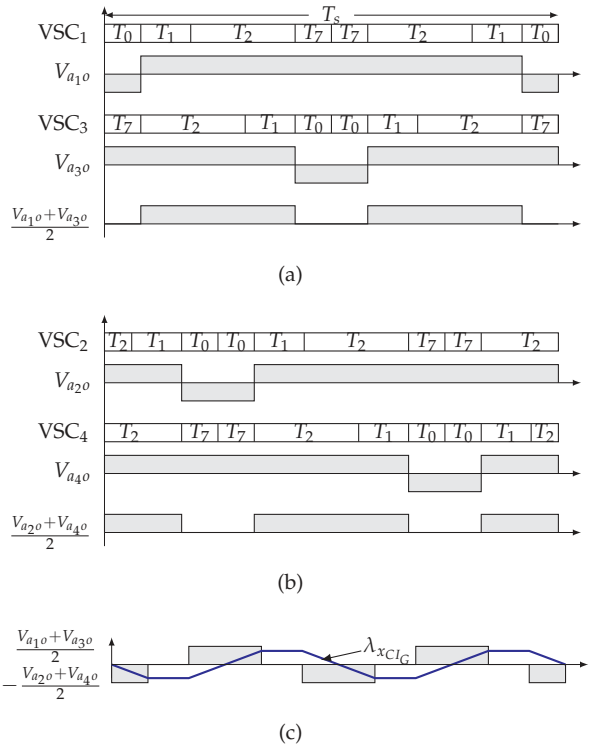


Fig. I.10: Voltage waveforms for four parallel interleaved VSCs for the modulation index $M = 1$ and space vector angle $\psi = 45°$. (a) Pole voltages of the individual VSCs and their average voltage of the high side converter group, (b) Pole voltages of the individual VSCs and their average voltage of the low side converter group, (c) The difference of the average voltages of the high side converter group and the low side converter group and their associated flux linkage.

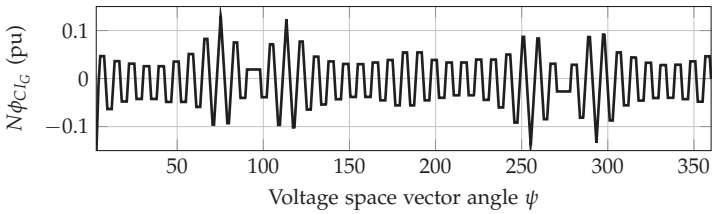


Fig. I.11: Flux linkage of the CI_G ($\lambda_{x_{CI_G}}$) over a complete fundamental period. The flux linkage is normalized to $V_{dc}T_s$.

where N_{CI_G} is the number of turns in each of the coils of the CI$_G$ and $\phi_{CI_{G,max}}$ is the maximum value of the flux in the CI$_G$. Using (I.30) and (I.39), the ratio

Table I.1: System Parameters for simulation and experimental studies

Parameters	Values
Total power S	11 kVA
No. of VSCs	4
Interleaving angle	90°
DC-link voltage V_{dc}	650 V
Switching frequency f_s	1250 Hz
PWM scheme	Space vector modulation
Line filter inductance L_f	2.3 mH (0.05 pu)

of the flux linkage in the CI_G to the flux linkage in the CI_H (or CI_L) is given as

$$\frac{N_{CI_G}\phi_{CI_{G,max}}}{N\phi_{x_{H,c}}} = \frac{1}{4} \tag{I.40}$$

as it is evident form (I.40), the size of the CI_G is approximately 25% than that of the CI_H. The maximum value of the flux density in the CI_G is given as

$$B_{CI_{G,max}} = \frac{V_{\mathrm{dc}}}{32N_{CI_G}A_{c_{CI_G}}f_s} \tag{I.41}$$

where $A_{c_{CI_G}}$ is the cross section area of the CI_G.

5 Finite Element Analysis and Comparative Evaluation

The size reduction achieved by the magnetic integration is demonstrated by comparing the volume of the proposed solution with the volume of the magnetic components of the system proposed in [1, 20] and also shown in Fig. I.2(b).

5.1 Finite Element Analysis

The simplified reluctance model is used for the analysis, which does not take into account the effects of the flux leakage. Therefore, (I.25) gives underestimated value as the total inductance offered to the line current is given by

$$L_{line} = L_f + \frac{L_{\sigma,II}}{4} + \frac{L_{\sigma,CI_G}}{2} \tag{I.42}$$

where $L_{\sigma,II}$ and L_{σ,CI_G} are the leakage inductances of the integrated inductor and the CI_G, respectively. On the other hands, inherent air gap exists in

Table I.2: Dimensions of the implemented inductor (refer Fig. I.5(b))

Parameters	A,B,E,F	C	D,G	l_g
Values (mm/mm^2)	25	75	85	1.0

Table I.3: Inductance values obtained using the finite element analysis

Inductance	L_s	L_{m_1}	L_{m_2}	L_{m_3}
Values (mH)	29.6	2.6	-22.3	2.5

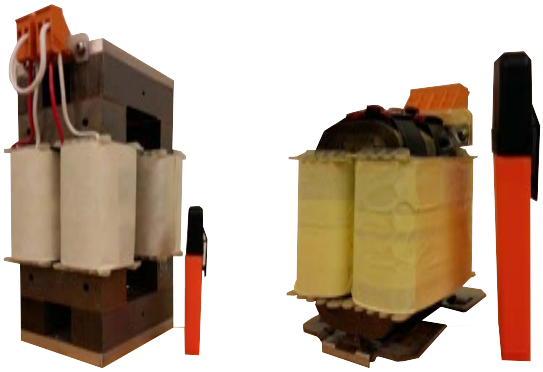
the cell structure due to the core joints, which tends to decrease the value of the L_f. Therefore the design equations derived in section IV can be used to get the parameters for the first design iteration and Finite Element Analysis (FEA) should be carried out in order to fine tune those design parameters.

The integrated inductor and the CI_G is designed using the design equations derived in section III and section IV for the converter system with four parallel VSCs. The system parameters are given in Table I.1. Amorphous alloy 2605SA1 is used for the cells of integrated inductor and for the CI_G core, whereas laminated steel with a lamination thickness of 0.35 mm is used for the bridge legs. The cells of the integrated inductor are constructed using four blocks. Due to the use of the laminated cores, the magnetic structure shown in Fig. I.5(b) is used (to avoid large eddy current losses in the core).

The dimensions of the implemented inductors are specified in Table I.2. The integrated inductor is assembled using the core blocks available in the laboratory. The stacking factor for the amorphous core blocks is taken to be 0.89, whereas it is assumed to be 0.96 for the laminated steel. The coils are wound using the AWG 16 enameled copper wire with the cross section area $A_{cu} = 1.31 \times 10^{-6}$ m^2. Each of the coils has 140 number of turns. The picture of the implemented integrated inductor is shown in Fig. I.12(a).

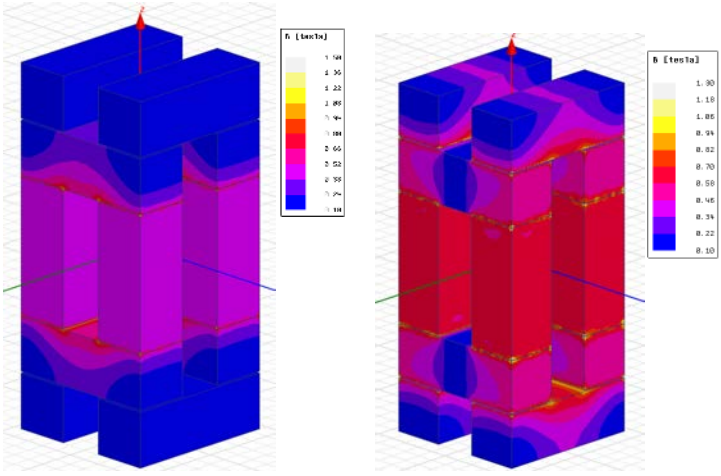
The finite element analysis has been carried out using Ansys Maxwell and the flux density distribution in the magnetic core is shown in Fig. K.11. The flux is mainly confined to the corresponding cells when the coils are excited with the phase shifted components of switched output voltage of the carrier frequency harmonics, as shown in Fig. I.13(a). On the other hand, the induced flux of coils of the HSCG cell links with the coils of the LSCG cell and vice-versa when the coils are excited with the common component of the current. As a result, the common component of the flux completes its path through the bridge legs and the air gaps, as shown in Fig. I.13(b).

The inductance values are obtained using the FEA and they are given as given Table I.3. The inductance offered to the line current is then calculated to be 3.1 mH using (K.34). The circulating current inductance matrix $\boldsymbol{L_c}$ is



(a) (b)

Fig. I.12: Pictures of the implemented inductor. (a) Integrated inductor, (b) Coupled inductor to suppress the circulating current between the high-side converter group and the low-side converter group (CI_G).



(a) (b)

Fig. I.13: The flux density distribution in the magnetic core. (a) Phase shifted components of switched output voltage of the carrier frequency harmonics are applied across the coils, (b) Coils are excited with the common component of the current.

calculated as

$$\boldsymbol{L_c} = 2\begin{bmatrix} 52 & 5.1 \\ 5.1 & 52 \end{bmatrix} \text{mH} \tag{I.43}$$

The circulating current between the HSCG and the LSCG is suppressed

Table I.4: Design parameters of the coupled inductor CI_G

Parameters	Values
Cross-section area of the core $A_{c_{CI}}$	4.6×10^{-4} m^2
Number of turns N_{CI}	53
Cross section area of the conductor A_{cu}	2.62×10^{-6} m^2 (AWG 13)

using the CI_G. The CI_G is realized using the POWERLITE C-cores form the Metglas. Two AMCC16-B cores are stacked together to achieve core cross-section area of 4.6×10^{-4} m^2. The FEA has been carried out for the CI_G and the inductance matrix calculated and it is given as

$$\boldsymbol{L}_{\mathrm{CI}_G} = \begin{bmatrix} 3.5 & -3.27 \\ -3.27 & 3.5 \end{bmatrix} \mathrm{mH} \tag{I.44}$$

Therefore the inductance offered to the line current by the leakage inductance of the CI_G is 0.1 mH and the inductance offered to the circulating current between the HSCG and the LSCG is 13.54 mH.

5.2 Comparative Evaluation

The volume of the different active materials of the proposed filter arrangement is compared with the volume of the state-of-the-art solution, shown in Fig. I.2(b) for the the system parameters specified in the Table I.1. Moreover, the losses in the magnetic components in both the cases are also compared.

The bridge legs of the integrated inductor and the line filter inductor in Fig. I.2(b) is assumed to be made from the 0.35 mm laminated silicon steel, whereas the amorphous alloys 2605SA1 is considered as a magnetic material for the cells of the integrated inductor and for the CI_H, CI_L, and CI_G in Fig. I.2(b). As the core losses in the amorphous alloys 2605SA1 is lower compared to the laminated silicon steel, it is used for cells of the magnetic structures which carry the switching frequency circulating flux component. However, the price of the amorphous alloys 2605SA1 is higher compared to the laminated silicon steel. Therefore to reduce the cost, laminated silicon steel is used for the bridge legs, which carry the common flux component with predominant fundamental frequency component. The design of the CI_G that is used to suppress the current between the HSCG and the LSCG is taken to be the same in both cases. The flux densities in the cores and the current density in the coils are taken to be the same in both the cases.

Table I.5: Volume comparison of the active materials of the magnetic components in the proposed solution with the state-of-the-art solution shown in Fig. I.2(b)

Material	State-of-the-art	Proposed	% reduction
Amorphous alloy 2605SA1	1.477 Ltr.	1.221 Ltr.	17.3%
Laminated steel	1.28 Ltr.	0.63 Ltr.	49%
Copper	0.385 Ltr.	0.337 Ltr.	12.4 %

5.2.1 Volumetric Comparison

The volume of the different materials in both the cases for all the three phases are given in Table I.5. In the filter arrangement shown in Fig. I.2(b), the windings of the line filter inductor carries full line current and it is completely eliminated in the proposed solution. Therefore, the designer may choose to increase the number of turns in the coils of the integrated inductor to reduce the size of the amorphous alloy. In this comparison, the number of turns in the integrated inductor is taken to be 10% higher than the number of turns in the CI_H and CI_L in the filter arrangement shown in Fig. I.2(b). This results in the 17.3% saving in the amorphous alloy and 12.4% reduction in copper. Furthermore, the volume of the laminated steel is reduced by 49% in the proposed solution.

5.2.2 Losses Comparison

The Improved Generalized Steinmetz Equation (IGSE) [21, 22] is used to calculate the core losses. The core losses per unit volume is given as

$$P_{fe,v} = \frac{1}{T}\int_0^T k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{I.45}$$

where ΔB is the Peak-to-peak value of the flux density. α, β and k_i are the constants determined by the material characteristics. These constants for both the amorphous alloys and the laminated silicon steel are given in Table I.6. The flux waveform has major and minor loops and the core losses due to these loops are evaluated separately.

The copper loss is evaluated by considering the ac resistance of the winding, which takes into account the skin and proximity effects [23]. The total winding losses are given as

$$P_{cu} = R_{dc} \sum_{h=1}^{\infty} k_{p_h} I_h^2 \tag{I.46}$$

Table I.6: Steinmetz parameters of the amorphous alloys 2605SA1 and the laminated silicon steel

Material	k_i	α	β
Amorphous alloy 2605SA1	0.62	1.51	1.74
Laminated steel	0.96	1.55	1.87

Table I.7: Core and copper losses comparison. The losses of all the three phases are listed.

Item	load	State-of-the-art	Proposed	% reduction
Core losses (W)	0.5 pu	35.6	27.3	23%
	1 pu	39.8	29	27%
Copper losses (W)	0.5 pu	21.5	15.1	29%
	1 pu	76.3	55.8	26%

where

$$k_{p_h} = \sqrt{h}\Delta\Big[\frac{\sinh(2\sqrt{h}\Delta)+\sin(2\sqrt{h}\Delta)}{\cosh(2\sqrt{h}\Delta)-\cos(2\sqrt{h}\Delta)} + \frac{2}{3}(m^2-1)\frac{\sinh(\sqrt{h}\Delta)-\sin(\sqrt{h}\Delta)}{\cosh(\sqrt{h}\Delta)+\cos(\sqrt{h}\Delta)}\Big] \tag{I.47}$$

and $\Delta = T_c/\delta$. R_{dc} is the dc resistance of the coil, m is the number of layers in the coil, I_h is the hth harmonic component of the leg current. T_c is the thickness of the coil and δ is the skin depth.

The core and the copper losses of the proposed integrated inductor are evaluated and the total losses of all the three integrated inductor (for three phase system) are given in Table I.7. The inductor losses in the case of the state-of-the-art solution are also evaluated at the 50% of the rated load and 100% of the rated load conditions. The losses in the integrated inductor are low compared to the state-of-the-art solution at both the loading conditions. The total losses in the integrated inductors at the rated load conditions are 84.8 W, compared to the 116.1 W in the case of the state-of-the-art solutions (27% reduction). The worst case losses in one integrated inductor is 28.2 W (84.8/3 W), out of which 18.6 W is the total copper losses in all the four coils. Since the coils are exposed to the ambient air, the generated heat can be easily dissipated through natural convection.

6 Simulation and the Experimental Results

The simulation and the experimental results for the four parallel interleaved VSCs are presented in this section for the system parameters specified in Table I.1.

6.1 Simulation Results

The time domain simulation has been carried out using PLECS, where the simplified model of the integrated inductor, shown in Fig. 6, has been implemented using the permeance-capacitance analogy. The simulated flux density waveforms in the various parts of the magnetic structure of the integrated inductor and the CI_G are shown in Fig. I.14 and Fig. I.15, respectively. Fig. I.14(a), shows the flux density waveform in the limb of the cell, which is a vector addition of the common flux component and the circulating flux component. The circulating flux is confined to the cell and therefore the flux in the yoke has a switching frequency component as a major harmonic component, which is shown in Fig. I.14(b). The common flux component flows out of the cell and completes its path through the air gaps and the bridge leg, as shown in Fig. I.14(c). Due to the magnetic integration, the common flux component of the cell of the HSCG completes its path through the limbs of the cell of the LSCG and vice-versa. As a result, a dedicated return path is avoided. Moreover, for the unity power factor applications, the common flux component is maximum when the circulating flux component is minimum and vice-versa as shown in Fig. I.14. As the flux in the limb is the addition of these two components, the cross section area of the limb can be made smaller compared to the individual inductor case. This leads to substantial reduction of the volume of the integrated inductor.

The circulating current between the HSCG and the LSCG is suppressed using the CI_G. The CI_G is subjected to half of the dc-link voltage and the flux has a major harmonic component at the 2nd carrier harmonic component. The flux density in the CI_G is shown in Fig. I.15, which demonstrates that the flux reversal takes place at twice the switching frequency.

The simulated circulating currents between the VSCs of the HSCG and between the VSCs of the LSCG are shown in Fig. I.16(a) and Fig. I.16(b), respectively. The integrated inductor offers high inductance to the circulating currents and suppresses them effectively. The additional CI_G is also very effective in suppressing the circulating current between the HSCG and the LSCG, as shown in Fig. I.16(c).

The simulated currents of phase *a* are shown in Fig. I.17. The output current of the VSCs of the HSCG are only shown. However, the output current of the VSCs of the LSCG also demonstrates similar current waveform quality. The line current is shown in Fig. I.17(d), which has a very small ripple component. This demonstrates effective line current filtering functionality of the integrated inductor.

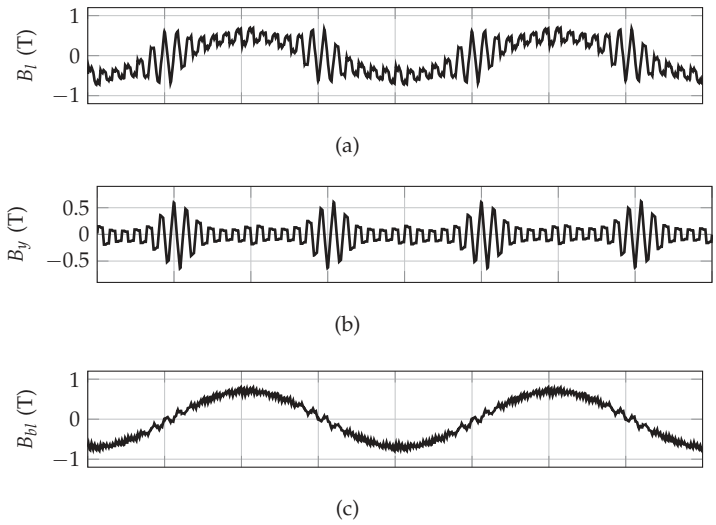


Fig. I.14: Simulation results at rated operating conditions. (a) Flux density in the limb of the cell of the integrated inductor, (b) Flux density in yoke of the cell, (c) Flux density in the bridge leg.

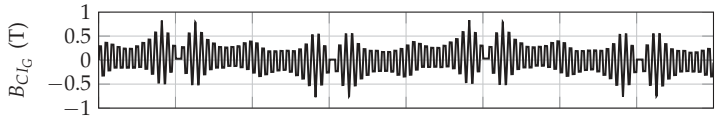


Fig. I.15: Simulation results. (a) Flux density waveform in the coupled inductor that is used to suppress the circulating current between the high side and the low side converter group.

6.2 Experimental Results

The experimental results were obtained for the system specified in Table I.1. Four VSCs were connected in parallel. The carrier signals of these parallel connected VSCs were interleaved by an interleaving angle of 90°. The VSCs were modulated using the space vector modulation, using TMS320F28346 floating-point digital signal processor. The dc-link was connected to the dc power supply and the ac-side is connected to the three-phase resistive load of 13.33 Ω.

The output current of phase *a* of the individual VSCs of both the HSCG and the LSCG is shown in Fig. I.18. The individual VSCs are operated with the switching frequency of 1.25 kHz, and the switched output voltages of the individual VSCs has a major harmonic component at the carrier frequency harmonics. Due to the interleaved carrier signals, these voltage components are phase shifted and appears across the closed path formed due to the inter-

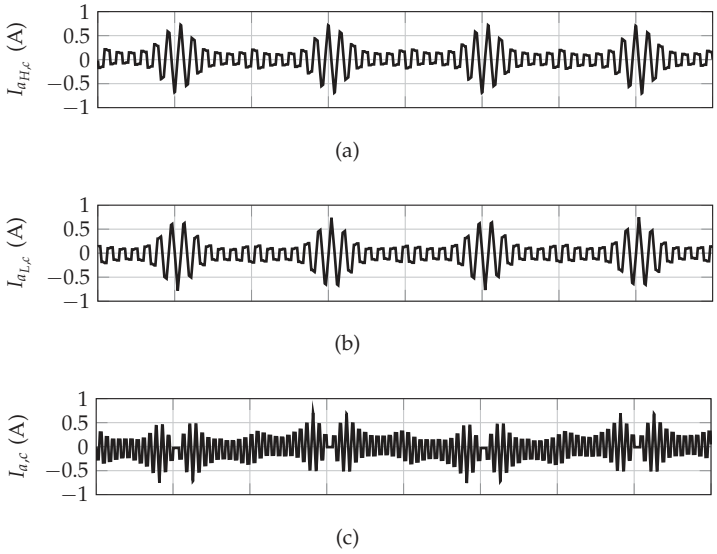


Fig. I.16: Simulated current waveforms at rated operating conditions. (a) Circulating current between the VSCs of the high side converter group $I_{a_{H,c}}$, (b) Circulating current between the VSCs of the low side converter group $I_{a_{L,c}}$, (c) Circulating current between the high side converter group and the low side converter group $I_{a,c}$.

leaved operation and the common dc-link. The integrated inductor offers the circulating current inductance to these voltage components. As it is evident from Fig. I.19, the circulating current between the VSCs of the HSCG (as well as between the VSCs of the LSCG) is suppressed very effectively. This shows that the integrated inductor offers high inductance to the phase shifted voltage components and effectively suppresses the circulating current.

The output current of both the HSCG and the LSCG along with their circulating currents are shown in Fig. I.19. The measured peak value of the circulating current between the VSCs of the HSCG is 0.8 A, which is around 13% of the amplitude of the output current of the individual VSCs. The circulating current between the HSCG and the LSCG is effectively suppressed by the CI_G, as it is evident from Fig. I.20. The resultant line current of all the three phases are also shown in Fig. I.20. The integrated inductor also offers the desired inductance to the resultant line current, which demonstrates the line current filtering functionality of the integrated inductor.

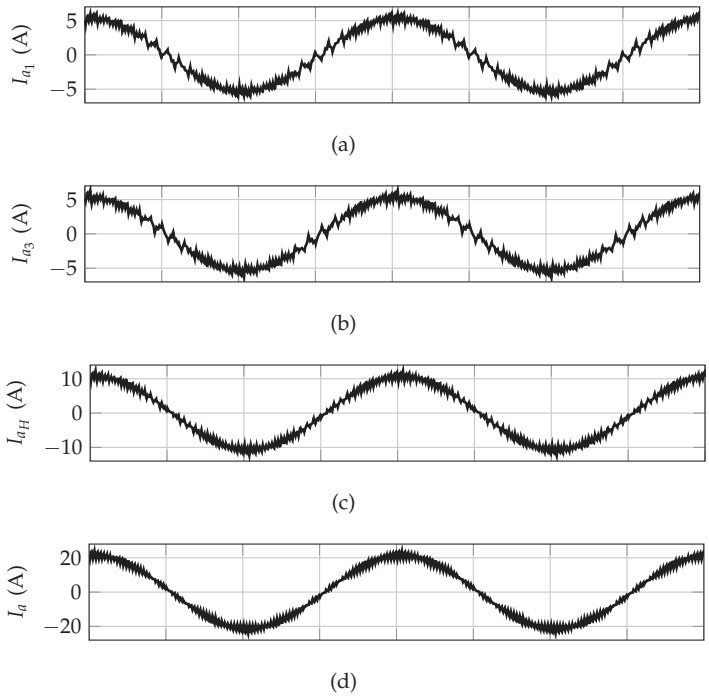


Fig. I.17: Simulated current waveforms of phase a at rated operating conditions. (a) Output current VSC_1 (I_{a_1}), (b) Output current VSC_3 (I_{a_3}), (c) Resultant current of the high side converter group (I_{a_H}), (d) Line current I_a.

7 Conclusion

An integrated inductor for the parallel interleaved VSCs connected in a whiffletree configuration is proposed in this paper. The proposed integrated inductor suppresses the circulating current between the parallel interleaved VSCs. In addition, it offers the desired inductance to the line current as well. The converters are divided into a high-side converter group and a low-side converter group. The fundamental component of the flux in the cell of the high side converter group is equal to the fundamental component of the flux in the cell of the low-side converter group. Because of the unique arrangement of the coils in the proposed inductor, the fundamental component of the flux of the high-side converter group completes its path through the limbs of the cells of the low-side converter group. Therefore, the dedicated magnetic structure for the return path for the fundamental flux component is avoided. Moreover, the magnetic integration also leads to substantial size reduction of the limbs. As a result, compared to the state-of-the-art solution, 49% re-

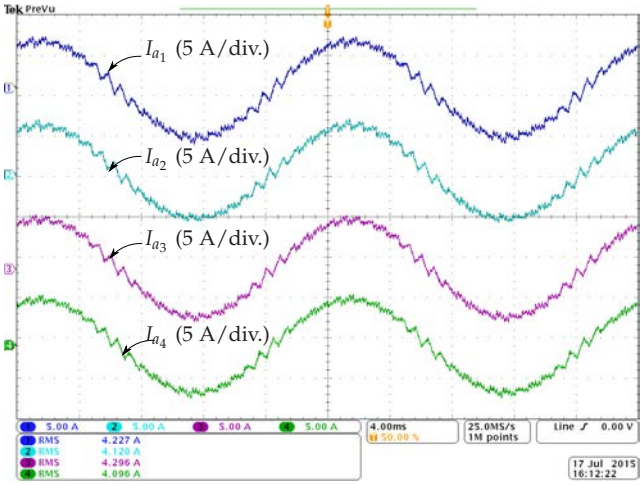


Fig. I.18: Experimental waveforms of the phase a of the output current of the individual VSCs. (a) Ch1: Output current of VSC_1 (I_{a_1}), Ch2: Output current of VSC_2 (I_{a_2}), Ch3: Output current of VSC_3 (I_{a_3}), Ch4: Output current of VSC_4 (I_{a_4}).

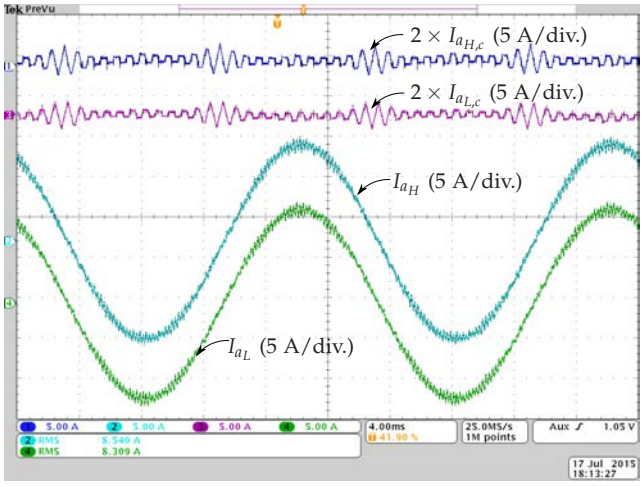


Fig. I.19: Experimental waveforms of the phase a. (a) Ch1: Circulating current between the VSCs of the high-side converter group ($2 \times I_{a_{H,c}}$), Ch2: Output current of the high-side converter group (I_{a_H}), Ch3: Circulating current between the VSCs of the low-side converter group ($2 \times I_{a_{L,c}}$), Ch4: Output current of the low-side converter group (I_{a_L}).

duction in the volume of the laminated silicon steel, 17.3% reduction in the volume of the amorphous alloy, and 12.4% reduction in the volume of the copper can be achieved for the system parameters considered in this paper.

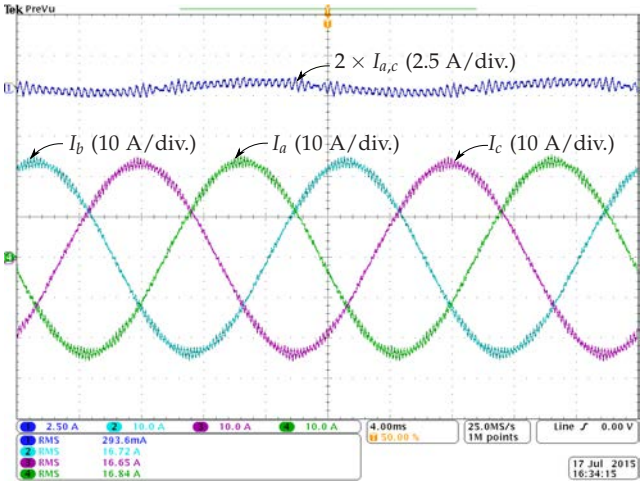


Fig. I.20: Experimental waveforms. (a) Ch1: Circulating current between the high-side converter group and the low-side converter group ($2 \times I_{a,c}$), Ch2: Resultant line current of phase a (I_a), Ch3: Resultant line current of phase b (I_b), Ch4: Resultant line current of phase c (I_c).

The operation of the proposed system has been discussed and the losses are analyzed. The analysis is supported by the simulations and the experimental results.

References

[1] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[2] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[3] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, 2008.

[4] D. Zhang, F. Wang, R. Burgos, L. Rixin, and D. Boroyevich, "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042–1054, 2010.

[5] J. Prasad and G. Narayanan, "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan 2014.

[6] X. Mao, A. Jain, and R. Ayyanar, "Hybrid interleaved space vector PWM for ripple reduction in modular converters," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1954–1967, 2011.

[7] K. Xing, F. Lee, D. Borojevic, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, 1999.

[8] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[9] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Design of the trap filter for the high power converters with parallel interleaved VSCs," in *Proc. 40th Annual Conference on IEEE Industrial Electronics Society, IECON 2014*, Oct 2014, pp. 2030–2036.

[10] Z. Xu, R. Li, H. Zhu, D. Xu, and C. Zhang, "Control of parallel multiple converters for direct-drive permanent-magnet wind power generation systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1259–1270, March 2012.

[11] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[12] R. Hausmann and I. Barbi, "Three-phase multilevel bidirectional DC-AC converter using three-phase coupled inductors," in *Proc. IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009.*, Sept 2009, pp. 2160–2167.

[13] F. Forest, T. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire, "Optimization of the supply voltage system in interleaved converters using intercell transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 934–942, 2007.

[14] F. Forest, E. Laboure, T. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, 2009.

[15] J. Salmon, J. Ewanchuk, and A. Knight, "PWM inverters using split-wound coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2001–2009, 2009.

[16] B. Cougo, T. Meynard, and G. Gateau, "Parallel Three-Phase Inverters: Optimal PWM Method for Flux Reduction in Intercell Transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[17] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Modified discontinuous pwm for size reduction of the circulating current filter in parallel interleaved converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3457–3470, July 2015.

[18] G. Gohil, L. Bede, R. Maheshwari, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Parallel interleaved VSCs: influence of the PWM scheme on the design of the coupled inductor," in *Proc. 40th Annual Conference on IEEE Industrial Electronics Society, IECON 2014*, Oct 2014, pp. 1693–1699.

[19] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[20] K. Matsui, Y. Murai, M. Watanabe, M. Kaneko, and F. Ueda, "A pulsewidth-modulated inverter with parallel connected transistors using current-sharing reactors," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 186–191, Apr 1993.

[21] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, 2002, pp. 36–41.

[22] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Thirty-Sixth IAS Annual Meeting, IEEE Industry Applications Conference.*, vol. 4, 2001, pp. 2203–2210 vol.4.

[23] P. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers,*, vol. 113, no. 8, pp. 1387–1394, August 1966.

Paper J

Optimized harmonic filter inductor for dual-converter fed open-end transformer topology

Ghanshyamsinh Gohil,
Lorand Bede,Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been submitted for the publication in the
IEEE Transactions on Power Electronics

The layout has been revised.

Abstract

Many high power converter systems are often connected to the medium voltage network using a step-up transformer. In such systems, the converter-side windings of the transformer can be configured as an open-end and multi-level voltage waveforms can be achieved by feeding these open-end windings from both ends using the dual-converter. An LCL filter with separate converter-side inductors for each of the converter is commonly used to attenuate the undesirable harmonic frequency components in the grid current. The magnetic integration of the converter-side inductors is presented in this paper, where the flux in the common part of the magnetic core is completely canceled out. As a result, the size of the magnetic component can be significantly reduced. A multi-objective design optimization is presented, where the energy loss and the volume are optimized. The optimization process takes into account the yearly load profile and the energy loss is minimized, rather than minimizing the losses at a specific operating point. The size reduction achieved by the proposed inductor is demonstrated through a comparative evaluation. Finally, the analysis is supported through simulations and experimental results.

1 Introduction

Many high power converter systems are often connected to the medium voltage network and a step-up transformer is used to match the voltage levels of the converter with the medium voltage grid. In some applications, the transformer is also required for providing galvanic isolation. In such systems, the converter-side windings of the transformer can be configured as an open-end. This open-end transformer winding can be fed from both the ends using the two-level Voltage Source Converters (VSCs) [1], as shown in Fig. J.1. The number of levels in the output voltages is the same as that of the three level Neutral point clamped (NPC) converter and each of the two-level VSC operates with the half of the dc-link voltage than the dc-link voltage required for the three level NPC. This enables the simple and proven two-level VSC to be used in medium voltage applications. For example, converter system connected to the 3.3 kV grid can be realized using the dual-converter with two-level VSCs having a switch voltage rating of 4.5 kV. However, Common Mode (CM) circulating current flows through the closed path if both the VSCs are connected to a common dc-link. The CM circulating current can be suppressed either by using the CM choke [2, 3] or by employing a proper Pulse Width Modulation (PWM) scheme to ensure complete elimination of the CM voltage [4, 5]. However, in many applications, isolated dc-links can be derived from the source itself and such extra measures for CM circulating current suppression may not be required. For example, the isolated dc-links can be obtained in

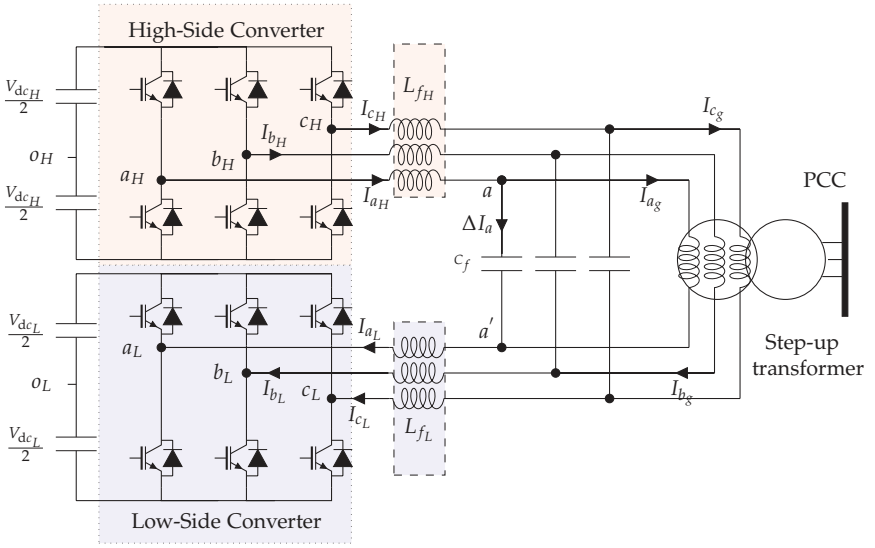


Fig. J.1: The system configuration of the dual converter fed open-end winding transformer topology with two separate dc-links. The open-end primary windings are fed from two-level voltage source converters.

1. PhotoVoltaic (PV) systems by dividing the total number of arrays into two groups to form separate dc-links [1].

2. Wind Energy Conversion System (WECS): isolated dc-links can be obtained by using a dual stator-winding generator [6].

Therefore the analysis presented in this paper is mainly focused on the dual converter fed open-end transformer topology with two separate dc-links.

An *LCL* filter is commonly used in high power grid-connected applications [7] and one of the possible arrangement of the *LCL* filter for the dual-converter fed open-end transformer topology is shown in Fig. J.1. The leakage inductance of the transformer is considered to be a part of the grid-side inductor of the *LCL* filter. Two VSCs (denoted as High-Side Converter (HSC) and Low-Side Converter (LSC) in Fig. J.1) are connected to a common shunt capacitive branch of the *LCL* filter through the converter-side inductors L_{f_H} and L_{f_L}, respectively. The magnetic integration of the L_{f_H} and L_{f_L} is presented in this paper. As a result of this magnetic integration, the flux in the common part of the magnetic core is completely canceled out. This leads to substantial reduction in the size of the converter-side inductor.

This paper is organized as follows: The operation principle of the dual-converter fed open-end transformer topology is briefly discussed in Section II. The magnetic structure of the proposed integrated inductor is described

in Section III. Section IV discusses the design procedure in general and the multi-objective optimization of the integrated inductor. The size reduction achieved by the magnetic integration is also demonstrated by comparing the volume of the integrated inductor with the separate inductor case for the 6.6 MVA, 3.3 kV WECS and it is presented in Section V. The simulation and the experimental results are finally presented in Section VI.

2 Dual-Converter Fed Open-End Transformer Topology

The operation of the dual-converter fed open-end transformer converter is briefly described in this section. The dual-converter system consists of the HSC and the LSC is shown in Fig. J.1. A Two-level VSC is used for both the HSC and the LSC. However, the discussion presented in this paper is also applicable to other converters as well.

The reference voltage space vector $\overrightarrow{V^*}$ is synthesized by modulating the HSC and the LSC. The magnitude of the reference voltage space vectors of the HSC and the LSC is half than that of the desired reference voltage space vector $\overrightarrow{V^*}$ ($|\overrightarrow{V_H^*}| = |\overrightarrow{V_L^*}| = |\overrightarrow{V^*}|/2$). The reference voltage space vector angle of the HSC is kept the same as that of the desired voltage space vector ($\psi_H = \psi$), whereas the reference voltage space vector angle of the LSC is shifted by an angle 180° ($\psi_L = \psi_H + 180°$), as shown in Fig. K.2.

From Fig. J.1, the voltage across the shunt capacitive branch C_f of the LCL filter is given as

$$V_{xx'} = (V_{x_H o_H} - V_{x_L o_L}) - L_{f_H}\frac{dI_{x_H}}{dt} - L_{f_L}\frac{dI_{x_L}}{dt} + V_{o_H o_L} \tag{J.1}$$

where the subscript x represents the phases $x = \{a, b, c\}$. As the dc-links are separated, the common-mode components of the voltages in (J.1) do not drive any common-mode circulating current. As a result, only the differential mode current would flow through the inductors. For the dual converter system, these currents are equal.

$$I_{x_H} = I_{x_L} = I_x \tag{J.2}$$

where I_{x_H} and I_{x_L} are the currents in the phase x of the HSC and LSC, respectively. Assuming $L_{f_H} = L_{f_L} = L_f/2$ and using (J.1) and (J.2), the voltage across the converter-side inductor is given as

$$L_f\frac{dI_x}{dt} = (V_{x_H o_H} - V_{x_L o_L}) - V_{xx'} + V_{o_H o_L} \tag{J.3}$$

where L_f is the equivalent converter-side inductance of the LCL filter. A single magnetic component with the inductance L_f is realized by the magnetic

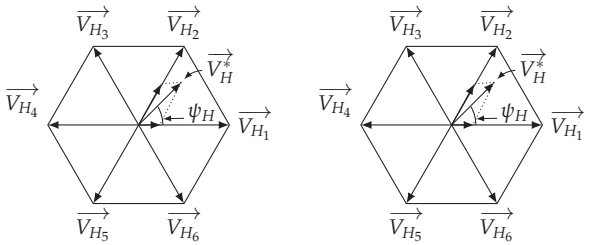


Fig. J.2: Reference voltage space vector and its formation by the geometrical summation. (a) Reference voltage space vector for the HSC, (b) Reference voltage space vector for the LSC.

integration of the L_{f_H} and L_{f_L} and the structure is discussed in the following section.

3 Integrated Inductor

In this paper, a three-phase inductor is chosen for the illustration due its wide-spread use in the high power applications. However, it is important to point out that the same analysis can be used for the single-phase inductor as well. The three-phase three-limb converter-side inductor for both the HSC and the LSC are shown in Fig. J.3(a). These two inductors can be magnetically integrated as shown in Fig. J.3(b), where both the inductors share a common magnetic path. The magnetic structure has six limbs, on which the coils are wound. The upper three limbs belong to the L_{f_H}, whereas the lower three limbs receive the coils corresponding to the L_{f_L}. The upper limbs are magnetically coupled using the top bridge yoke, whereas the lower three limbs are magnetically coupled using the bottom bridge yoke. The upper and the lower limbs share a common yoke, as shown in Fig. J.3(b).

Considering three-phase three-wire system

$$I_a + I_b + I_c = 0 \tag{J.4}$$

and at a particular instance

$$I_a = -(I_b + I_c) \tag{J.5}$$

The flux distribution in the magnetic structure for this case (the positive value of the I_a and the negative values of the I_b and I_c) is shown in Fig. J.3(b). The simplified reluctance model of this magnetic structure is shown in Fig. J.4, where $\Re_L$, $\Re_g$, and $\Re_Y$ are the reluctances of the limb, the air gap, the top and

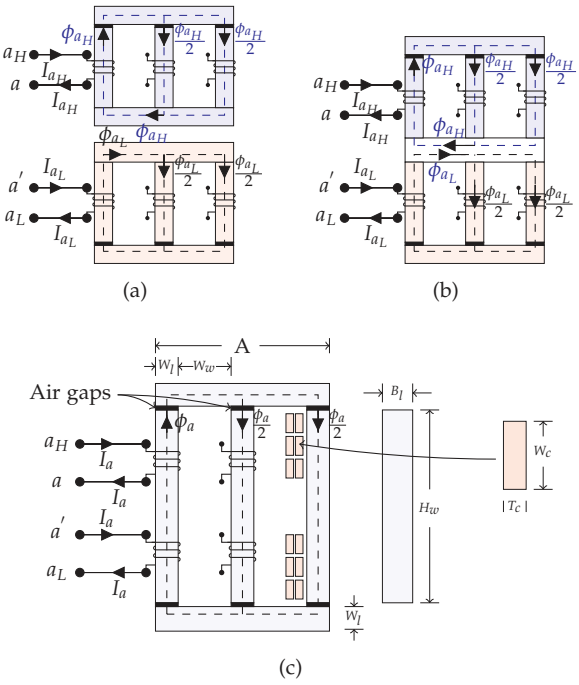


Fig. J.3: Magnetic structure. (a) Separate inductors for the HSC and the LSC, (b) Flux cancellation through magnetic integration, (c) Proposed integrated inductor.

the bottom bridge yokes, respectively. The reluctance of the common yoke is represented as $\Re_{Y1}$. ϕ_{a_H}, ϕ_{b_H}, and ϕ_{c_H} are the fluxes in the upper three limbs whereas ϕ_{a_L}, ϕ_{b_L}, and ϕ_{c_L} are the fluxes in the lower three limbs. ϕ_1, and ϕ_2 represent the fluxes in the common yokes, as shown in Fig. J.4. By solving the reluctance network, the fluxes in various parts of the integrated inductor are obtained and they are given as

$$\phi_{a_H} = \frac{NI_{a_H}}{\Re_g + \Re_L + \Re_Y},\ \phi_{a_L} = \frac{NI_{a_L}}{\Re_g + \Re_L + \Re_Y} \tag{J.6}$$

$$\phi_{c_H} = \frac{NI_{c_H}}{\Re_g + \Re_L + \Re_Y},\ \phi_{c_L} = \frac{NI_{c_L}}{\Re_g + \Re_L + \Re_Y} \tag{J.7}$$

and

$$\phi_{b_H} = \frac{NI_{b_H}}{\Re_g + \Re_L},\ \phi_{b_L} = \frac{NI_{b_L}}{\Re_g + \Re_L},\ \phi_1 = 0,\ \phi_2 = 0 \tag{J.8}$$

The flux components in the common yoke (ϕ_1 and ϕ_2) are zero and therefore the common yoke can be completely removed, as shown in Fig. J.3(c). The integrated inductor has only two yokes, compared to four in the case of the

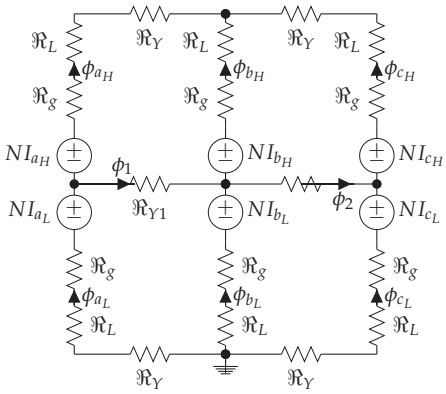


Fig. J.4: Simplified reluctance model of the magnetic structure shown in Fig. J.3(b).

separate inductors. As a result, substantial reduction in the volume of the inductor can be achieved through magnetic integration of L_{f_H} and L_{f_L}.

By analyzing the magnetic structure shown in Fig. J.3(c) and neglecting the asymmetry introduced by the three-limb structure (by neglecting $\Re_Y$), the value of the L_f is obtained as

$$L_f = \frac{4N^2}{2\Re_g + 2\Re_L} \tag{J.9}$$

The reluctance of the air gap is generally large compared to the reluctance of the magnetic material. Therefore, simplified expression for the converter side filter inductor is given as

$$L_f \approx \frac{2N^2}{\Re_g} \approx \frac{2\mu_0 N^2 A_g^{'}}{l_g} \tag{J.10}$$

where μ_0 is the permeability of the free space, l_g is the length of the air gap of one limb and $A_g^{'}$ is the effective cross-sectional area of the air gap after considering the effects of the fringing flux. The effective cross-sectional area of the air gap $A_{g'}$ is obtained by evaluating the cross-section area of the air gap after adding l_g to each dimension in the cross-section.

4 Design of the Integrated Inductor

A design methodology is demonstrated in this section by carrying out the design of the integrated inductor for the high power WECS. The system specifications of the WECS is given in Table K.3. The WECS operates with the

Table J.1: System specifications and parameters for simulation and hardware study

Parameters	Simulations	Experiment
Power S	6.6 MVA (6 MW)	11 kVA (10 kW)
Switching frequency f_{sw}	900 Hz	900 Hz
AC voltage (line-to-line) V_{ll}	3300 V	400 V
Rated current	1154 A	15.8 A
DC-link voltage ($V_{\mathrm{dc}_H} = V_{\mathrm{dc}_L}$)	2800 V	330 V
Modulation index range	$0.95 \leq \mathrm{M} \leq 1.15$	$0.95 \leq \mathrm{M} \leq 1.15$
L_g (including transformer leakage)	525 μH (0.1 pu)	4.2 mH (0.1 pu)

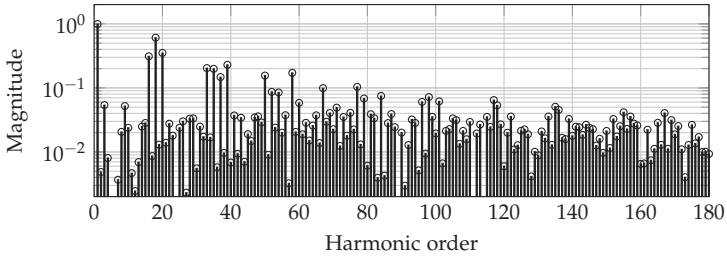
power factor close to unity and in this case, the 60° Discontinuous Pulse-Width Modulation (commonly referred to as a DPWM1 [8]) scheme could result up to 50% switching loss reduction compared to the continuous modulation scheme. Therefore DPWM1 is used to modulate the HSC and the LSC. Using this specifications, the design of the integrated inductor is carried out and the design steps are illustrated hereafter.

4.1 Value of the converter-side inductor L_f

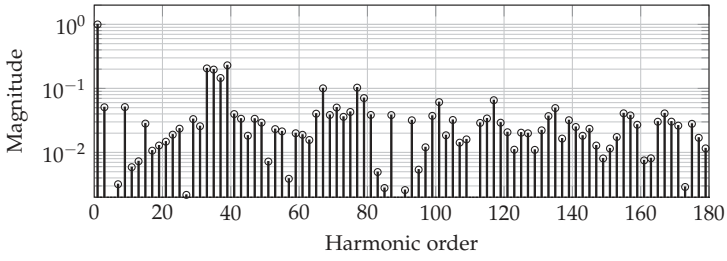
The harmonic spectra of the switched output voltage of the HSC is shown in Fig. J.5(a). The major harmonic components in the switched output voltage of the individual converter appears at the carrier frequency (900 Hz), whereas these components are substantially reduced in the resultant voltage, as shown in Fig. K.5(b). The spectrum comprises the maximum values of the individual voltage harmonic components of the resultant voltage, over the entire operating range is obtained and it is defined as a Virtual Voltage Harmonic Spectrum (VVHS) [9]. Using VVHS, the required admittance for the hth harmonic component is obtained as

$$Y_h^* = \frac{I_{h,BDEW}^*}{V_{h,VVHS}} \tag{J.11}$$

where $I_{h,BDEW}^*$ is the specified BDEW current injection limit of the hth harmonic component (refer to [10]) and $V_{h,VVHS}$ is the maximum values of the hth harmonic components over the entire operating range. The value of the filter parameters are then chosen such that the designed filter has a lower admittance than the required value of the filter admittance for all the harmonic frequency components of interest (upto 180th harmonic frequency component in case of the BDEW standard) [11]. Once the value of L_f is obtained, an optimized design can be carried out.



(a)



(b)

Fig. J.5: Simulated harmonic spectrum of the switched voltages with the modulation index $M = 1$ and the switching frequency of 900 Hz. (a) Switched output voltage of the high-side converter $V_{a_H o_H}$ (normalized with respect to the $V_{\mathrm{dc}}/2$), (b) Resultant voltage ($V_{a_H o_H} - V_{a_L o_L}$) (normalized with respect to the V_{dc}).

4.2 Core Loss Modeling

The Improved Generalized Steinmetz Equation (IGSE) [12, 13] is used to calculate the core losses. The core losses per unit volume is given as

$$P_{fe,v} = \frac{1}{T}\int_0^T k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{J.12}$$

where α, β and k_i are the constants determined by the material characteristics. ΔB is the peak-to-peak value of the flux density and T is the switching interval. The flux waveform has major and minor loops and these loops are evaluated separately.

4.2.1 Major Loop

Assuming the inductance value to be constant, the flux density in the limb corresponding to the phase x is given as

$$B_x(t) = \frac{L_f I_{x,f}(t)}{2NA_c} \tag{J.13}$$

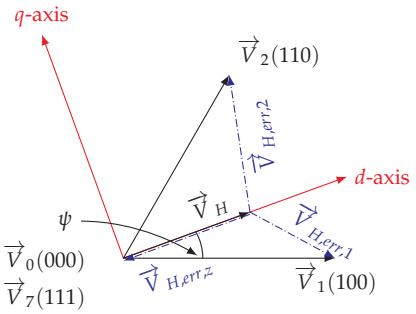


Fig. J.6: The active and zero vectors to synthesize given reference vector and corresponding error voltage vectors.

where A_c is the cross-sectional area of the limb, $I_{x,f}$ is the fundamental component of the current.

4.2.2 Minor Loop

The reference space vector $\overrightarrow{V_H^*}$ and $\overrightarrow{V_L^*}$ are synthesized using active and zero voltage vectors and the volt-second balance is maintained by choosing appropriate dwell time of these vectors. The application of the discrete vectors results in an error between the applied voltage vector and the reference voltage vector, as shown in Fig. J.6 for the HSC. Similarly, the error voltage vectors for the LSC also exists due to the finite sampling. These error voltage vectors lead to the minor loop in the flux density waveform and it is evaluated by performing time integral of the error voltage vector.

The time integral of the error voltage vector is known as the harmonic flux vector [14, 15] and the difference of the harmonic flux vectors of the HSC and the LSC are directly proportional to the flux in the integrated inductor. In the reference frame, rotating synchronously at the fundamental frequency, the instantaneous error voltage vectors can be decomposed into d-axis and the q-axis components and they are for the HSC given as (see Fig. J.6)

$$\begin{aligned}
\overrightarrow{V}_{\boldsymbol{H,err,1}} &= \frac{2}{3}V_{dc}\{(\cos\psi_H - \frac{3}{4}M) - j\sin\psi_H\} \\
\overrightarrow{V}_{\boldsymbol{H,err,2}} &= \frac{2}{3}V_{dc}\{[\cos(60^\circ - \psi_H) - \frac{3}{4}M] \\
&\quad + j\sin(60^\circ - \psi_H)\} \\
\overrightarrow{V}_{\boldsymbol{H,err,z}} &= -\frac{1}{2}V_{dc}M
\end{aligned} \tag{J.14}$$

Similarly, the d-axis and the q-axis components of instantaneous error voltage vectors of the LSC are also obtained. Then the difference of the d-axis com-

ponents of the harmonic flux vectors of the HSC and LSC and the difference of the q-axis components of the harmonic flux vectors of the HSC and LSC are evaluated separately as

$$\begin{aligned} B_{\mathrm{ac},d}(t) &= \frac{1}{2NA_c}\int(\overrightarrow{V}_{H,err,d} - \overrightarrow{V}_{L,err,d})dt \\ B_{\mathrm{ac},q}(t) &= \frac{1}{2NA_c}\int(\overrightarrow{V}_{H,err,q} - \overrightarrow{V}_{L,err,q})dt \end{aligned} \tag{J.15}$$

Using the d-axis and the q-axis components, the ripple component of the flux density in the limb corresponding to the phase a is obtained as

$$B_a = B_{\mathrm{ac},d}\cos\psi - B_{\mathrm{ac},q}\sin\psi \tag{J.16}$$

The VSCs are assumed to be modulated using the asymmetrical regularly sampled PulseWidth Modulation (PWM), where the reference voltage space voltage vector is sampled twice in a carrier cycle.

Using this information, the core loss calculations have been carried out for the major loop and each of the minor loops.

4.3 Copper Loss Modeling

The copper loss is evaluated by considering the ac resistance of the winding, which takes into account the skin and proximity effects [16]. The total winding losses due to the harmonic frequency components of the coil current is [17]

$$P_{cu} = R_{dc}\sum_{h=1}^{\infty} k_{p_h} I_{x_h}^2 \tag{J.17}$$

where

$$\begin{aligned} k_{p_h} =& \sqrt{h}\Delta\Big[\frac{\sinh(2\sqrt{h}\Delta)+\sin(2\sqrt{h}\Delta)}{\cosh(2\sqrt{h}\Delta)-\cos(2\sqrt{h}\Delta)} \\ &+ \frac{2}{3}(m^2-1)\frac{\sinh(\sqrt{h}\Delta)-\sin(\sqrt{h}\Delta)}{\cosh(\sqrt{h}\Delta)+\cos(\sqrt{h}\Delta)}\Big] \end{aligned} \tag{J.18}$$

and $\Delta = T_c/\delta$ and R_{dc} and R_{ac} are the dc and the ac resistance of the coil, respectively. m is the number of layers in the coil, T_c is the thickness of the conductor, and δ is the skin depth. I_{x_h} is the hth harmonic frequency component of the line current I_x. The harmonic spectrum of the resultant voltage is obtained analytically [18] and the hth harmonic frequency component of the line current I_x is obtained as

$$I_{x_h} = Y_{H,LCL}V_h \tag{J.19}$$

where V_h is the hth harmonic frequency component of the resultant voltage and $Y_{H,LCL}$ is the admittance offered by the LCL filter to the hth harmonic frequency component.

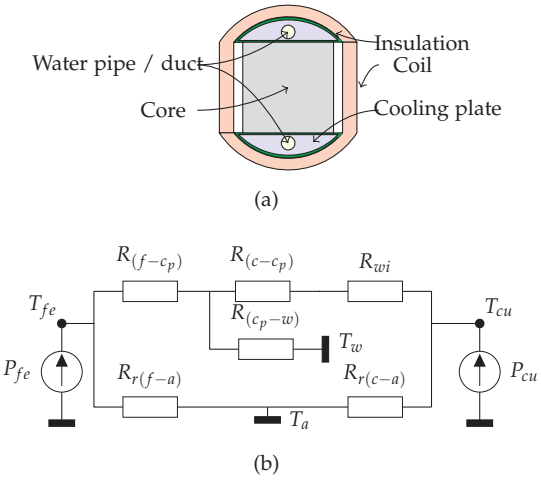


Fig. J.7: Simplified thermal model of the integrated inductor. P_{fe} and P_{cu} are the core and copper losses, respectively.

4.4 Thermal Modeling

The liquid cooling of the inductor is considered and the cooling arrangement is shown in Fig. J.7(a). The semi-circular aluminum cooling plates with the duct to carry the coolant is considered. This cooling plate is electrically insulated using the epoxy resin. As the heat transfer is anisotropic for the laminated steel, two cooling plates along the edges that are perpendicular to the lamination direction are considered. The hot spot temperature in both the core and the coil (T_{fe} and T_{cu}, respectively) is estimated using the equivalent thermal resistance network [19], shown in Fig. J.7(b). For the simplicity of the analysis, the temperature in the core and the coil is assumed to be homogeneous.

The heat transfer mechanism due to the convection and the radiation is considered, where $R_{cv(f-w)}$ and $R_{cv(c-w)}$ are the convection thermal resistance between the core and coolant (water) and between the coil and coolant, respectively. Similarly, $R_{r(f-a)}$ and $R_{r(c-a)}$ represent the radiation thermal resistance between the core and the ambient and between the coil and the ambient, respectively. The radiation thermal resistance value is obtained using the formulas presented in [19].

The thermal resistance between the cooling plate and the coolant is given as

$$R_{(c_p-w)} = \frac{1}{h_{c_p-w} A_{c_p-w}} \tag{J.20}$$

where h_{c_p-w} is the heat transfer coefficient and A_{c_p-w} is the coolant contact surface. The heat transfer coefficient is

$$h_{c_p-w} = 3130\,(\frac{q}{785.4D_d^2})^{0.87}(100D_d)^{-0.13} \tag{J.21}$$

where q is the coolant flow rate in [l/s] and D_d is the diameter of the duct in [m]. The thermal resistance between the core and duct surface is given as

$$R_{(f-c_p)} = \frac{2L_{eq}}{\lambda_{cp}(A_{c_pf} + \pi D_d L_d)} + \frac{T_i}{\lambda_i A_{c_pf}} \tag{J.22}$$

where L_{eq} is the equivalent distance from the cooling surface to the duct, $A_{c_{pf}}$ is the contact area of the cooling plate with the core, L_d is the length of the duct, and λ_{cp} is the thermal conductivity of the aluminum. T_i is the thickness of the insulation and λ_i is the thermal conductivity of the insulation. Using (J.20) and (J.22), the thermal resistance between the core and the coolant is obtained as

$$R_{cv(f-w)} = R_{(f-c_p)} + R_{(c_p-w)} \tag{J.23}$$

In a similar manner, the thermal resistance between the coil and the coolant $R_{cv(c-w)}$ can be also obtained. However, in the heat flow path of the copper losses, there is an additional layer of the insulation material, which is represented as R_{wi} in Fig.J.7(b).

4.5 Loading Profile and Energy Yield

The typical wind profile and the power output of a wind turbine over an one year span is shown in Fig. J.8. As it is evident from Fig. J.8, the power processes by the converter varies in large range and optimizing the inductor for a specific loading condition may result in the suboptimal overall performance. Therefore, instead of optimizing the inductor efficiency at specific loading condition, the energy loss is minimized. In addition to the energy loss minimization, the volume minimization is also considered and multi-objective optimization has been carried out. The energy loss (kWh) per year is calculated using the loading profile and loss modeling and it is used into the optimization algorithm.

4.6 Optimization Process

The multi-objective optimization has been performed, which minimize a vector of objectives $F(X)$ and returns the optimal parameters values of X.

$$\min F(X) \tag{J.24}$$

where

$$F(X) = [F_1(X), F_2(X)] \tag{J.25}$$

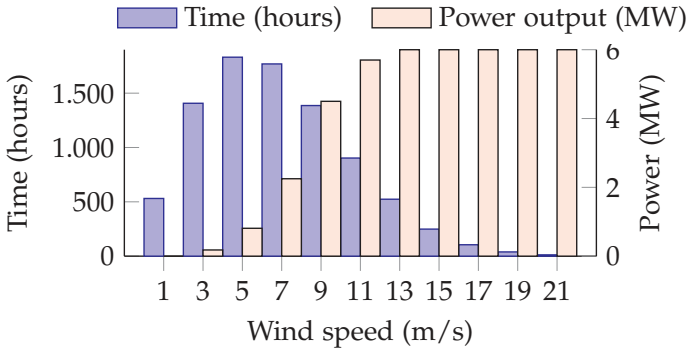


Fig. J.8: Wind profile and associated output power of a typical 6 MW wind turbine.

where $F_1(X)$ returns the energy loss (kWh) and $F_2(X)$ returns the volume of the active parts of the inductor (ltr.). The parameters that are optimized are

$$X = [N\ B_m\ J\ m\ W_c]^T \tag{J.26}$$

where B_m is the maximum flux density and J is the current density. W_c is the width of the coil (refer Fig. J.3(c)). Once the system specifications and the constraints are defined, the optimization has been carried out. As the number of turns N and the number of layers m only take the integer values, mixed-integer optimization problem has been formulated. The steps followed for optimizing the system specified in Table K.3 is shown in Fig. J.9 and explained briefly hereafter.

4.6.1 Step 1: Value of the converter-side inductor L_f

The leakage inductance of the transformer is considered as a part of the grid-side inductor L_g and the use of any additional inductor is avoided. Therefore, the value of the L_g is fixed and the values of the L_f and C_f are obtained while observing the following constraints:

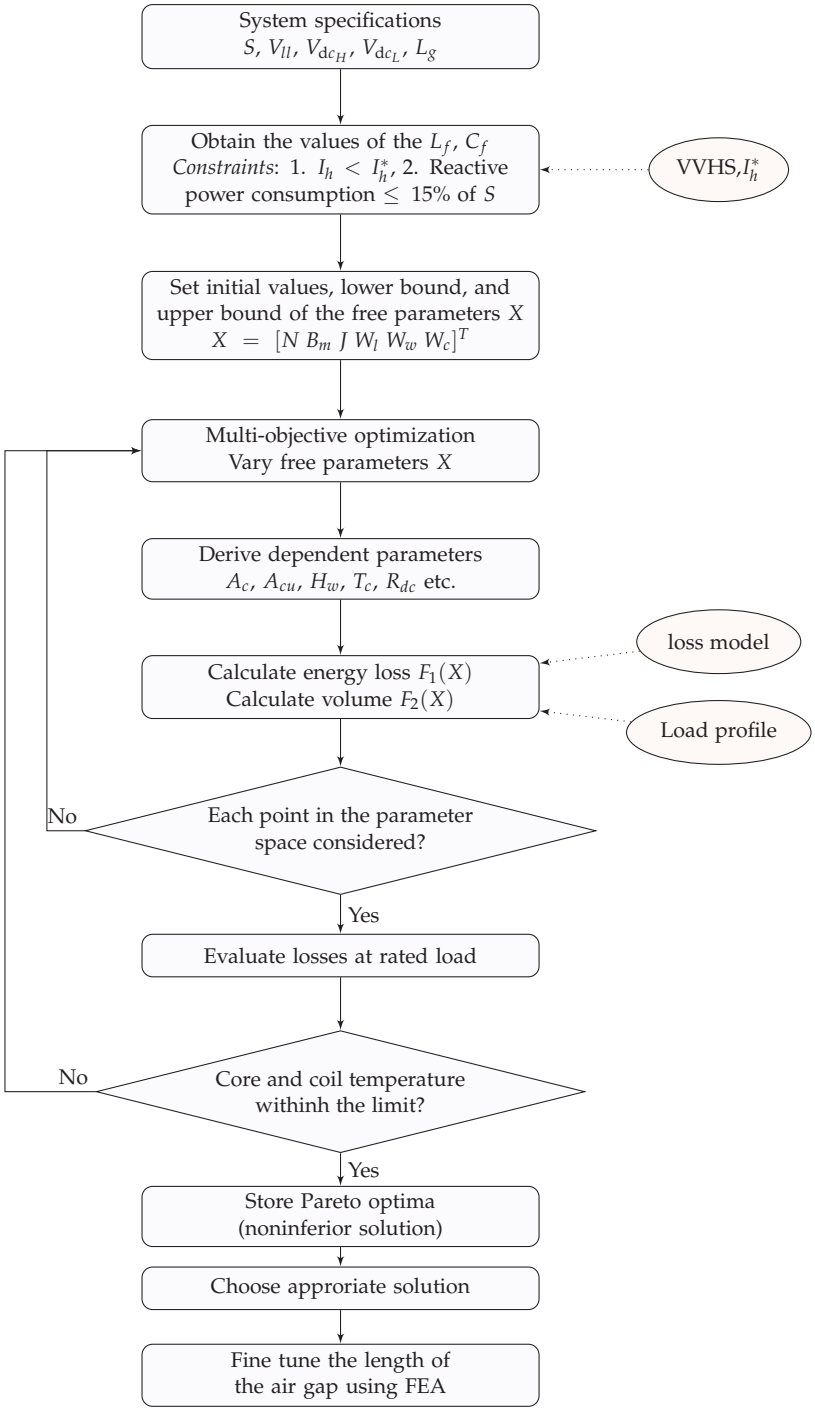


Fig. J.9: Block diagram, which illustrates the steps of the optimization procedure.

Table J.2: Values of L_f and C_f of the LCL filter

Parameters	Values
L_f	1200 μH (0.22 pu)
Shunt capacitance $C_f + C_d$	289 μF (0.15 pu)

1. $I_h < I_h^*$ where h is the harmonic order ($2 \leq h \leq 180$)
2. Reactive power consumption in shunt branch $\leq$ 15% of rated power.

The calculated values of the L_f and C_f are listed in Table J.2.

4.6.2 Step 2: Derive dependent design variables

The dependent design variable are derived from the free design variables and the system specifications. The cross-sectional area of the core is obtained as

$$A_c = \frac{L_f I_{max}}{2NB_m} \tag{J.27}$$

where I_{max} is the rated current. The dimensions of the core is then obtained as $W_l D_l = A_c/k_s$, where k_s is the stacking factor. For simplicity, $W_l = B_l$ is assumed in this study. The cross-section area of the conductor is obtained as

$$A_{cu} = W_c T_c = \frac{I_{max}}{J} \tag{J.28}$$

4.6.3 Step 3: Objective function evaluation

The objective functions $F_1(x)$ and $F_2(x)$ are evaluated for the given set of parameters and specific mission profile. The core losses and the copper loss for each of the specific loading conditions, shown in Fig. J.8, are evaluated. Using this information, the energy loss over one year period is evaluated. Similarly, the volume of both the core and the copper is also calculated.

4.6.4 Step 4: Air gap length

The liquid cooling effectively removes the heat generated due to the copper losses and allows designers to reduce the constant losses (mostly core losses) by increasing the number of turns N. This leads to an improvement in the energy efficiency. However, a larger number of turns also results in larger air gap, which leads to higher fringing flux. The solution is to use several small air gaps, which is achieved by using the discrete core blocks. The length of each of these air gaps and core blocks is limited to 2.5 mm and 30 mm, respectively. If any of these quantities is violated, the solution is discarded.

Table J.3: Parameter values of the selected design.

Item	Value	Item	Value	Item	Value
N	25	A_c	30200 mm^2	B_m	1.36 T
W_w	140 mm	J	4.08 A/mm^2	W_c	33 mm
A_{cu}	396 mm^2	H_w	980 mm	k_s	0.92
k_w	0.6	T_c	12 mm	m	2
k_i	0.96	α	1.55	β	1.87

4.6.5 Step 5: Temperature estimation

The core and the copper losses are evaluated at the rated load conditions and the results are fed to the thermal network shown in Fig. J.7(b). By solving the thermal network, temperature of the core (T_{fe}) and the coil (T_{cu}) is obtained. This gives the worst case temperature rise. If the temperature rise is above the prescribed value, the solution is discarded and the optimization steps are again executed for a new set of free variables.

4.6.6 Step 6: Pareto optima solutions

The energy loss and the volume of the inductor are closely coupled and competes with each other. For example, In a given system, the reduction in the volume often leads to the rise in the losses. As a result, there is no unique solution to the optimization problem and several noninferior solutions (Pareto front) are obtained. These solutions are stored. Depending upon the application, suitable design (out of these noninferior solutions) is chosen.

4.6.7 Step 7: FEA analysis

The length of the air gap during the optimization process is obtained using the simplified reluctance model. This may lead to the inductance value to deviate slightly from the desired value. Moreover, other non linearities are also neglected in the simplified model and it is very necessary to perform the Finite Element Analysis (FEA) to fine tune the length of the air gap so that the desired value of the inductance can be obtained. This has been achieved using by performing 'Optimetrics 'analysis in Ansys Maxwell.

5 Designed Parameters and Volumetric Comparison

A non-inferior (Pareto optimal) solution is obtained as shown in Fig. J.10, where the reduction in the energy loss requires increase in the volume. Out

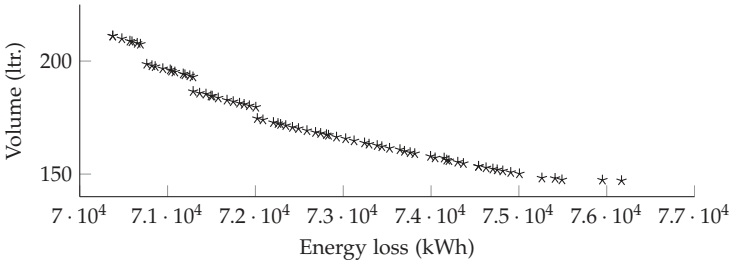


Fig. J.10: Calculated volume and energy loss of the integrated inductor for different Pareto optimal solutions.

Table J.4: Inductances values obtained using the finite element analysis. All values are in μ H.

Coil	a_H	b_H	c_H	a_L	b_L	c_L
a_H	375	−84	−62	115	−19	−39
b_H	−84	384	−84	−19	104	−19
c_H	−62	−84	375	−39	−19	115
a_L	115	−19	−39	375	−84	−62
b_L	−19	104	−19	−84	384	−84
c_L	−39	−19	115	−62	−84	375

of these several possible design solutions, one that suits the application the most, has been selected. The parameter values of the selected design are given in Table J.3.

The volume of the inductor is 187.1 ltr. and the energy loss over one year span is 72899 kWh. The coils are designed to carry the rated current (1154 A) and can be wound using copper bars. The major harmonic component in the coil current is at 1.8 kHz and at this frequency, the increase in the ohmic losses in the ac resistance of the coil due to skin effect is insignificant. Therefore, the use of the copper bars for the coils is considered.

Multiple are gaps are achieved using the discrete core blocks and the length of each of the air gap is fine tuned using the FEA analysis. The FEA analysis is performed on the inductor geometry given in Table J.3. The length of each of the air gap is fine tuned and it is found to be 2.46 mm. The flux density distribution in the inductor core is shown in Fig. J.11. The inductance matrix is also obtained from the FEA and it is given in J.4. The line filter inductance is obtained from these value and it is given as

$$L_f = 1184\,\mu\text{H} \tag{J.29}$$

The core and the copper losses of the inductor over the whole operating range is shown in Fig. J.12. The core losses and the copper losses at the full

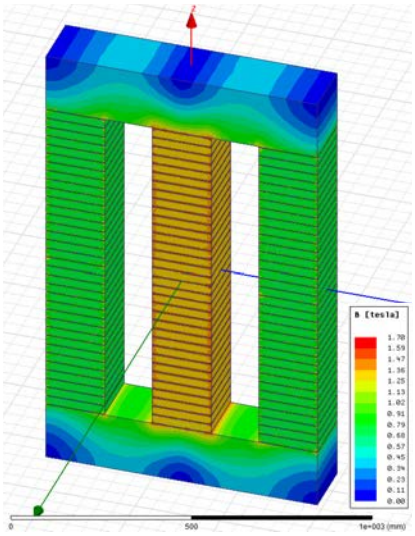


Fig. J.11: Flux density distribution in the magnetic core. Both the coils on the central limb carry 1630 A current (peak of the rated current), whereas the other four coils on the side limbs carry half of peak value of the rated current in the opposite direction (-815 A).

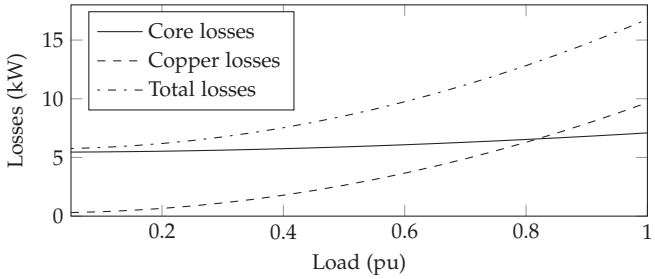


Fig. J.12: Core and copper losses of the integrated inductor with different loading conditions.

load conditions are 7.09 kW and 9.67 kW, respectively. The coolant flow in each of the duct is taken to be 0.06 l/s and the duct diameter D_d is 0.01 m. The inlet temperature of the coolant is assumed to be 20°C. The core temperature at the rated load is calculated to be 74 °C, whereas the temperature of the coil is found to be 86 °C.

5.1 Volumetric comparison

The magnetic integration leads to a reduction in the size of the inductor. This has been demonstrated by comparing the volume of the integrated inductor

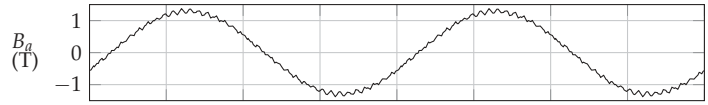


Fig. J.13: Simulated flux density waveform in the limb of phase a.

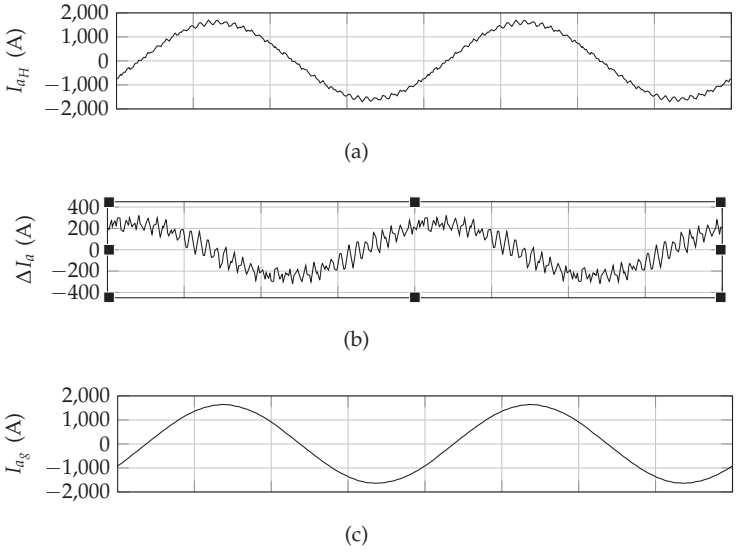


Fig. J.14: Simulation results. (a) Flux density waveform in the limb of phase a, (b) Output current of the high-side converter I_h, (c) Current through the shunt branch of the LCL filter, (d) Current through the open-end transformer windings.

with the volume of the inductors in a separate inductor case. The values of the current density of the copper, the maximum flux density in the core and the number of turns N are taken to be the same in both the cases. The volume of the magnetic material of the integrated inductor is calculated to be 132.2 ltr, compared to the 177.3 ltr. for the separate inductors. This demonstrates around 25.4% reduction in the magnetic material, which translates to 314 kg reduction in the weight of the magnetic material (assuming the use of the grain oriented steel).

6 Simulation and Hardware Results

The time domain simulations have been carried out using PLECS. The parameters used in the simulations are specified in Table K.3. The integrated

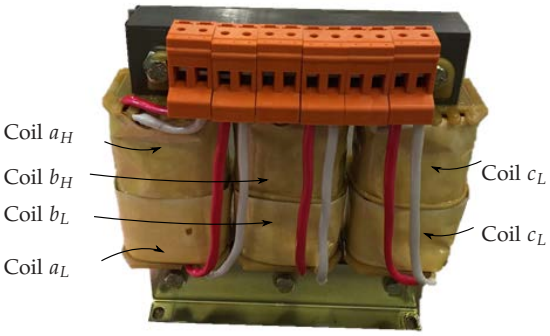


Fig. J.15: Photo of the implemented inductor.

inductor is modeled using the magnetic toolbox, which uses the permanence model.

The converter is operated at the rated power and the simulated flux density waveform in one of the limb is shown in Fig. J.13. The flux density has a dominant fundamental frequency component with major harmonic component at the 2nd carrier harmonic frequency. The output current of the HSC is shown in Fig. J.14(a), which has a major harmonic component at 2nd carrier frequency harmonic. As the leg current in the HSC and the LSC is the same ($I_{a_H} = I_{a_L}$), only the current of the HSC I_{a_H} is shown. The shunt branch of the LCL filter offers low impedance path to the harmonic components, as shown in Fig. J.14(b). As a result, the injected grid currents have the desired waveform quality, as shown in Fig. J.14(c).

A small scale prototype has been built to verify the effectiveness of the proposed inductor. The specifications of the small scale system is given in Table J.2. The integrated inductor is realized using the standard laminated steel (0.35 mm) and the coils are wound using the AWG 11. Each coils have 102 turns and the length of the air gap is 2.014 mm. The photo of the inductor prototype is shown in Fig. J.15. The converter-side inductance is 9 mH (0.195 pu) and the capacitance of the shunt branch is 24 μF (0.11 pu). The dc-link voltage was derived from the dc power supply and the ac power source from the California Instruments (MX-35) was used to emulate the grid. The converter was operated at the rated load conditions and the experimental results are shown in Fig. J.16. The harmonic spectra of the injected current is shown in Fig. J.17, where it is evident that the harmonic injection limits are obeyed.

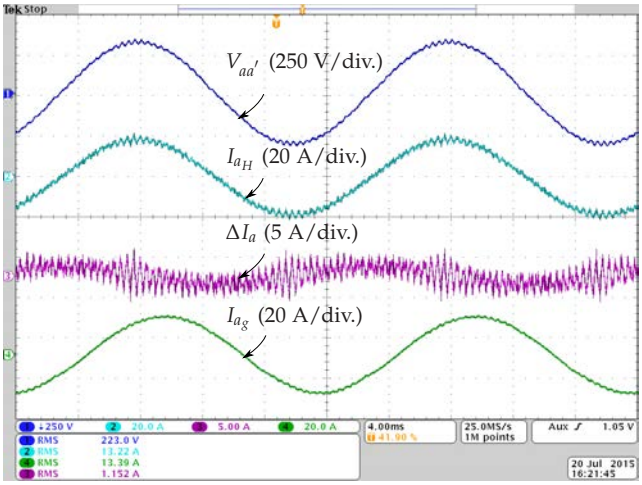


Fig. J.16: Experimental results with the system operated at the rated load. Ch1: Voltage across the shunt capacitive branch of phase *a* of an *LCL* filter, Ch2: Phase *a* current of the high side converter, Ch3: Current through the shunt branch of the *LCL* filter, Ch4: Phase *a* grid current.

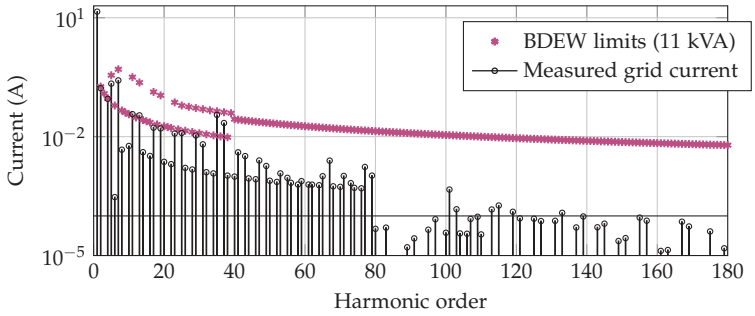


Fig. J.17: Harmonic spectra of the measured grid current and associated BDEW harmonic injection limits.

7 Conclusion

An integrated inductor for the the dual-converter fed open-end transformer topology is proposed. The dual-converter system often comprises of two identical VSCs. These two VSCs use two separate converter-side inductors for the *LCL* filter implementation. For the dual-converter system, the output currents of the given phase of both VSCs are equal. This property of the dual-converter system is exploited to cancel out the flux in one of the yokes of both the inductors through the magnetic integration. Moreover, a multi-objective

optimization has been performed to identify best possible solutions which leads to the minimization of the energy loss and minimization of the volume of the inductor. The size reduction achieved through magnetic integration is demonstrated by comparing the volume of the proposed solution with the separate inductor case. The integrated inductor leads to 25.4% reduction in the volume of the magnetic material. This translates to 314 kg reduction in the weight of the magnetic component for the 6.6 MVA, 3.3 kV WECS system. The performance of the filter has been verified by simulation and experimental studies.

References

[1] G. Grandi, C. Rossi, D. Ostojic, and D. Casadei, "A new multilevel conversion structure for grid-connected pv applications," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4416–4426, Nov 2009.

[2] H. Stemmler and P. Guggenbach, "Configurations of high-power voltage source inverter drives," in *Proc. of Fifth European Conference on Power Electronics and Applications*, Sep 1993, pp. 7–14 vol.5.

[3] T. Boller, J. Holtz, and A. Rathore, "Optimal pulsewidth modulation of a dual three-level inverter system operated from a single DC link," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 1610–1615, Sept 2012.

[4] N. Bodo, M. Jones, and E. Levi, "A space vector pwm with common-mode voltage elimination for open-end winding five-phase drives with a single DC supply," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2197–2207, May 2014.

[5] M. R. Baiju, K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, May 2004.

[6] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 1893–1909, May 2008.

[7] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 708–719, March 2012.

[8] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[9] A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, 2011.

[10] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[11] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[12] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, 2002, pp. 36–41.

[13] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Thirty-Sixth IAS Annual Meeting, IEEE Industry Applications Conference.*, vol. 4, 2001, pp. 2203–2210 vol.4.

[14] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based PWM-vsi drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan 1999.

[15] G. Narayanan and V. T. Ranganathan, "Analytical evaluation of harmonic distortion in PWM AC drives using the notion of stator flux ripple," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 466–474, 2005.

[16] P. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers,*, vol. 113, no. 8, pp. 1387–1394, August 1966.

[17] W. Hurley, E. Gath, and J. Breslin, "Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 369–376, Mar 2000.

[18] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved three-phase voltage source converters," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3400–3414, May 2016.

[19] A. V. d. Bossche and V. C. Valchev, *Inductors and Transformers for Power Electronics*. Boca Raton, FL: CRC Press, 2004.

Paper K

Dual Converter Fed Open-end Transformer Topology with Parallel Converters and Integrated Magnetics

Ghanshyamsinh Gohil,
Lorand Bede,Remus Teodorescu,
Tamas Kerekes, and Frede Blaabjerg

The paper has been submitted for the publication in the
IEEE Transactions on Industrial Electronics

The layout has been revised.

Abstract

In the high power applications, the converter system is often connected to a medium-voltage network using a step-up transformer. The converter-side winding of the transformer is configured as an open-end and both the ends of the windings are fed from two different converter groups. Each converter group comprises of two parallel Voltage Source Converters (VSCs). The harmonic quality of the resultant voltage of each of the converter group is improved by interleaving the carrier signals of the parallel VSCs. However, an additional inductive component is required to suppress the circulating current that flows between the parallel interleaved VSCs. An integrated inductor is proposed which suppresses the circulating current in both the converter groups. In addition, the functionality of the line filter inductor is also integrated. Flux in various parts of the integrated inductor is analyzed and a design procedure is also described. The volume and the losses of the proposed solution are compared with that of the state-of-art solution. The control of the proposed converter system is discussed. The analysis has been verified by the simulation and experimental results.

Nomenclature: Paper K

$A_g^{'}$ Effective cross-section area of the air gap.

A_w Window area.

B_{m_l} Permissible value of the flux density in the limb.

B_{m_y} Permissible value of the flux density in the yoke.

C_d Damping capacitor.

C_f Shunt capacitive branch of the *LCL* filter.

I_r Rated current.

I_x Resultant line current.

I_h hth harmonic frequency component of the leg current.

I_{x_H} Resultant line current of the high-side converter group.

I_{x_L} Resultant line current of the low-side converter group.

I_{x_k} Leg current of phase x of the k VSC.

$I_{x_{H,c}}$ Circulating current between the parallel interleaved VSCs of the high-side converter group.

$I_{x_{L,c}}$ Circulating current between the parallel interleaved VSCs of the low-side converter group.

J Current density.

K_s Stacking Factor.

K_w Window utilization factor.

L_c Circulating current inductance.

L_f Line filter inductance.

L_g Grid-side incductor of the LCL filter.

M Modulation index, defined as the ratio of the peak of the reference signal to the half of the dc-link voltage.

N Number of turns.

R_d Damping resistor.

R_{ac} AC resistance of the coil.

R_{dc} DC resistance of the coil.

S VA rating of the converter.

T_c Thickness of the conductor.

T_s Switching interval.

V_x Resultant phase voltage.

$V_{x_H o_H}$ Resultant switched output voltage of high-side converter group.

$V_{x_L o_L}$ Resultant switched output voltage of low-side converter group.

V_{ph} Rated phase voltage.

$V_{x_k o_H}$ Switched output voltage of phase x of k^{th} VSC with respect to the o_H.

$V_{x_k o_L}$ Switched output voltage of phase x of k^{th} VSC with respect to the o_L.

V_{x_s} Resultant switched output voltage of phase x.

$V_{x_{C,f}}$ Voltage across the filter capacitor.

ΔB Peak-to-peak value of the flux density.

$\Re_l$ Reluctance of a limb.

$\Re_y$ Reluctance of the top, the bottom, and the common yoke.

$\Re_{bl}$ Reluctance of a bridge leg.

$\Re_{g_1'}$ Equivalent reluctance of an air gap g_1.

$\Re_{g_2'}$ Equivalent reluctance of an air gap g_2.

$\mathbf{V_H^*}$ Reference voltage space vector for HSCG.

$\mathbf{V_L^*}$ Reference voltage space vector for LSCG.

$\boldsymbol{I_c}$ Vector representing the circulating current component of the leg currents of phase x.

$\boldsymbol{I_r}$ Vector representing the resultant current component of leg currents of phase x.

$\boldsymbol{I}$ Vector representing the leg currents of phase x.

$\boldsymbol{L_c}$ Circulating current inductance matrix.

$\boldsymbol{V_p}$ Switched output voltage vector.

$\boldsymbol{V_v}$ Voltage vector, representing the potential of the common points of the HSCG and the LSCG.

$\boldsymbol{V}$ Coil voltage vector.

$\boldsymbol{\phi}$ Vector representing the flux that links with the corresponding coils.

δ Skin depth.

μ_0 Permeability of the air.

$\phi_{bl_{max}}$ Maximum value of the flux in the bridge legs.

$\phi_{l_{max}}$ Maximum value of the flux in the limbs.

$\phi_{x,k}$ Total flux linking k coil of phase x.

$\phi_{x_{by}}$ Flux in a bottom yoke.

$\phi_{x_{cy}}$ Flux in a common yoke.

$\phi_{x_{k,c_{max}}}$ Maximum value of the circulating flux component.

$\phi_{x_{ty}}$ Flux in a top yoke.

$\phi_{y_{max}}$ Maximum value of the flux in the top and the bottom yokes.

ψ_H Reference voltage space vector angle for HSCG.

ψ_L Reference voltage space vector angle for LSCG.

ψ_{max} voltage space vector angle for which the circulating flux component achieves its maximum value.

l_{g_1} Air gap length between the cell and the bridge leg.

l_{g_2} Length of the air gap in the cell structure.

m Number of layers in the coil.

x Subscript, which represents phases a, b, and c.

1 Introduction

The demand for a high power grid-connected converters has increased in recent years. However, a power handling capability of the state-of-the-art semiconductor devices is limited. Therefore the standard two-level Voltage Source Converter (VSC) alone can not meet the desired high power level in such applications. One of the ways to increase the current level is to connect several VSCs in parallel [1, 2]. However, the cabling in case of the low voltage high current converter systems is a major design challenge [3].

For the given power, the current can be reduced by using a medium voltage converter. A three-level neutral point diode clamped (3L-NPC) topology is commonly used [4]. However, an extra control efforts are required to balance the dc-link capacitor voltage [5]. Moreover, the semiconductor loss distribution is unequal [6] and this may lead to the de-rating of the VSC [3]. On the other hand, the two-level VSC is used extensively in many industrial applications due to its simple power circuitry and proven technology. Therefore, it is highly desirable to realize the medium voltage converter system using the standard two-level VSC.

Many grid-connected applications use transformer between the converter system and a grid for matching the voltage levels. Also in some applications, the grid codes demand galvanic isolation. In such systems, the primary winding can be configured as an open-end winding and can be fed from both the ends using two-level VSCs [7]. The number of levels in the output voltage is same as that of the 3L-NPC and each of the two-level VSC operates with the half of the dc-link voltage than that of the 3L-NPC. However, common-mode (CM) circulating current flows through the closed path if both the VSCs are connected to the common dc-link. The CM circulating current can be suppressed either by using a CM choke [8] or by employing proper Pulse Width Modulation (PWM) scheme to ensure complete elimination of the CM voltage [9, 10]. However, in many applications, isolated dc-links can be readily derived from the source itself and such extra measures for the CM circulating current suppression may not be required. For example, the isolated dc-links can be obtained in

1. PhotoVoltaic (PV) systems by dividing the total number of arrays into two groups to form separate dc-links [7].

2. Wind Energy Conversion System (WECS): isolated dc-links can be obtained using the dual stator-winding generator [11].

Therefore, the analysis presented in this paper is mainly focused on the dual converter fed open-end transformer topology with two separate dc-links.

In a dual converter fed open-end transformer topology, each VSC has to process the rated current. In many high power applications, single two-level

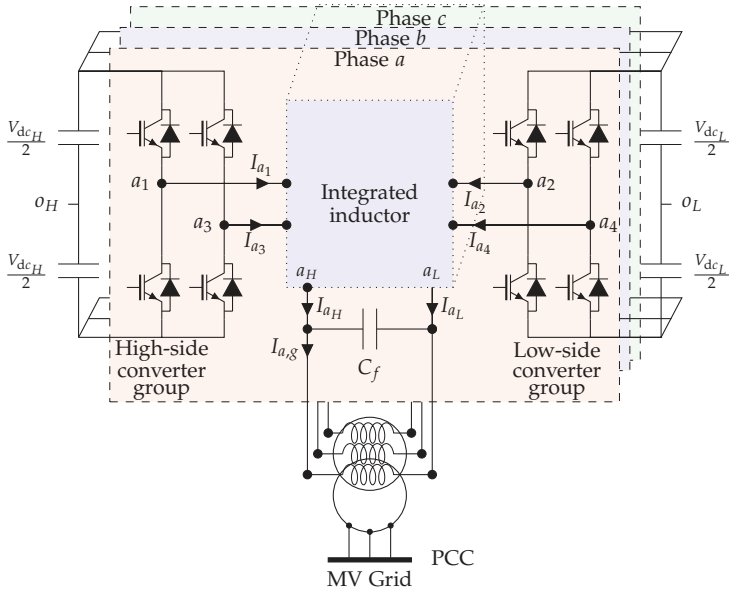


Fig. K.1: The system configuration of the dual converter fed open-end winding transformer topology with two separate dc-links. The open-end primary windings are connected to the two converter groups, with each converter groups having two parallel interleaved two-level voltage source converters. The integrated inductor is used to suppress the circulating current between the parallel VSCs of both the converter groups and also used for the line current filtering.

VSC may not be able to supply the rated current. To overcome this problem, parallel connection of the two-level VSCs in each of the converter groups of the open-end transformer topology is proposed, as shown in Fig. K.1. In this way, both the voltage and the current handling capability of the converter can be increased.

Another issue in the high power converter is the limited switching frequency capability of the semiconductor devices [12]. Therefore, large filter components are generally employed in order to comply with the stringent power quality requirements imposed by the utility [13]. This lead to the increased cost, size and losses. The size of the filter components can be reduced by improving the harmonic quality of the output voltage of each of the converter group by interleaving the carrier signals of the parallel connected VSCs [14–16]. However, circulating current is generated between the parallel VSCs due to hardware and control asymmetries and carrier interleaving further aggravates this problem. This unwanted circulating current increases stress on the semiconductor switches and causes additional losses and it should be suppressed.

The circulating current between the parallel VSCs can be suppressed by

providing magnetic coupling between the parallel interleaved legs of the corresponding phases [17–19]. Therefore, in addition to a line filter inductor, a circulating current filter inductor is also required. The size of these inductors can be significantly reduced by integrating them into a single magnetic component [20, 21]. A magnetic integration of both the circulating filter inductor and the line filter inductor of both the converter groups is presented in this paper and the design methodology is also described. The paper is organized as follows: the system is described in Section II. The integrated inductor is analyzed in Section III. The design of the integrated inductor is illustrated in Section IV. The control scheme and the comparative evaluation is presented in Section V. Section VI finally summarizes the simulation and hardware results.

2 System Description

A dual converter fed open-end winding transformer topology with two separate dc-links is shown in Fig. K.1. Four two-level three phase VSCs are used. Out of these four VSCs, VSC_1 and VSC_3 are connected in parallel and share the same dc-link. The carrier signals of these two parallel two-level VSCs are interleaved. As a result, three-level resultant voltage waveforms can be achieved [15, 20]. Therefore, the parallel connection of the VSC_1 and the VSC_3 can be treated as a single three-level converter and referred to as a High-Side Converter Group (HSCG). Similarly, the parallel connection of the VSC_2 and VSC_4 forms another converter group, which is referred to as a Low-Side Converter Group (LSCG). The low-voltage side of the transformer winding is configured as an open-end and fed from the both the ends using the HSCG and the LSCG.

The carrier signals of the parallel connected VSCs are symmetrical interleaved and phase shift between the carrier signals is given in Table K.1. The phase shift between the carrier signals of the VSCs of each of the converter groups is 180°. As a result, the switched output voltages of the respective phases of both the VSCs are also phase shifted and yield three-level resultant voltage waveform. As a result, harmonic performance similar to the three-level converter can be achieved from the two parallel interleaved two-level VSCs. However, the instantaneous potential difference appears across the close path when the carrier signals are interleaved. This potential difference could drive large circulating current between the parallel VSCs due to the use of the common dc-link. This leads to the increase in the stress and the losses of the semiconductor devices and the passive components. Therefore, it is important to suppress the circulating current to some acceptable value to realize the full potential of the carrier interleaving.

Table K.1: Phase shift between the carrier signals

Converter	VSC_1	VSC_2	VSC_3	VSC_4
Phase shift	0°	90°	180°	270°

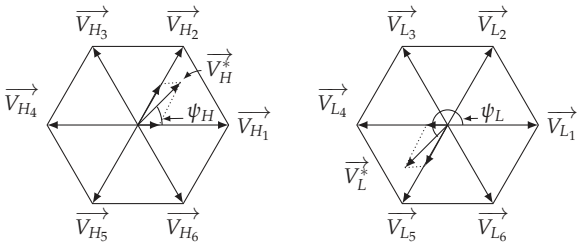


Fig. K.2: Reference voltage space vector and its formation by the geometrical summation. (a) Reference voltage space vector for the VSCs of the high-side converter group, (b) Reference voltage space vector for the VSCs of the low-side converter group. The voltage space vector angle of the low-side converter group $\psi_L = 180^\circ + \psi_H$.

2.1 Modulation

The reference voltage space vectors of both the HSCG and the LSCG have same magnitude. However, the respective voltage space vector angles (ψ_H and ψ_L) have a phase difference of 180°, as shown in Fig. K.2. VSCs in both the converter groups are modulated using the 60° clamp discontinuous PWM (DPWM1) scheme [22]. The clamping intervals of 60° are arranged around the positive and negative peak of the fundamental reference voltage. For the applications, where the displacement power factor is close to unity, the switching is avoided when the current through the devices is near its peak. As a result, the switching losses can be reduced upto 50% compared to that of the continuous space vector modulation [23]. As most of the grid-connected renewable energy systems operate with the power factor close to one, the DPWM1 is considered as a modulation scheme in this paper.

2.2 Harmonic Quality Assessment

The dwell times of the respective voltage vector is same in both of the parallel VSCs of the given converter group. However, because of the interleaving of the carrier signal, they are applied at the different time duration, as shown in Fig. K.3(a). The switching sequences and the switched output voltage of the individual VSCs (with respect to their individual fictitious reference points,

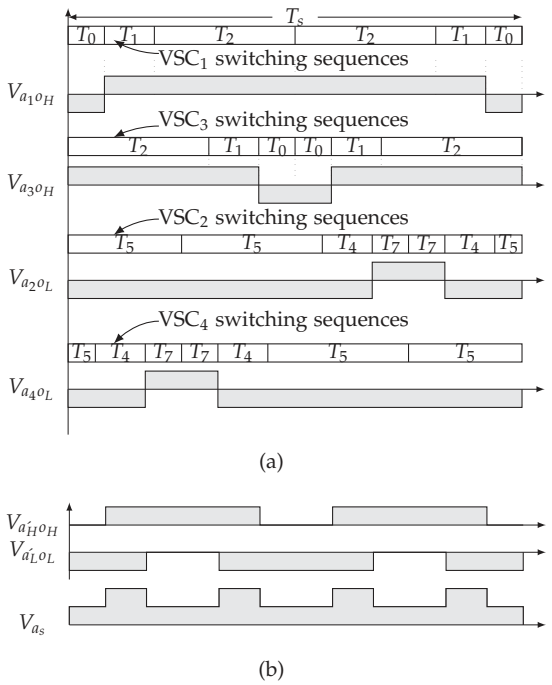


Fig. K.3: The switching sequences and switched output voltages of phase a for $M = 1$ and $\psi_H = 45°$. (a) Individual switched output voltages, (b) Switched output voltages of the high-side converter group $V_{a'_Ho_H}$, the low-side converter group $V_{a'_Lo_L}$, and the resultant switched output voltage V_{a_s}.

as shown in Fig. K.1) for a particular switching cycle is shown in Fig. K.3(a).

For the parallel interleaved VSCs, the resultant switch output voltage of a given phase is the average of the individual switched output voltages of the parallel interleaved legs of that phase and for the HSCG, it is given as

$$V_{x'_Ho_H} = \frac{V_{x_1o_H} + V_{x_3o_H}}{2} \tag{K.1}$$

Similarly, the resultant output voltage of the LSCG is given as

$$V_{x'_Lo_L} = \frac{V_{x_2o_L} + V_{x_4o_L}}{2} \tag{K.2}$$

The resultant switched output voltages of both of the groups ($V_{x'_Ho_H}$ and $V_{x'_Lo_L}$) are also shown in Fig. K.3(b), which exhibits three-level voltage waveforms. The simulated resultant voltage waveform of the HSCG over a fundamental period is shown in Fig. K.4(a). The closed form theoretical harmonic solution for resultant voltage for asymmetrical regular sampled DPWM1 is

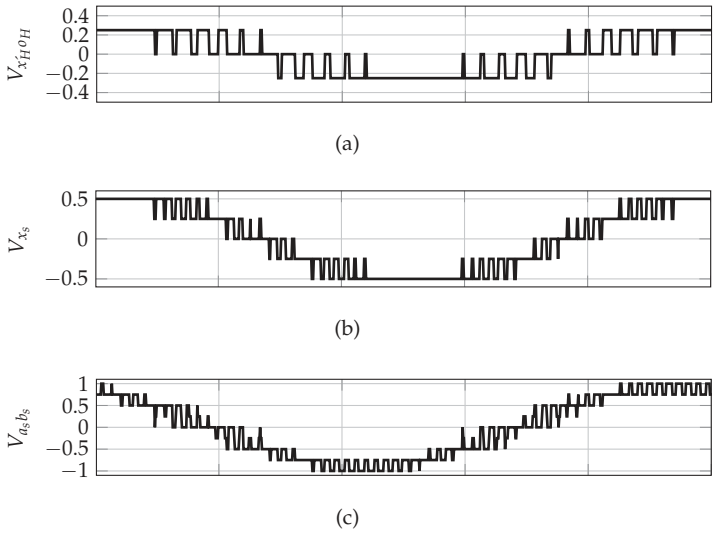


Fig. K.4: Switched voltages with the modulation index $M = 1$ and the switching frequency of 750 Hz, These voltages are normalized to $(V_{\mathrm{dc}_H} + V_{\mathrm{dc}_L})/2$. (a) Resultant switched output voltage of the high-side converter group, (b) Resultant switched output voltage, (c) Resultant line to line voltage $V_{a_s b_s}$.

derived in [15] and it is used to obtain the harmonic spectra of the resultant voltage of both the converter groups. The magnitude of the given harmonic components is the same in the output voltages of the parallel VSCs. However, the odd multiple of the switching frequency harmonic and their side band harmonics are phase shifted. As a result, the magnitude of these harmonic components is considerably reduced in the $V_{x'_H o_H}$ and the $V_{x'_L o_L}$, as shown in Fig. K.5(a).

The resultant switched output voltage V_{x_s} is the difference of the resultant switched output voltages of the HSCG and the LSCG and it is given as

$$V_{x_s} = V_{x'_H o_H} - V_{x'_L o_L} \tag{K.3}$$

The resultant switched output voltage of phase a (V_{a_s}) in a given switching period is shown in Fig. K.3(b) and the simulated waveform over a fundamental period is shown in Fig. K.4(b). The V_{a_s} has a multi-level voltage waveforms and the major harmonic component appears at the $4th$ carrier harmonic frequency component, as shown in Fig. K.5(b). The resultant switched output voltage has significant triplen baseband harmonic component. However, due to the three-wire system and isolated dc-links, these voltage components do not generate any triplen harmonic frequency current. The resultant line-to-line voltage, which determines the quality of the output current is also

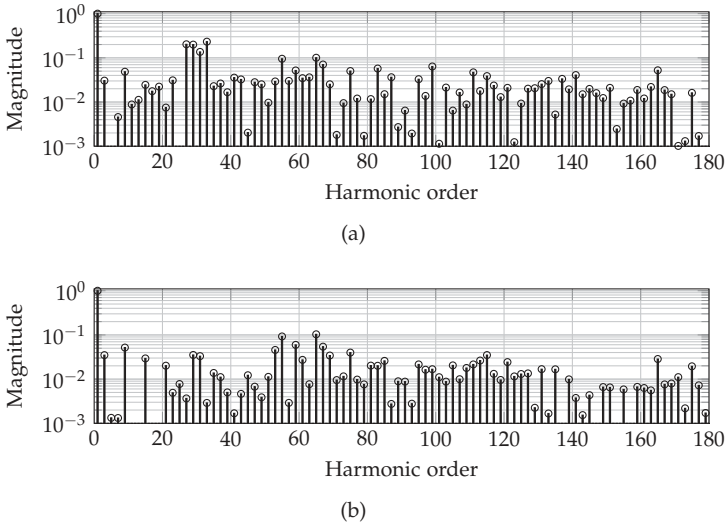


Fig. K.5: Theoretical harmonic spectrum of the switched voltages with the modulation index $M = 1$ and the switching frequency of 750 Hz. (a) Resultant switched output voltage of the high-side converter group, normalized to $V_{\mathrm{dc}_H}/2$, (b) Resultant switched output voltage, normalized to $\frac{V_{\mathrm{dc}_H}+V_{\mathrm{dc}_L}}{2}$.

shown in Fig. K.4(c).

3 Integrated Inductor

The switched output voltage exhibits five-level voltage waveform as discussed in section II. However, the circulating current flows between the parallel interleaved VSCs of the HSCG (as well as between the VSCs of the LSCG). The integrated inductor suppresses these circulating currents. Moreover, the integrated inductor also combines the functionalities of the converter-side inductor L_f of the LCL filter (which is required to achieve desired harmonic quality of the injected line current). The magnetic structure and the analysis of the integrated inductor is presented in this section.

3.1 Magnetic Structure of Integrated Inductor

The physical layout of the proposed integrated inductor is shown in Fig. K.6. The magnetic core is composed of three identical cells for each of the phases of the three-phase system. Each cell has two limbs and these limbs are magnetically coupled to each other using the top, the common, and the bottom yokes. This arrangement forms two windows in each of the cells. Top

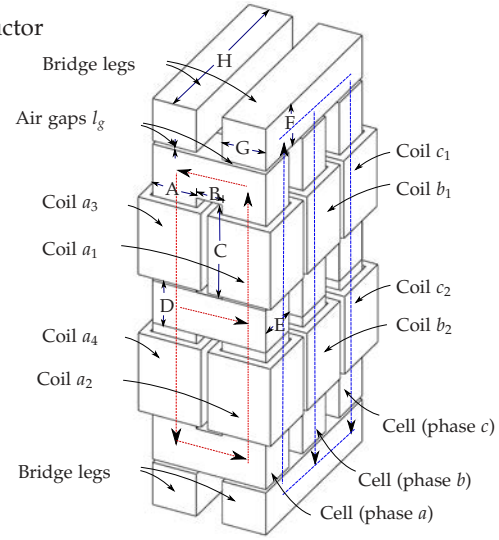


Fig. K.6: Physical layout of the proposed integrated inductor.

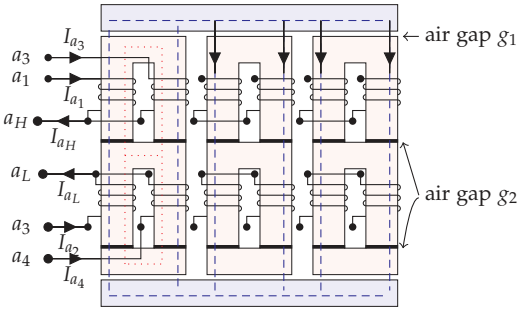


Fig. K.7: Magnetic core structure of the integrated inductor. The flux paths are illustrated when the coils of phase a are excited.

window provides the space to receive the coils corresponding to the HSCG (coils x_1 and x_3). Similarly, the coils of the LSCG are also placed around the limbs and accommodated in the bottom window area of the cell, as shown in Fig. K.6. The cells of all the three phases are magnetically coupled to each other using the bridge legs. Necessary air gaps (g_1 as shown in Fig. K.7) are introduced between the cells and the bridge legs in order provide energy storage to achieve desired value of the converter-side inductor L_f. Similarly small air gaps (g_2 as shown in Fig. K.7) are also provided in the cell structure to obtain the desired value of the circulating current inductance.

The starting terminals of both the coils of phase x, housed in the top window, are connected to the output terminals of phase x of the VSCs of the HSCG (x_1 and x_3), whereas the ending terminals are connected together

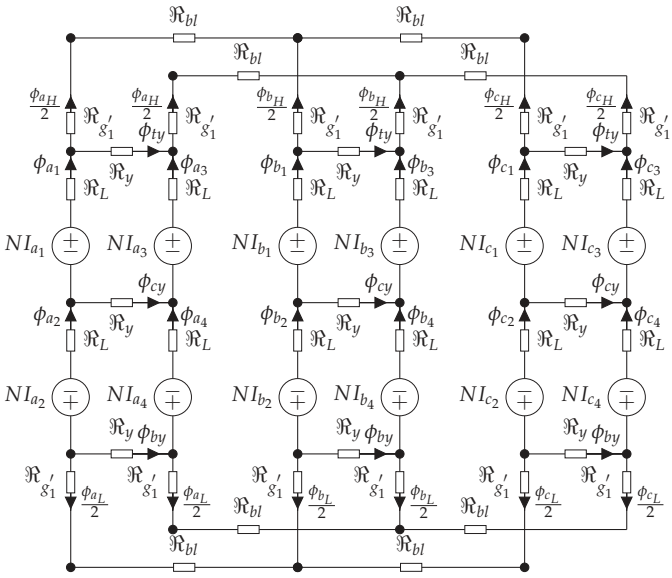


Fig. K.8: Simplified reluctance model of the integrated inductor.

to from the common connection point x_H, as shown in Fig. K.7. Similarly, the output terminals of the phase x of the VSCs of the LSCG (x_2 and x_4) are connected to the starting terminals of the coils housed in the bottom window and ending terminals are connected to the common point x_L. Both of the coils of the particular converter group are wound in the same direction. However, the direction of the coils of the HSCG cell is opposite to the direction of the coils of the LSCG cell, as shown in Fig. K.7.

3.2 Flux Linking with the Coils

The simplified reluctance model of the proposed inductor is shown in Fig. K.8. The permeability of the magnetic material is assumed to be constant and the effect of the leakage flux is neglected. The analysis is presented for one of the phases. By solving the reluctance model, the flux linking with each of the coils is given as

$$\phi_{x_1} = \frac{L_1}{N}(I_{x_1} + I_{x_3}) + \frac{L_2}{2N}(I_{x_1} - I_{x_3}) - \frac{L_3}{2N}(I_{x_2} - I_{x_4}) \tag{K.4}$$

$$\phi_{x_2} = -\frac{L_1}{N}(I_{x_2} + I_{x_4}) - \frac{L_2}{2N}(I_{x_2} - I_{x_4}) + \frac{L_3}{2N}(I_{x_1} - I_{x_3}) \tag{K.5}$$

$$\phi_{x_3} = \frac{L_1}{N}(I_{x_1} + I_{x_3}) - \frac{L_2}{2N}(I_{x_1} - I_{x_3}) + \frac{L_3}{2N}(I_{x_2} - I_{x_4}) \tag{K.6}$$

$$\phi_{x_4} = -\frac{L_1}{N}(I_{x_2} + I_{x_4}) + \frac{L_2}{2N}(I_{x_2} - I_{x_4}) - \frac{L_3}{2N}(I_{x_1} - I_{x_3}) \tag{K.7}$$

where

$$L_1 = \frac{N^2}{2\Re_L + 2\Re_{bl} + 2\Re_{g_1'}} \tag{K.8}$$

$$L_2 = \frac{4N^2(\Re_L + \Re_y)}{(2\Re_L + \Re_y)(2\Re_L + 3\Re_y)} \tag{K.9}$$

$$L_3 = \frac{2N^2\Re_y}{(2\Re_L + \Re_y)(2\Re_L + 3\Re_y)} \tag{K.10}$$

R_L is the sum of the reluctance of the limb and the reluctance of the air gap g_2 and it is given as $R_L = R_l + \Re_{g_2'}$.

The flux in the top and the bottom yokes of the cell are given as

$$\phi_{x_{ty}} = \frac{L_2}{2N}(I_{x_1} - I_{x_3}) - \frac{L_3}{2N}(I_{x_2} - I_{x_4}) \tag{K.11}$$

$$\phi_{x_{by}} = \frac{L_2}{2N}(I_{x_2} - I_{x_4}) - \frac{L_3}{2N}(I_{x_1} - I_{x_3}) \tag{K.12}$$

and flux in the common yoke is:

$$\phi_{x_{cy}} = \frac{N}{2\Re_l + 3\Re_y}(-I_{x_1} - I_{x_2} + I_{x_3} + I_{x_4}) \tag{K.13}$$

From the fluxes, the voltage across each of the coils can be obtained as

$$\boldsymbol{V} = \overrightarrow{\boldsymbol{V_p}} - \boldsymbol{V_v} = N\frac{d}{dt}\boldsymbol{\phi} \tag{K.14}$$

where $\boldsymbol{V}$, $\overrightarrow{\boldsymbol{V_p}}$ and $\boldsymbol{V_v}$ are the voltage vectors and they are represented as

$$\boldsymbol{V} = \begin{bmatrix} V_{x_1x_H} & V_{x_2x_L} & V_{x_3x_H} & V_{x_4x_L} \end{bmatrix}^T \tag{K.15}$$

$$\overrightarrow{\boldsymbol{V_p}} = \begin{bmatrix} V_{x_1o_H} & V_{x_2o_L} & V_{x_3o_H} & V_{x_4o_L} \end{bmatrix}^T \tag{K.16}$$

$$\boldsymbol{V_v} = \begin{bmatrix} V_{x_Ho_H} & V_{x_Lo_L} & V_{x_Ho_H} & V_{x_Lo_L} \end{bmatrix}^T \tag{K.17}$$

$$\boldsymbol{\phi} = \begin{bmatrix} \phi_{x_1} & \phi_{x_2} & \phi_{x_3} & \phi_{x_4} \end{bmatrix}^T \tag{K.18}$$

3.3 Line Filter Inductor and Circulating Current Inductor

The leg currents I_{x_k} has two components:

1. Resultant line current component (comprises of fundamental frequency component and small ripple current component).
2. Circulating current component.

Assuming equal current sharing between the parallel connected VSCs, the leg current vector can be decomposed as

$$\boldsymbol{I} = \boldsymbol{I_r} + \boldsymbol{I_c} \tag{K.19}$$

where

$$\boldsymbol{I} = \begin{bmatrix} I_{x_1} & I_{x_2} & I_{x_3} & I_{x_4} \end{bmatrix}^T \tag{K.20}$$

$$\boldsymbol{I_r} = \begin{bmatrix} \frac{I_{x_H}}{2} & \frac{I_{x_L}}{2} & \frac{I_{x_H}}{2} & \frac{I_{x_L}}{2} \end{bmatrix}^T \tag{K.21}$$

$$\boldsymbol{I_c} = \begin{bmatrix} I_{x_{H,c}} & I_{x_{L,c}} & -I_{x_{H,c}} & -I_{x_{L,c}} \end{bmatrix}^T \tag{K.22}$$

where the resultant current components are

$$I_{x_H} = I_{x_1} + I_{x_3}\,,\; I_{x_L} = I_{x_2} + I_{x_4} \tag{K.23}$$

and circulating current components are given as

$$I_{x_{H,c}} = \frac{I_{x_1} - I_{x_3}}{2} \text{ and } I_{x_{L,c}} = \frac{I_{x_2} - I_{x_4}}{2} \tag{K.24}$$

Using (K.14), the voltages across the coil x_1 and x_3 are obtained and substituting the leg currents in these equation yield

$$V_{x_1 o_H} - V_{x_H o_H} = L_1 \frac{dI_{x_H}}{dt} + L_2 \frac{dI_{x_{H,c}}}{dt} - L_3 \frac{dI_{x_{L,c}}}{dt} \tag{K.25}$$

$$V_{x_3 o_H} - V_{x_H o_H} = L_1 \frac{dI_{x_H}}{dt} - L_2 \frac{dI_{x_{H,c}}}{dt} + L_3 \frac{dI_{x_{L,c}}}{dt} \tag{K.26}$$

Averaging the voltages across the coils of the HSCG (K.25) and (K.26) yields

$$V_{x'_H o_H} - V_{x_H o_H} = L_1 \frac{dI_{x_H}}{dt} \tag{K.27}$$

where $V_{x'_H o_H}$ is the average value of the switched output voltages of the HSCG, as given in (K.1). Similarly, the voltages across the coils x_2 and x_4 are given as

$$V_{x_2 o_L} - V_{x_L o_L} = -L_1 \frac{dI_{x_L}}{dt} - L_2 \frac{dI_{x_{L,c}}}{dt} + L_3 \frac{dI_{x_{H,c}}}{dt} \tag{K.28}$$

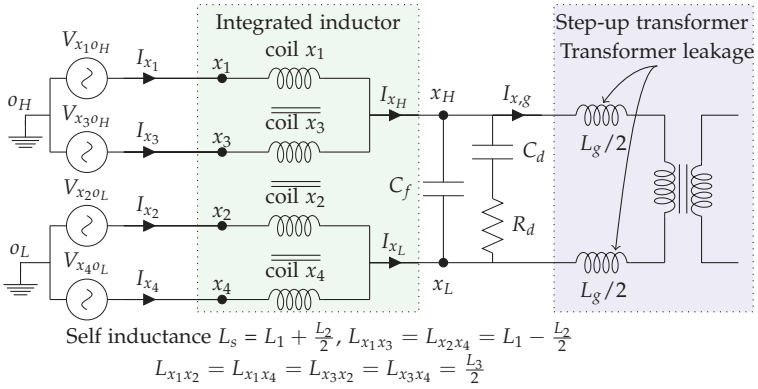


Fig. K.9: Electrical equivalent circuit of the integrated inductor. The integrated inductor offers inductance L_c to the circulating current and inductance L_f to the resultant line current. The LCL filter is used for the line current filtering, where L_f acts like a converter-side inductance of the LCL filter. The transformer leakage inductance L_g is used a grid-side inductance. The damping branch R_d/C_d is used in parallel with the capacitive branch C_f to provide damping.

$$V_{x_4o_L} - V_{x_Lo_L} = -L_1\frac{dI_{x_L}}{dt} + L_2\frac{dI_{x_{L,c}}}{dt} - L_3\frac{dI_{x_{H,c}}}{dt} \tag{K.29}$$

and averaging the voltage across the coils of the LSCG gives

$$V_{x'_Lo_L} - V_{x_Lo_L} = L_1\frac{dI_{x_L}}{dt} \tag{K.30}$$

where $V_{x'_Lo_L}$ is the average value of the switched output voltage of the LSCG, as given by (K.2).

The electrical equivalent circuit of the integrated inductor is derived and it is shown in Fig. K.9. For the open-end transformer topology, the resultant line current $I_x = I_{x_H} = -I_{x_L}$. Substituting this in (K.27) and (K.30) give

$$V_{x_s} - V_{x_{C,f}} = 2L_1\frac{dI_x}{dt} \tag{K.31}$$

where V_{x_s} is the resultant switched voltage and and $V_{x_{C,f}}$ is the voltage across the line filter capacitor C_f and given as

$$V_{x_s} = \left(\frac{V_{x_1o_H} + V_{x_3o_H}}{2}\right) - \left(\frac{V_{x_2o_L} + V_{x_4o_L}}{2}\right) \tag{K.32}$$

and

$$V_{x_{C,f}} = V_{x_Ho_H} - V_{x_Lo_L} \tag{K.33}$$

Since two separate dc-links are employed, the common mode circulating current between the HSCG and the LSCG is zero and I_{x_H} and I_{x_L} only have

the differential current components. Therefore, using (K.31), the line filter inductance L_f is given as

$$\begin{aligned} L_f &= \frac{2N^2}{2\Re_l + 2\Re_{bl} + 2\Re_{g_1'} + 2\Re_{g_2'}} \\ &= \mu_0 N^2 \left(\frac{A_{g_1'}}{l_{g_1}} + \frac{A_{g_2'}}{l_{g_2}}\right) \end{aligned} \tag{K.34}$$

where $A_{g_1'}$ and $A_{g_2'}$ are the effective cross-section area of an air gaps g_1 and g_2, respectively and it can be obtained by evaluating the cross-section area of the air gap after adding length of the air gap to each dimension in the cross-section.

For the parallel interleaved VSCs, the switched output voltages of the parallel interleaved legs are phase shifted and the difference of these voltages drives the circulating current. Using (K.25) and (K.26), the difference of the switched output voltages of the parallel VSCs of the HSCG are given as

$$V_{x_1 o_H} - V_{x_3 o_H} = 2L_2 \frac{dI_{x_{H,c}}}{dt} - 2L_3 \frac{dI_{x_{L,c}}}{dt} \tag{K.35}$$

similarly, subtracting (K.29) from (K.28) yields

$$V_{x_2 o_L} - V_{x_4 o_L} = 2L_3 \frac{dI_{x_{H,c}}}{dt} - 2L_2 \frac{dI_{x_{L,c}}}{dt} \tag{K.36}$$

Using (K.35) and (K.36), the circulating currents are described as

$$\begin{bmatrix} V_{x_1 o_H} - V_{x_3 o_H} \\ V_{x_2 o_L} - V_{x_4 o_L} \end{bmatrix} = \boldsymbol{L_c} \frac{d}{dt} \begin{bmatrix} I_{x_{H,c}} \\ I_{x_{L,c}} \end{bmatrix} \tag{K.37}$$

where $\boldsymbol{L_c}$ is the circulating current inductance matrix and given as

$$\boldsymbol{L_c} = \begin{bmatrix} 2L_2 & -2L_3 \\ -2L_3 & 2L_2 \end{bmatrix} \tag{K.38}$$

The value of L_c should be should be chosen to limit the circulating current to some acceptable limits.

4 Design Methodology

The design equations for the integrated inductor are derived in this section. The design methodology is also illustrated by carrying out the design of the integrated inductor for 12 MVA, 3.3 kV Wind Energy Conversion System (WECS).

4.1 Design Equations

The flux linking with each of the coils can be decomposed into three categories:

1. Fundamental frequency flux component.
2. Ripple component of the flux with dominant component at $4th$ carrier frequency harmonic.
3. Circulating flux with dominant component at $1st$ carrier frequency harmonic.

The ripple component of the flux is very small compared to the fundamental frequency component and the circulating flux component. Therefore, the effect of the ripple component is neglected in the design.

4.1.1 Fundamental Frequency Flux Component $\phi_{x_{k,f}}$

Using (K.4), the fundamental component of the flux linking with the coil is given as

$$\phi_{a_{k,f}}(t) = \frac{L_f S}{3\sqrt{2}NV_{ph}} \cos(\psi - \theta) \tag{K.39}$$

$\phi_{a_{k,f}}$ attains its maximum value for the space vector angle $\psi = \theta$.

4.1.2 Circulating Flux Component $\phi_{x_{k,c}}$

From (K.4) and (K.6), the circulating flux components that links with the coils of the HSCG are obtained as

$$\phi_{a_{1,c}}(t) = -\phi_{a_{3,c}}(t) = \frac{L_2}{N} I_{a_{H,c}} - \frac{L_3}{N} I_{a_{L,c}} \tag{K.40}$$

By obtaining the values of the $I_{a_{H,c}}$ and $I_{a_{L,c}}$ form (K.37) and substituting in (K.40) yields

$$\phi_{a_{1,c}}(t) = -\phi_{a_{3,c}}(t) = \frac{\lambda_H(t)}{2N} \tag{K.41}$$

where

$$\lambda_H(t) = \int (V_{a_1 o_H} - V_{a_3 o_H}) dt \tag{K.42}$$

Similarly, the circulating flux component that links with the coils of the LSCG are obtained as

$$\phi_{a_{2,c}}(t) = \frac{1}{2N} \int (V_{a_2 o_L} - V_{a_4 o_L}) dt = \frac{\lambda_L(t)}{2N} \tag{K.43}$$

The analysis of the variation of the $\lambda_H(t)$ with the modulation index M and the space vector angle ψ is presented in [24, 25]. The peak value of the $\lambda_H(t)$

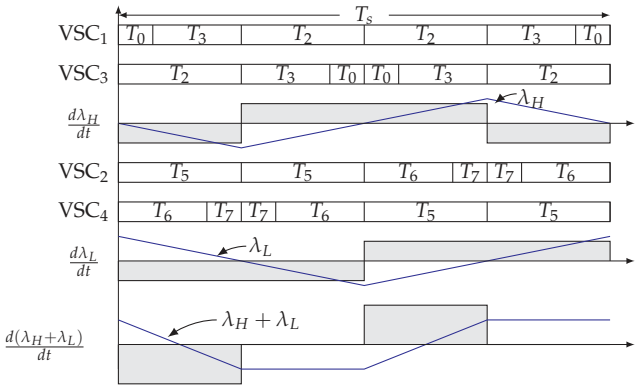


Fig. K.10: The switching sequences and switched output voltage difference of the HSCG and the LSCG for phase a for $M = 1$ and $\psi_H = 84.7^\circ$.

is different in every sampling interval due to the change in the dwell times of the voltage vector. Let the maximum value out of these peak values is $\lambda_{H_{max}}$ and it is given as

$$\lambda_{H_{max}} = \begin{cases} \frac{\sqrt{3}M}{4} V_{\mathrm{dc}_H} T_s, & 0 \leq M < 1/\sqrt{3} \\ \frac{1}{4} V_{\mathrm{dc}_H} T_s, & 1/\sqrt{3} \leq M < 2/\sqrt{3} \end{cases} \tag{K.44}$$

For the grid connected applications, the modulation index M varies in a small range close to one. Therefore, the maximum value of the circulating flux component is given as

$$\phi_{a_{1,c_{max}}} = \frac{V_{\mathrm{dc}_H} T_s}{8N} \tag{K.45}$$

The $\phi_{a_{1,c}}(t)$ achieves $\phi_{a_{1,c_{max}}}$ value at the space vector angle ψ_{max}, as shown in Fig. K.10 and ψ_{max} is given as

$$\psi_{max} = 120^\circ - \arcsin(\frac{1}{\sqrt{3}M}) \tag{K.46}$$

4.1.3 Maximum Flux Value in the Bridge Legs

The common component of the fluxes that links with coils x_1 and x_3 pass through the bridge legs and the maximum value of this flux component is given as

$$\phi_{bl_{max}} = \frac{L_f S}{3\sqrt{2} N V_{ph}} \tag{K.47}$$

4.1.4 Maximum Flux Value in the Top and the Bottom Yokes

The circulating component of the flux is confined in the cell. Therefore, the maximum value of the flux in the top and the bottom yokes $\phi_{y_{max}}$ is

$$\phi_{y_{max}} = \frac{V_{\mathrm{dc}_H} T_s}{8N} \tag{K.48}$$

4.1.5 Maximum Flux Value in the Common Yoke

Using (K.13), the flux in the common yoke is obtained as

$$\phi_{cy}(t) = \frac{-2N}{2\Re_l + 3\Re_y}(I_{a_{H,c}} + I_{a_{L,c}}) \tag{K.49}$$

Substituting the values of $I_{a_{H,c}}$ and $I_{a_{L,c}}$ in (K.49) yields

$$\phi_{cy}(t) = \frac{1}{2N}[\lambda_H(t) + \lambda_L(t)] \tag{K.50}$$

The difference of the switched output voltages of the HSCG and the LSCG are shown in Fig. K.10. The voltage level of the $d(\lambda_H(t) + \lambda_L(t))/dt$ is $V_{\mathrm{dc}_H} + V_{\mathrm{dc}_L}$, which is twice as that of the $d\lambda_H(t)/dt$ and $d\lambda_L(t)/dt$. However, the duration for which this voltage appears is half than that of the $d\lambda_H(t)/dt$ and $d\lambda_L(t)/dt$. The maximum value of the $\phi_{cy}(t)$ is given as

$$\phi_{cy_{max}} = \frac{(V_{\mathrm{dc}_H} + V_{\mathrm{dc}_L})T_s}{16N} \tag{K.51}$$

Assuming $V_{\mathrm{dc}_H} = V_{\mathrm{dc}_L}$, the value of the $\phi_{cy_{max}} = \phi_{y_{max}}$. Therefore, despite the common yoke carrying sum of the circulating fluxes of the HSCG and the LSCG, the required cross-section area of the common yoke is the same as that of the top and the bottom yokes. This also leads to the volume reduction of the integrated inductor.

4.1.6 Maximum Flux Value in the Limb

The flux in the limb is given as

$$\phi_{a_l}(t) = \phi_{a_{1,f}}(t) + \phi_{a_{1,c}}(t) \tag{K.52}$$

As it is evident from (K.39), the space voltage vector angle at which the $\phi_{a_{1,f}}$ attains the maximum value depends on the displacement power factor angle. Whereas, the space vector angle at which the $\phi_{a_{1,c}}$ attains the maximum value depends on the modulation index M, as given in (K.46). Therefore, in order to obtain the worst case value of the flux $\phi_{l_{max}}$, the operating range of the θ and M should be known. For the WECS application, the converter should be

Table K.2: Values of the flux in the limb for different voltage space vector angles

Value	Conditions
$N\phi_{a_l}(t) \mid_{\psi=0^\circ} = \frac{L_f S}{3\sqrt{2}V_{ph}}$	$\theta = 0^\circ$
$N\phi_{a_l}(t) \mid_{\psi=30^\circ} = \frac{0.978 L_f S}{3\sqrt{2}V_{ph}} + \frac{0.354 V_{\mathrm{dc}_H} T_s}{8}$	$\theta = 18^\circ$, $M = 0.95$
$N\phi_{a_l}(t) \mid_{\psi=82.5^\circ} = \frac{0.429 L_f S}{3\sqrt{2}V_{ph}} + \frac{V_{\mathrm{dc}_H} T_s}{8}$	$\theta = 18^\circ$, $M = 0.95$

able to supply the current with the displacement power factor within a range of 0.95 lagging to 0.95 leading [13]. Therefore, the displacement power factor angle varies from -18° to 18° ($-18^\circ \leq \theta \leq 18^\circ$). The modulation index in grid connected application varies in a small range in vicinity to one and therefore M is assumed to be vary between 0.95 to 1.1 ($0.95 \leq M \leq 1.1$). The flux linkage in the limb for different space voltage vector angels for specific operating conditions are given in Table K.2. The maximum value of the flux in the limb $\phi_{l_{max}}$ is maximum out of the flux values given in Table K.2.

4.2 Design Example

The integrated inductor is designed for the 13.2 MVA, 3.3 kV WECS. A small scale prototype has been also designed and built. The system parameters of both the systems are specified in Table K.3. The parameters of the line filter are obtained using the procedure outlined in [15, 26]. The functionalities of the converter-side inductor L_f and the circulating current inductor are integrated in the designed inductor.

The line filter inductor for the high power systems generally requires large air gap and it is often realized by having several discrete air gaps. However, in the case of the proposed integrated inductor, the length of the air gap in the cell structure (l_{g2}) is limited by the required value of the circulating current inductance as given in (K.9), (K.10), and (K.38). The design example of the high power system is considered to demonstrate how to address this issue and two possible approaches are presented.

4.2.1 Integrated Inductor Using Discrete Bridge Blocks

In this approach, several discrete core blocks with an air gap in between them are inserted between the cell and the bridge legs to realized several discrete air gaps. The first iteration of the design parameters are obtained using the steps illustrated below and then the Finite Element Analysis (FEA) is carried out to fine tune the design parameters.

Table K.3: System Parameters for Simulation and Experimental Study

Parameters	Simulation study	Experiment
Power	13.2 MVA (12 MW)	11 kVA (10 kW)
Switching frequency	750 Hz	750 Hz
AC voltage (line-to-line)	3300 V	400 V
$V_{\mathrm{dc}_H} = V_{\mathrm{dc}_L}$	2900 V	350 V
Base impedance	0.825 Ω	14.54 Ω
Base inductance	2.6 mH	46.3 mH
Base capacitance	3.9 mF	0.218 mF
L_f	370 μH (0.14 pu)	6.1 mH (0.135 pu)
L_g	290 μH (0.11 pu)	5 mH (0.11 pu)
$C_f = C_d$	193 μF (0.05 pu)	11 μF (0.05 pu)
L_c	2.2 mH (0.85 pu)	39 mH (0.85 pu)

The maximum value of the flux density in the limb is obtained as

$$B_{l_{max}} = \frac{1}{NA_{c_l}}\Big(\frac{0.429L_fS}{3\sqrt{2}V_{ph}} + \frac{V_{\mathrm{dc}_H}T_s}{8}\Big) \tag{K.53}$$

Each of the windows should be able to carry two coils with half of the rated current flowing through it. Therefore,

$$N = \frac{K_wA_wJ}{I_r} \tag{K.54}$$

Using (K.53) and (K.54), the product of the cross section area of the limb and the window area is obtained as

$$A_{c_l}A_w = \frac{I_r}{B_{m_l}JK_w}\Big(\frac{0.429L_fS}{3\sqrt{2}V_{ph}} + \frac{V_{\mathrm{dc}_H}T_s}{8}\Big) \tag{K.55}$$

Suitable core to match the area product requirement should be selected. Once the value of A_{c_l} is know, the number of turns in each coil is obtained using (K.53) and it is given as

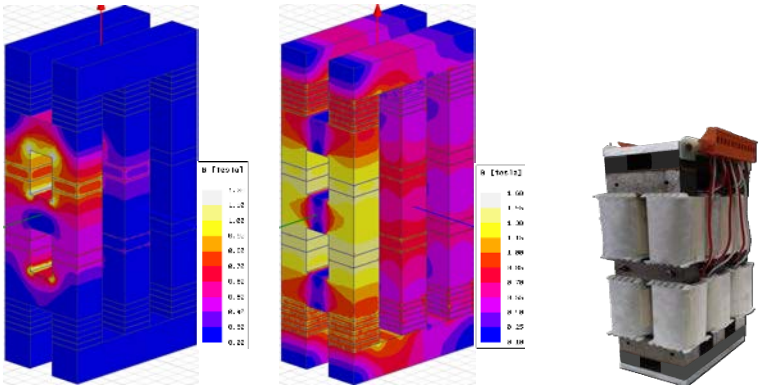
$$N = \frac{1}{B_{m_l}A_{c_l}}\Big(\frac{0.429L_fS}{3\sqrt{2}V_{ph}} + \frac{V_{\mathrm{dc}_H}T_s}{8}\Big) \tag{K.56}$$

where $A_{c_l} = K_s \times A \times E$ for the geometrical parameters shown in Fig. K.6. Only the circulating flux component flows through the yokes and the cross-section area of the yokes can be obtained as

$$A_{c_y} = \frac{V_{\mathrm{dc}_H}T_s}{8NB_{m_y}} \tag{K.57}$$

Table K.4: Parameters of the designed integrated inductor. See Fig. K.6 for definitions. All parameters are given in mm.

System	A,B,E,F,G	C	D	H	N	A_{cu} (mm^2)
12 MW	205	300	180	1025	14	400
10 kW	25	75	25	25	104	2.62



(a) (b) (c)

Fig. K.11: The flux density distribution in the magnetic core. (a) Phase shifted components of switched output voltage of the carrier frequency harmonics are applied across the coils (space vector angle is 240°. Therefore, phase c is clamped to the dc bus, so the coils of the cells of only phase a and phase b are excited), (b) Coils are excited with the common component of the current (I_{a_k} = 1600 A, $I_{b_k} = I_{c_k}$ =-800A), (c) Photograph of the implemented inductor for a 11 kVA prototype.

The cross section area of the bridge leg can be obtained from the (K.47) and it is given as

$$A_{c_{bl}} = \frac{L_f S}{3\sqrt{2} N B_{m_{bl}} V_{ph}} \tag{K.58}$$

and the $A_{c_{bl}} = K_s \times G \times F$. The inductance offer to the circulating current is given as

$$L_c \approx 2L_2 = \frac{2N^2}{\Re_{g_2'}} = \frac{2\mu_0 N^2 A_{g_2'}}{l_{g_2}} \tag{K.59}$$

Using (K.59), the value of the l_{g_2} is obtained. Once l_{g_2} is know, the value of l_{g_1} is obtained using (K.34).

The design parameters obtained using the outlined procedure is fine tuned using the FEA and they are specified in Table K.4. Two air gaps having 3 mm length each is inserted in the cell structure and six discrete air gaps

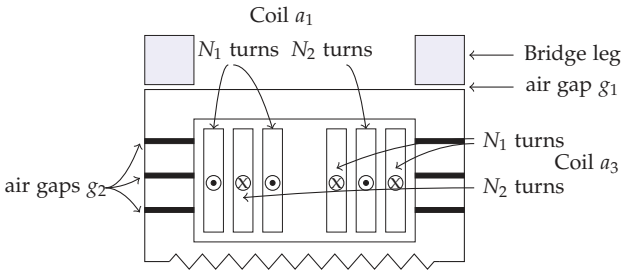


Fig. K.12: Integrated inductor with split winding arrangement. Each coil is divided into two groups.

of 2.6 mm length have been inserted between cell and the bridge legs. The window utilization factor K_w is taken to be 0.3 and the current density is considered to be J =3 A/mm^2. The flux density distribution is shown in Fig. K.11(a) and Fig. K.11(b). The inductance values are obtained using the FEA and the L_f and L_c are calculated to be 395 uH and 2.2 mH, respectively.

4.2.2 Integrated Inductor Using Split Windings

In above mentioned approach, several discrete air gaps are realized using the bridge blocks as shown in Fig. K.11(a) and Fig. K.11(b). The requirement of the additional bridge blocks can be avoided by introducing discrete air gaps in the cell structure (which increases the value of the l_{g_2}). However, this leads to the increase in the reluctance of the limb $\Re_L$, which in turn result into the low value of the circulating current inductance L_c. For the given l_{g_2}, high value of the L_c can be achieved by increasing the number of turns. However, increasing the number of turns also affects the value of the L_f and demands larger value of the l_{g_1}, as it is evident from (K.34). The values of both the L_f and L_c depends on the number of turns and may sometime cause design bottleneck. This can be addressed by using the split coils, as shown in Fig. K.12.

The coil arrangement of the HSCG of the phase a is shown in Fig. K.12 for the illustration. The number of turns in coil a_1 is split in two parts. The first part with N_1 number of the turns is wound around the limb a_1 with the coil direction shown in Fig. K.12, whereas other part with N_2 turns wound around limb a_3 in the opposite direction of that of the first part. The same arrangement has been done for the coil a_3 as well. In this arrangement, the common component of the flux produced by N_1 turns of the coil a_1 is in opposite to the common component of the flux produce by the N_2 turns of the coil a_3. On the other hand, the circulating flux components produced by the N_1 turns of the coil a_1 and N_2 turns of the coil a_3 are in the same

Table K.5: Design Equations for integrated inductor with split windings

Parameter	Value
$\phi_{a_{k,fmax}} = \phi_{bl_{max}}$	$\frac{L_f S}{3\sqrt{2}(N_1-N_2)V_{ph}}$
$\phi_{a_{1,cmax}} = \phi_{y_{max}}$	$\frac{V_{\mathrm{dc}_H} T_s}{8(N_1+N_2)}$
$\phi_{cy_{max}}$	$\frac{(V_{\mathrm{dc}_H}+V_{\mathrm{dc}_L})T_s}{16(N_1+N_2)}$
L_f	$\mu_0(N_1-N_2)^2(\frac{A'_{g_1}}{l_{g_1}}+\frac{A'_{g_2}}{l_{g_2}})$
L_c	$\frac{2}{l_{g_2}}\mu_0(N_1+N_2)^2 A'_{g_2}$

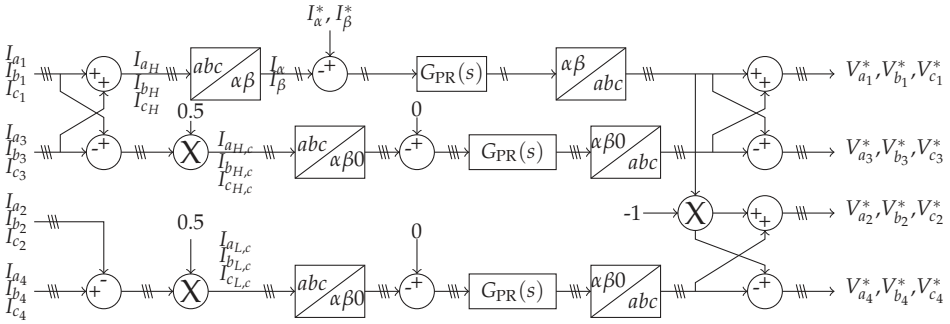


Fig. K.13: Control scheme. The active and reactive currents are controlled by controlling the resultant output current of the high-side converter group. As $I_{a_H} = -I_{a_L}$, the resultant current of the LSCG is also indirectly controlled. The circulating current between the parallel VSCs in both the converter groups is also controlled.

direction. As result, the desired value of the L_f and L_c can be obtained by choosing proper values of the N_1 and N_2. The relevant design equations are given in Table K.5.

5 Control Schemes and Performance Evaluation

5.1 Control Scheme

In this study, it is assumed that the dc-link voltages of both the HSCG and the LSCG are maintained to be equal. Therefore, the control scheme is designed to inject the desired active and reactive current, as shown in Fig. K.13. The parameter mismatch between the parallel converter may cause fundamental frequency component to be present in the circulating current, which may cause the saturation of the integrated inductor. Therefore, the control scheme

ia also designed to maintain equal current sharing between the parallel VSCs so that the fundamental frequency component in the circulating current is ensured to be zero.

5.1.1 Active and Reactive Current Control

The active and the reactive currents are controlled by controlling the resultant output current of the HSCG I_{a_H}. As $I_{a_H} = -I_{a_L}$, the resultant current of the LSCG is also indirectly controlled. The control variables are transformed into a $\alpha\beta$ frame and controlled using the Proportional-Resonant (PR) controller. The PR controller is represented as $G_{\mathrm{PR}}(s)$ and it is given as

$$G_{\mathrm{PR}}(s) = K_p + k_i \frac{s}{s^2 + \omega_0^2} \tag{K.60}$$

where ω_0 is the angular speed of the grid voltage and k_{p_c} and k_{i_c} are the proportional and the integral gain of the PR controller. The control and PWM delay is represented by the first order approximation of the $G_d(s)$, where $G_d(s) = e^{-\frac{sT_S}{4}}$. From Fig. K.9 and using (K.31), (K.32), and (K.33), the filter transfer $G_f(s) = I_x(s)/V_x(s)$ is derived as

$$G_f(s) = \frac{1}{sL_f} \frac{s^3 + s^2 \frac{C_f + C_d}{C_f C_d R_d} + s \frac{1}{L_g C_f} + \frac{1}{L_g C_f C_d R_d}}{s^3 + s^2 \frac{C_f + C_d}{C_f C_d R_d} + s \frac{L_f + L_g}{L_f L_g C_f} + \frac{L_f + L_g}{L_f L_g C_f C_d R_d}} \tag{K.61}$$

The parameters of the designed filter are given in Table K.3. The continuous transfer functions are discretized and the current controller parameters are calculated in the discrete time domain using the root locus theory. The parameters of the PR controller of the active and reactive current controller are $K_p = 3.1$ and $K_i = 605$.

5.1.2 Circulating Current Control

The circulating current between the parallel VSCs in both the HSCG and the LSCG is controlled by modifying the reference voltage generated by the active and reactive current control loop. The circulating current is obtained from the leg currents. As the leg currents are sampled at the top and the bottom of the carrier signals, the switching frequency ripple component is filtered out. The fundamental frequency component of the circulating current is then controlled to be zero using the Proportional-Resonant (PR) controller, represented by G_{PR_c} in Fig. K.13. As the circulating currents also have a zero sequence component, it is also controlled (in addition to the $\alpha\beta$ component of the circulating current) using the PR controller. The model describing the circulating current behavior is given by (K.37) and it is used to derive the controller gains, which are obtained as $k_{p_c} = 8.22$ and $k_{i_c} = 4305$.

Table K.6: Semiconductor losses at different loading conditions

Load	0.25 pu	0.5 pu	0.75 pu	1 pu
Conduction losses (kW)	5.48	13.43	23.45	35.65
Switching losses (kW)	20.6	39.0	52.67	70.0
Total (kW)	26.08	52.43	76.12	105.65

5.2 Loss Evaluation

The semiconductor losses and the losses in the integrated inductor are evaluated in this section.

5.2.1 Semiconductor Losses

For the system specifications considered in this study, the VSCs can be realized using the 4.5 kV, 1200 A Insulated Gate Bipolar Transistor (IGBT). The use of the IGBT FZ1200R45KL3-B5 from the Infineon Technologies is considered. The losses are calculated using PLECS, where the required data are obtained from the device data sheet. The semiconductor losses at various loading conditions are given in Table K.6.

5.2.2 Inductor Losses

The core and the copper losses of the integrated inductor are calculated for the high power system, with the design parameters given in Table K.4.

The Improved Generalized Steinmetz Equation (IGSE) [27, 28] is used to calculate the core losses. The core losses per unit volume is given as

$$P_{fe,v} = \frac{1}{T}\int_0^T k_i \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{K.62}$$

where α, β and k_i are the constants determined by the material characteristics. The time domain simulation of the integrated inductor is carried out using the magnetic toolbox in PLECS, which uses permeance-capacitance analogy to model the inductor. The simulated flux density waveforms in the various parts of the magnetic structure of the integrated inductor are shown in Fig. K.14. The flux in the yoke has a major harmonic component at the carrier harmonic frequency, whereas the flux in the bridge legs is mainly comprised of the fundamental frequency component, as shown in Fig. K.14(d). The flux in the limb is the addition of the common flux component and circulating flux component, as shown in Fig. K.14(a). The maximum value of the flux in the common yoke is the same as that of the top and the bottom yoke as shown in Fig. K.14(b), which is in agreement with the analysis presented in

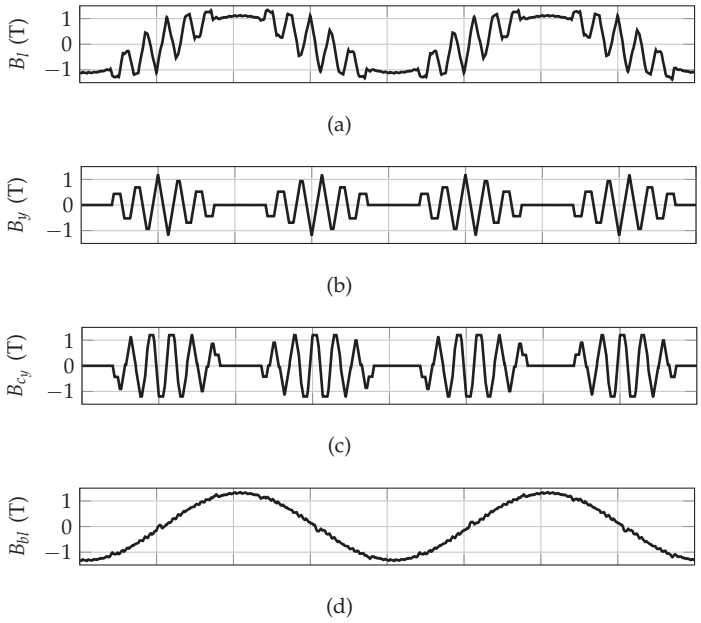


Fig. K.14: Simulation results at rated operating conditions. (a) Flux density in the limb of the cell of the integrated inductor, (b) Flux density in yoke of the cell, (c) Flux density in the common yoke, (d) Flux density in the bridge leg.

section IV. Core losses due to these components are evaluated separately.

The copper loss is evaluated by considering the ac resistance of the winding, which takes into account the skin and proximity effects [29]. The total winding losses are given as [30]

$$P_{cu} = R_{dc} \sum_{h=1}^{\infty} k_{p_h} I_h^2 \tag{K.63}$$

where

$$\begin{aligned} k_{p_h} = &\sqrt{h}\Delta \Big[\frac{\sinh(2\sqrt{h}\Delta) + \sin(2\sqrt{h}\Delta)}{\cosh(2\sqrt{h}\Delta) - \cos(2\sqrt{h}\Delta)} \\ &+ \frac{2}{3}(m^2 - 1) \frac{\sinh(\sqrt{h}\Delta) - \sin(\sqrt{h}\Delta)}{\cosh(\sqrt{h}\Delta) + \cos(\sqrt{h}\Delta)} \Big] \end{aligned} \tag{K.64}$$

and $\Delta = T_c/\delta$.

The core and the copper losses of the integrated inductor at different loading conditions are calculated and given in Table K.7.

Table K.7: Core and copper losses of the integrated inductor at different loading conditions

Load	0.25 pu	0.5 pu	0.75 pu	1 pu
Copper losses (kW)	1.03	2.85	5.89	10.17
Core losses (kW)	5.1	5.52	5.88	6.26
Total (kW)	6.13	8.37	11.77	16.43

Table K.8: Design parameters of the coupled inductor and harmonic filter inductor in the separate inductor case.

Parameter	Turns	Coil current	Core cross-sectional area
Coupled inductor	14	1154 A	32.6×10^{-3} m^2
Line inductor	9	2308 A	47.43×10^{-3} m^2

Table K.9: Volumetric comparison in ltr.

Material	Amorphous	Laminated steel	Copper
Separate inductor	336	373	105
Integrated inductor	351	172	62
% change	+ 4.4%	- 53.8%	- 40.9%

5.3 Comparative Evaluation

The advantages offered by the integrated inductor is demonstrated by comparing its volume and losses with that of the separate inductor case. The values of the inductance, the flux density, the current density, and the window utilization factor are assumed to be the same in both the cases. Typically the Coupled Inductor (CI) is used to suppress the circulating current between the parallel VSCs and it is considered for circulating current suppression between the parallel VSCs in both the converter groups for the separate inductor case. Each of the converter groups are assumed to have separate line filter inductor with the value $L_f/2$ and with the coil current of $I_x = I_{x_H} = -I_{x_L}$. Two limb magnetic structure is considered for the CI, whereas the line filter inductor is assumed to be realized using the three-phase three-limb inductor. The design parameters of the CIs and the line filter inductors, considered for the separate inductor case, are given in Table K.8.

The line filter inductor is assumed to be made from the grain oriented laminated steel with lamination thickness of 0.35 mm, whereas the use of the amorphous alloys 2605SA1 is considered for the CIs. The volume of the various materials is compared and given in Table K.9. The integrated inductor leads to the 26.2% reduction in the volume of the magnetic material and

Table K.10: Total core and copper losses for the separate inductors case at different loading conditions

Load	0.25 pu	0.5 pu	0.75 pu	1 pu
Copper losses (kW)	1.55	4.64	9.81	17.04
Core losses (kW)	6.27	7.08	8.12	8.93
Total (kW)	7.82	11.72	17.93	25.97

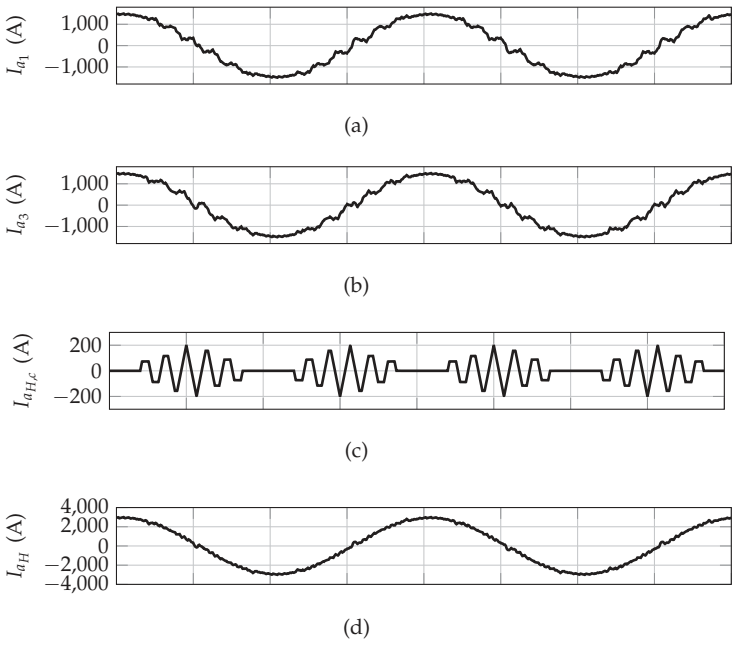


Fig. K.15: Simulation current waveforms. (a) Output current of VSC1 I_{a_1}, (b) Output current of VSC3 I_{a_3}, (c) Circulating current $I_{a_{H,c}}$, (d) Output current of high-side converter group I_{a_H}.

40.9% reduction in the volume of the copper.

The core and the copper losses in the separate inductor case are evaluated and given in Table K.10. As evident from Table K.7 and Table K.10, the losses in the case of the integrated inductor are less compared to the separate inductor case over the whole operating range. This not only increase the system efficiency but also reduces the cooling requirement.

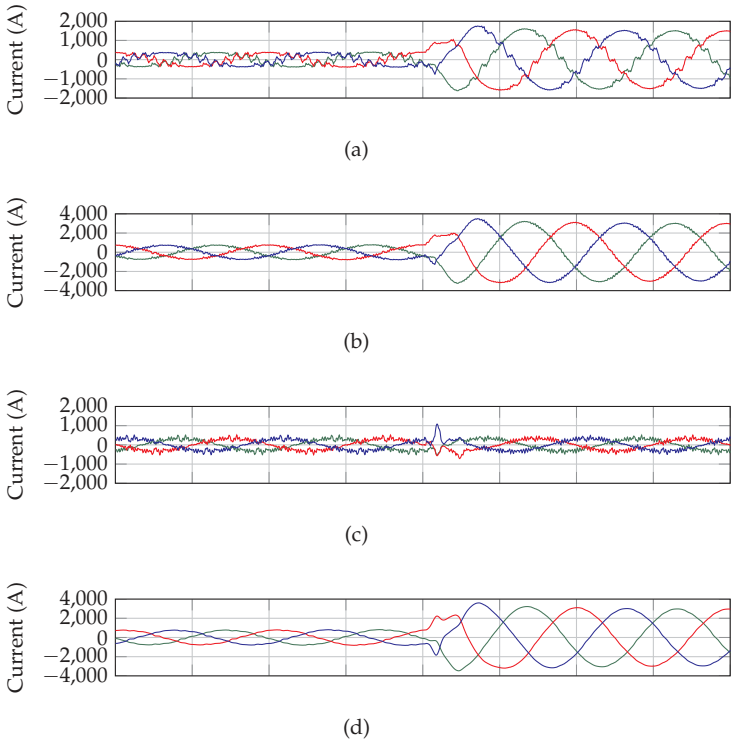


Fig. K.16: Simulated waveforms for a step response of the current control when the reference current was changed from 0.25 pu to 1 pu. (a) Leg currents of all phases of VSC1 (I_{a_1}, I_{b_1}, I_{c_1}), (b) Resultant current of the high-side converter group (I_{a_H}, I_{b_H}, I_{c_H}), (c) Current through the shunt capacitive branch of the *LCL* filter, (d) Injected grid current ($I_{a,g}$, $I_{b,g}$, $I_{c,g}$).

6 Simulation and Experimental Results

Time-domain simulations are carried out using PLECS. Fig. K.15 shows the simulated waveforms of the phase *a* at the rated load operation. The circulating current between the VSCs of the HSCG is shown in Fig. K.15(c), which is within the defined limit. The current waveforms of only the HSCG are shown as the waveforms of the LSCG are also identical ($I_{x_H} = -I_{x_L}$). The waveform of the output current of the HSCG has very small ripple component as shown in Fig. K.15(d), which proves the effectiveness of the integrated inductor.

Figs. K.16 shows the simulated current waveforms for a step response of the current control when the reference current was changed from 0.25 pu to 1 pu. The corresponding flux density waveforms for the phase *a* are also shown in Fig. K.17. As it is evident for the Fig. K.17(b), the dc component is avoided in the circulating flux due to the simultaneous sampling of the

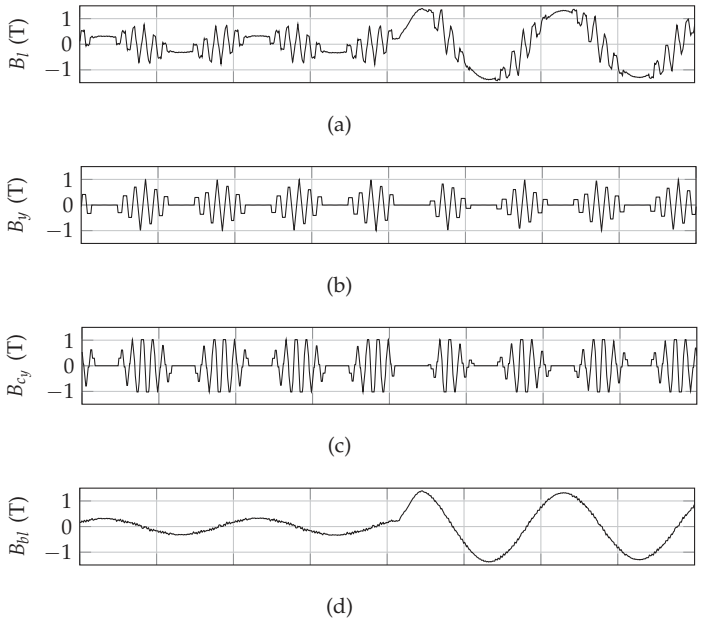


Fig. K.17: Simulated flux density waveforms for a step response when the reference current was changed from 0.25 pu to 1 pu. (a) Flux density in the limb of the cell of the integrated inductor, (b) Flux density in yoke of the cell, (c) Flux density in the common yoke, (d) Flux density in the bridge leg.

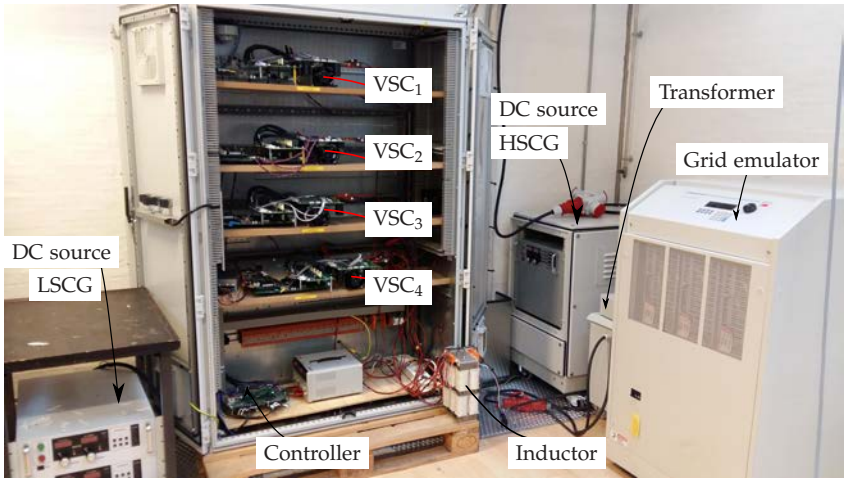


Fig. K.18: Experimental setup.

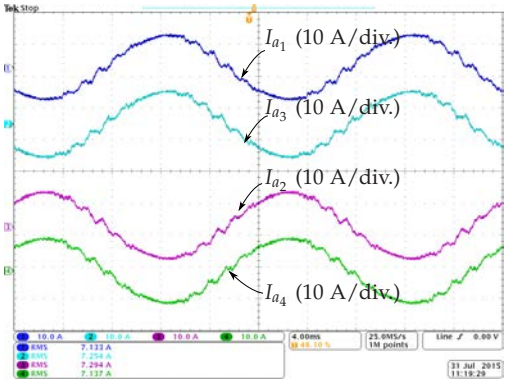


Fig. K.19: Output current of phase a of the individual VSCs. (a) Ch1: I_{a_1}, Ch2: I_{a_3}, Ch3: I_{a_2}, Ch4: I_{a_4}.

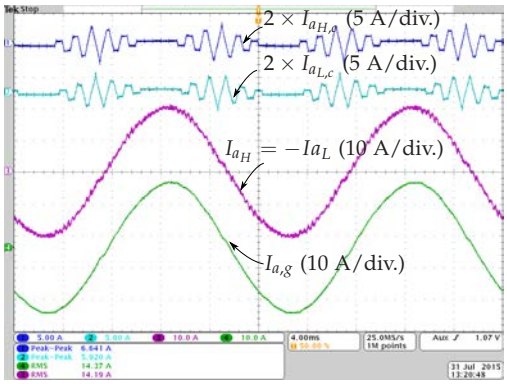


Fig. K.20: Experimental waveforms of the phase a. (a) Ch1: Circulating current between the VSCs of the high-side converter group ($2 \times I_{a_{H,c}}$), Ch2: Circulating current between the VSCs of the low-side converter group ($2 \times I_{a_{L,c}}$), Ch3: Output current of the high-side converter group (I_{a_H}), Ch4: Output current ($I_{a,g}$).

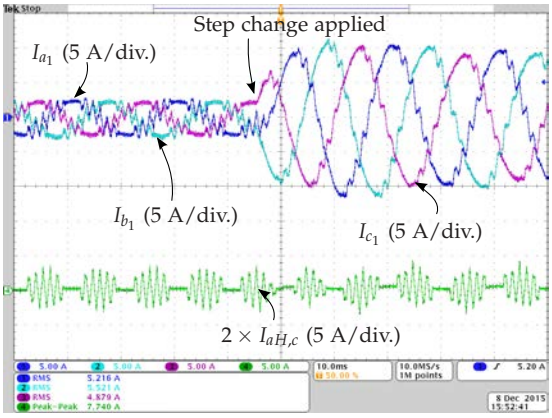
parallel VSCs [31]. As a result, the inductor saturation during the transient is avoided.

The experimental setup is shown in Fig. K.18. The results were obtained for the system shown in Fig. K.1. The electrical equivalent circuit of the integrated inductor along with the *LCL* filter arrangement is shown in Fig. K.9. The VSCs of the HSCG and the LSCG are connected to separate dc-link, fed from two isolated dc supplies. The VSCs were modulated using the DPWM1 and the modulator is implemented using TMS320F28346 floating-point digital signal processor. The implemented inductor was built and its photograph is shown in Fig. K.11(c). The dimensions of the implemented inductor are

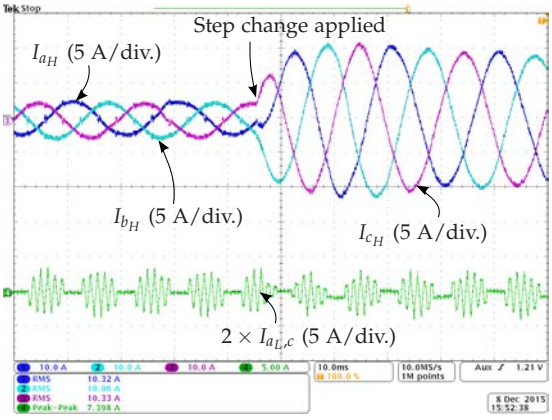
specified in Table K.4. The cell structure is realized using amorphous alloys 2605SA1, whereas laminated steel is used for the bridge legs.

The integrated inductor offers inductance L_c to the circulating current and inductance L_f to the resultant line current. The LCL filter is used for the line current filtering, where L_f is used as a converter-side inductance of the LCL filter. The Y/Δ transformer is used with the star-side winding reconfigured as an open-ended winding. The leakage inductance of the transformer is measured to be 3.1 mH. The transformer leakage along with the discrete 1.9 mH inductor forms the grid-side inductor L_g. The damping branch R_d/C_d is used in parallel with the capacitive branch C_f to provide damping. The system parameters are specified in Table K.3.

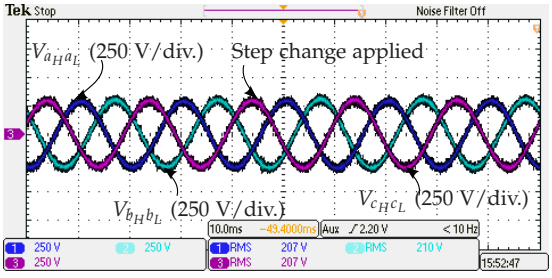
The output currents of phase a of the individual VSCs of both the HSCG and the LSCG during the steady-state operating condition (of rated active power) are shown in Fig. K.19. The individual VSCs are operated with the switching frequency of 750 Hz, and the switched output voltages of the individual VSCs has a major harmonic component at the carrier frequency harmonics. However, these voltage components are phase shifted for two parallel interleaved VSCs and the integrated inductor offers very high inductance (L_c=39 mH) to these components. As a result, the circulating current between the VSCs of the HSCG $I_{a_{H,c}}$ is effectively suppressed, as shown in Fig. K.20. The measured peak value of the circulating current between the VSCs of the HSCG is 1.6 A, which is around 15% of the amplitude of the output current of the individual VSCs. The circulating current between the VSCs of the LSCG $I_{a_{L,c}}$ is also suppressed to 1.6 A (peak value), as shown in Fig. K.20. In addition to the desired fundamental frequency component, the resultant current of the HSCG I_{a_H} also has ripple current components with the major harmonic frequency component at the $4th$ carrier harmonics. These high frequency ripple components are attenuated in the injected grid current $I_{a,g}$ by the LCL filter, as it is evident from the $I_{a,g}$ waveform in Fig. K.20.



(a)



(b)



(c)

Fig. K.21: Experimental waveforms for a step response when the reference current was changed from 0.25 pu to 1 pu. (a) Ch1: I_{a_1}, Ch2: I_{b_1}, Ch3: I_{c_1}, and Ch4: $I_{a_{H,c}}$, (b) Ch1: I_{a_H}, Ch2: I_{b_H}, Ch3: I_{c_H}, and Ch4: $I_{a_{L,c}}$, (c) Ch1: $V_{a_H a_L}$, Ch2: $V_{b_H b_L}$, and Ch3: $V_{c_H c_L}$.

The experimental waveforms when a step change (0.25 pu to 1 pu) is applied in the reference current are shown in Fig. K.21. Fig. K.21(a) shows the leg current of all the phases of the VCS_1, along with the circulating current between the VSCs of the HSCG $I_{a_H,c}$. The resultant line current of the all three phases of the HSCG are shown in Fig. K.21(b). The integrated inductor offers the desired line filter inductance (converter-side inductance of the LCL filter), as it is evident from the waveform quality of the resultant line current of the HSCG. The circulating between the parallel converters of the LSCG is also shown in Fig. K.21(b). The simultaneous sampling of the parallel VSCs avoids the dc flux injection during the transient conditions, as evident from the circulating currents $I_{a_H,c}$ and $I_{a_L,c}$. The circulating current controller also ensures the saturation free operation of the integrated inductor by controlling the fundamental frequency component in the circulating current to be zero.

7 Conclusion

The current handling capability enhancement of the open-end transformer topology for the high power grid-connected applications is proposed. The converter-side winding of the transformer is configured as an open-ended and fed from the two converter groups. Each of the converter groups have two VSCs connected in parallel to achieve high current rating. The carrier signals of the VSCs are interleaved to improve the harmonic performance. The integrated inductor is also proposed, which suppresses the circulating current between the parallel interleaved VSCs and also offer the desired inductance for the line current filtering. The line filter inductors of both the HSCG and the LSCG are also integrated. As the common flux components of the HSCG and the LSCG are the same, they completely cancel each other. As a result, only four bridge legs are required compared to eight in the case of the separate inductors. The use of the integrated inductor leads to 26.2% reduction in the volume of the magnetic material and 40.9% reduction in the volume of the copper for the 12 MW, 3.3 kV WECS. The integrated inductor is analyzed and the design methodology is proposed. The scheme to control the active and the reactive component of the injected current and the fundamental component of the circulating current in $I_{aH,c}$ and $I_{aL,c}$ is also proposed. The analysis is also supported by the simulations and the experimental results.

References

[1] M. Baumann and J. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link cur-

rent balancing," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042–3053, 2007.

[2] R. Jones and P. Waite, "Optimised power converter for multi-MW direct drive permanent magnet wind turbines," in *Proc. European Conference on Power Electronics and Applications (EPE 2011)*, Aug 2011, pp. 1–10.

[3] F. Blaabjerg and K. Ma, "Future on power electronics for wind turbine systems," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 1, no. 3, pp. 139–152, Sept 2013.

[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sept 1981.

[5] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, July 2010.

[6] T. Bruckner, S. Bernet, and P. Steimer, "Feedforward loss control of three-level active npc converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1588–1596, Nov 2007.

[7] G. Grandi, C. Rossi, D. Ostojic, and D. Casadei, "A new multilevel conversion structure for grid-connected pv applications," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4416–4426, Nov 2009.

[8] T. Boller, J. Holtz, and A. Rathore, "Optimal pulsewidth modulation of a dual three-level inverter system operated from a single DC link," *IEEE Trans. Ind. Appl.*, vol. 48, no. 5, pp. 1610–1615, Sept 2012.

[9] N. Bodo, M. Jones, and E. Levi, "A space vector pwm with common-mode voltage elimination for open-end winding five-phase drives with a single DC supply," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2197–2207, May 2014.

[10] M. R. Baiju, K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, May 2004.

[11] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 1893–1909, May 2008.

[12] K. Fujii, P. Koellensperger, and R. De Doncker, "Characterization and comparison of high blocking voltage IGBTs and IEGTs under hard- and soft-switching conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 172–179, Jan 2008.

[13] "Technical guidline: Generating plants connected to the medium-voltage network." BDEW Bundesverband der Energie- und Wasserwirtschaft e.V., [Online]. Available: http://www.bdew.de, June 2008.

[14] S. K. T. Miller, T. Beechner, and J. Sun, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs." Ieee, 2007, pp. 29–35.

[15] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Line filter design of parallel interleaved vscs for high-power wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6775–6790, Dec 2015.

[16] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Design of the trap filter for the high power converters with parallel interleaved VSCs," in *Proc. 40th Annual Conference on IEEE Industrial Electronics Society, IECON 2014*, Oct 2014, pp. 2030–2036.

[17] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673–679, Nov 1995.

[18] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. 28th Annual IEEE Power Electronics Specialists Conference, 1997. PESC '97 Record.*, vol. 2, 1997, pp. 1164–1170 vol.2.

[19] J. Salmon, J. Ewanchuk, and A. Knight, "PWM inverters using split-wound coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2001–2009, 2009.

[20] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved three-phase voltage source converters," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3400–3414, May 2016.

[21] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "An integrated inductor for parallel interleaved vscs and pwm schemes for flux minimization," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7534–7546, Dec 2015.

[22] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ: Wiley-IEEE Press, 2003.

[23] A. Hava, R. Kerkman, and T. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, 1998.

[24] G. Gohil, R. Maheshwari, L. Bede, T. Kerekes, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Modified discontinuous pwm for size reduction of the circulating current filter in parallel interleaved converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3457–3470, July 2015.

[25] G. Gohil, L. Bede, R. Maheshwari, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Parallel interleaved VSCs: influence of the PWM scheme on the design of the coupled inductor," in *Proc. 40th Annual Conference on IEEE Industrial Electronics Society, IECON 2014*, Oct 2014, pp. 1693–1699.

[26] A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, 2011.

[27] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, 2002, pp. 36–41.

[28] J. Li, T. Abdallah, and C. Sullivan, "Improved calculation of core loss with nonsinusoidal waveforms," in *Thirty-Sixth IAS Annual Meeting, IEEE Industry Applications Conference.*, vol. 4, 2001, pp. 2203–2210 vol.4.

[29] P. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers,*, vol. 113, no. 8, pp. 1387–1394, August 1966.

[30] W. Hurley, E. Gath, and J. Breslin, "Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 369–376, Mar 2000.

[31] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes, and F. Blaabjerg, "Integrated inductor for interleaved operation of two parallel three-phase voltage source converters," in *Proc. 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sept 2015, pp. 1–10.

ISSN (online): 2246-1248
ISBN (online): 978-87-7112-511-5

AALBORG UNIVERSITY PRESS