Modulation Strategy for Multiphase Neutral-Point-Clamped Converters

Iraide López, Salvador Ceballos, Josep Pou, Jordi Zaragoza, Jon Andreu, IñigoKortabarria, and Vassilios G. Agelidis

***Abstract*—This paper presents a novel modulation strategy for *n*-phase neutral-point-clamped (NPC) converters. The proposed modulation strategy is able to control and completely remove the low frequency neutral-point (NP) voltage oscillations for any operation point and load types. Even when unbalanced and/or nonlinear loads are considered, the NP voltage remains under total control. Consequently, the strategy is very attractive for *n*-phase active filters. In addition, it enables the use of low capacity film capacitors in NPC converters.**

The proposed modulation takes the carrier-based modulation strategy as a basis. It is formulated following a generalized approach that makes it expandable to *n*-phase NPC converters. In addition, the NP voltage is controlled directly using a closed-loop algorithm that does not rely on the use of the linear control regulators or the additional compensators used in other modulation algorithms. Therefore, no tuning of parameters is required and it performs optimally for any operating conditions and kind of loads, including unbalanced and nonlinear loads. Although the high frequency harmonic content of the output voltages may increase, the weighted total harmonic distortion generated by the proposed strategy is similar to that of a standard sinusoidal pulse-width modulated strategy. The proposed modulation algorithm has been tested in a four-leg NPC converter prototype performing as a three- and four-phase system and operating with balanced and unbalanced loads.

***Index Terms*—Multilevel multiphase converter, neutral-point-clamped (NPC) converter, pulsewidth-modulated inverters, carrier-based modulation, three-level converter, voltage balance**

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I. Introduction

Since the publication of the first work in multiphase drive technology on 1969 [1], the interest of the research community on multiphase systems has increased considerably. At first, this technology did not attract much attention. However, with the development of some technical areas such as ship propulsion [2]–[4], wind energy systems [5]–[7], electric traction, including electric and hybrid vehicles [8], [9], multiphase active filters [10], and the aero-spacial industry [11], [12], multiphase drives have attracted increased interest with many works published in the last ten years. In [13], a review of the current state of the art in this area was presented.

The advantages of multiphase speed drivers with regards to their three-phase counterparts are numerous [13]–[15]:

- Fault tolerance capability, since a multiphase machine can operate with several faulty phases, as long as there are at least three healthy phases.
- Improved efficiency. The stator excitation in a multiphase machine produces a field with lower harmonic content.
- Multiphase machines have lower power handling requirements per phase. Consequently, power semiconductors with lower power rates can be used.
- Improved reliability.

In another vein, multilevel converters (predominantly three-level) have become industrially accepted and a well established technology for medium and high-voltage three-phase drives [16]–[22]. The numerous advantages of the multilevel technology compared to the classic two-level converters include [20], [23]:

- Better quality of the output voltages.
- Better electromagnetic compatibility (lower *dv/dt*).
- Operation with lower switching frequencies (lower switching losses).
- High voltage capability.
- Smaller common mode voltage (reducing the stress in the motor bearings).
- The possibility for fault tolerant operation in some modular configurations.

Several multilevel converter topologies have been proposed in the last three decades. An introduction to these topologies and a comparison between them in terms of structure, modularity, looses, and quality of the synthesized output voltages is made in [16], [20], [24], and [25]. Among all the multilevel topologies, the three-level neutral-point-clamped (NPC) converter [26] is probably the most popular and extended one due its simple circuit structure and less number of capacitors.

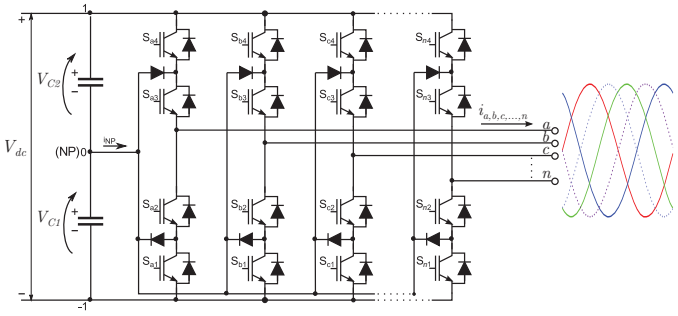


Figure 1. *n*-phase three-level NPC converter.

This paper focuses on this topology and develops a generalized modulation strategy for multiphase NPC converter drives (Fig. 1).

Several publications propose modulation algorithms for multilevel multiphase drives. Some of them follow a space vector PWM (SVPWM) approach [27]–[31]. However, when the converter has more than three phases, the number of switching vectors increases exponentially, according to the rule l^n (where l is the number of converter levels, and n is the number of phases). In addition, the space vector diagram changes from a 2-D plane, for three-phase converters, to a (n-1)-D vector diagram for converters with more than three phases [27]. Consequently, an increase in the number of phases implies dealing with a high number of switching vectors and with sophisticated vector diagrams, making the implementation of SVPWM complex. This fact complicates the application of SVPWM algorithms for multilevel multiphase systems and increases the calculation requirements of the digital controller.

Several solutions have been proposed with the aim of simplifying the implementation of SVPWM algorithms for *n*-phase converters. [28] proposes a space vector decomposition (SVD) based strategy for a three-level five-phase converter, in which a decomposition of the variables into two orthogonal planes is conducted. In [29], a similar methodology is reported for a three-level seven-phase NPC converter. SVM formulation is also used in [30] and [31], where a methodology for the duty cycle calculation of multilevel multiphase converters is derived using a two-level approach. The computation complexity is independent of the number of levels, but the use of matrix formulation is required. The matrix size is a function of the number of phases. Therefore, the higher the number of phases, the larger the matrix dimensions. Consequently, implementing the modulation in multiphase converters is costly and time consuming.

Carried-based PWM modulation strategies (CBPWM) have also been reported in the technical literature. CBPWM strategies are easily extended from two-level to multilevel structures, and are well-established for three-level three-phase systems [32]–[35]. Likewise, CBPWM strategies are independent of the number of phases, thus, extension to multiphase systems is relatively simple.

A comparison of CBPWM and SVPWM strategies for a three-level five-phase NPC converter is presented in [36]. SVPWM and CBPWM are compared in terms of voltage and current waveform distortion and algorithm implementation complexity. Three CBPWM strategies are used to perform the comparison analysis. The first one is a pure CBPWM strategy without any zero-sequence voltage injection [37], [38]. The second one is a CBPWM algorithm with single zero-sequence injection according to the min-max principle to extend the modulation index range of linear modulation region [39]. The last one is a CBPWM with double zero-sequence injection based on [40]. It aims to reduce the harmonic distortion in the output voltages. All compared CBPWM techniques are simpler and require less computation time than their SVPWM counterparts. Therefore, they are better suited for multiphase industrial applications.

However, none of the CBPWM strategies used for the comparison in [36] includes neutral-point (NP) voltage balance control. NP voltage control is crucial for NPC converters [41], [42], especially when they perform as active filters or are connected to unbalanced electrical systems. In those situations, the amplitude of the low frequency NP voltage oscillations increases considerably and, under certain nonlinear loads, the NP voltage becomes instable [43]. Several CBPWM modulation strategies able to completely control/remove the NP voltage oscillations have been proposed for three-phase NPC converters [44]–[46] and multiphase *n*-level diode-clamped-converters [47], [48]. The modulation algorithm introduced in this paper belongs to this group of modulation strategies. It has the following features:

- The algorithm is formulated following a generalized and recursive approach that makes it extendible to *n*-phase converters.
- It is based on a CBPWM approach. Hence, it is not necessary to deal with sophisticated vector diagrams with many vectors when the number of phases increases.
- It is able to completely control the NP voltage, thus removing the low frequency NP voltage oscillations of multiphase NPC converters under any working condition.
- It is indicated for unbalanced and/or nonlinear loads.

In addition, it adds the following new features to the already published algorithms [44], [45], [47] and [48]:

- The NP voltage is directly controlled using a closed-loop algorithm that does not involve any linear controllers, such as proportional controllers, proportional-integral (PI) controllers, linear-quadratic regulators etc., or compensators used in other modulation algorithms. Therefore, it is no need to tune any regulator.
- The number of switching commutations is the minimum required to have total control over the NP voltage.

The paper is organized as follows. Firstly, the basis of the modulation algorithm is analysed in Section II. Section III presents simulation and experimental results for three- and and four-phase NPC converters under balanced and unbalanced load conditions. Section IV compares the proposed modulation algorithm with previous published modulation strategies, and Section V concludes the paper.

II. Basis of the Modulation Strategy

The proposed modulation strategy uses a CBPWM approach where each phase is controlled by means of a modulation

signal. A zero-sequence voltage injection to extend the linear modulation region is used. Hence, the normalized modulation signals for an *n*-phase electrical system are:

$$v'_a = v_a + v_{off}, \quad (1)$$
$$v'_b = v_b + v_{off}, \quad (2)$$
$$...$$
$$v'_n = v_n + v_{off}, \quad (3)$$

where:

$$v_{off} = -\frac{max(v_a, v_b, ..., v_n) + min(v_a, v_b, ..., v_n)}{2} \quad (4)$$

is the normalized zero-sequence voltage and v_a, v_b, ..., v_n, are the normalized phase voltages.

The locally-averaged NP current in each switching period can be expressed as:

$$\overline{i}_{NP} = i_a d_{NP_a} + i_b d_{NP_b} + ... + i_n d_{NP_n}, \quad (5)$$

where i_a, i_b, ..., i_n are the output currents and d_{NP_a}, d_{NP_b}, ..., d_{NP_n} are the NP duty cycles that represent the time that each phase remains connected to the NP per switching period. The line on top of i_{NP} in (5) indicates locally-averaged magnitude, where the averaging interval is the switching period. For the sake of simplicity, this notation will be omitted in the rest of the paper.

CBPWM strategies, such as those introduced in [32]–[35], only allow to switch the converter phases between the *dc* bus positive rail and the NP, when the corresponding normalized modulation signal is positive, or between the negative rail and the NP when the modulation signal is negative. Under these circumstances the relationships between the normalized modulation signals and the NP duty cycles are given by:

$$d_{NP_a} = 1 - |v'_a|, \quad (6)$$
$$d_{NP_b} = 1 - |v'_b|, \quad (7)$$
$$...$$
$$d_{NP_n} = 1 - |v'_n|. \quad (8)$$

Consequently, the way to control the NP current is though the modif cation of the zero-sequence voltage. It has been demonstrated in previous publications that these modulation strategies are not able to achieve zero NP current calculated on average over every switching period. Therefore, low frequency NP voltage oscillations, or even NP voltage instabilities, depending on the converter load, may appear [43].

Nevertheless, if the converter phases are allowed to switch between the positive, NP, and the negative rails of the *dc* bus in each switching period, the NP duty cycles can be reduced and set to any desired value between the upper limit imposed by (6)-(8) and zero. Consequently, i_{NP} can be controlled in each switching period. The average NP current calculated over a switching period should be zero to maintain the NP voltage balanced. There are multiple solutions to achieve this, the most obvious one consists on making all the NP duty cycles equal to zero (this solution makes the three-level NPC converter work as a two level converter). However, in order to maintain the switching frequency and the distortion of the output voltage waveforms under reasonable limits, it is necessary to reduce the number of phases commutating between the three levels to the minimum. Appendix A demonstrates that a three-phase NPC converter only requires a single phase to commutate between the three voltage levels (positive *dc* bus, negative *dc* bus, and NP) in each switching period to completely remove the NP voltage oscillations. This phase can be the one that contributes with the maximum absolute value to the NP current, that is, the phase that makes maximum the term $\mid i_x d_{NP_x} \mid$ in (5).

However, this cannot be extrapolated to multiphase systems. Appendix B demonstrates that a four-phase NPC converter connected to an unbalanced load requires two phases switching between the three voltage levels during certain intervals in order to have total control over the NP voltage. Therefore, development of a general modulation strategy valid for *n*-phase NPC converters requires endowing the algorithm with a mechanism to discern the minimum number of phases switching between the three voltage levels in each switching period.

The modulation strategy proposed in this paper is based in these ideas. The sequence of actions that the algorithm has to perform in each modulation period is the following:

- **Step 1:** Calculation of the NP current reference i^*_{NP}. The algorithm calculates the reference value of the NP current required to balance the NP voltage of the NPC converter. This value is calculated according to the following expression:

  $$i^*_{NP} = \frac{\Delta v_{NP}}{T_s} 2C, \quad (9)$$

  where T_s is the switching period and Δv_{NP} is the deviation of the NP voltage with respect to its reference value, i.e. Δv_{NP}=v_{C1}-$\frac{v_{dc}}{2}$, where v_{C1} is the voltage of the lower *dc* bus capacitor (see Fig. 1).
- **Step 2:** Calculation of the NP current i_{NP} that would circulate through the NP if a standard CBPWM were used. This current is calculated by means of (5).
- **Step 3:** Selection of the phases that have to commutate between three voltage levels and calculation of their NP duty cycles. Depending on the value of the NP voltage v_{C1}, and the instantaneous values of i^*_{NP} and i_{NP} calculated in Steps 1 and 2, several cases can take place. Fig. 2 shows a block diagram with the actions that the algorithm has to perform in each case. Fig. 3 illustrates examples of the cases that can be produced.
  - **Case a:** If ($0<i_{NP}<i^*_{NP}$) or ($i^*_{NP}<i_{NP}<0$) it is not necessary that any phase of the converter switches between the three voltage levels because the NP current produced by standard CBPWM has a magnitude and direction that tends to compensate for the NP voltage imbalance.
    Therefore, the NP duty cycles of all the converter phases are calculated according to (6)-(8). Since in this condition all the phases switch between two voltage levels, the number of switching transitions and, consequently, the switching losses are reduced. This is an important difference of this algorithm compared to similar ones [44], [45], [47], [48].

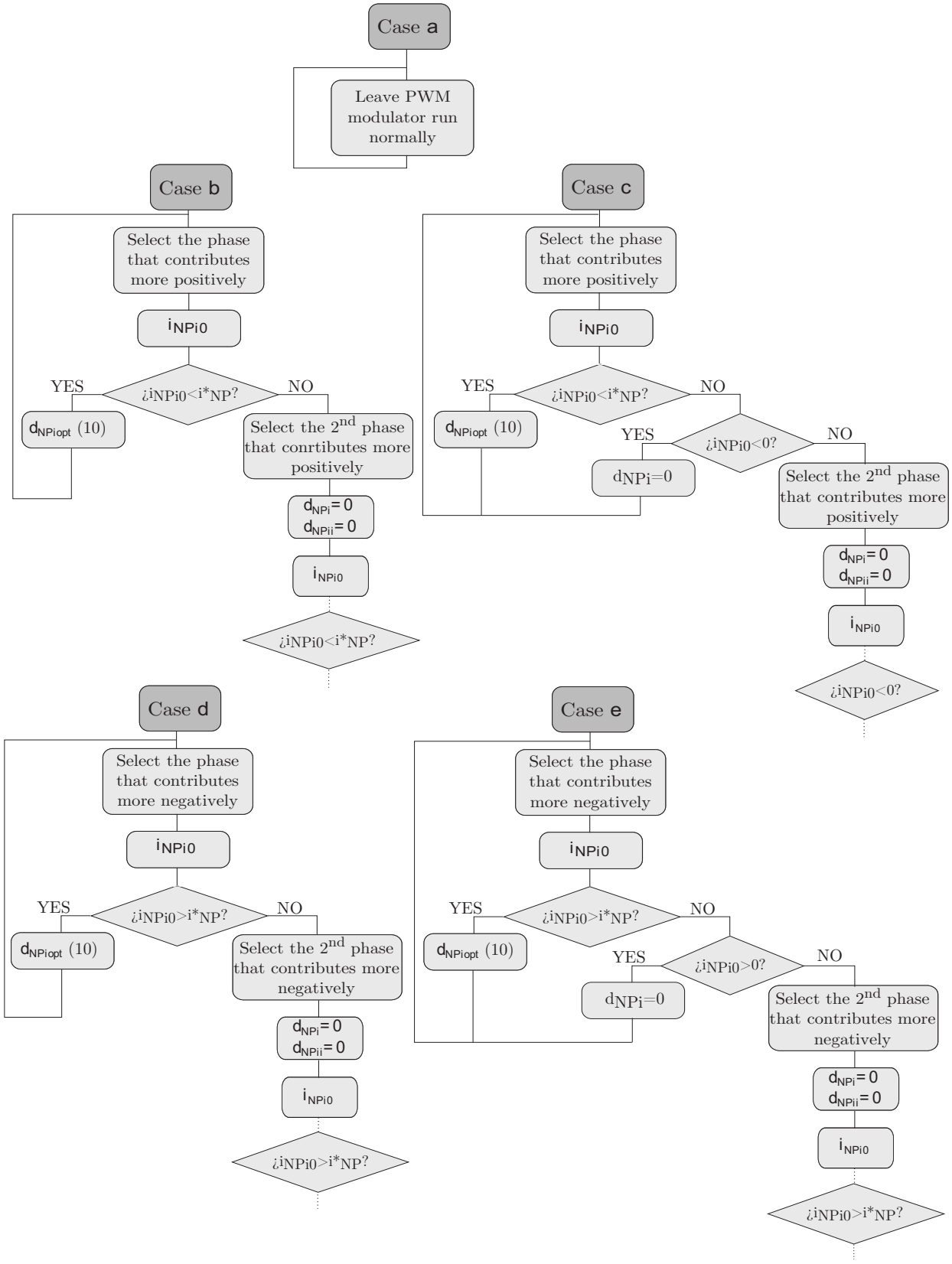


Figure 2. Modulation strategy f owchart.

– **Case b:** If ($v_{NP} > \frac{v_{dc}}{2}$) and ($i_{NP} > i^*_{NP}$). In this case the NP current generated with the standard CBPWM tends to decrease the value of the NP voltage below $\frac{v_{dc}}{2}$. Consequently it is necessary to reduce the NP

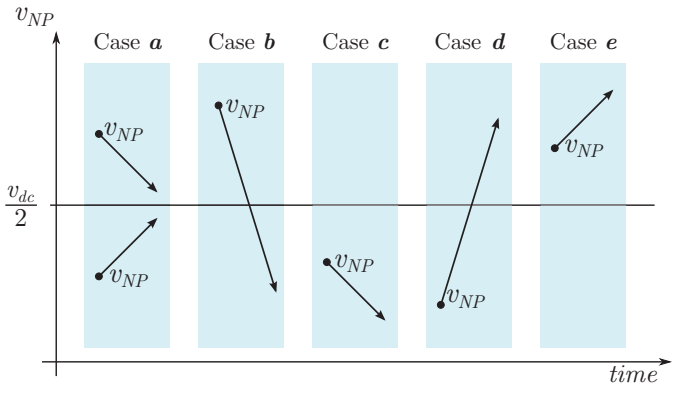


Figure 3. Tendency of the NP voltage for the different cases if standard CBPWM were applied.

current making it equal to i^*_{NP}. To achieve this, some of the phases have to commutate between the three voltage levels of the *dc* bus. To find out these phases, the following procedure can be followed (see Fig. 2):

- Select the phase with the higher contribution to the NP current. Let us denote this phase with the subscript *i*.
- Set the NP duty cycle of this phase to zero, that is d_{NP_i}=0, and calculate $i_{NP_{i0}}$ using (5).
- If ($i_{NP_{i0}}$<i^*_{NP}) then it is possible to reach the desired value of i^*_{NP} making the selected phase switch between the three voltage levels. The NP duty cycle of the selected phase is calculated using the following expression:

$$d_{NP_{i_{opt}}} = \frac{i^*_{NP} - i_a d_{NP_a} - ... - i_n d_{NP_n}}{i_i}. \quad (10)$$

- If ($i_{NP_{i0}}$>i^*_{NP}), fix d_{NP_i}=0, select the phase with the second highest contribution to the NP current and repeat the process.
- Repeat the previous process with as many phases as necessary until the NP current reaches the reference value.

– **Case c:** If ($v_{NP} < \frac{v_{dc}}{2}$) and ($i_{NP}$>0). In this case the NP current generated with the standard CBPWM again tends to decrease the value of the NP voltage below $\frac{v_{dc}}{2}$. Consequently, it is necessary that some of the phases commutate between the three voltage levels of the *dc* bus. The main difference between this case and the previous one is that, since i^*_{NP}<0 and i_{NP}>0, it might be not possible to make the NP current equal to i^*_{NP}. Nevertheless, it will be always possible to fix the NP current to a value below or equal to zero. Therefore, there will be a tendency to balance the NP voltage. The procedure to determine the NP duty cycles of the phases that have to switch between the three voltage levels is as follows (see Fig. 2):

- Select the phase with the highest contribution to the NP current. Let us denote this phase with the subscript *i*.
- Set the NP duty cycle of this phase to zero, that is d_{NP_i}=0, and calculate $i_{NP_{i0}}$ using (5).
- If ($i_{NP_{i0}}$<i^*_{NP}) then it is possible to reach the desired value of i^*_{NP} making the selected phase switch between the three voltage levels. The NP duty cycle of the selected phase is calculated according to (10).
- If ($i_{NP_{i0}}$>i^*_{NP}) and ($i_{NP_{i0}}$<0), then set d_{NP_i}=0.
- If ($i_{NP_{i0}}$>0), fix d_{NP_i}=0, select the phase with the second highest contribution to the NP current and repeat the process.
- Repeat the previous process with as many phases as necessary until the NP current reaches the reference value or is below zero.

– **Case d:** If ($v_{NP} < \frac{v_{dc}}{2}$) and ($i_{NP}$<$i^*_{NP}$). This case is similar to Case b but for negative values of the NP current. Consequently, the procedure to calculate the NP duty cycles is equivalent in both cases (see Fig. 2).

– **Case e:** If ($v_{NP} > \frac{v_{dc}}{2}$) and ($i_{NP}$<0). This case is equivalent to Case c but for opposite NP currents. Consequently, a similar procedure should be followed (see Fig. 2).

- **Step 4:** Calculate the NP duty cycles of the phases that do not have to switch between three voltage levels using (6)-(8).
- **Step 5:** Calculate the positive and negative duty cycles by:

$$dl_i = \frac{1 - d_{NP_{i_{opt}}} - v'_i}{2}, \quad (11)$$

$$dh_i = 1 - d_{NP_{i_{opt}}} - dl_i, \quad (12)$$

where dl_i and dh_i are the negative and positive duty cycles and represent the time per switching period that the phase *i* remains connected to the positive and negative *dc* bus rails, respectively.

Once the positive, NP and negative duty cycles have been calculated, they are compared with a timer and the switching events of the phases are generated accordingly. The proposed modulation strategy is very appropriate to be programmed in a digital signal processor. In order to show how it works, a numerical example is shown. Let us consider a four-phase NPC converter connected to an unbalanced load. The *dc* bus is formed by two 1-mF capacitors and it is connected to a v_{dc}=5000 V source. The switching frequency is 1 kHz and the modulation index is *m*=0.8. In the steady state, the normalized reference voltages of the converter are:

- v_a=0.8sin(ωt) V,
- v_b=0.8sin$\left(\omega t + \frac{\pi}{2}\right)$ V,
- v_c=0.8sin($\omega t + \pi$) V,
- v_d=0.8sin$\left(\omega t + \frac{3\pi}{2}\right)$ V,

where ω=2πf, with *f*=50 Hz.

Let us also suppose the converter is connected to an unbalanced load that produces the following set of phase currents:

- i_a=60cos(ωt) A,
- i_b=100cos($\omega t + \pi$) A,

- i_c=40cos(ωt) A,
- i_d=0 A.

Finally, let's assume that the NP voltage is v_{C1}=2495 V.

Accordingly to the previous description of the algorithm, the following steps have to be followed:

Step 1: Calculate the NP current reference using (9):

$$i^*_{NP} = \frac{v_{C1} - \frac{v_{dc}}{2}}{T_s} 2C = -10A.$$

Step 2: Calculate i_{NP} using (5)-(8). Let us suppose that the system is being evaluated at t=0. Consequently, v_a=0, v_b=0.8, v_c=0, v_d=-0.8, i_a=60 A, i_b=-100 A, i_c=40 A, and i_d=0 A. According to (6)-(8), d_{NP_a}=1, d_{NP_b}=0.2, d_{NP_c}=1 and d_{NP_d}=0.2. Therefore, using (5), i_{NP}=80 A.

Step 3: Selection of the phases that must commutate between three voltage levels and calculation of their NP duty cycles. In this example ($v_{NP} < \frac{v_{dc}}{2}$) and ($i_{NP}$>0), consequently the Case c is selected. Accordingly to this case, the following procedure has to be followed:

- Select the phase that makes maximum the term $|i_x(1-|v_x|)|$. In this example, this is the phase a (x=a).
- Set the duty cycle of phase a to zero and calculate the NP current i_{NPa0} using (5)-(8). In this example i_{NPa0}=20 A.
- i_{NPa0}>0, consequently d_{NP_a} is fixed to zero d_{NP_a}=0 and the phase with the second highest contribution to the NP current is calculated. In this example this is the phase c.
- The NP optimum duty cycle of phase c is calculated according to (10) to obtain the desired NP current reference i^*_{NP}:
  d_{NP_c}=0.25

Step 4: Calculate the NP duty cycles of phases b and d using (6)-(8):
d_{NP_b}=0.2,
d_{NP_d}=0.2.

Step 5: Calculate the positive and negative duty cycles of all the phases using (11) and (12):
dl_a=0.5, dh_a=0.5,
dl_b=0, dh_b=0.8,
dl_c=0.375, dh_c=0.375,
dl_d=0.8, dh_d=0.

Following these simple steps, the duty cycles of a four phase converter connected to an unbalanced load and with an initial NP voltage deviation have been calculated. In the example, two phases have to switch between the three voltage levels to obtain a NP current able to compensate for the NP voltage deviation.

III. Simulation and Experimental Results

Experimental validation of the modulation strategy has been conducted in a 20-kW test-rig. The experimental platform, comprises a three-level four-phase NPC converter connected to a star R-L load (Fig. 4). The *dc* bus has two capacitors of 1.1 mF connected in series. The *dc* bus voltage is 250 V.

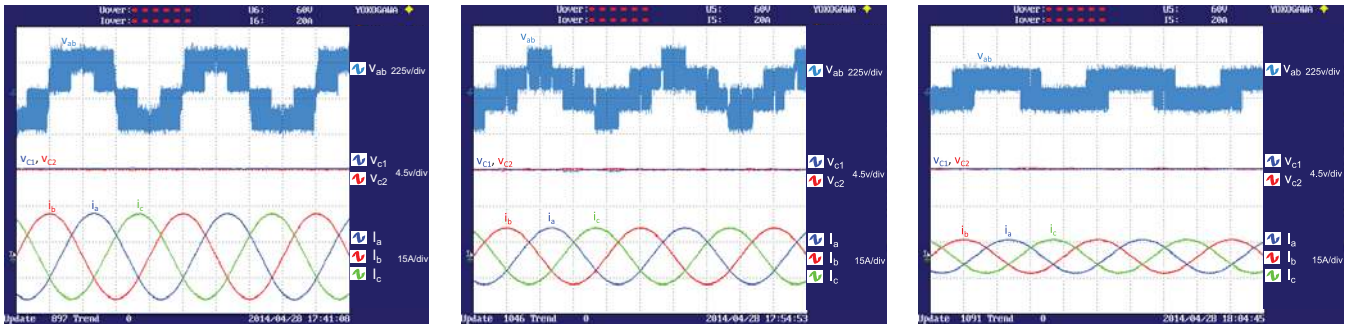
Figure 4. Experimental platform.

The frequency of the carriers is 2.5 kHz, and the fundamental frequency of the generated *ac* voltages has been set to 20 Hz, low enough to emphasize the effect of the low frequency NP voltage oscillations. Several case studies have been conducted to validate the proposed modulation strategy.

A. Three-Level Three-Phase NPC

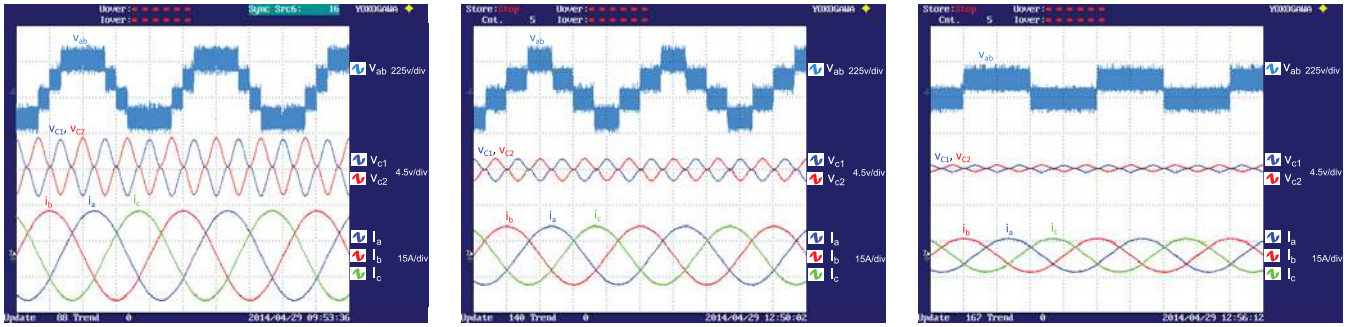
1) Balanced load conditions: In this test only three converter phases are used. Thus, the converter performs as a three-phase system. Fig. 5 shows the experimental results obtained when the converter is connected to a balanced three-phase star-connected *R-L* load (R=5 Ω, L=10 mH) for m=1.15, m=0.7, and m=0.4 respectively. The figure displays the line-to-line voltage v_{ab}, the voltage of the *dc*-link capacitors v_{C1} and v_{C2}, and the output currents $i_{a,b,c}$. Fig. 6 shows equivalent results when the standard CBPWM is used. It can be appreciated how the proposed modulation strategy cancels completely the low frequency NP voltage oscillations and maintains the NP voltage under complete control. Conversely, there are NP voltage oscillations when standard CBPWM is used.

2) Unbalanced load conditions: In this test, an unbalanced *R-L* load ($R_{a,b}$=5 Ω, $L_{a,b}$=10 mH, and open circuit in phase c) is connected to the converter output. Fig. 7 and Fig. 8 show the results of the proposed modulation strategy and the standard CBPWM, respectively. Observe that the amplitude of the low frequency NP voltage oscillations increase significantly reaching peak-to-peak values of up 40 V for the maximum modulation index when the standard CBPWM is used. When the proposed modulation strategy is used, some NP voltage oscillations with a frequency twice the fundamental one and with very low amplitude can be observed (see Fig.7). These oscillations are caused by the inability of the *dc* power supply connected to the *dc*-bus to maintain completely constant the *dc*-voltage. Under unbalanced loads the instantaneous power provided by the *dc* power supply is not constant but oscillating and the source is not able to maintain a fixed *dc*-bus voltage. Consequently, as the proposed modulation strategy tends to maintain the NP voltage to $\frac{V_{dc}}{2}$, any *dc*-bus voltage oscillation is reflected in the NP voltage. This argumentation explains what the cause of the low frequency NP voltage oscillations



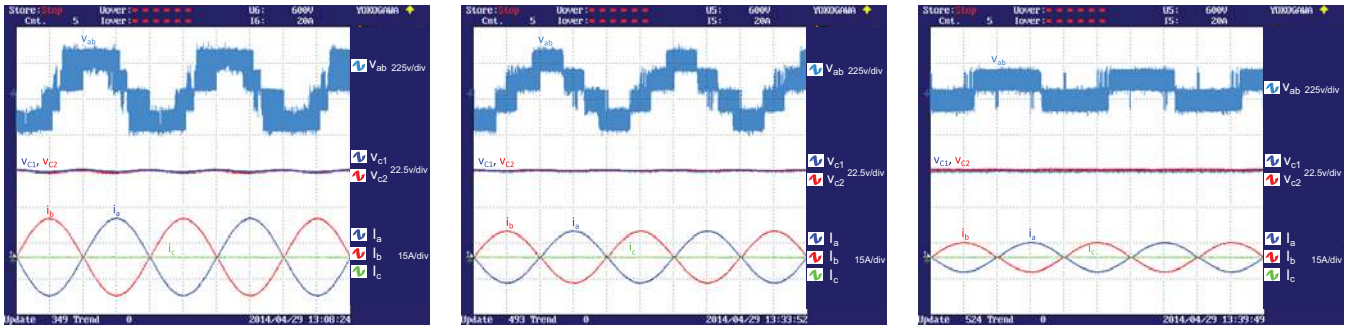
(a) (b) (c)

Figure 5. Three-level three-phase NPC conf guration. Results applying the proposed algorithm with (a) m=1.15, (b) m=0.7, and (c) m=0.4.



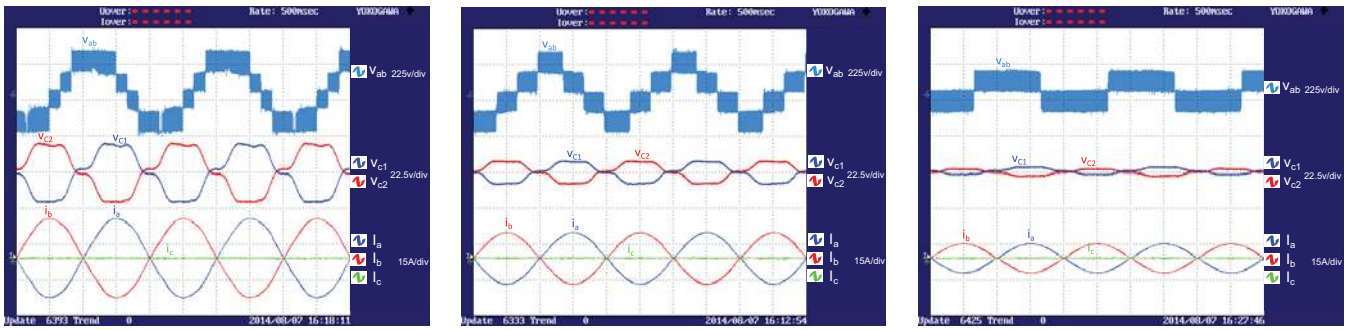
(a) (b) (c)

Figure 6. Three-level three-phase NPC conf guration. Results applying the standard CBPWM algorithm with (a) m=1.15, (b) m=0.7, and (c) m=0.4.



(a) (b) (c)

Figure 7. Three-level three-phase NPC conf guration. Results connected to an unbalanced load applying the proposed algorithm with (a) m=1.15, (b) m=0.7, and (c) m=0.4.

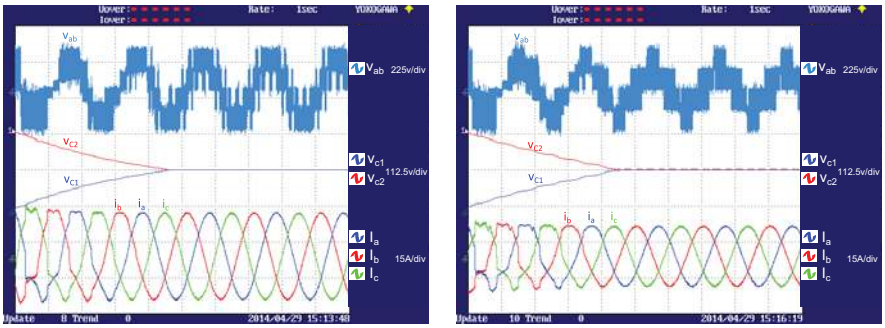


(a) (b) (c)

Figure 8. Three-level three-phase NPC conf guration. Results connected to an unbalanced load applying standard CBPWM algorithm with (a) m=1.15, (b) m=0.7, and m=0.4.

that appear in Fig. 7 is and corroborates the good performance of the proposed modulation strategy.

3) Unbalanced NP voltage: In this test the *dc*-link capacitors are forced to have an initial voltage imbalance. The initial



(a) (b)

Figure 9. Three-level three-phase NPC conf guration with an initial NP voltage imbalance applying the proposed algorithm with (a) m=1 and (b) m=0.7.

voltages of the upper and lower *dc* capacitors are 250 V and 0 V, respectively. Fig. 9 shows the capacitor voltages when the proposed modulation strategy is used. It can be observed that the *dc*-link capacitor voltages reach the reference value ($\frac{v_{dc}}{2}$). This fact demonstrates the capability of the proposed algorithm to i) balance the NP voltage even under such a big initial voltage unbalance, and ii) remove the NP voltage oscillations. Fig. 9 also shows a low-frequency distortion in the line-to-line voltages and the output currents caused by the modulation strategy when the NP voltage is unbalanced. Nevertheless, since the algorithm is able to balance the NP voltage at all the times under any operating conditions, NP voltage unbalances are not expected. Consequently, no low frequency distortion will be produced in the output voltages and currents. In those applications that require an unbalanced NP voltage, the proposed modulation strategy is not applicable directly and a feedforward compensation term is required.

B. Three-Level Four-Phase NPC

1) Unbalanced load conditions: Due to symmetry of a four-phase electrical system, no low frequency NP voltage oscillations would occur under balanced load condition. Therefore, the proposed algorithm performs as a traditional CBPWM modulation strategy. However, as it is demonstrated in the Appendix B and has been shown in the numerical example introduced in the previous section, the situation is different if the four-phase NPC converter is connected to an unbalanced load. In this case, it might be necessary to switch one or two phases between the three *dc* voltage levels to control the NP current and remove the low frequency NP voltage oscillations that otherwise would occur. Fig. 10 shows experimental results obtained when the proposed modulation strategy is used and the four-phase NPC converter is connected to an unbalanced *R-L* load for m=1, m=0.7, and m=0.4. Fig. 11 shows the results obtained when a standard CBPWM strategy is used under the same working conditions. One can observe again the ability of the proposed modulation algorithm to cancel completely the low frequency NP voltage oscillations. These results show the viability and good performance of the proposed algorithm for NPC converters with more than three phases.

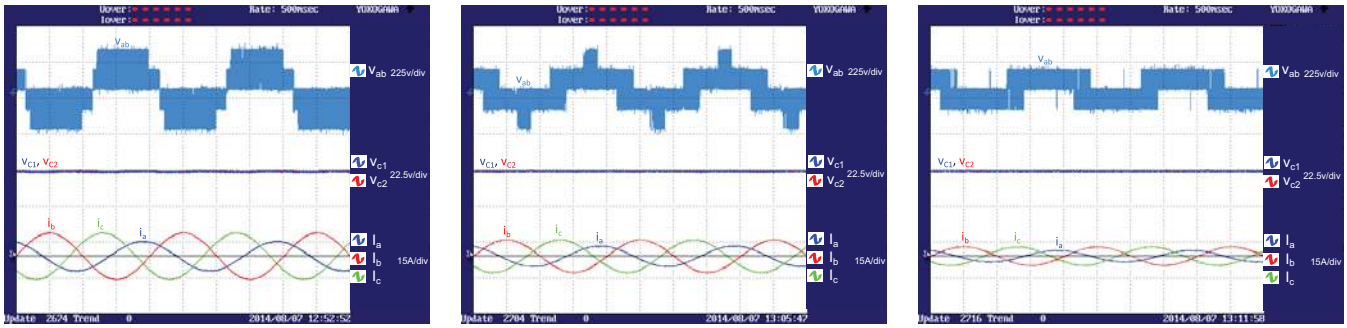
2) Unbalanced NP voltage: Fig. 12 shows the results when an initial imbalance is forced in the *dc*-link capacitor voltages of a four-phase NPC converter connected to unbalanced *ac* *R-L* load. Even under these extreme operating conditions, the proposed modulation strategy is able to compensate the initial voltage imbalance and remove the low frequency NP voltage oscillations.

C. Distortion Analysis

The proposed modulation strategy forces some phases of the converter to switch between three voltage levels to maintain the NP voltage under control. Consequently, the high frequency harmonic content of the output voltage increases when the proposed technique is used. This is clearly appreciated comparing the results of Fig. 5 and Fig. 6. However, despite the increase on the high frequency harmonic content of the voltage waveforms, the generated currents are still nicely sinusoidal. To analyse the quality of the output voltage waveforms, the total harmonic distortion (THD) and the weighted total harmonic distortion (WTHD) have been considered. In addition, the harmonic representations of the voltage waveforms have been obtained. Fig. 13(a) shows the results obtained when the standard CBPWM modulation strategy is used in a three-phase NPC converter switching at 2.5 kHz. A peak-to-peak low frequency NP voltage oscillation of $\pm 15\%$ has been assumed. Fig. 13(b) shows the results when the proposed modulation strategy is used. The proposed modulation strategy produces higher THD values due to the larger high frequency components. However, the WTHD is similar in both modulation strategies. This is due to the low frequency distortion caused by the low frequency NP voltage oscillations when the standard CBPWM is used. As a consequence, the f lter requirements would be similar for both modulation strategies.

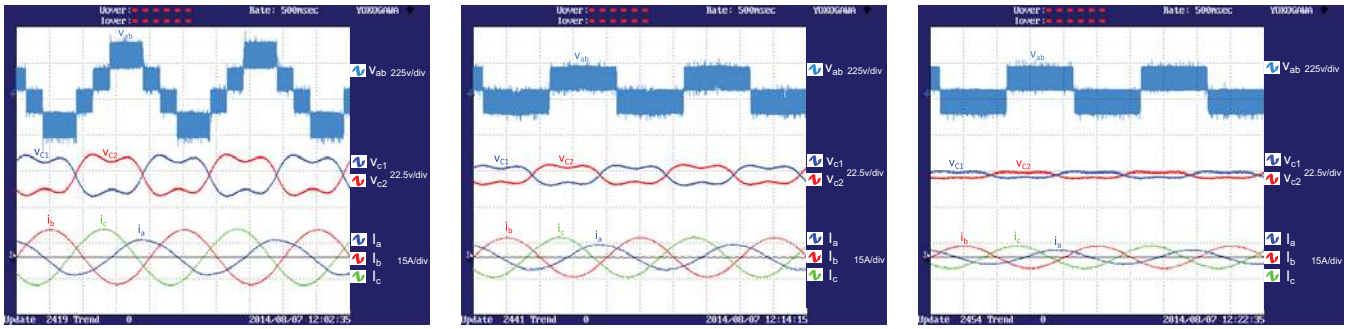
D. NP Voltage oscillations

Previous experimental results demonstrate the capacity of the proposed modulation technique to control the NP voltage and to cancel the low frequency NP voltage oscillations for some specif c operating conditions. To extend this study, the NP voltage oscillations for any operating condition have been computed using Matlab/Simulink. Fig. 14 shows the normalized amplitude of the low frequency NP voltage oscillations for all modulation indexes and power factors for three and four-phase NPC converters respectively. The normalized NP voltage amplitude is def ned as [41]:



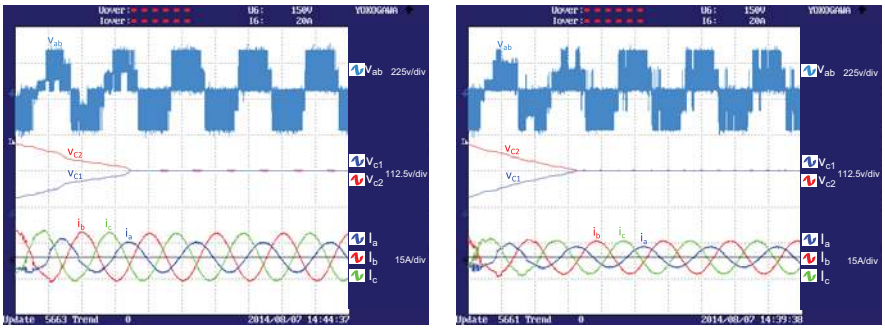
(a) (b) (c)

Figure 10. Three-level four-phase NPC conf guration connected to an unbalanced load applying the proposed algorithm with (a) m=1, (b) m=0.7, and (c) m=0.4.



(a) (b) (c)

Figure 11. Three-level four-phase NPC conf guration connected to an unbalanced load applying standard CBPWM algorithm with (a) m=1, (b) m=0.7, and (c) m=0.4.



(a) (b)

Figure 12. Three-level four-phase NPC conf guration. Initial capacitor voltage imbalance applying the proposed algorithm with (a) m=1 and (b) m=0.7.

$$\frac{\Delta V_{NPn}}{2} = \frac{\Delta V_{NP}/2}{I_{RMS}/fC} \tag{13}$$

where I_{RMS} is the RMS value of the output currents, f is the output frequency, C is the value of the dc-link capacitors and ΔV_{NPn} the peak-to-peak value of the low frequency oscillations.

Due to the symmetry of the load, only the Nyquist sequence [49] of the output current has been considered for the four-leg converter.

The normalized amplitude is always zero regardless the operating conditions. Consequently, these results conf rm the capacity of the proposed modulation technique to eliminate the low frequency NP voltage oscillation for any operating condition, including high modulation indexes and low power factors which are the more critical conditions for the NPC converter.

IV. Benchmarking

In order to evaluate the performance of the modulation technique presented in this paper, the THD, speed of capacitor voltage recovery, and number of switching transitions are benchmarked against the modulation technique introduced in [48].

Fig. 15 shows a comparison in terms of THD of the line-to-line voltage waveforms of an three-phase NPC converter for different load conditions, modulation indexes, and modulation strategies. When the converter is connected to a balanced load with zero power factor (PF=0) (see Fig. 15(a)), both modulation strategies generate the same waveforms. Consequently, the

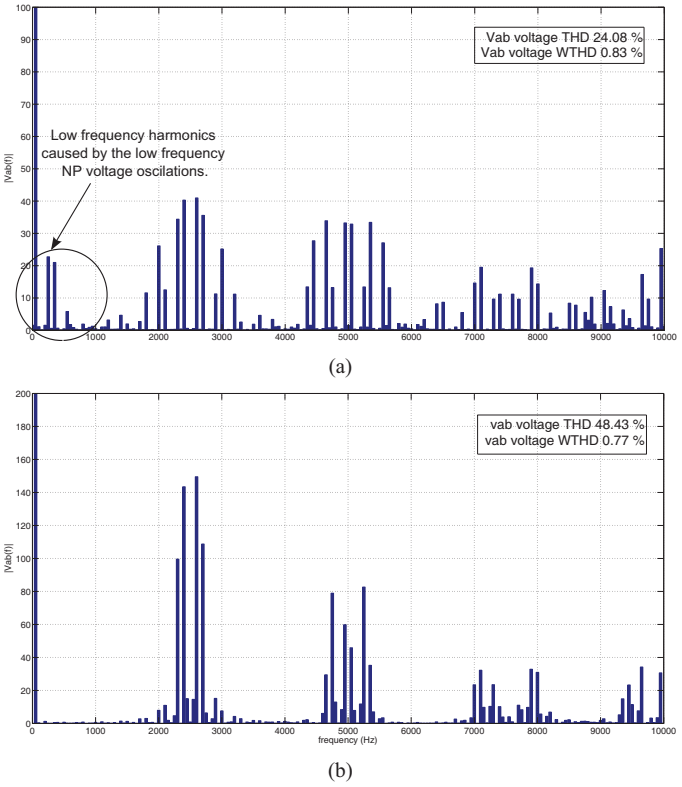


Figure 13. Spectra of the line-to-line voltages with m=1.15. (a) Standard CBPWM and (b) proposed modulation strategy.

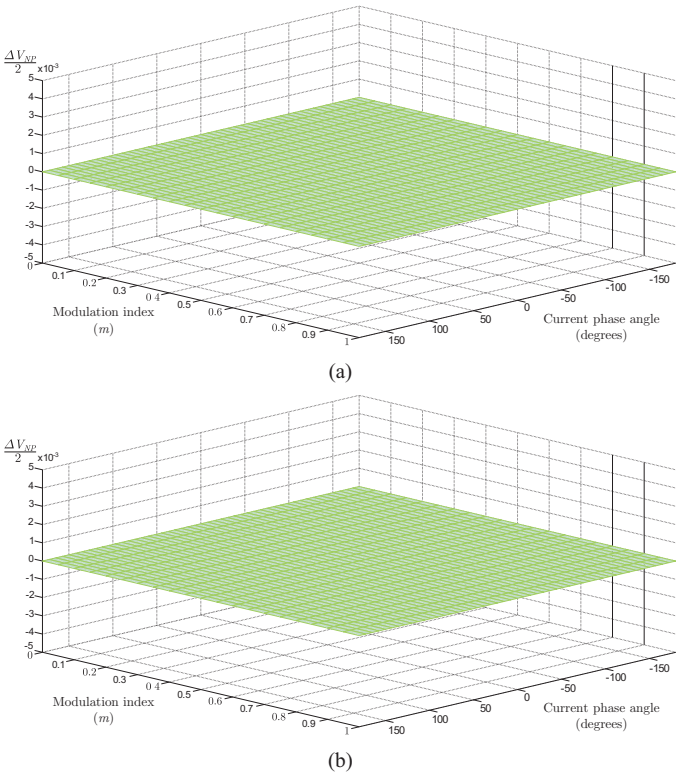


Figure 14. Normalized amplitude of the low-frequency NP voltage oscillations: (a) three-phase NPC converter; (b) four-phase NPC converter.

THD values are identical. When the PF=1 (see Fig 15(b)), the THD values obtained using the proposed modulation strategy

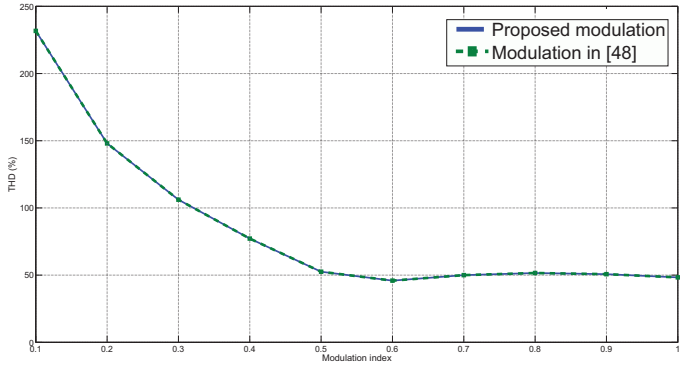
Table I
NUMBER OF SWITCHING IN PER-UNIT REGARDING TO [48] WITH m=1.

Operating conditions	Proposed modulation	Modulation in [48]
Balanced load 3-phase NPC PF=0, PF=1	1	1
Unbalanced load (one phase is in open circuit), 3-phase NPC PF=0, PF=1	0.92	1
Balanced load 5-phase NPC PF=1	0.81	1
Unbalanced load (phase b is left in open circuit), 5-phase NPC PF=0	0.75	1

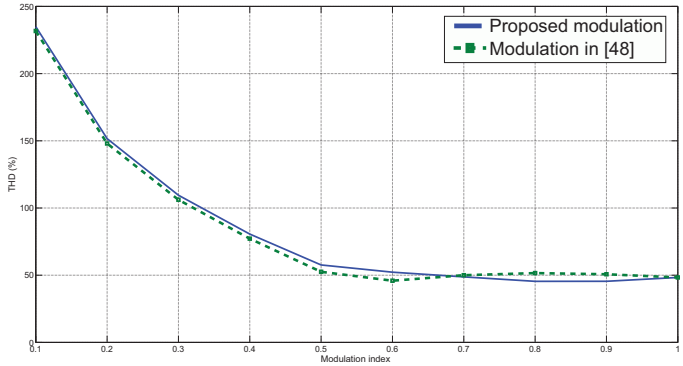
are higher for low modulation indices. However, they are lower for high modulation indexes, which are the most usual working conditions in several applications. Finally, Fig. 15(c) shows the THD results for unbalanced load conditions (one phase of the converter is in open circuit). The THD of the output voltages generated by the proposed modulation algorithm is again lower at high modulation indexes. The THD reduction showed in Fig. 15(c) is strongly related with the way the modulation technique introduced in this paper behaves. The proposed modulation algorithm allows all the phases of the converter to commutate simultaneously between two voltage levels if switching among three voltage levels is not required for NP voltage balance (the Case *a* in Fig. 2 and Section II is selected). This breaks the regularity of the line-to-line voltage pattern but, since all the phases of the converter switch between two voltage levels, the THD values are lower.

Fig. 16 compares the capacity of the proposed modulation strategy to balance the NP voltage under an initial voltage imbalance. A star connected R-L (R=5 Ω, L=10 mH) load have been used. The modulation index and switching frequency have been f xed to 0.75 and 2.5 kHz respectively. 0.175 mF dc-bus capacitors have been assumed.The proposed algorithm is able to balance the NP voltage but the dynamic response is slower than that of the algorithm presented in [48]. The main reason for this is the reduction on the number of switching transitions imposed by the proposed algorithm. If the working conditions are such that the algorithm goes into the Case *a* detailed in Section II, the NP current is adequate but not the optimum to control the NP voltage. Case *a* prioritizes the reduction of the switching frequency over any other feature. Consequently, the dynamic response of the proposed modulation algorithm is slower.

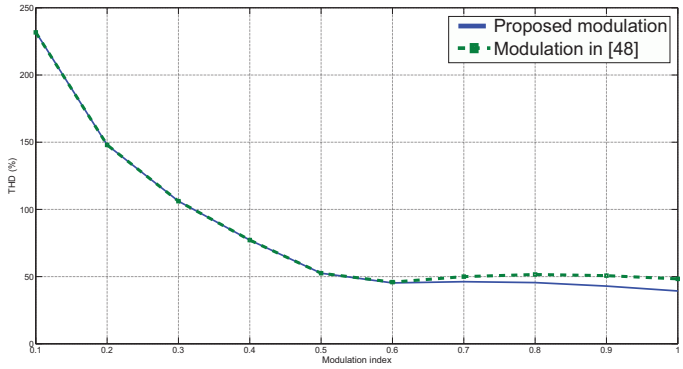
Finally, Table I compares the switching frequencies produced by both modulation strategies. This table shows the switching frequency of the algorithms with respect to the switching frequency of the algorithm introduced in [48] for different load conditions. As it can be observed, the proposed algorithm reduces signif cantly the switching frequency for some operating conditions. In addition, the maximum switching frequency is never higher than that produced by [48] regardless the type of load and working conditions.



(a) Balance load with PF=0.



(b) Balance load with PF=1.



(c) Unbalanced load conditions.

Figure 15. THD of the line-to-line voltage waveforms for different load conditions: (a) balanced load PF=0; (b) balanced load PF=1; (c) unbalanced load.

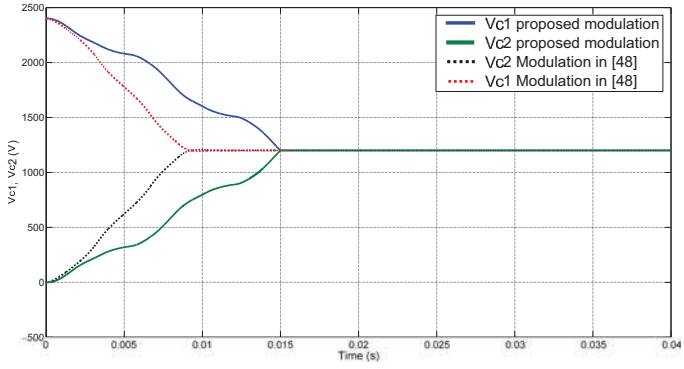


Figure 16. Dinamics of NP voltage balance.

V. Conclusion

This paper has introduced a new PWM algorithm for *n*-phase NPC converters. The algorithm is able to completely remove the low frequency NP voltage oscillations. Consequently, it helps to overcome one of the most important problems of NPC converters. In addition, it avoids the use of linear controllers and it is generalizable to *n*-phase converters with a relatively low effort. Subsequently, it can be implemented on a low cost digital controller. The algorithm provides a good trade-off solution between implementation complexity and performance. Depending on the operating conditions, the WTHD of the generated voltage waveforms take similar values than those with standard CBPWM. The switching frequency of the power devices is higher than with the standard CBPWM, but the proposed modulation strategy is able to cancel the low frequency NP voltage oscillations completely and regulate the two *dc*-link capacitor voltages to the reference value $\left(\frac{v_{dc}}{2}\right)$. This can be achieved for any number of phases of the converter and operating with any kind of load. All these facts qualify the NPC converter with the proposed modulation strategy to be used in active f ltering applications, where the converter has to work with unbalanced and/or nonlinear loads. Additionally, since the low frequency capacitor voltage oscillations can be completely removed, the proposed modulation strategy enables the use of low capacity f lm capacitors in NPC converters.

Appendix A

This appendix demostrates that it is enough to switch a single phase of a three-phase NPC converter between the three voltage levels to achieve an instateneous NP current equal to zero (i_{NP}=0).

Let us suppose the set of three phase voltages given by (1)-(4). At a given instant, v_b is assumed to have the maximum value and v_c the minimum one, i.e. v_{max}= v_b and v_{min}= v_c.

Using (5)-(8) the NP current can be expressed as:

$$\begin{aligned} i_{NP} = i_a \left(1 - \left| v_a - \frac{v_{max}+v_{min}}{2} \right|\right) + \dots \\ i_b \left(1 - \left| v_{max} - \frac{v_{max}+v_{min}}{2} \right|\right) + \dots \\ i_c \left(1 - \left| v_{min} - \frac{v_{max}+v_{min}}{2} \right|\right). \end{aligned} \tag{14}$$

Consequently:

$$\begin{aligned} i_{NP} = i_a \left(1 - \left| v_a - \frac{v_{max}+v_{min}}{2} \right|\right) + \dots \\ i_b \left(1 - \left| \frac{v_{max}-v_{min}}{2} \right|\right) + \dots \\ i_c \left(1 - \left| \frac{v_{min}-v_{max}}{2} \right|\right). \end{aligned} \tag{15}$$

Since i_a+i_b+i_c=0:

$$\begin{aligned} i_{NP} = i_a \left(1 - \left| v_a - \frac{v_{max}+v_{min}}{2} \right|\right) - \\ i_a \left(1 - \left| \frac{v_{min}-v_{max}}{2} \right|\right). \end{aligned} \tag{16}$$

If v_a+v_b+v_c=3v_0, where v_0 is a zero-sequence component included in the reference signals, as follows:

$$v_a = v_{a0} + v_0, \tag{17}$$
$$v_b = v_{b0} + v_0, \tag{18}$$
$$v_c = v_{c0} + v_0, \tag{19}$$

with v_{a0}+v_{b0}+v_{c0}=0, then:

$$i_{NP} = i_a \left(1 - \left|\frac{3v_{a0}}{2}\right|\right) - i_a \left(1 - \left|\frac{2v_{b0} + v_{a0}}{2}\right|\right). \tag{20}$$

Let us def ne d_{NP_a}=$\left(1 - \left|\frac{3v_{a0}}{2}\right|\right)$ and d_{NP_y}=$\left(1 - \left|\frac{2v_{b0}+v_{a0}}{2}\right|\right)$. Since v_b=v_{max}, then v_{b0} will also be the maximum reference signal respect to v_{a0} and v_{c0}. Consequently:

$$3|v_{a0}| < |2v_{b0} + v_{a0}| \longrightarrow d_{NP_a} > d_{NP_y}. \tag{21}$$

Therefore, it is possible to obtain a NP current equal to zero commutating the phase *a* between the three voltage levels.

Appendix B

This appendix demonstrates that obtaining an instantaneous NP current equal to zero in a four-phase NPC converter under unbalanced load conditions sometimes requires two phases to switch between the three voltage levels. This is demonstrated with a numerical example.

Let us suppose the followings set of normalized output voltages with *m*=1:

$$\begin{aligned} v_a &= sin\left(\omega t\right), \\ v_b &= sin\left(\omega t - \frac{\pi}{2}\right), \\ v_c &= sin\left(\omega t + \pi\right), \\ v_d &= sin\left(\omega t + \frac{\pi}{2}\right). \end{aligned} \tag{22}$$

Let us suppose that the converter is connected to an unbalanced load which provides an output current def ned by the following Nyquist sequence [49]:

$$\begin{aligned} i_a &= Isin\left(\omega t + \varphi\right), \\ i_b &= Isin\left(\omega t + \pi + \varphi\right), \\ i_c &= Isin\left(\omega t + \varphi\right), \\ i_d &= Isin\left(\omega t + \pi + \varphi\right). \end{aligned} \tag{23}$$

At *t*=0 v_a=0, v_b=1, v_c=0 and v_d=1. Consequently, d_{NP_b}=d_{NP_d}=0. Therefore, the NP current is calculated as:

$$i_{NP} = d_{NP_a} Isin(\varphi) + d_{NP_c} Isin(\varphi), \tag{24}$$

with d_{NP_a}=(1-|v$_a$|) and d_{NP_c}=(1-|v$_c$|). Consequently, i_{NP}=0 if and only if the NP duty cycle of phase *a* and *c* are forzed to zero. Therefore, these two phases have to switch between the positive and negative *dc*-bus rails at *t*=0.

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