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Molecular doping for control of gate bias stress in organic thin film transistors

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The key active devices of future organic electronic circuits are organic thin film transistors (OTFTs). Reliability of OTFTs remains one of the most challenging obstacles to be overcome for broad commercial applications. In particular, bias stress was identified as the key instability under operation for numerous OTFT devices and interfaces. Despite a multitude of experimental observations, a comprehensive mechanism describing this behavior is still missing. Furthermore, controlled methods to overcome these instabilities are so far lacking. Here, we present the approach to control and significantly alleviate the bias stress effect by using molecular doping at low concentrations. For pentacene and silicon oxide as gate oxide, we are able to reduce the time constant of degradation by three orders of magnitude. The effect of molecular doping on the bias stress behavior is explained in terms of the shift of Fermi Level and, thus, exponentially reduced proton generation at the pentacene/oxide interface. © *2014 AIP Publishing LLC*.
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A continuously driven organic thin film transistor (OTFT) shows a decreasing current between source and drain electrode, I_D, over time. Commonly, this behavior is described by a stretched exponential decay of the threshold voltage, V_T, and explained with a slow charge trapping within the channel—at the gate-insulator interface of the transistor.[1] Therefore, V_T shifts towards the applied value of gate voltage, lowering I_D. The observation of gate bias stress has been reported for widely different material systems,[2–6] such as OTFTs based on silicon oxide (SiO_2),[7,8] organic dielectric layers,[9–11] as well as for thin-film transistors using a-Si:H, poly-Si, and metal-oxide semiconductor materials.[12–16] Equation (1) describes this stretched exponential decay, where $V_{T,max}$ is the maximum threshold shift after infinite time, τ is the time constant, and β is the stretching exponent

$$\Delta V_T = V_{T,\max}\left(1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right). \quad (1)$$

Typical values for τ are in the range of 10^3 s and usually strongly depend on transistor preparation and measurement conditions. In particular, temperature, ambient conditions (humidity),[17] light exposure, and gate voltage were found to have a major impact. Meanwhile, β was observed to be more or less constant in the range of about 0.2 to 0.4.[18] Several fundamentally different underlying mechanisms were proposed to explain bias stress behavior, including: (i) proton generation at the organic/dielectric interface and further migration into the dielectric,[7] (ii) slow trapping of mobile charges,[8] (iii) bipolaron formation mechanism,[10] and (iv) migration of carriers into electronic states of the dielectric.[9]

In particular, for p-type OTFTs with SiO_2 as gate dielectric, the bias stress mechanism of proton generation at the organic/SiO_2 interface and their migration into the bulk of SiO_2 is widely accepted.[18] This mechanism includes two steps that differ in timescale:

(1) Fast (<1 ms) proton generation is governed by the oxygen/water redox couple $4H^+ + O_2 + 4e^- \leftrightarrow 2H_20$, where holes in pentacene (p5+) are in equilibrium with protons on the surface of the SiO_2 in the redox half reaction $p5^+ + e^- \leftrightarrow p5$. The rate of reaction is proportional to $\exp(-E_a/kT)$, where E_a is an activation energy which, according to Bobbert *et al.*, is proportional to the HOMO level of the organic semiconductor.[18] Consequently, the only way to alleviate the bias stress for a given semiconductor and interface would be to minimize the supply of water at the organic/oxide interface. (2) After protons are generated, a slow (>1 s) reversible migration of the protons into the bulk of SiO_2 towards the gate electrode is observed (Figure 1(a)). Mobile protons, located between the accumulation channel and the gate, are thus screening the gate electric field. Therefore, the effective electric field, E_G, in the channel becomes

$$E_G = \frac{V_{GS}}{d} - \frac{n(t)}{\varepsilon\varepsilon_0}, \quad (2)$$

where V_{GS} is the applied gate voltage, e is the elementary charge, $\varepsilon\,\varepsilon_0$ is the dielectric permittivity of the insulator, $n(t)$ is the density of protons, and d is the thickness of the dielectric. Consequently, this screening of the electric field leads to a shift of V_T and a decrease of I_D. The proton migration mechanism has also a characteristic feature, observed in experiments, which is called anomalous bias stress effect.[7] Anomalous bias stress occurs, when the stressing voltage is

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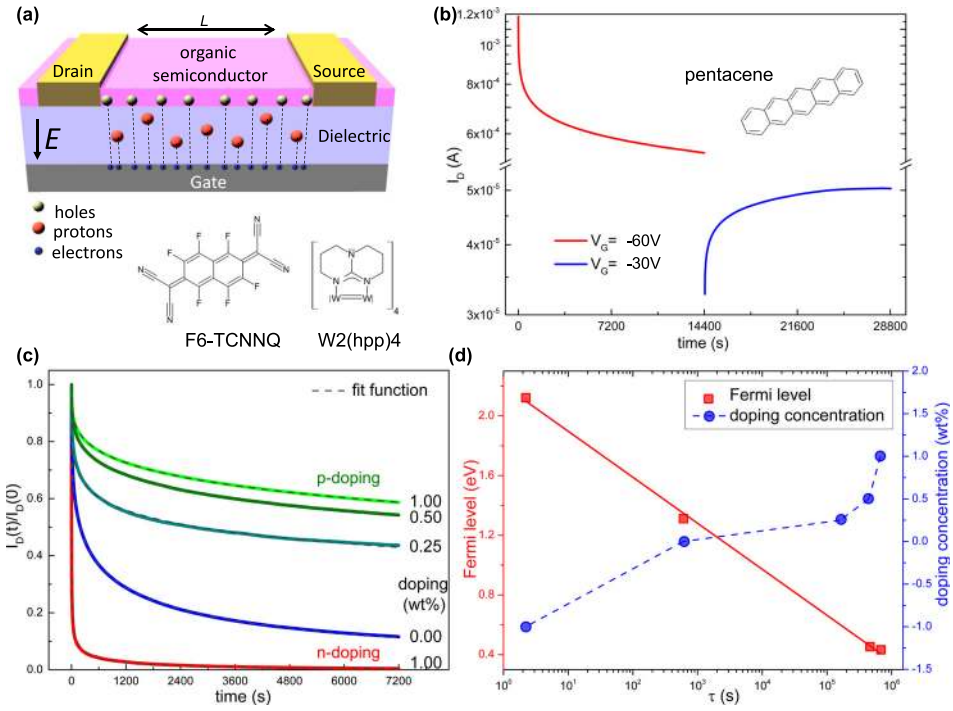

FIG. 1. Experimental observation of influence of molecular doping on bias stress of pentacene based OTFTs. (a) Scheme of the used transistor geometry. The red dots symbolize protons that are diffusing into the dielectric and screening the gate electric field. Furthermore, the chemical structures of the used materials pentacene, F6-TCNNQ, and W2(hpp)4 are shown. (b) Anomalous bias stress of a pentacene transistor p-doped with 0.25 wt. % F6-TCNNQ. The transistor is stressed at $V_{GS} = -60$ V for 4 h before the voltage is reduced to its half. At the reduced voltage, the current starts to increase, as it recovers from the previous stressing period. (c) Time dependent current decrease of p- and n-type doped pentacene transistors. A stretched exponential fit with Eq. (4) for each curve is plotted in dashed lines. (d) Bias stress time constant τ as a function of molecular doping concentration (blue) and, thus, correlated Fermi level (red). The errors of the UPS measurements are estimated to be smaller than 0.05 eV.

reduced to a lower value after a previous stress period. In this case, I_D recovers up to a certain maximum, before it starts to follow the normal bias stress characteristic again.

In this Letter, we report a study of the effect of molecular p- and n-type doping of the OTFT channel on the bias stress behavior. For our experiments, we chose pentacene on SiO_2 as a well-known, high mobility benchmark material. We show that even marginal doping has a very pronounced effect on the bias stress time constant τ and, thus, the reliability of OTFTs.

The general setup of the coplanar transistors is sketched in Figure 1(a). These transistors were prepared on chips of a highly conductive p-doped silicon wafer with a 230 nm thick thermally grown oxide ($C_i = 14.6$ nF/cm^2). On top of the silicon dioxide, interdigitated 30 nm thick Au finger structures were deposited in a lift-off process (Fraunhofer IPMS, Dresden, Germany). As a result, for source and drain electrode, a channel length, L, of 20 μm and a channel width, W, of 10 mm were realized. These chips were cleaned in an ultrasonic bath with acetone, ethanol, and isopropanol for 10 min each and treated with an O_2-plasma for an additional 10 min.[19] Subsequently, the chips were transferred to a UHV evaporation system with a base pressure below 10^{-7} mbar and heated for 30 min at 100 °C. Afterwards, pentacene was evaporated, with a layer thickness of 30 nm. In case of the doped transistors, either the p-dopant 2,2′-(perfluoronaphthalene-2,6-diylidene)dimalononitrile (F6-TCNNQ) or the n-dopant tetrakis(1,3,4,6,7,8-hexahydro-2H-pyrimido[1,2-a] pyrimidinato)ditungsten (W2(hpp)4) (Novaled AG, Dresden, Germany) was coevaporated.[20,21] Here, only the first 10 nm of the pentacene film were doped to avoid poor on/off ration of the OTFTs.[23] Furthermore, in order to keep high mobility of OTFTs, we only used low doping concentrations, since higher concentrations cause a drop of mobility due to the structural changes in the pentacene film.[24] A rotary shutter, described by Tietze *et al.*, was used to ensure high accuracy of the doping concentration.[22] Afterwards, the chips were transferred to a measurement station under nitrogen atmosphere without exposure to air.

Characteristics of transistors were measured with two Keithley source measurement units (SMU), one Keithley 2611A for the source/drain contacts and Keithley 2400 for the gate contact. All measurements were done without illumination of the samples. V_T and charge carrier mobility, μ, were extracted from the transfer characteristic in the saturation regime[25] on the basis of formula (4), with drain current, I_D, gate-source voltage, V_{GS}, channel length, L, channel width, W, and dielectric capacity, C_i

$$I_D = \frac{WC_i\mu}{2L}(V_{GS} - V_T)^2. \tag{3}$$

Actual bias stress measurements were started after the initial characterization and 30 min waiting period that is appropriate for a recovery of the transistor. During the measurement process, constant voltages were applied to drain and gate electrode. The bias stress behavior is often described with the decrease of V_T according to formula (1), but such measurements lead to an interruption of the bias stress for each measurement point. Alternatively, we directly measured current decrease during stress time. Under the condition that V_T will ultimately reach the value of the applied V_{GS} ($V_{T,max} = V_{GS} - V_{T,0}$), I_D will decrease in a similar behavior

$$I_D = I_0 \exp(-2(t/\tau)^{\beta}). \tag{4}$$

The scheme of the studied devices is shown in Figure 1(a). Transistors based on pentacene with doping ratios of 1 wt. %, 0.5 wt. %, and 0.25 wt. % F6-TCNNQ (p-dopant) or 1 wt. % of W2(hpp)4 (n-dopant) are measured and compared to intrinsic pentacene. For intrinsic samples, neither a variation of channel length, L, nor a change in the semiconductor layer thickness shows an influence on the bias stress behavior.

TABLE I. Characteristic parameters of measured bottom-contact transistors.

Doping material	Fermi level (eV)	*I*on/*I*off ratio	μ (cm^2/V s)	τ (s)	β
1.0 wt. % W2(hpp)4	2.12[a]	69 600	0.036	2.21	0.21
0.0 wt. % Intrinsic	1.31[a]	35 200	0.12	605	0.32
0.25 wt. % F6-TCNNQ	N/A	507	0.22	160 000	0.21
0.5 wt. % F6-TCNNQ	0.46[a]	93.6	0.54	442 000	0.27
1.0 wt. % F6-TCNNQ	0.43[a]	49.4	0.20	67 3000	0.28

[a]cf. supplementary material.

This indicates that the observed charging effect happens at the interface or at least close-by in the accumulation channel. Degradation of I_D is found to be reversible. After a certain time of relaxation, correlated to the previous stress time, the initial performance of the transistor is restored. Without a recovery time and subsequently performed stress periods at various gate voltages, the transistors show anomalous behavior as reported by Matters *et al.*[7] (Figure 1(b)). In accordance with literature,[9,18] charge-carrier mobility is not affected during the stress period and remains constant (Table I). Thus, the current decrease is directly connected to a shift of V_T. Hence, we can discuss the typical bias stress behavior without influence of irreversible transistor degradation. Figure 1(c) shows the result of time-dependent current measurements during the applied bias stress. A dashed line illustrates a stretched exponential fit with formula (4). Fitting parameters are listed in Table I. While the stretching parameter β is always in the range of 0.21 to 0.32, the time constant τ is dramatically affected by doping. With p-doping, the bias stress time constant is significantly increased, while n-doping reduces τ by two orders of magnitude.

Since we observe anomalous bias stress in all our experiments, as exemplarily shown for the p-doped transistor (0.25 wt. %) in Figure 1(b), we conclude that proton migration indeed remains the underlying mechanism of the observed bias stress. Thus, we argue that a significant change of τ is caused by a change of the rate of proton generation happening during step (1) of the mechanism described above. Since the entire sample set is prepared under the same conditions, the amount of available water remains the same as well as mobility of ions in the bulk of SiO_2. Therefore, the only possible explanation left is that the proton generation rate is changed. This rate is given by the rate of electrochemical reaction, which in turn depends on the position of the Fermi level (i.e., electrochemical potential) of the doped film. In Figure 1(d), τ is plotted over the molecular doping ratio. The doped pentacene films are investigated on separate substrates via ultraviolet photoelectron spectroscopy (UPS). See supplementary material for the UPS measurement data.[29] These measurements were already published elsewhere[26] and allow an estimation of the Fermi level in the pentacene layer depending on its doping concentration. Within this estimation, an error smaller than 0.05 eV can be assumed. The results are listed in Table I and are also plotted in Figure 1(d) (red squares). From this plot, we can deduce an exponential correlation between Fermi level and τ that supports our explanation.

The disadvantage of p-type doped pentacene transistors is a reduced on/off-ratio, as the doped layer still has a low resistance in the off-state of the transistor. This problem is especially true for the coplanar transistor geometries used here. See supplementary material for the corresponding transfer characteristics. Staggered depletion or inversion transistors[26,27] with only very thin p-type doped channel layers retain the possibility to control the bias stress time constant without influencing the off-current as it was shown in a separate experimental series of pentacene transistors in a staggered geometry on an aluminum oxide as a gate dielectric. See supplementary material for preparation details and bias stress measurement data. In these samples, the doped channel layer is thin enough that the channel can be fully depleted and the transistors can be turned off completely.

As presented, molecular doping is able to control the time constant of the bias stress effect in OTFTs over orders of magnitude. Thus, it can significantly improve device-stability of OTFTs for their application in logic circuits. The processing of doped layers is already established in the OLED industry and can be easily adopted. With the design of staggered transistors having a thin doped layer at the interface to the gate oxide only,[26–28] this effect can be used without a strong disturbance for the normal transistor performance. On the contrary, controlled escalation of bias stress allows investigations for electrical memory device operation mechanisms. However, the relation between bias stress time constant and Fermi level above shown contributes an important argument in the discussion and a deeper understanding of bias stress phenomena, in general.

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