

# Monolayer-level controlled incorporation of nitrogen at Si–SiO<sub>2</sub> interfaces using remote plasma processing

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(Received 1 February 1999; accepted 2 August 1999)

We demonstrate three different ways to incorporate nitrogen at Si–SiO<sub>2</sub> interfaces: (i) an O<sub>2</sub>/He plasma oxidation of the Si surface followed by an N<sub>2</sub>/He plasma nitridation, (ii) an N<sub>2</sub>/He plasma nitridation of the Si surface, and (iii) a Si<sub>3</sub>N<sub>4</sub> film deposition on to the Si surface. The two-step interface formation, the O<sub>2</sub>/He plasma oxidation followed by the N<sub>2</sub>/He plasma nitridation, is shown to yield significantly better interface device properties than the other two approaches. These differences in interface properties are explained by an application of constraint theory based on comparisons of the average bonding coordination of the dielectric layer at the interface with the Si substrate. © 1999 American Vacuum Society. [S0734-2101(99)03806-3]

## I. INTRODUCTION

Incorporation of nitrogen atoms at the Si–SiO<sub>2</sub> interface has been shown to improve metal–oxide–semiconductor field-effect-transistor (MOSFET) device performance and reliability.<sup>1–5</sup> Techniques for the incorporation of nitrogen at the Si–SiO<sub>2</sub> interface fall into six broad categories. These are: (i) interface nitridation by thermal annealing of the SiO<sub>2</sub> in an ammonia (NH<sub>3</sub>),<sup>6,7</sup> nitrous oxide (N<sub>2</sub>O)<sup>8,9</sup> or nitric oxide (NO)<sup>10,11</sup> ambients, (ii) direct thermal oxidation/nitridation of the Si surface in N<sub>2</sub>O<sup>12,13</sup> or NO,<sup>14</sup> (iii) ion implantation of N<sub>2</sub> into the Si substrate followed by the thermal oxidation,<sup>15,16</sup> (iv) N<sub>2</sub>O remote plasma-assisted oxidation/nitridation of the Si surface,<sup>17,18</sup> (v) the N<sub>2</sub>/He remote plasma nitridation technique described in this article, as well as (vi) chemical vapor deposition (CVD) of Si<sub>3</sub>N<sub>4</sub> on to the Si surface. Two important aspects in preparing device quality dielectrics with nitrided interface are (i) “monolayer-level” controlled nitrogen incorporation at the Si–SiO<sub>2</sub> interface, and (ii) creation of a low defect state density and robust (reliable) Si–SiO<sub>2</sub> interface. Using thermal or plasma-assisted oxidation/nitridation of the Si surface in N<sub>2</sub>O or NO source gases, oxide growth and interfacial nitridation processes proceed concurrently and as such it is generally difficult to control independently the oxide thickness  $t_{ox}$  and the degree of nitridation for ultrathin gate oxides ( $t_{ox} < 3$  nm). This is especially true for the high-temperature thermal processing because of potential differences in thermal activation energies for the oxide growth and interfacial nitridation. The focus in this article is on low temperature plasma-assisted processes in which selective excitation of reactive species is controlled by plasma excitation processes.

The IBM group<sup>19–23</sup> developed a low-temperature direct-plasma CVD process for gate dielectric fabrication. This was a two-step process comprised of (i) a plasma oxidation of a

Si surface, which was covered by an approximately 1.0-nm-thick native oxide, followed by (ii) a plasma-assisted SiO<sub>2</sub> deposition from O<sub>2</sub> and SiH<sub>4</sub> at 350 °C. The plasma-assisted deposition was done in a capacitively-coupled reactor in which the O<sub>2</sub> and SiH<sub>4</sub> source gases were heavily diluted ( $> 10^3:1$ ) with He. The total pressure and radio-frequency (rf) power density were respectively  $\sim 1$  Torr and  $0.02–0.04$  W cm<sup>–2</sup>. This process had one major drawback relating to control of interface properties: the  $\sim 1.0$ -nm-thick native oxide was not removed prior to plasma processing so that the Si–SiO<sub>2</sub> interface formed by the plasma oxidation step prior to film deposition required *undercutting* the native oxide. This low temperature process is therefore similar to conventional thermal oxidation where native oxide layers are generally present at the time the Si wafers are inserted into the oxidation furnace. Devices fabricated from dielectrics formed in this way showed good electrical properties, demonstrating the importance of forming the Si–SiO<sub>2</sub> interface prior to the bulk oxide deposition. Finally, this process was not extended to include the incorporation nitrogen at the Si–SiO<sub>2</sub> interface by either replacing the plasma-assisted oxidation with a plasma oxidation/nitridation step using a nitrogen containing oxidant, or by a postoxidation nitridation process.

The SONY group<sup>24–27</sup> deposited SiO<sub>2</sub> films using a parallel-plate plasma CVD reactor with mesh electrodes at 270 °C for thin film transistor (TFT) applications. The oxide thickness was 100 nm, and the interface formed during the plasma deposition step. The deposition rate was  $6$  nm min<sup>–1</sup> at rf power (13.56 MHz) of 5 W. Sano *et al.*<sup>26,27</sup> found that annealing these SiO<sub>2</sub> films in an H<sub>2</sub>O vapor ambient at 270 °C for 30 min efficiently improved the electrical properties, including reductions of the interfacial trap and fixed positive oxide charge densities. The key step was the postoxide deposition anneal in H<sub>2</sub>O vapor. It is likely that this H<sub>2</sub>O anneal oxidized the interface between

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the Si substrate and the plasma-deposited oxide film thereby creating the final device interface, suggesting again that controlled interfacial oxidation is a crucial factor in improved device performance.

Our research group at North Carolina State University has developed a remote plasma process for forming ultrathin gate-dielectrics that has been designed to provide separate and independent control of interface formation. <sup>17,18,28,29</sup> Yasuda *et al.* <sup>28,29</sup> prepared device quality Si–SiO<sub>2</sub> interfaces and bulk oxide films by a three-step process: (i) low-temperature (200–300 °C) remote plasma-assisted O<sub>2</sub>/He oxidation of a hydrogen-terminated Si surface to form the Si–SiO<sub>2</sub> interface (~0.5–0.6 nm of SiO<sub>2</sub>) followed by (ii) a SiO<sub>2</sub> bulk film deposition by remote plasma-enhanced chemical vapor deposition (RPECVD) and finally (iii) a low-temperature (400 °C) postdeposition anneal to reduce the OH concentration in the bulk oxide film. This process sequence was shown to yield a *separate and independent* control of interface formation and bulk film deposition, representing an improvement over the process of Bright *et al.* <sup>23</sup> The three step process of Yasuda *et al.* was applied to capacitors, and demonstrated densities of interface defects,  $D_{it}$ , at midgap determined from capacitance–voltage ( $C-V$ ) measurements in the low  $10^{10}$  cm<sup>-2</sup> range. <sup>28</sup> Lee *et al.* <sup>17,18</sup> demonstrated an alternative low-thermal budget three-step ultrathin oxide dielectrics with nitrided interfaces: (i) an N<sub>2</sub>O/He remotely activated plasma oxidation/nitridation of the Si surface to form and nitrided Si–SiO<sub>2</sub> interface (~0.5–0.6-nm-thick SiO<sub>2</sub>) followed by (ii) a bulk oxide deposition by RPECVD and then (iii) a postoxide deposition rapid thermal anneal at 900 °C for 30 s. The interfacial nitrogen, at a level of approximately one monolayer (~ $7 \times 10^{14}$  cm<sup>-2</sup>) increased the resistance to peak transconductance degradation after hot-carrier stressing of *n*-channel MOSFETs with oxide thicknesses ~5.5 nm by about a factor of 5 with respect to devices with oxide gate dielectrics and no interface nitridation. <sup>18</sup>

In this article, we demonstrate three different ways to incorporate the nitrogen at the Si–SiO<sub>2</sub> interface designated hereafter as processes I–III: (i) process I: an O<sub>2</sub>/He 300 °C plasma oxidation of the Si surface followed by an N<sub>2</sub>/He plasma nitridation, (ii) process II: an N<sub>2</sub>/He 300 °C plasma nitridation of the Si surface, and (iii) process III: a Si<sub>3</sub>N<sub>4</sub> 300 °C RPECVD direct deposition onto the Si surface. After each of these interface formation steps, SiO<sub>2</sub> films are deposited by RPECVD at 300 °C, and the stacked dielectric is annealed at 900 °C in an inert nonoxidizing ambient to complete the dielectric formation process. Using these techniques, we demonstrate *separate and independent* control of the oxide thickness and the amount of nitrogen incorporated at the Si–SiO<sub>2</sub> interface; however, only process I yields device-quality interfaces.

## II. EXPERIMENTAL PROCEDURES

### A. Processing system

Process steps were performed in a multichamber ultrahigh-vacuum (UHV) system, which is shown in Fig. 1,

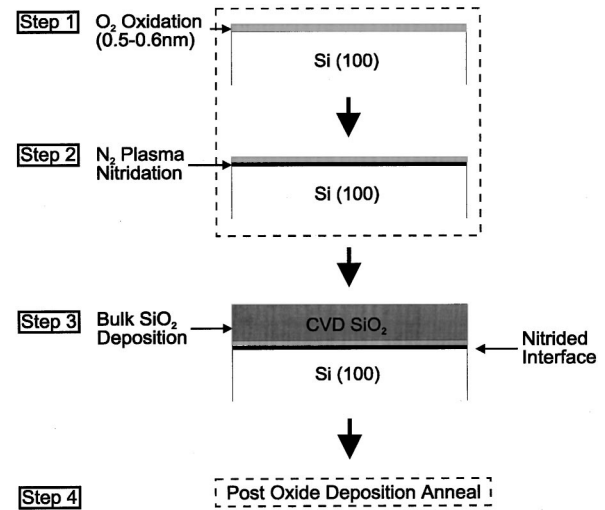


Fig. 1. Process sequence for two-step interface formation (process I): (i) O<sub>2</sub>/He plasma oxidation of Si surface followed by (ii) N<sub>2</sub>/He plasma nitridation at 0.3 Torr, (iii) bulk SiO<sub>2</sub> film deposition, and (iv) postoxide deposition anneal.

and contains: (i) a load-lock chamber, (ii) a remote plasma processing chamber for oxidation, nitridation, and bulk film deposition, (iii) a rapid thermal annealing (RTA) chamber, (iv) a buffer chamber, and (v) a surface analysis chamber with Auger electron spectroscopy (AES). Remote plasma processing<sup>30</sup> offers wide range process capabilities for dielectric applications; oxidation, nitridation, and oxide, nitride and oxynitride alloy deposition (see Fig. 2). There are two ways to implement remote plasma processing; (i) ‘‘UP’’ stream processes in which all process gases go through the plasma tube and are remotely excited by the rf plasma, e.g., O<sub>2</sub>/He for oxidation of Si surfaces and N<sub>2</sub>/He plasma nitridation of Si surfaces and (ii) ‘‘DOWN’’ stream processes in which one, or more of the process gases is injected from a

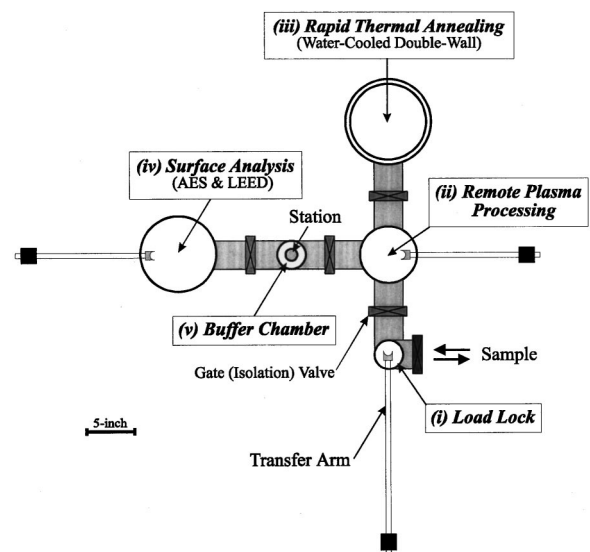


Fig. 2. Top-view of UHV multichamber system: (i) load lock, (ii) remote plasma processing, (iii) rapid thermal annealing, (iv) surface analysis, and (v) buffer chambers.

gas dispersal ring, and therefore are not directly excited by the remote plasma, e.g., SiO<sub>2</sub> deposition and Si<sub>3</sub>N<sub>4</sub> deposition processes in which SiH<sub>4</sub> is injected through the downstream dispersal ring.

The Si(100) substrates used in these studies were prepared by first growing 10 nm of sacrificial oxide on a chemically clean and HF rinsed surface. This was accomplished by dry oxidation in O<sub>2</sub> at 900 °C. Prior to the different nitridation processing steps described below, the sacrificial oxide was removed by rinsing in dilute HF before loading into the system described in Sec. II A.

## B. Nitridation processings

### 1. Process I: O<sub>2</sub>/He plasma oxidation of Si followed by N<sub>2</sub>/He plasma nitridation

This process for incorporation nitrogen at the Si–SiO<sub>2</sub> interface includes two plasma processing steps performed at a substrate temperature of 300 °C: (i) a remotely plasma-assisted O<sub>2</sub>/He oxidation of the Si surface at 300 °C to form a ~0.5–0.6-nm-thick superficial oxide, followed by (ii) a remotely activated N<sub>2</sub>/He plasma nitridation to incorporate the nitrogen atoms at the Si–SiO<sub>2</sub> interface. Figure 1 illustrates this process sequence for interface nitridation. The oxidation (the first step) creates a device quality Si–SiO<sub>2</sub> interface and grows ~0.6 nm of SiO<sub>2</sub>, and the nitridation (the second step) controls the degree of nitrogen at the Si–SiO<sub>2</sub> interface by varying the N<sub>2</sub>/He plasma exposure time. For the oxidation process, an O<sub>2</sub>/He mixture with flow rates of 20 sccm for O<sub>2</sub> and 200 sccm for He is injected through the plasma excitation tube of the processing system (UP stream). The process pressure and rf power at 13.56 MHz were 0.3 Torr and 30 W, respectively. For the nitridation process, the N<sub>2</sub>/He discharge was initiated using flows of 60 sccm N<sub>2</sub> and 160 sccm He; the process pressure was 0.3 Torr; the rf power was 30 W. The bulk SiO<sub>2</sub> layer was formed by RPECVD with 2%-SiH<sub>4</sub> in He and O<sub>2</sub>/He gas mixtures as the respective source gases for Si and O. The O<sub>2</sub>/He mixture was injected through the rf plasma region, but the SiH<sub>4</sub> gas was injected DOWN stream through a showerhead dispersal ring outside of the plasma excitation region. The gas flow rates and process pressure were adjusted to prevent back streaming of the SiH<sub>4</sub> into the plasma generation region of the reactor. The gas flow ratios for O<sub>2</sub>, He, and 2%-SiH<sub>4</sub> in He were, respectively, 20, 200, and 10 sccm. Postoxide deposition annealing was performed in the on-line rapid thermal annealing (RTA) chamber at 0.3 Torr at 900 °C for 30 s in a He ambient. The postoxide deposition anneal reduces chemical and structural strain in the bulk film and at the Si–SiO<sub>2</sub> interface.<sup>31,32</sup> This process sequence can be characterized as an “oxide first” process, whereas processes II and III are each “nitride first” processes.

### 2. Process II: N<sub>2</sub>/He plasma nitridation of Si

This nitride first process sequence uses the second, third, and fourth steps that have been described in the preceding section to achieve a nitrided interface; i.e., the N<sub>2</sub>/He plasma-assisted nitridation at 300 °C, bulk SiO<sub>2</sub> deposition

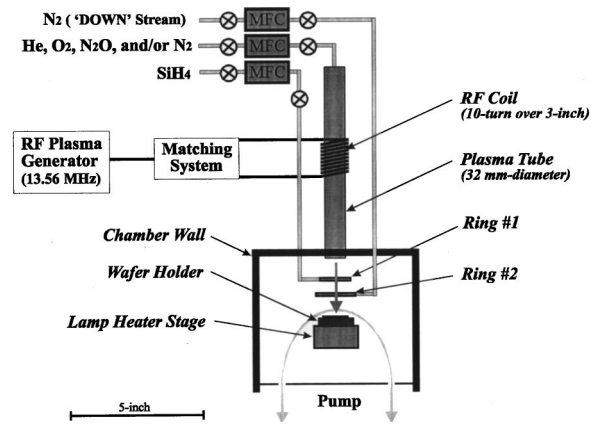


Fig. 3. Cross-sectional view of remote plasma processing chamber.

at 300 °C, and RTA at 900 °C. Specifically, this process is a remote plasma nitridation of the Si surface, and does not involve an oxidation step prior to the nitridation.

### 3. Process III: Si<sub>3</sub>N<sub>4</sub> film deposition on Si

A third way to confine nitrogen at the Si–SiO<sub>2</sub> interface is two-step nitride first deposition process sequence: (i) a thin Si<sub>3</sub>N<sub>4</sub> deposition by RPECVD directly onto the Si substrate, followed by (ii) a bulk SiO<sub>2</sub> deposition by RPECVD onto the deposited nitride interfacial layer (Fig. 3). Both process temperatures were 300 °C. For the Si<sub>3</sub>N<sub>4</sub> deposition,<sup>33</sup> the flow rates for N<sub>2</sub>, He, and 2%-SiH<sub>4</sub> in He were 60, 200, and 10 sccm, respectively. For the SiO<sub>2</sub> deposition, the flow rates for O<sub>2</sub>, He, and 2%-SiH<sub>4</sub> in He were 20, 200, and 10 sccm, respectively. As in process II, the 2%-SiH<sub>4</sub> in He was injected DOWN stream from the plasma region through a showerhead injector, and the other process gases were injected UP stream through the plasma tube and subjected to direct plasma excitations. Both depositions were performed at an rf power of 30 W. The process pressures were 0.2 and 0.3 Torr, for the Si<sub>3</sub>N<sub>4</sub> and SiO<sub>2</sub> depositions, respectively. Postdeposition annealing was carried out in the on-line RTA chamber at 900 °C at 0.3 Torr for 30 s in He ambient.

## C. Interface analysis

The substrates used in these studies were 50-mm-diam *n*-type (phosphorus doped) Si(100) with a resistivity of 0.02–0.045 Ω cm (~5 × 10<sup>17</sup> cm<sup>-3</sup>). For each of the processes discussed below the Si substrate preparation was the same. After a conventional wet chemical RCA clean, a 10-nm-thick sacrificial oxide was grown in dry O<sub>2</sub> in a conventional thermal furnace at 900 °C. Immediately before loading the sample into the multichamber processing system, the sacrificial oxide was removed by etching in a dilute HF (1 wt %) solution, rinsed in a running distilled (DI) water for 20 s, and then dried in flowing N<sub>2</sub>.

AES was performed in the on-line analysis chamber of the multichamber system to quantify the initial stages of oxidation/nitridation of the Si surface using a 3 keV electron beam. Secondary ion mass spectrometry (SIMS) analyses



were done at Evans East, NJ, using  $\text{CsN}^+$  ions for depth profiling of the interfacial nitrogen. Nuclear reaction analysis (NRA) was carried out at the IBM T.J. Watson Research Center, NY, for nitrogen concentration calibration.<sup>34</sup>

#### D. Device fabrication and electrical characterization

For device fabrication and electrical characterization studies, the substrates were 50-mm-diam phosphorus-doped *n*-type Si(100) with a resistivity of 0.02–0.045  $\Omega\text{ cm}$  ( $\sim 5 \times 10^{17}\text{ cm}^{-3}$ ) and boron-doped *p*-type Si(100) with a resistivity of 0.05–0.07  $\Omega\text{ cm}$  ( $\sim 5 \times 10^{17}\text{ cm}^{-3}$ ). The use of heavily doped Si wafers reduces spreading resistance and thereby minimizes parasitic series resistance, and accompanying voltage drops in the bulk Si. MOS capacitors with field oxide isolation structures were made on Si(100) wafers using conventional photolithography processes. All devices studied have an area of  $10^{-4}\text{ cm}^2$ , i.e., the linear dimensions of these devices were 100  $\mu\text{m}$  by 100  $\mu\text{m}$ .

For the electrical characterization, (i) gate currents or current density versus gate voltages ( $I-V$  or  $J-V$ ) characteristics and (ii) capacitance versus gate voltage ( $C-V$ ) characteristics were measured. The  $C-V$  measurements were used to determine an equivalent oxide thickness, and to estimate densities of interfacial defects, both interface traps,  $D_{it}$ , and fixed positive charge. For the  $I-V$  or  $J-V$  measurements, the gate electrode was biased positively (substrate injection mode) for the *n*-type Si in order to maintain the substrate in an accumulation state.

### III. RESULTS

#### A. Process I: $\text{O}_2/\text{He}$ plasma oxidation of Si followed by $\text{N}_2/\text{He}$ plasma nitridation

Interfacial oxidation/nitridation of the Si surface produces a device quality interface using  $\text{O}_2/\text{He}$  remote plasma oxidation process<sup>28</sup> and then incorporates nitrogen at the Si–SiO<sub>2</sub> interface using the  $\text{N}_2/\text{He}$  remote plasma nitridation at 0.3 Torr. The first step,  $\text{O}_2/\text{He}$  plasma-assisted oxidation process has three functions; it (i) removes carbon contamination from the Si surface,<sup>17,28</sup> (ii) creates a device quality Si–SiO<sub>2</sub> interface, and (iii) grows  $\sim 0.5$ – $0.6\text{ nm}$  of SiO<sub>2</sub> as shown in Fig. 4. Figure 4 (i) shows a differential AES spectrum from the Si substrate after the RCA clean, that reveals an  $\sim 0.7$ -nm-thick chemical oxide and carbon contamination ( $\text{C}_{\text{KLL}}$  feature at  $\sim 272\text{ eV}$ ) on the Si. This chemical oxide was removed using a 1 weight (wt) % HF:H<sub>2</sub>O solution, which did not completely remove the carbon contamination, see Fig. 4 (ii). Additionally, the carbon contamination did not disappear following heating to 300 °C in the UHV-compatible chamber as shown in Fig. 4 (iii). However as shown in Fig. 4 (iv), the  $\text{O}_2/\text{He}$  plasma reduced the carbon contamination level, consistent with the results presented in Refs. 17 and 28. If residual carbon was at the Si–SiO<sub>2</sub> interface at a level  $> \sim 0.5\text{ at. \%}$ , then it would be observable by AES since the oxide thickness of  $\sim 0.5\text{ nm}$  is less than the electron escape depth of the electrons associated with the  $\text{C}_{\text{L}_{\text{VV}}}$  Auger feature ( $\sim 1\text{ nm}$ ). Therefore it is concluded that

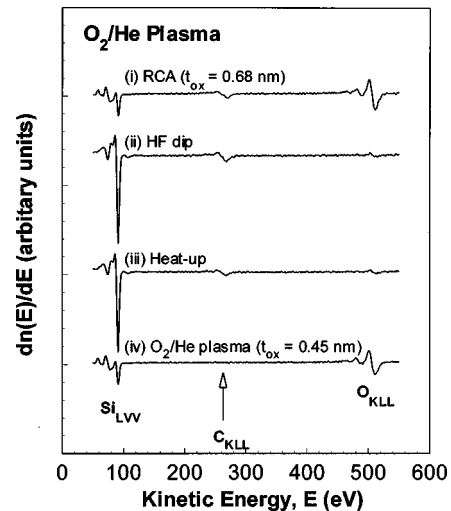


Fig. 4. On-line differential AES spectra of Si surfaces after (i) RCA clean, (ii) rinse in 1 wt % of HF, (iii) 300 °C heating for 10 min in UHV system, and (iv) a 5 s  $\text{O}_2/\text{He}$  plasma oxidation of Si surface. The electron beam energy was 3 keV.

the  $\text{O}_2/\text{He}$  plasma removed carbon contamination from the Si surface (Si–SiO<sub>2</sub> interface) to the level of AES detection limit,  $\sim 0.5\text{ at. \%}$ , and formed a superficial SiO<sub>2</sub> layer on the Si.

The second step,  $\text{N}_2/\text{He}$  plasma nitridation of the superficial oxide was studied using on-line AES. Figure 5 shows differential AES spectra for (i) 15 s  $\text{O}_2/\text{He}$  plasma oxidation of the Si surface followed by (ii)–(v)  $\text{N}_2/\text{He}$  plasma nitridation treatments ranging from 30 to 120 s. The incorporation of nitrogen atoms is reflected in the evolution of  $\text{N}_{\text{KLL}}$  AES peak at  $\sim 379\text{ eV}$ . The intensity of  $\text{N}_{\text{KLL}}$  increased monotonically as the exposure time to the  $\text{N}_2/\text{He}$  plasma postoxidation treatment was increased. This demonstrated that longer ex-

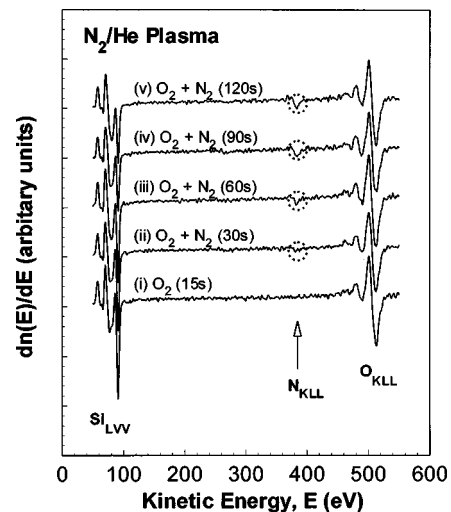


Fig. 5. On-line AES spectra using a 3 keV electron beam. Differential spectra are after (i) a 15 s  $\text{O}_2/\text{He}$  plasma oxidation of Si surface followed by (ii)–(v)  $\text{N}_2/\text{He}$  plasma nitridation of the superficial oxide for 30, 60, 90, and 120 s, respectively.

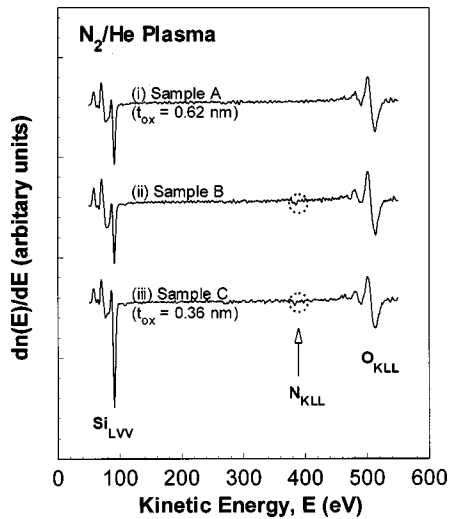


FIG. 6. On-line differential AES spectra using a 3 keV electron beam. Differential spectra are after (i) a 15 s  $O_2/He$  plasma oxidation of Si surface (sample A) followed by (ii) 60 s  $N_2/He$  plasma postoxidation nitridation (sample B), and (iii) *ex situ* HF dip and on-line RTA at 900 °C (sample C).

posure times resulted in increased nitrogen incorporation either at the Si–SiO<sub>2</sub> interface or in the bulk of  $\sim 0.6$ -nm-thick oxide layer.

The following experiments established that the nitrogen incorporation was at the Si–SiO<sub>2</sub> interface; i.e., at the metallurgical boundary between the Si substrate and the SiO<sub>2</sub> layer. The top AES trace in Fig. 6 (sample A) is after 15 s  $O_2/He$  plasma oxidation of the Si surface which formed an  $\sim 0.6$ -nm-thick oxide. There is no detectable  $N_{KLL}$  feature at  $\sim 379$  eV. Following the 60 s  $N_2/He$  plasma exposure produced a weak  $N_{KLL}$  feature as is evident in the middle AES trace in Fig. 6 (sample B). The wafer was then removed from the UHV system, etched in a very dilute HF (0.5 wt %) to remove most of the thin oxide layer. The sample was reinserted into the UHV system, annealed in He at 900 °C for 30 s in the on-line RTA module, and then analyzed again using the on-line AES. The AES spectrum is shown in the bottom trace of Fig. 6 (sample C). A comparison between the Si–O (at  $\sim 76$  eV) and Si–Si (at  $\sim 91$  eV) traces of the  $Si_{LVV}$  AES spectra between the middle and lower traces of Fig. 6 shows the oxide thickness is significantly reduced by the *ex situ* HF etching from  $\sim 0.6$  nm to less than 0.4 nm; however, the weak  $N_{KLL}$  feature remains almost unchanged. This establishes that the post oxidation nitridation processing introduces nitrogen atoms at the Si–SiO<sub>2</sub> interface.

SIMS analyses have been used to quantify the nitrogen content at the interface. Four samples with different nitridation times from 30 to 120 s were studied. Each sample was subjected to (i) 15 s  $O_2/He$  plasma oxidation followed by interface nitridation, (ii) bulk oxide deposition by RPECVD ( $\sim 7.0$  nm thick) followed by (iii) on-line 900 °C postoxide deposition anneal. Based on a standard reference sample at Evans East, NJ, the interfacial nitrogen concentration (areal density) has been determined by integration of the SIMS depth profile. This demonstrated that the 90 s  $N_2/He$  nitridation incorporated approximately one monolayer of nitrogen

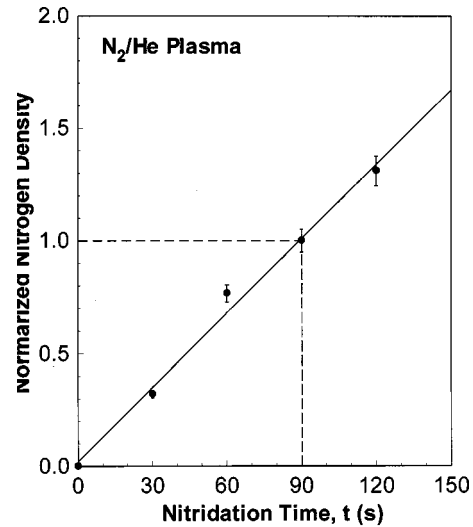


FIG. 7. Normalized areal density determined from SIMS data with respect to the 90 s nitridation as a function of nitridation time. One monolayer of nitrogen ( $\sim 7 \pm 1 \times 10^{14} \text{ cm}^{-2}$ ) was achieved at an exposure time of 90 s.

( $\sim 7 \pm 1 \times 10^{14} \text{ cm}^{-2}$ ) at the interface. NRA studies supported the SIMS analysis and data reduction by showing that the 90 s  $N_2/He$  plasma nitrogen process incorporated  $\sim 8.4 \pm 1 \times 10^{14} \text{ cm}^{-2}$  nitrogen atoms at the interface.<sup>34</sup> Figure 7 presents the normalized integrated areal densities with respect to the 90 s nitridation data as a function of nitridation time, which show interfacial nitrogen concentration increased linearly with nitrogen plasma exposure time.

This interfacial nitridation process has been used in the fabrication of MOS capacitors with thickness range from 4.5 (FN tunneling region) down to 2.0 nm thick (direct tunneling region) on *n*-Si(100) substrates using aluminum (Al) gate electrodes. Figure 6 includes a series of  $J$ – $V$  traces for devices with Al gate electrodes and a 4.5-nm-thick gate oxide on *n*-Si(100) wafers. The gate electrode was biased positively so that gate current flowed from the substrate to the gate electrode in the so-called *substrate injection* mode. The sequence of traces in this figure demonstrates the effect of the interfacial nitrogen is to reduce the tunneling current in the FN region (Fig. 8). This reduction is not due to an oxide thickness change and/or a flat band voltage shift that results from incorporation of nitrogen at the Si–SiO<sub>2</sub> interface. Figure 9 displays that high frequency and quasistatic  $C$ – $V$  measurements for devices fabricated: (i) without interface nitridation, and (ii) with the 90 s  $N_2/He$  plasma nitridation processes. The two  $C$ – $V$  curves were essentially identical. This means that the effective oxide thickness and flat band voltage are the same with and without the interfacial nitrogen. Therefore, the leakage current reductions in the FN region are not due to differences in the oxide thickness or flat band voltage shifts. In this regard, it is important to note that interfacial nitridation would not change the physical thickness of the dielectrics by more than 0.1 nm, which falls within the uncertainty of the capacitance determination of oxide equivalent dielectric thickness. A model calculation showed that a 0.1 nm difference in physical thickness cannot account

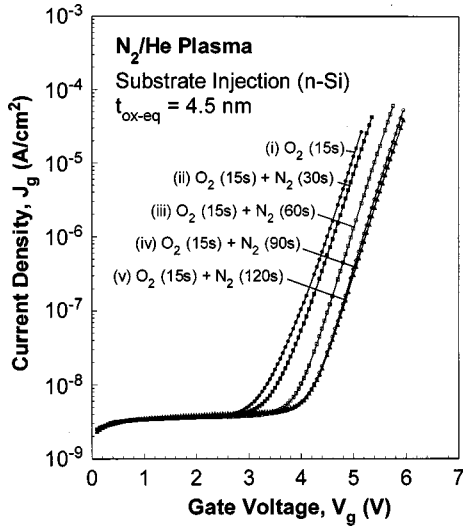


FIG. 8. Substrate injection mode (gate-electrode biased positively)  $J-V$  traces for devices with 4.5-nm-thick gate oxides on  $n$ -Si(100). These traces demonstrate the effect of increasing interfacial nitrogen up the one monolayer level in reducing tunnel currents in the FN regime. The gate electrode was Al.

for the differences in current between the first and last two traces in Fig. 4. In addition, the positions of the flat band voltage, with respect to each other, as well as their absolute positions are consistent with fixed positive charge densities  $< 10^{11} \text{ cm}^{-2}$ , independent of the interface nitridation.

**B. Process II:  $N_2/He$  plasma nitridation of Si**

This is a direct nitridation of the Si surface using a remotely activated  $N_2/He$  plasma. Figure 10 shows initial stages of the  $N_2/He$  plasma nitridation of the Si surface as studied by on-line AES. The oxygen AES features (at  $\sim 510 \text{ eV}$ ) was not observed. The oxygen contamination was well

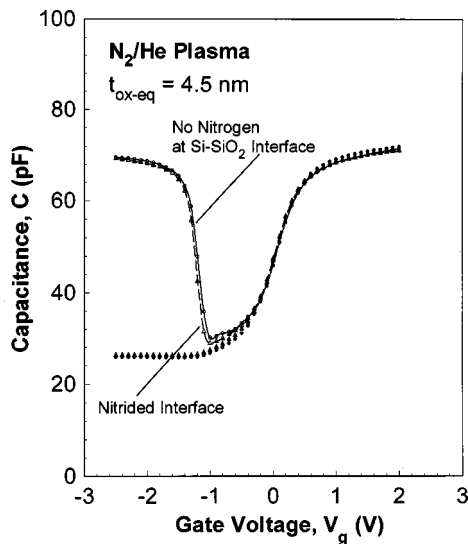


FIG. 9. High-frequency (1 MHz) and quasistatic  $C-V$  measurements of devices in Fig. 8 with (i) without nitridation (no nitrogen at interface), and (ii) with a 90 s nitridation process. The gate electrode was Al.

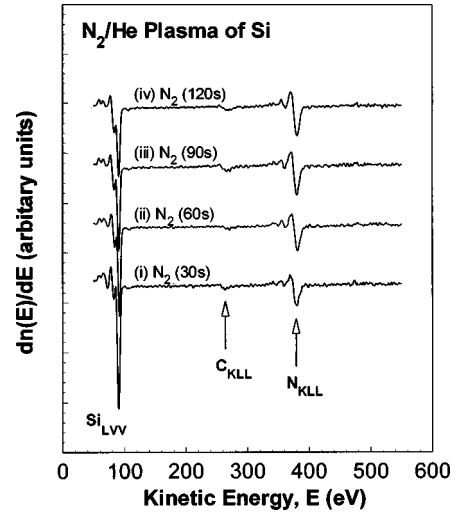


FIG. 10. On-line differential AES spectra using a 3 keV electron beam following  $N_2/He$  plasma nitridation of a Si surface for (i) 30, (ii) 60, (iii) 90, and (iv) 120 s. This is for a *direct* nitridation of Si surface using a *remotely* activated  $N_2/He$  plasma.

below the AES detection limit ( $\sim 0.5 \text{ at. } \%$ ). However, a carbon AES feature at  $\sim 272 \text{ eV}$  was observed. This means, unlike the  $O_2/He$  plasma process, the  $N_2/He$  plasma nitridation was not effective in removing carbon contamination from the Si surface, see Fig. 5 for this comparison.

Using this AES intensity ratio and the following equation, we can then estimate a thickness of nitrided layer on the Si surface:

$$t_{SiN} = \lambda \ln \left( 1 + \frac{I_{Si-Si}^o}{I_{Si-N}^o} \frac{I_{Si-N}}{I_{Si-Si}} \right), \tag{1}$$

where,  $t_{SiN}$ =nitride thickness (nm),  $\lambda$ =electron escape depth (attenuation length);  $\sim 0.6 \text{ nm}$ ,  $I_{Si-N}^o$ =Si-N signal from a thick  $Si_3N_4$  surface (reference sample),  $I_{Si-Si}^o$ =Si-Si signal from a clean Si surface (reference sample),  $I_{Si-Si}$ = $Si_{LVV}$  substrate signal at  $\sim 91 \text{ eV}$  from a thin nitride on the Si and  $I_{Si-N}$ = $Si_{LVV}$  nitrogen shifted signal at  $\sim 83 \text{ eV}$  from a thin nitride on the Si. Figure 11 shows the thickness of the nitride layer,  $t_{SiN}$ , as a function of nitridation time. The nitridation rate is initially fast and then tends to saturate. This indicates that the thin nitrided layer on the Si prevents the further nitridation of the Si surface so that the process is in effect self-limiting. The nitride thickness is fit by the following relationship for first-order reaction kinetics:

$$t_{SiN} = 0.69 \{ 1 - \exp(-0.011 t_N) \} \text{ (nm)}, \tag{2}$$

where,  $t_{SiN}$ =nitride thickness (nm) and  $t_N$ =nitridation time (min). The prefactor term (in nm) is equivalent to approximately 1.5 molecular layers of  $Si_3N_4$ , and the exponential prefactor term, 0.011 (in min) is the inverse of the effective rate constant for the formation of the nitride layer. This fit first-order kinetics suggests that the nitridation process slows down considerably after about one to two monolayers of nitride are formed on the Si substrate.

We have analyzed the SIMS data to determine the interfacial nitrogen areal density. We prepared four samples with

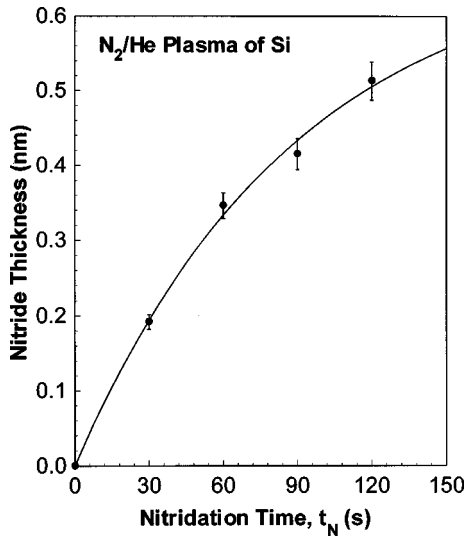


FIG. 11. Thickness of the nitrided layer in Fig. 10 as a function of  $N_2/He$  plasma exposure time.

different  $N_2/He$  plasma nitridation times from 30 to 120 s, and completed the test structures with the REPCVD deposition of  $\sim 7.0$ -nm-thick bulk oxide film followed by  $900^\circ C$  postoxide deposition on-line anneal in an inert ambient. Figure 12 displays the nitrogen SIMS depth profile using  $CsN^+$  ions which shows that as the  $N_2/He$  plasma exposure time was increased, the peak concentration of nitrogen at the Si– $SiO_2$  interface was increased. Using this SIMS data and the standard sample at Evans East, NJ, the equivalent areal density of nitrogen atoms at the interface is calculated. Figure 13 compares the areal density of (i) process II, the direct  $N_2/He$  plasma nitridation of the Si surface for 30–120 s and (ii) process I, the two-step interface formation, the  $O_2/He$  plasma oxidation of the Si surface followed by the  $N_2/He$  plasma nitridation for 45 and 90 s data. For the process we

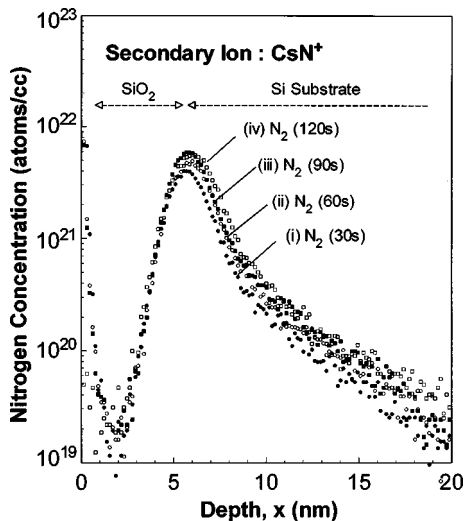


FIG. 12. SIMS depth profiles of four different interfacial nitridation times; (i) 30, (ii) 60, (iii) 90, and (iv) 120 s. Total oxide thickness was  $\sim 6$  nm. The secondary ions for SIMS detection were  $CsN^+$ .

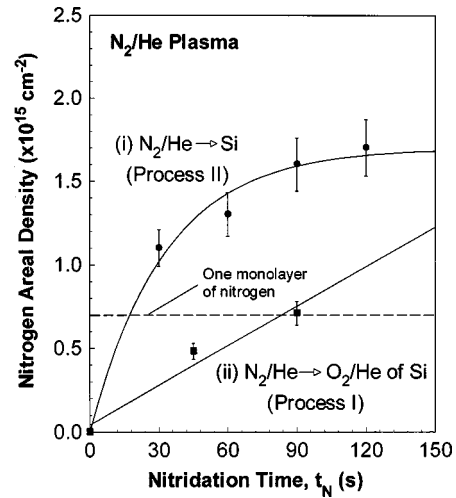


FIG. 13. Comparisons of areal density from SIMS data vs time for (i)  $N_2/He$  plasma nitridation of Si surface (process II) and (ii) two-step interface formation process of  $O_2/He$  plasma oxidation of Si surface followed by  $N_2/He$  plasma nitridation (process I).

have designated as process I, i.e., the two-step interface process, the areal density increased linearly with nitridation time (see Fig. 7), whereas for the direct  $N_2/He$  nitridation of the Si, the process we have designated as process II, the nitrogen areal density at the interface exhibited a saturation behavior due to a self-limiting process for nitride layer growth. The interfacial nitrogen incorporation of the direct nitridation process (process II) is faster and incorporates more nitrogen initially than the two-step interface formation process (process I), and then tends to saturate after the formation of about one to two monolayers are formed.

We have fabricated the MOS capacitors for the electrical characterization of this direct interfacial nitridation processing. The test devices structures were prepared in the following way: test device (i):  $O_2/He$  plasma oxidation of the Si+REPCVD  $SiO_2$  deposition from  $O_2/He$  and  $SiH_4$ , test device (ii): 30 s  $N_2/He$  nitridation of the Si+REPCVD  $SiO_2$  from  $O_2/He$  and  $SiH_4$  and test device (iii): 90 s  $N_2/He$  nitridation of the Si+REPCVD  $SiO_2$  from  $O_2/He$  and  $SiH_4$ . The total equivalent oxide thickness, as determined from  $C-V$  measurements, was  $3.8 \pm 0.1$  nm for all samples. All samples were subjected to on-line postoxide deposition anneal at  $900^\circ C$  at 0.3 Torr for 30 s in He ambient.

Similar to the two-step interface formation (process I), which was demonstrated to reduce tunneling in the FN regime (see Fig. 8), a reduction of tunnel current in the FN regime was also observed for the devices with the nitrided interfaces. Figure 14 displays current density plotted as function of gate voltage for (i) no nitrogen atoms at the Si– $SiO_2$  interface, (ii)  $\sim 1.1 \times 10^{15} \text{ cm}^{-2}$  nitrogen in the interfacial nitride layer, and (iii)  $\sim 1.6 \times 10^{15} \text{ cm}^{-2}$  nitrogen in the interfacial nitride layer. However, as more nitrogen was incorporated in the interfacial layer, there was a large flat band voltage shift in the negative direction, as determined from  $C-V$  data. Figure 15 shows the flat band voltage for (i) a reference oxide sample with no nitrogen at the interface, and

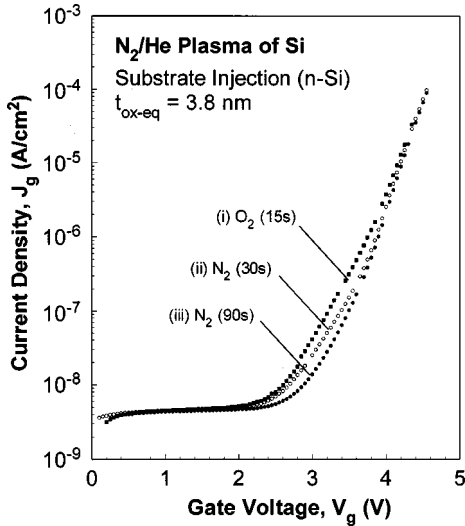


FIG. 14. Substrate injection mode (gate-electrode biased positively)  $J-V$  traces for 3.8-nm-thick gate oxide on  $n$ -Si(100). These are plotted as a function of gate voltage. These traces demonstrate the effects of interfacial nitrogen reducing tunnel currents in the FN region. The gate electrode was Al.

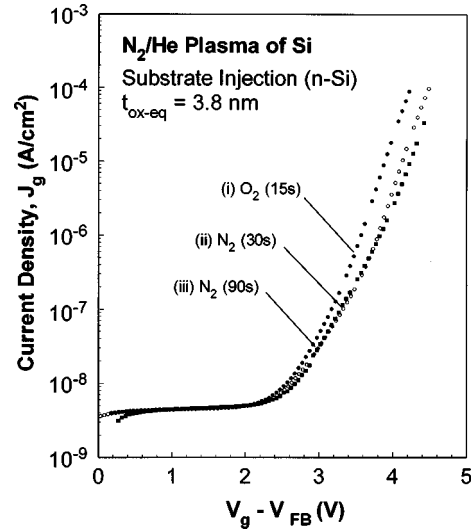


FIG. 16.  $J$  vs  $(V_g - V_{fb})$  traces in the substrate injection mode for devices with for (i) no nitrogen at interface, (ii) 30 s and (iii) 90 s direct interfacial nitridation. The equivalent oxide (electrical) thickness was 3.8 nm for all three samples. Gate electrode was Al.

for two samples with interface nitridation time of (ii) 30 s and (iii) and 90 s. Figure 16 replots the FN region tunneling currents versus gate voltage minus flat band voltage ( $V_g - V_{fb}$ ). Although some reduction in FN tunneling current was observed as function of increasing  $(V_g - V_{fb})$ , the reductions of tunneling current for this direct nitridation process were not as large as compared with those of the two-step interface formation process (process I).

**C. Process III:  $Si_3N_4$  film deposition directly onto Si**

The third technique for interfacial nitridation is a direct deposition by 300 °C RPECVD of a  $Si_3N_4$  film onto the Si surface. Figure 17 shows AES traces for initial stages of

$Si_3N_4$  deposition on the Si surface. Similar to the direct  $N_2/He$  plasma nitridation of the Si surface (process II), the  $Si_3N_4$  deposition process was not effective in removing carbon contamination from the Si surface as evidenced by the  $C_{KLL}$  AES feature is at  $\sim 272$  eV. After a 180 s deposition, the  $C_{KLL}$  Auger signal was no longer observed; however, this is attributed to the carbon being buried at the  $Si_3N_4/Si$  interface. As shown in Fig. 17, after 180 s of deposition, the nitride layer thickness was larger than the AES electron escape depth for electrons from the  $Si_{LVV}$  transitions. In addition, the signal associated with  $C_{KLL}$  AES electrons was significantly attenuated. Using these Auger intensities and Eq. (1), the nitride layer thickness has been determined. Figure 18 illustrates that the nitride thickness increased as linear

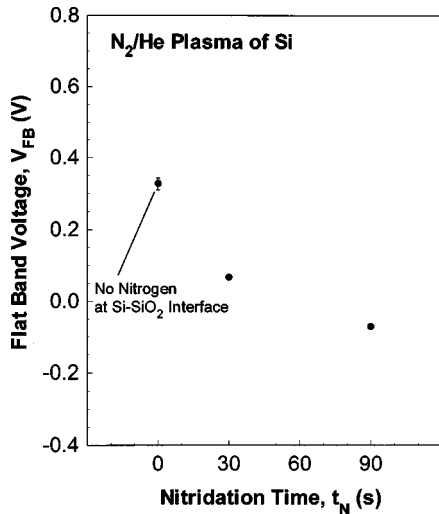


FIG. 15. Flat band voltage shift as a function of interfacial nitridation time. The flat band voltage was determined by analysis of high frequency  $C-V$  data. The gate electrode was Al.

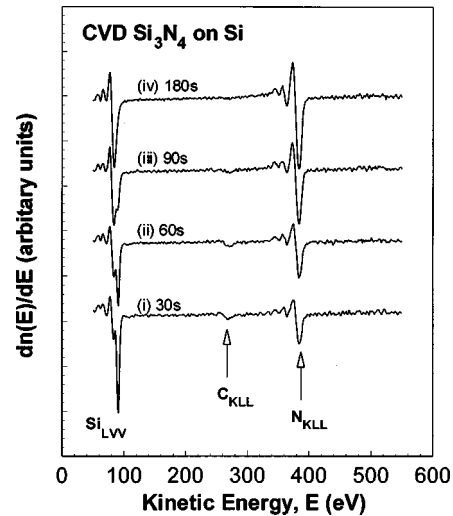


FIG. 17. On-line differential AES spectra using a 3 keV electron beam. The spectra are  $Si_3N_4$  thin film depositions onto a Si surface. Deposition times were (i) 30, (ii) 60, (iii) 90, and (iv) 180 s.



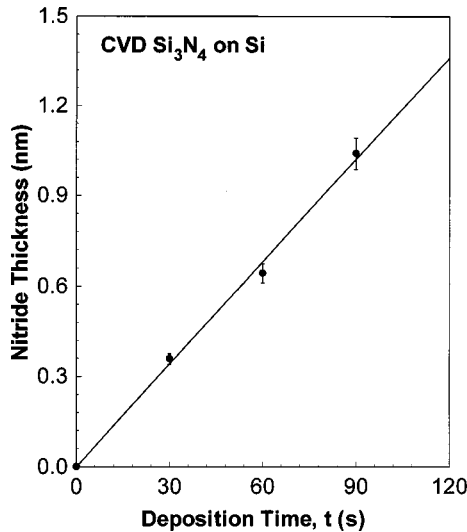


FIG. 18. Thickness of deposited nitride layer in Fig. 17 as a function of deposition time.

function deposition time as expected for deposition process. The thickness of one molecular  $\text{Si}_3\text{N}_4$  is approximately 0.42 nm, as estimated from the density of  $\text{Si}_3\text{N}_4$ , so that a 60 s deposition forms approximately 1.4 molecular layers of silicon nitride.

MOS capacitors were fabricated and used for electrical characterization. The test devices included the following dielectric structures: test device (i):  $\text{O}_2/\text{He}$  plasma oxidation of the  $\text{Si}+300^\circ\text{C}$  RPECVD  $\text{SiO}_2$  deposition from  $\text{O}_2/\text{He}$  and  $\text{SiH}_4$ , test device (ii):  $\sim$ one molecular layer of deposited  $\text{Si}_3\text{N}_4$  ( $\sim$ 0.4 nm) on the  $\text{Si}+300^\circ\text{C}$  RPECVD  $\text{SiO}_2$  from  $\text{O}_2/\text{He}$  and  $\text{SiH}_4$  and test device (iii):  $\sim$ two molecular layers  $\text{Si}_3\text{N}_4$  ( $\sim$ 0.8 nm) on the  $\text{Si}+300^\circ\text{C}$  RPECVD  $\text{SiO}_2$  from  $\text{O}_2/\text{He}$  and  $\text{SiH}_4$ . All of the stacked dielectrics were annealed at  $900^\circ\text{C}$  at 0.3 Torr for 30 s in He in the on-line RTA chamber. The total “equivalent” oxide thickness was maintained  $\sim 4.3 \pm 0.1$  nm for all samples as determined from  $C-V$  measurements. This was achieved by systematically varying the thickness of the deposited oxide layers. Assuming that the dielectric constant of the nitride layer is approximately twice that as  $\text{SiO}_2$ , this means that the nominal “physical” thicknesses of the dielectric layers in these devices were: test device (i) 4.3 nm, test device (ii) 4.5 nm, and test device (iii) 4.7 nm. The deposition time for the  $\text{SiO}_2$  was adjusted to compensate for the nitride layer thickness, so that test device (iii) had the shortest  $\text{SiO}_2$  deposition time.

Figure 19 shows high-frequency  $C-V$  traces for the three samples in both sweep directions, i.e., from accumulation to depletion and back to accumulation. Due to the fast sweeping gate bias, the  $C-V$  traces exhibited a deep depletion effect. The depletion layer width becomes wider than in thermal equilibrium and the capacitance decreases below its thermal equilibrium saturation value.<sup>35,36</sup> No hysteresis effects were observed in the steep part of the  $C-V$  trace, indicating a relative low density of slow oxide or interface traps. However, we did observe a large negative flat band voltage shift that increased with increasing interfacial  $\text{Si}_3\text{N}_4$  layer thick-

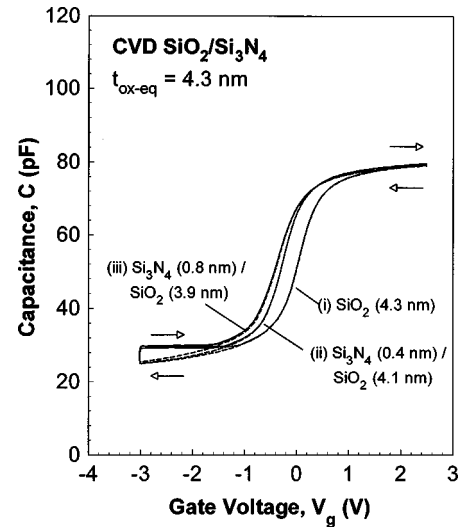


FIG. 19. High-frequency (1 MHz)  $C-V$  traces (in both directions) for devices with (i) no nitrogen, (ii) one and (iii) two molecular layers of  $\text{Si}_3\text{N}_4$  at the interface. The equivalent oxide (electrical) thickness was 4.3 nm for all samples. The gate electrode was Al, and the arrows indicate the sweep directions.

ness. Figure 20 plots the flat band voltage as a function of the thickness of the interfacial  $\text{Si}_3\text{N}_4$  layer. The 0.4- and 0.8-nm-thick  $\text{Si}_3\text{N}_4$  layers correspond respectively to approximately one- and two-molecular layers of  $\text{Si}_3\text{N}_4$  at the interface. Unlike the two-step interfacial oxidation/nitridation (process I), the interfacial deposited  $\text{Si}_3\text{N}_4$  layer produced a large flat band voltage shift indicating a high density of fixed positive charge,  $\sim 10^{12} \text{ cm}^{-2}$ .

Reductions in tunnel current were also observed when one- to two-molecular layers of  $\text{Si}_3\text{N}_4$  were interposed between the Si substrate and the deposited thick  $\text{SiO}_2$ . Figure 21 shows current density versus gate voltage-flat band voltage traces for the three test devices identified above with an oxide equivalent thickness of  $4.3 \pm 0.1$  nm as determined

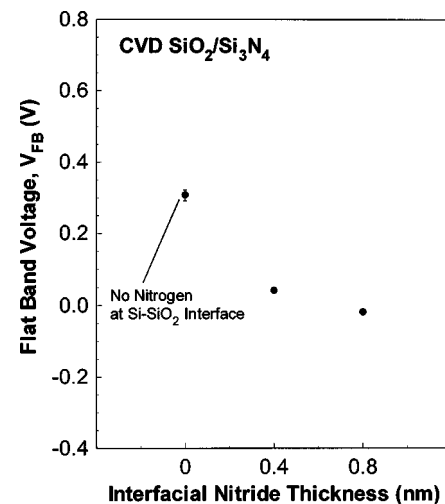


FIG. 20. Flat band voltage shift as a function of interfacial nitride thickness for the devices in Fig. 19. The flat band voltage was determined by analysis of high frequency  $C-V$  data. The gate electrode was Al.

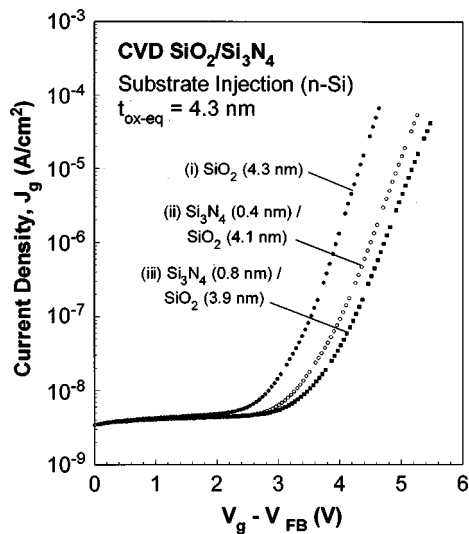


FIG. 21.  $J$  vs  $(V_g - V_{fb})$  traces in the substrate injection mode for devices of Fig. 19 with (i) no nitrogen at the interface, and (ii) one and (iii) two molecular layers of  $\text{Si}_3\text{N}_4$  at interface. The equivalent oxide (electrical) thickness was 4.3 nm for all samples. The gate electrode was Al.

from accumulation bias capacitance. The tunneling current in Fig. 21 decreased as thickness of  $\text{Si}_3\text{N}_4$  layer at the interface increased. When we plotted the current density versus gate voltage minus the flat band voltage ( $V_g - V_{fb}$ ), the leakage current reduction was more pronounced than for process I, compare Figs. 8 and 21. However, it is difficult to make direct quantitative comparisons between the  $J-V$  traces for the two interface nitridation processes discussed above. In particular even though the reductions in  $J$  with increasing nitridation are comparable, the areal densities of nitrogen atoms differ by factors of approximately ten for the 0.4-nm-thick nitride film and twenty for the 0.8-nm-thick nitride film when compared to the monolayer nitridation of process I.

Finally, Fig. 22 displays high frequency and quasistatic  $C-V$  traces for the same three test devices of this section. Interfacial nitridation via  $\text{Si}_3\text{N}_4$  deposition reduced the tunneling currents but the interfacial defect density increased significantly,  $D_{it}$  levels determined by conventional analysis of high frequency and quasistatic  $C-V$  traces, increased from the mid  $10^{10} \text{ cm}^{-2}$  range for the devices fabricated by process I, to more than  $15 \times 10^{11} \text{ cm}^{-2}$  for the devices with deposited nitride layers shown in Fig. 22. Fixed positive charge, determined by shifts of the  $C-V$  traces to more negative voltages increased by more than an order of magnitude into the  $10^{12} \text{ cm}^{-2}$  range. This increased density of interface state has been shown to effect the channel mobilities in both  $n$ - and  $p$ -channel MOSFET devices.<sup>37,38</sup> In particular Misra *et al.*<sup>37</sup> have shown that peak values of electron mobility are reduced by a factor of 2 in the  $n$ -channel MOSFET's, whereas peak values of the hole mobility are reduced by more than a factor of 10–20 in  $p$ -channel MOSFETs. These results indicate that charged defects associated with direct deposition of  $\text{Si}_3\text{N}_4$  onto Si are associated with donor-like defects that reside in the lower half of the silicon band gap.

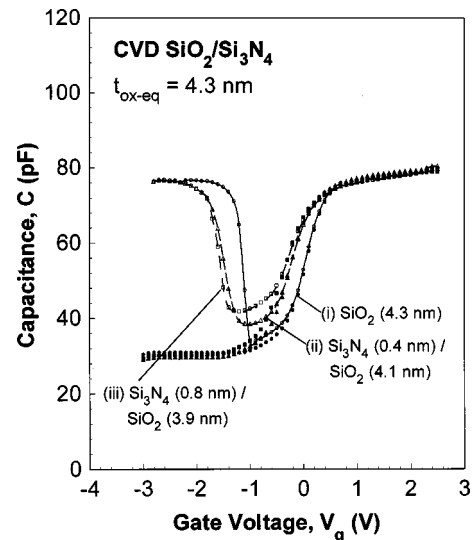


FIG. 22. High-frequency (1 MHz) and quasistatic  $C-V$  measurements for devices in Fig. 19 with (i) no nitrogen, (ii) one and (iii) two molecular layers of  $\text{Si}_3\text{N}_4$  at interface. The equivalent oxide (electrical) thickness was 4.3 nm for all samples. The gate electrode was Al.

#### IV. DISCUSSION

We have investigated three different ways of incorporating nitrogen at the Si-dielectric interface: process (I)  $\text{O}_2/\text{He}$  plasma oxidation of the Si surface followed by the  $\text{N}_2/\text{He}$  plasma nitridation, process (II)  $\text{N}_2/\text{He}$  plasma nitridation of the Si surface, and process (III)  $\text{Si}_3\text{N}_4$  film deposition on the Si surface. Based on significant negative shifts of the flat band voltage that increased as the nitrogen incorporation at the interface increased, we have demonstrated the processes labeled (II) and (III) degraded device performance through the development of large densities of fixed positive charge in the dielectric in the immediate vicinity of the Si-dielectric interface. All three processes resulted in decreases in FN tunneling current, however, the shifts in flat band voltage, as well as increases in interfacial defects,  $D_{it}$ , render processes (II) and (III) useless for advanced device structures.

It is necessary to explain why postoxidation, interface nitridation of process (I) and the direct oxidation/nitridation using  $\text{N}_2\text{O}$ ,<sup>18</sup> each of which incorporates monolayer levels of nitrogen at the interface improve device performance and reliability, whereas higher concentrations of nitrogen as in processes (II) and (III) clearly degrade interface electrical properties. The experiments reported in Refs. 37 and 38, have shown that the problem is not with the RPECVD film itself, since insertion of as little as 0.5 nm of  $\text{SiO}_2$  between the Si substrate and the deposited nitride restores electrical performance and reliability to values comparable or exceeding those of devices with optimized oxide dielectrics of the same equivalent thickness.

Lucovsky and co-workers have found that the average bonding coordination  $N_{av}$  at the dielectric-Si interface is key to understanding the origin of interfacial defect generation.<sup>39</sup> Reference 39 has extended constraint theory, originally proposed by Phillips<sup>40</sup> to explain the ease of glass formation in

TABLE I. Average bonding coordination,  $N_{av}$ , at Si-dielectric interfaces.

Si-dielectric interface system	Average coordination ( $N_{av}$ )
Si-SiO <sub>2</sub> (1.5 molecular layers)	2.8
Si-Si <sub>3</sub> N <sub>4</sub> (1.5 molecular layers)	3.5
Si-Si <sub>3</sub> N <sub>4</sub> ( $t$ )-SiO <sub>2</sub>	
$t$ =nitride layer thickness	$t=0.4$ nm, 3.3
	$t=0.8$ nm, 3.4
Si-N(1.0 monolayer)-SiO <sub>2</sub> (1.5 molecular layers)	2.9
Si-SiO <sub>2</sub> ( $t$ )-Si <sub>3</sub> N <sub>4</sub>	$t=0.5$ nm, 2.9
*1.5 molecular layers of SiO <sub>2</sub>	

materials such as As<sub>2</sub>S<sub>3</sub>, GeSe<sub>2</sub>, and SiO<sub>2</sub>, to the interface between noncrystalline dielectrics and semiconductor. Phillips demonstrated that the condition for ideal glass formation corresponded to matching bonding constraints per atom in the context of valence forces to the network dimensionality.<sup>40</sup> This demonstrated that ideal random covalent networks, which form the basis for glass formation occurred when  $N_{av}$  was in a range between 2.4 and 2.7. In extending the constraint theory formulation, Lucovsky *et al.* focused on differences between interface nitridation to establish a link the relationship between average interfacial coordination and defect properties.<sup>39</sup> Results presented in Ref. 41 initially extended the Phillips theory<sup>40</sup> bulk glasses to thin films, suggesting that an average coordination per atom of approximately three separates device quality thin films from films with increasing defect densities. The results presented in Ref. 39 confirmed that  $N_{av} \sim 3$  also provides a demarcation value between device quality and highly defective interfaces, with defect values of about  $5 \times 10^{10}$  cm<sup>-2</sup> defining this boundary. Applying the model of Ref. 39, Table I includes a calculation of the  $N_{av}$  for interfaces studied in this article. The interfaces that show excellent electronic properties, Si-SiO<sub>2</sub>, and monolayer nitrided Si-N-SiO<sub>2</sub> formed by process (I), have  $N_{av}$  values of 2.8 and 2.9, respectively, whereas the interface formed by processes (II) and (III), have values in excess of 3, consistent with the criterion developed in Ref. 39. For completeness the table also demonstrates that the insertion of about one and a half molecular layers of SiO<sub>2</sub> ( $\sim 0.5$ – $0.6$  nm) yields a value of  $N_{av} < 3$  in accordance with the significant improvement in electrical properties that has been reported.<sup>37,38</sup>

## V. CONCLUSIONS

We have demonstrated three different plasma-assisted interface nitridation processes: (i) process I - O<sub>2</sub>/He plasma oxidation of the Si surface followed by N<sub>2</sub>/He plasma nitridation, (ii) process II - N<sub>2</sub>/He plasma nitridation of the Si surface, and (iii) process III - deposition Si<sub>3</sub>N<sub>4</sub> film on the Si surface. Process I is an oxide-first process, while processes II and III are both nitride first processes. For process I, the first step, the 300 °C remote plasma assisted O<sub>2</sub>/He oxidation of the Si surface reduces significantly/removes carbon contamination, creates a device quality Si-SiO<sub>2</sub> interface, and forms  $\sim 0.6$  nm of SiO<sub>2</sub> which served as a substrate for the RPECVD deposition of dielectric films. The second step, a

300 °C remote plasma assisted N<sub>2</sub>/He plasma nitridation controls the degree of the nitrogen incorporation at the Si-SiO<sub>2</sub> interface. AES studies of etched back surfaces confirmed the nitrogen was localized at the interface, and SIMS and NRA analysis established that a 90 s plasma exposure time incorporated approximately one monolayer of interfacial nitrogen ( $\sim 7 \pm 1 \times 10^{14}$  cm<sup>-2</sup>). This monolayer nitrogen incorporation reduced tunneling current direct<sup>42</sup> and FN and tunneling regimes.

Consider next process II, the direct nitridation of a Si surface. Unlike process I, the direct nitridation of Si using N<sub>2</sub>/He plasma process did not remove carbon contamination from the Si surface. Monitoring nitrogen content as a function of nitridation time by AES established that this interfacial nitridation process was effectively self-limiting, slowing down considerably after about two monolayers of nitride formation. The nitridation process for the first molecular layer was very fast, and in contrast to process I, it is more difficult to control incorporation of nitrogen in the range extending up to about one monolayer. The electrical properties of this interface as monitored by  $C$ - $V$  measurements were degraded as indicated by flat band voltage shifts in the negative direction that increased with increasing nitridation time. In addition, reductions in tunneling current in the FN regime were reduced with respect to those obtained with process I.

Process III was the direct deposition by RPECVD at 300 °C of Si<sub>3</sub>N<sub>4</sub> onto the Si surface. This process also did not remove carbon contamination. As in a typical CVD process, the amount of nitrogen, or equivalently, thickness of the nitrided layer, increased linearly with increasing deposition time. Similar to process II the Si-Si<sub>3</sub>N<sub>4</sub> interface displayed a high defect density, as reflected in a large negative flat band voltage shift. However, the reductions in tunneling current as function of the voltage drop across the dielectric layer ( $V_g - V_{fb}$ ) were comparable to those obtained with monolayer nitridation in process I.

Therefore, among the three interfacial nitridation processes, process I, the two-step interface formation process displayed the best electrical results. This was consistent with the predictions of constraint theory as applied to crystalline-Si dielectric interfaces in Ref. 39.

## ACKNOWLEDGMENTS

This work is funded in part by the Office of Naval Research (ONR), the National Science Foundation-Engineering Research Center (NSF-ERC), and the Semiconductor Research Corporation (SRC). The authors also would like to thank Dr. D. Buchanan and Dr. S. Cohen for nuclear reaction analysis.

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