Monolayer-level controlled incorporation of nitrogen in ultrathin gate dielectrics using remote plasma processing: Formation of stacked ''N–O–N'' gate dielectrics

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A low thermal budget approach to monolayer-level controlled incorporation of nitrogen in ultrathin gate dielectrics using 300 °C, remote plasma processing is discussed. Incorporation of approximately 1 ML of nitrogen at the Si–SiO_2 interface in an ''N–O'' *structure* has been achieved by remote plasma-assisted oxidation of the Si surface followed by N_2/He remote plasma nitridation, each at a process pressure of 0.3 Torr. The interface nitridation reduces direct and Fowler–Nordheim tunneling by at least one order of magnitude, independent of film thickness. Incorporation of nitrogen at the top surface of the oxide in a concentration equivalent to about 1–2 molecular layers of silicon nitride in an ''O–N'' *structure* has been accomplished by N_2/He remote plasma nitridation at 300 °C, but at a reduced process pressure of 0.1 Torr. Top surface nitridation has been shown to prevent boron diffusion out of p^+ poly-Si gate electrodes during high-temperature activation anneals, e.g., at 1000 °C. Combining interfacial and top surface nitridation processes resulted in a ''N–O–N'' *structure* that was effective in reducing tunneling leakage currents and suppressing boron out-diffusion from p^+ poly-Si gate electrodes. *© 1999 American Vacuum Society.* [S0734-211X(99)20506-9]

I. INTRODUCTION

As devices are aggressively scaled to smaller feature sizes to increase integration densities, the thickness of gate dielectrics must be decreased to meet the required goals for ultra-large scale integrated-circuit (ULSI) device performance. Once the thickness of the gate oxide dielectric is reduced below about 3 nm into the regime of direct tunneling, gate leakage current becomes an important consideration in device performance and reliability. It is in this regime of direct tunneling that the gate leakage becomes comparable to the source-to-drain junction leakage of metal–oxide–semiconductor field-effect transistor (MOSFET) devices.

Monolayer-level nitrogen incorporation at the Si–SiO_2 interface in MOSFETs has been demonstrated to (i) improve performance; e.g., current drive;[1–4] (ii) increase immunity to hot-carrier stress degradation;[5,6] (iii) suppress stress-induced leakage currents (SILC);[7] (iv) reduce electron traps;[8] and (v) improve charge to breakdown and time to breakdown.[8] Therefore, controlled incorporation of nitrogen into ultrathin gate dielectrics emerges as an important factor in future generations of advanced MOSFET devices. Momose *et al.*[9] quantified both device performance and reliability as a function of the interfacial nitrogen concentration. According to their study, the optimum nitrogen concentration at the Si–dielectric interface is in a range from about 0.2 to 1.0 at. %. However, for *p*-channel metal–oxide–semiconductor (PMOS) devices with ''heavily'' boron-implanted ($\sim 5\times 10^{15}$–1×10^{16} cm^{-2}) poly-Si gate electrodes, this ''light'' nitridation is not sufficient to prevent boron diffusion through the oxide to the nitrided interface. Consistent with these observations, and in accord with a model developed by Fair,[10,11] a nitrogen concentration of less than about 10 at. % has a negligible effect on inhibiting boron diffusion.

Although ''heavy'' interfacial nitridation effectively suppresses boron diffusion into the channel region of the substrate, device performance and reliability suffer severe degradation if boron atoms pile up at the Si–SiO_2 interface.[9] In addition, when boron transport is stopped at a ''heavily'' nitrided Si–SiO_2 interface, boron atoms also accumulate in the bulk oxide film after the high-temperature activation/drive-in annealing and degrade device reliability.[12] Therefore, it would be better to suppress boron atom transport at the top surface of the oxide for PMOS devices with p^+ poly-Si gate electrodes. The results discussed above suggest that a ''N–O–N'' *structure*, with a ''lightly'' nitrided Si–SiO_2 interface ($\sim$1 at. %) and a more ''heavily'' nitrided top surface of the gate oxide ($>$10 at. %), is an ideal gate dielectric structure for the many advanced devices, which include oxides $<$3 nm thick.

In this article, we demonstrate independently controlled monolayer-level incorporation of nitrogen (i) at the Si–SiO_2 interface and (ii) on the top surface of the oxide in a ''N–O–N'' *structure* by low-temperature (300 °C) remote plasma-assisted processing. We then show that the nitrogen concentrations and profiles achieved by this combination of

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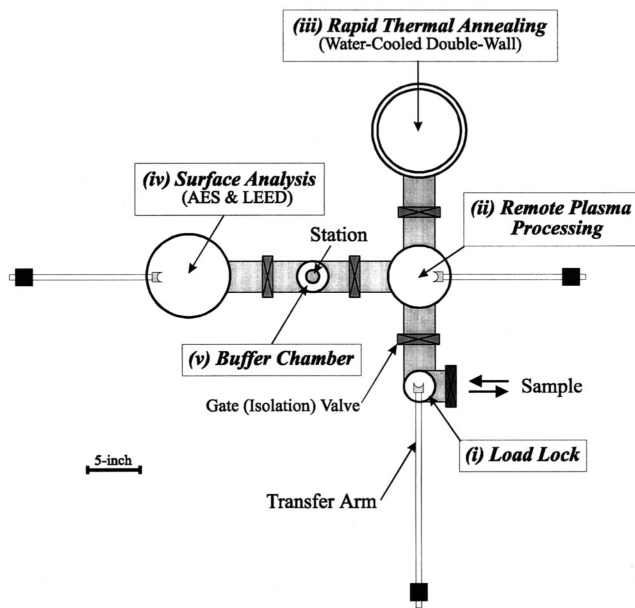

FIG. 1. Top view of UHV multichamber system with (i) load lock, (ii) remote plasma processing, (iii) rapid thermal annealing, (iv) surface analysis, and (v) buffer chambers.

processing steps are sufficient to reduce tunnel leakage currents and prevent boron diffusion out of p^+ poly-Si gate electrodes. This makes low-temperature remote plasma processing an attractive alternative for fabricating advanced complementary metal–oxide–semiconductor (CMOS) devices.

II. EXPERIMENTAL PROCEDURES

The processing steps for fabricating ''*N–O–N*'' *structures* were performed in a multichamber system, which is shown in Fig. 1. This system contains: (i) a load-lock chamber; (ii) a remote plasma processing chamber for oxidation, nitridation, and bulk film deposition; (iii) a rapid thermal annealing (RTA) chamber; (iv) a buffer chamber to isolate the surface analysis chamber from the remote plasma processing chamber; and (v) a surface analysis chamber with Auger electron spectroscopy (AES). The process for incorporation of nitrogen at the Si–SiO_2 interface combines two 300 °C steps: (i) plasma-assisted oxidation of a hydrogen-terminated Si surface using remotely excited O_2/He, followed by (ii) plasma-assisted nitridation using remotely excited N_2/He. The plasma oxidation creates a device-quality Si–SiO_2 interface and approximately 0.5–0.6 nm of SiO_2, and the plasma nitridation step controls the concentration of nitrogen atoms incorporated at the Si–SiO_2 interface by varying the N_2/He plasma exposure time. For the oxidation process, the flow rates through the plasma tube (upstream delivery) were 20 sccm of O_2 and 200 sccm of He. For the nitridation process, the upstream flow rates through the plasma tube were 60 sccm N_2 and 160 sccm He. For each of these steps, the process pressure was 0.3 Torr, and the rf power at 13.56 MHz was 30 W.

Device structures were completed by depositing SiO_2 films at 300 °C onto the nitrided interface layer. Previous studies indicated that the ~0.6 nm interface layer was sufficient to prevent ''subcutaneous'' oxidation of the SiO_2 interface during the plasma deposition step,[13] thereby providing separate and independent control of interface formation and bulk film deposition. The bulk SiO_2 deposition was performed by a remote plasma-enhanced chemical-vapor deposition (RPECVD) process using 2% SiH_4 in He and O_2/He as the respective atomic source gases for Si and O. The O_2/He mixture was injected upstream and rf plasma excited as in the oxidation step; however, the SiH_4 gas was injected downstream through a gas dispersal ring located outside of the plasma excitation region.[14] The gas flow ratios for O_2, He, and 2% SiH_4 in He were 20, 200, and 10 sccm, respectively. Postoxide film deposition annealing was performed in the on-line RTA chamber at 900 °C for 30 s at a pressure of 0.3 Torr in a He ambient. This postoxide deposition anneal has been demonstrated to reduce chemical and structural strain at the Si–SiO_2 interface and in the bulk oxide film.[15,16]

Controlled incorporation of nitrogen at the top surface of an oxide film, deposited by RPECVD, was achieved by a second N_2/He plasma nitridation process. The nitridation was done using remotely activated upstream injection of a N_2/He mixture through the plasma tube. The process temperature was 300 °C and the rf input power at 13.56 MHz was 30 W. The process pressure was reduced to 0.1 Torr, which allowed the plasma to penetrate the processing chamber, converting the remote reactor into an afterglow reactor. The gas flows were 60 sccm N_2 and 160 sccm He. The concentration of nitrogen on the top surface of the oxide was controlled by the time of the plasma exposure. The differences between the interface and top surface plasma nitridation processes are in the respective process pressures, which control the balance between neutral and charged nitrogen species *injected* into the process chamber. The active species for the interface nitridation are nitrogen atoms, whereas the active species for the top surface nitridation process in which the plasma afterglow penetrates into the deposition chamber are nitrogen ions.

For the materials characterization studies, the substrates used in these were 50-mm-diam phosphorus-doped *n*-type Si(100) with a resistivity of 0.02–0.045 Ω cm. The nominal electron concentration at room temperature was $\sim 5\times10^{17}$ cm^{-3}. After a standard wet chemical two-step RCA clean and a rinse in dilute HF (1 wt %), a 10-nm-thick sacrificial oxide was grown at 900 °C in dry O_2 by a conventional thermal oxidation process. Immediately before loading the sample into the multichamber processing system, the sacrificial oxide was removed by etching in a dilute HF (1 wt %) solution, rinsing in a flowing deionized (DI) water for 20 s, and then blow drying in flowing N_2.

AES was performed using a 3 keV electron beam in an on-line analysis chamber to quantify the initial stages of the oxidation and nitridation of the Si surface. To determine whether the nitridation process resulted in spatial localization of nitrogen atoms at the Si–SiO_2 interface, angle-resolved

TABLE I. Process sequence for (i) ''*N–O*,'' (ii) ''*O–N*,'' and (iii) ''*N–O–N*'' structures. See Fig. 2.

Process step in Fig. 1	(i) ''*N–O*''	(ii) ''*O–N*''	(iii) ''*N–O–N*''
No. 1 (oxidation)	√	√	√
No. 2 (nitridation)	√	Skip	√
No. 3 (bulk oxide deposition)	√	√	√
No. 4 (RTA)	√	√	√
No. 5 (top nitridation)	Skip	√	√

x-ray photoelectron spectroscopy (ARXPS) analyses, at 15°, 45°, and 75° takeoff angles with respect to the surface, were carried out at the University of Texas at Austin. Secondary-ion-mass spectroscopy (SIMS) analyses were done at EVANS EAST, NJ, using positive CsN^+-ion detection for depth profiling of the interfacial nitrogen concentration, and for determining the effective areal density of nitrogen atoms. Nuclear reaction analyses (NRA) were carried out at the IBM T.J. Watson Research Center, NY, for calibration/conformation of the nitrogen concentration.[17] Core-level XPS analyses were done using Beamline U4A at the National Synchrotron Light Source/Brookhaven National Laboratory, NY, at a photon energy of 150 eV to study the interfacial chemical bonding arrangements.

MOS capacitors with field oxide isolation were made on Si(100) wafers using conventional photolithography processes. For electrical characterization, the substrates were the same 50-mm-diam phosphorus-doped *n*-type Si(100) with a resistivity of 0.02–0.045 Ω cm and an effective electron concentration of $\sim 5\times 10^{17}$ cm^{-3}. For the current density–voltage ($J-V$) studies, the use of heavily doped Si wafers reduces spreading resistance, thereby minimizing any parasitic series resistance and the accompanying voltage drops in the bulk Si. Phosphorous-doped *n*-type Si(100) wafers with a resistivity of 5.0–10.0 Ω cm (effective electron concentration, $\sim 5\times 10^{15}$ cm^{-2}) were used in the studies for determining the effectiveness of top surface nitridation in blocking boron transport out of heavily ion-implanted p^+ poly-Si gate electrodes. Capacitance–voltage ($C-V$) measurements were used to determine an equivalent oxide thickness, and to estimate the densities of interfacial defects, both interface traps (D_{it}), and fixed positive charge. A frequency of 1 MHz was used for the high-frequency voltage sweeps.

III. RESULTS AND DISCUSSION

This article focuses on the role of nitrogen incorporation into ultrathin gate oxides, 5–2 nm thick. The approaches used to incorporate nitrogen into the oxide were remote plasma processing and rapid thermal annealing. The location of the incorporated nitrogen is either (A) at the Si–SiO_2 interface, ''*N–O*'' *structure*; (B) on the top surface of the oxide, ''*O–N*'' *structure*; or (C) both at the Si–SiO_2 interface and on the top surface of oxide, ''*N–O–N*'' *structure* (see Table I).

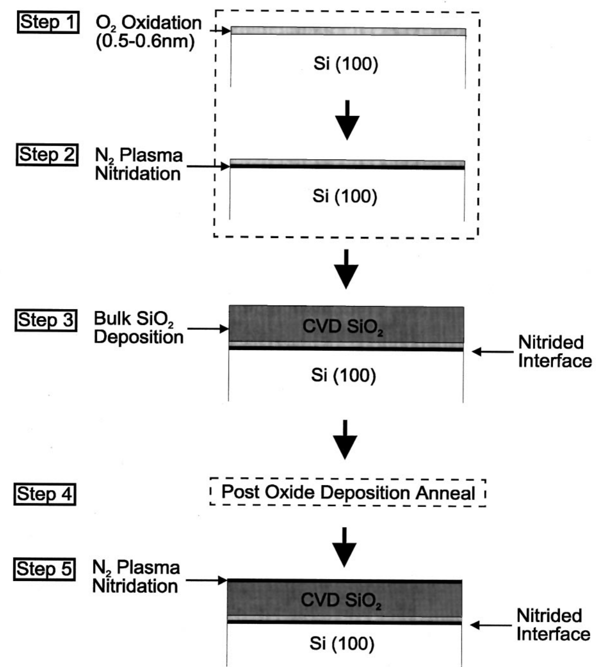

FIG. 2. Process sequence for fabrication of ''*N–O–N*'' *structure dielectrics*: (1) O_2/He plasma oxidation of Si surface, followed by (2) N_2/He plasma nitridation at 0.3 Torr, (3) bulk SiO_2 film deposition, (4) postoxide deposition anneal, and (5) N_2/He plasma nitridation of oxide at 0.1 Torr.

A. Incorporation of nitrogen at the Si–SiO_2 interface: The ''*N–O*'' *structure*

Processing for the ''*N–O*'' *structure* used steps 1–4 of the process sequence in Fig. 2. Interfacial oxidation/nitridation of a H-atom-terminated Si(100) surface has been shown to produce a device-quality interface first using the O_2/He remote plasma oxidation process and then incorporating nitrogen at the Si–SiO_2 interface via the N_2/He remote plasma nitridation at 0.3 Torr.[18] This O_2/He plasma process (the first step of the process sequence in Fig. 2) provides three functions; it (i) removes carbon contamination from the Si surface, (ii) creates a device-quality Si–SiO_2 interface, and (iii) grows ~0.5–0.6 nm of SiO_2.[19] Figure 3, trace (i), shows the differential AES spectrum from the Si substrate after the RCA cleaning step. A comparison of the relative intensities of the Si substrate Si_{LVV} AES feature at ~91 eV and the SiO_2 Si_{LVV} AES feature ~76 eV AES demonstrates that the RCA clean produces a ~0.7-nm-thick chemical oxide. There is also evidence for carbon contamination as indicated by the C_{KLL} AES peak at ~272 eV. The chemical wide was etched away using a 1 wt % HF:H_2O solution, but this did not completely remove the carbon contamination as shown in Fig. 3, trace (ii). Additionally, as shown in Fig. 3, trace (iii), the carbon contamination did not disappear following *in situ* heating to 300 °C. However, as shown in Fig. 3, trace (iv), the O_2/He plasma treatment was effective in reducing the carbon contamination level. Note that if the carbon were at the Si–SiO_2 interface, it would be observable by AES since the oxide thickness after the plasma treatment was ~0.4–0.5 nm, which is less than the electron escape

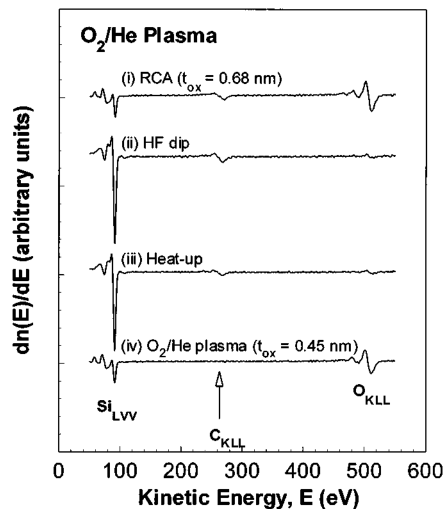

FIG. 3. On-line AES spectra of Si surfaces after: (i) RCA cleaning, (ii) 1 wt % of HF dip, (iii) 300 °C heating for 10 min in the UHV system, and (iv) 5 s O_2/He plasma oxidation of the Si surface. Electron-beam energy was 3 keV.

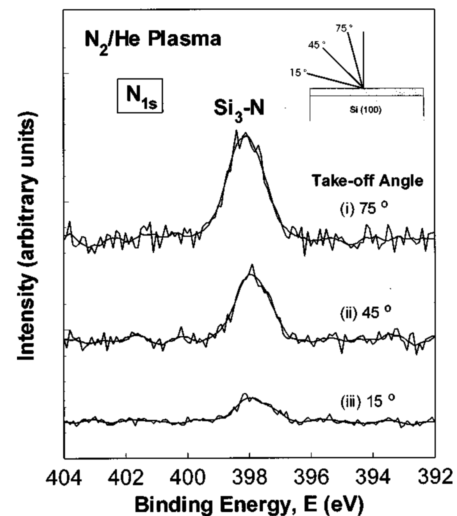

FIG. 5. ARXPS spectra of N_{1s} from O_2/He plasma oxidation of Si followed by 90 s N_2/He plasma nitridation and RTA. Takeoff angles were (i) 75°, (ii) 45°, and (iii) 15°. The takeoff angle is the angle between the film surface and the electron analyzer.

depth of the electrons (~1 nm) associated with the C_{LVV} Auger feature. Therefore, it is concluded that the O_2/He plasma reduces carbon contamination at the Si surface, and the Si–SiO_2 interface, during the formation of a superficially thin SiO_2 layer on the Si substrate. These observations and conclusions confirm a previously published result by Yasuada *et al.*[19]

The N_2/He plasma-assisted nitridation (the second step in Fig. 2) of the superficial oxide was also studied using on-line AES. Figure 4 shows differential AES spectra for (i) 15 s O_2/He plasma oxidation of the Si surface followed by (ii)–(v) N_2/He plasma nitridation treatments ranging from 30 to 120 s, in 30 m s increments. The notation, ''O_2+N_2 (60 s),'' means that the 15 s O_2/He plasma oxidation of the Si surface was followed by a 60 s N_2/He plasma nitridation. The incorporation of nitrogen atoms is reflected in the evolution of the N_{KLL} AES peak at ~379 eV. The intensity of the N_{KLL} feature increased monotonically as the exposure time to the N_2/He plasma was increased, demonstrating that longer exposure times resulted in increasing nitrogen atom incorporation, either at the Si–SiO_2 interface *or* in the bulk of ~0.6-nm-thick oxide layer.

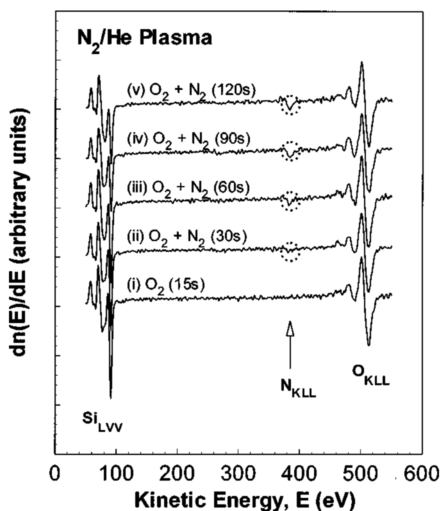

FIG. 4. On-line AES spectra, using a 3 keV electron beam, from (i) 15 s O_2/He plasma oxidation of Si surface followed by (ii)–(v) N_2/He plasma nitridation of the plasma-grown oxide for 30, 60, 90, and 120 s.

The issue is the ''exact'' location of the nitrogen: *at* the Si–SiO_2 interface *or in* the bulk of the superficial oxide layer. The following experiments using ARXPS established that the nitrogen incorporation was essentially *at* the Si–SiO_2 interface; i.e., at the metallurgical boundary between the Si substrate and the SiO_2 layer, and not uniformly distributed in the SiO_2 film, or at its top surface. Figure 5 shows the ARXPS spectra of the N_{1s} feature from the O_2/He plasma oxidation of the Si surface followed by the 90 s N_2/He plasma nitridation and RTA (900 °C) sample for takeoff angles of (i) 75°, (ii) 45°, and (iii) 15°. The ''takeoff'' angle is the angle between the wafer plane and the analyzer axis. The total SiO_2 dielectric layer thickness was ~1.0 nm. The normalized intensity of the N_{1s} peak decreased with decreasing the takeoff angle. Since the 15° takeoff angle enhances the surface sensitivity, this establishes that the nitrogen atoms were located not *on* the top surface of the thin plasma oxide or uniformly in the bulk of the oxide, but rather were closer to, or effectively *at* the Si–SiO_2 interface.[20–22] This observation is consistent with comparisons between the optical second-harmonic-generation signals from nitrided and non-nitrided Si–SiO_2 interfaces.[23]

SIMS has been used to quantify the nitrogen content at the Si–SiO_2 interface. We prepared four samples at different nitridation times ranging from 30 to 120 s; this was the second step of the process sequence used. The first, third, and fourth steps of this process sequence were the same for all four samples: (i) a 15 s O_2/He plasma oxidation, (ii) bulk oxide deposition (~7.0 nm-thick), followed by (iii) a 900 °C

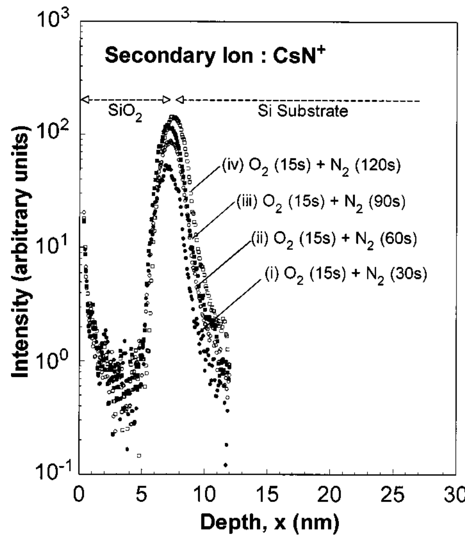

FIG. 6. SIMS depth profiles of four different interfacial nitridation times: (i) 30 s, (ii) 60 s, (iii) 90 s, and (iv) 120 s. The total oxide thickness was ~0.8 nm, and the detected secondary ions were CsN^+.

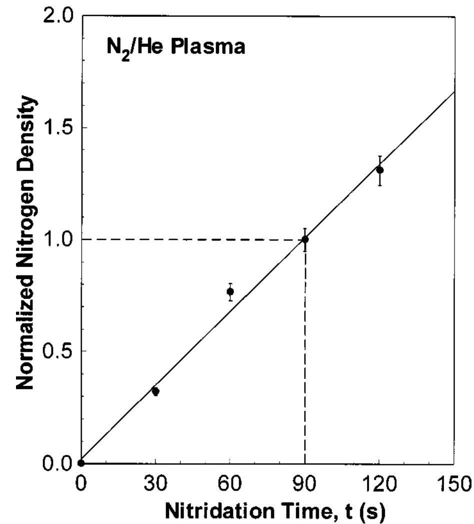

FIG. 7. Normalized SIMS areal density with respect to the 90 s nitridation as a function of nitridation time. One monolayer of nitrogen ($\sim 7 \pm 1 \times 10^{14}$ cm^{-2}) was achieved at an exposure time of 90 s.

postoxide deposition anneal. Figure 6 presents SIMS depth profiles, obtained by standard ion etching procedures, in which the detected species were CsN^+ ions. The peak intensity of nitrogen at the Si–SiO_2 interface increased with increasing exposure time to the N_2/He plasma, as did the integrated response. The depth profile reflects the depth of the nitrogen incorporation, as well as the effects of the ion-milling process which broadens the distribution. In particular, the sharp rise marks the spatial localization of nitrogen atoms at, or in the immediate vicinity of the Si–SiO_2 interface. To quantify the SIMS data, the features in Fig. 6 were integrated to obtain a normalized areal density of nitrogen atoms. Consistent with the spatial localization of the nitrogen atoms at the Si–dielectric interface, the relative sensitivity factor employed was for N atoms in a Si–host material.

Based on a standard reference sample prepared at EVANS EAST, NJ, by implantation of known amounts of N atoms into crystalline Si, the areal density of nitrogen atoms incorporated during the 90 s N_2/He nitridation step was approximately 1 ML of nitrogen, or $\sim 7 \pm 1 \times 10^{14}$ nitrogen atoms cm^{-2} localized at the Si–SiO_2 interface. NRA studies confirmed that the 90 s N_2/He plasma nitrogen process incorporated $\sim 8.4 \pm 1 \times 10^{14}$ nitrogen atoms cm^{-2} or approximately 1 ML.[17]. Figure 7 presents normalized integrated areal densities with respect to the 90 s exposure as a function of nitridation time. The interfacial nitrogen concentration is demonstrated to increase linearly with the nitrogen plasma exposure time.

This interfacial nitridation process has been used in the fabrication of MOS capacitors in a thickness range from 4.5 nm [Fowler–Nordheim (FN) tunneling region] down to 2.0 nm (direct tunneling region) on n-type Si(100) substrates using both aluminum (Al) and heavily phosphorus-doped n^+ poly-Si gate electrodes. Figure 8 includes a series of $J-V$ traces for a 4.5-nm-thick gate oxide on n-Si(100) wafers. The current flows from the substrate to the gate electrode in the so-called *substrate injection* mode. The traces in Fig. 8 demonstrate that interfacial nitrogen at the submonolayer and monolayer levels reduced significantly tunneling current in the FN region. Specifically, the tunneling current at any voltage above the threshold for FN injection decreases with increased nitridation time, and therefore, with increasing fractional interface nitridation. However, this reduction saturates for a nitridation time of 90 s, the time required for a single-monolayer to converge. This reduction is not due to an oxide thickness change and/or a flatband voltage shift that results from incorporation of nitrogen at the Si–SiO_2 interface. In particular, since there is only 1 ML of interfacial nitrogen, the equivalence of accumulation capacitance in devices with

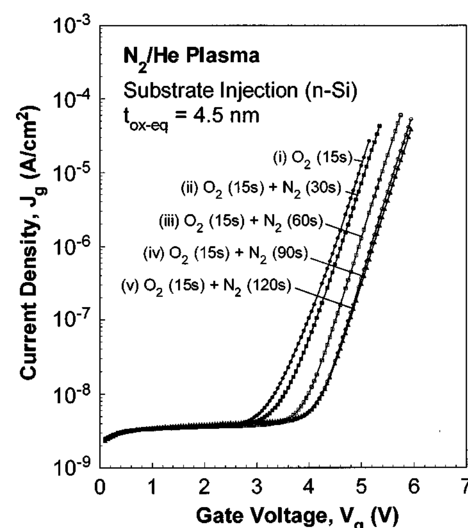

FIG. 8. Substrate injection mode (gate electrode biased positively) $J-V$ traces for 4.5-nm-thick gate oxide on n-Si(100), demonstrating the effect of interfacial nitrogen in reducing tunnel currents in the FN region. The gate electrode was Al. The flatband voltage is independent of interfacial nitridation so that data can be displayed as a function of gate voltage.

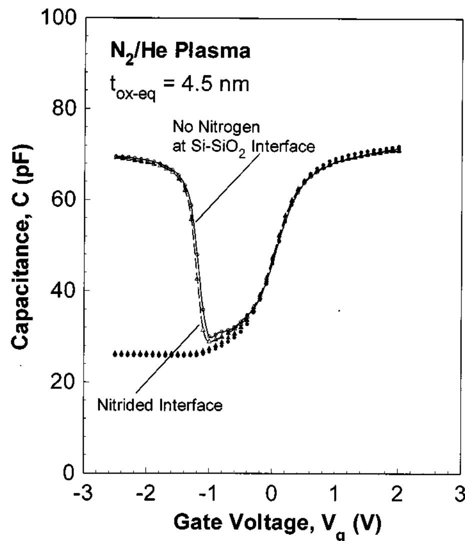

FIG. 9. High-frequency (1 MHz) and quasistatic $C-V$ measurements of devices (i) without interfacial nitridation and (ii) with a 90 s interfacial nitridation process. The gate electrode was Al.

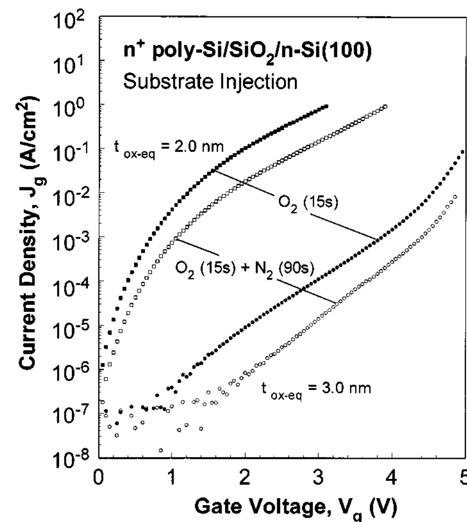

FIG. 10. Substrate injection mode (gate electrode biased positively) $J-V$ traces for 3.0- and 2.0-nm-thick gate oxide on n-Si(100), demonstrating the effect of the monolayer of interfacial nitrogen reducing tunnel currents in the direct tunneling region. The flatband voltage is independent of interfacial nitridation so that data can be displayed as a function of gate voltage. The gate electrode was phosphorus-implanted n^+ poly-Si.

and without interfacial nitridation is consistent with any increases in thickness for the nitrided interfaces being <0.1 nm. Calculations based on the WKB approximation indicate that differences in physical thickness of 0.1 nm cannot account for the observed reductions in tunneling current for devices with 1 ML of interfacial nitrogen. Figure 9 displays high-frequency and quasistatic $C-V$ measurements for devices (i) without the interfacial nitridation and (ii) with the 90 s N_2/He plasma nitridation step. The two $C-V$ curves are essentially identical. This means that the effective oxide thicknesses and flatband voltages are the same with and without the interfacial nitrogen. Therefore, the tunneling current reductions in the FN region are not due to an oxide thickness variation or a flatband voltage shift. Additionally, these results indicate that the nitrogen incorporation does not generate a measurable difference in fixed oxide charge, which would shift the $C-V$ curve along the voltage axis, e.g., in the negative x direction for fixed positive charge. Based on these measurements, the fixed positive charge difference between these two devices is $<10^{11}$ cm^{-2}.

As shown in Fig. 10, a reduction of direct tunneling current has also been observed for oxide thicknesses of 3.0 and 2.0 nm for substrate injection in MOS capacitors with n^+ poly-Si gate electrodes. The $J-V$ traces in Fig. 9 include reference devices without interface nitridation, as well as devices with monolayer nitrogen interface nitridation (the 90 s plasma treatment). It is important to note that this reduction of tunneling in the direct tunneling regime is the same for both samples, suggesting that the nitrogen incorporation is modifying the interfacial tunneling transmission probability.

We shall now discuss the relationship between interface structure and the electrical characteristics of devices with monolayer interface nitridation. Hao *et al.*[24] demonstrated that a new wet chemical wafer cleaning procedure (a modified RCA cleaning, a rinse in dilute HF, followed by immersion in a methanol/HF solution) prior to growth of an ultrathin (~4.2-nm-thick) oxide layer reduced leakage currents (see Fig. 1 of Ref. 24). This improvement in electrical performance was attributed to a smoother Si surface prior to oxidation.

Hedge *et al.*[25] investigated interface roughness of 4.0-nm-thick oxynitride films by atomic force microscopy (AFM) and cross-sectional transmission electron spectroscopy (XTEM). Compared with the control oxide (a 4.0-nm-thick thermal oxide grown at 800 °C in O_2 followed by a postoxidation anneal in N_2), the NO *oxynitride*, prepared by annealing the control oxide in a dilute nitric oxide (NO) ambient at 800 °C for 45 min, was smoother (by AFM) and had less interface roughness (by XTEM).

The experiment of Hao *et al.*[24] demonstrated that a smooth interface reduced leakage currents; while the experiment of Hegde *et al.*[25] showed the nitridation promoted an increase in the Si–SiO_2 interface smoothness. Therefore, the combination of these two experiments suggests that the incorporation of the nitrogen smoothes the Si–SiO_2 interfaces, and a physically smoother interface displays a reduced tunneling current. Therefore, an important aspect of reducing tunneling currents by interfacial nitridation in the plasma process described above is here assumed to be an increase in effective interface smoothness.

Experiments have demonstrated that there is a suboxide (SiO_x, $x<2.0$) transition layer between the substrate Si and stoichiometric bulk oxide,[26,27] that can manifest itself as interface roughness. The results of XPS experiments suggest that the incorporation of the nitrogen into this transition layer region modifies the interfacial structure, and in particular, reduces the degree of suboxide bonding.

To investigate the changes in interfacial chemical structure that were related to nitrogen incorporation on Si(100)

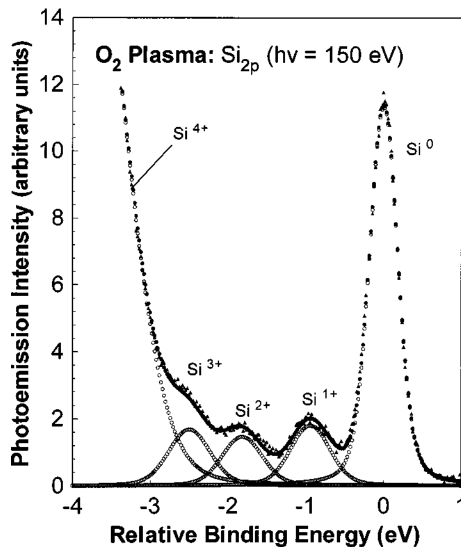

FIG. 11. Core-level $Si_{2p\ 1/2}$ XPS spectra for 15 s O_2/He plasma oxidation of the Si surface followed by annealing at 900 °C for 30 s in Ar ambient. The substrate was Si(100). The interfacial features have identified and fit with modified Lorentzian functions.

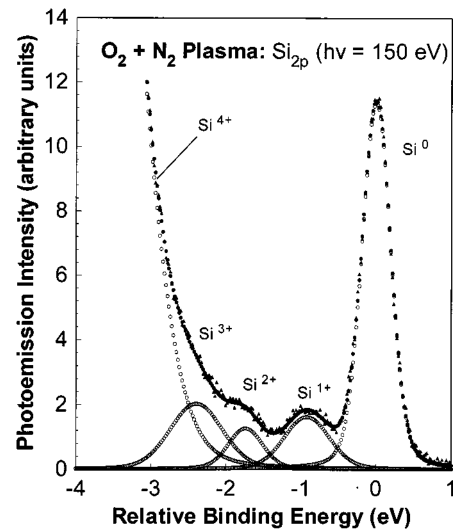

FIG. 12. Core-level $Si_{2p\ 1/2}$ XPS spectra for 15 s O_2/He plasma oxidation of the Si surface followed by 90 s N_2/He plasma nitridation and annealing at 900 °C for 30 s in Ar ambient. The substrate was Si(100). The interfacial features have been identified and fit with modified Lorentzian functions.

surfaces, we used core-level XPS with incident photon energy of 150 eV. The interfaces for this study were prepared by: (i) an O_2/He plasma oxidation of the Si surface followed by a 30 s 900 °C anneal in Ar ambient, and (ii) an O_2/He plasma oxidation, followed by a 90 s N_2/He plasma nitridation and then a 30 s 900 °C anneal in Ar. The dielectric thickness for each of these samples was ~1.0 nm. The details of the core-level XPS measurements are discussed in Ref. 27. Figures 11 and 12 show the core-level Si_{2p} XPS spectra from the above samples. The labels, Si^0, Si^{1+}, Si^{2+}, Si^{3+}, and Si^{4+}, are, respectively, Si^0; a Si atom in the substrate Si with four Si atom nearest neighbors, Si^{i+} ($i=1,2$, and 3); a Si atom in the SiO_x ($x<2$) transition region with i nearest-neighbor oxygen atom(s), and Si^{4+}; a Si atom in the SiO_2 layer with four oxygen neighbors.

There is some controversy regarding if the specific bonding configuration is the suboxide portion of the XPS spectrum;[28] however, there is no controversy regarding the assumption that the XPS spectral features between the Si^0 substrate peak, and the Si^{4+} SiO_2 peak are associated with the interface region between the Si substrate and the SiO_2 film. This means that the integrated spectral intensity of the Si^{1+}, Si^{2+}, and Si^{3+} reflects the areal density of suboxide bonding at the interface.[27,28] Note that an *ideal* Si(100)–SiO_2 interface would have 1 ML of suboxide bonding in the Si^{2+} state. Table II contains (i) the integrated peak density of the suboxide features normalized with respect to the integrated peak density of Si^0, (ii) the chemical shifts with respect to the Si^0 substrate feature, and (iii) the full width at half maximum (FWHM) of the Si^{1+}, Si^{2+}, Si^{3+}, and Si^{4+} states. Clearly, the suboxide density in the Si^{1+} and Si^{2+} are decreased with the incorporation of the nitrogen at the interface; these reductions are 8% for the Si^{1+} feature, and 33% for the Si^{2+} feature. The Si^{3+} state, however, increased with interfacial nitridation. This increase is in part due to Si–N bonding at the interface. For example, the chemical shift between the Si^{3+} feature for the non-nitrided and nitrided interface was 0.1 eV, and the FWHM of the Si^{3+} of the

TABLE II. Core-level PES data from Fig. 10 (O_2/He plasma process followed by RTA) and Fig. 11 (O_2/He process followed by N_2/He plasma and RTA): (i) integrated peak density of suboxide features normalized with respect to integrated peak density of Si^0, (ii) chemical shifts with respect to the Si^0 substrate feature, and (iii) full width at half maximum (FWHM).

		Si(1+)/Si(0)	Si(2+)/Si(0)	Si(3+)/Si(0)	
Normalized integrated peak density	O_2 plasma	0.358	0.294	0.349	
	O_2+N_2 plasma	0.330	0.198	0.472	
		Si(1+)	Si(2+)	Si(3+)	Si(4+)
Chemical shift (eV) from Si(0)	O_2 plasma	−0.94	−1.82	−2.50	−3.88
	O_2+N_2 plasma	−0.92	−1.74	−2.40	−3.82
FWHM (eV)	O_2 plasma	0.67	0.62	0.81	n/a
	O_2+N_2 plasma	0.71	0.52	0.90	n/a

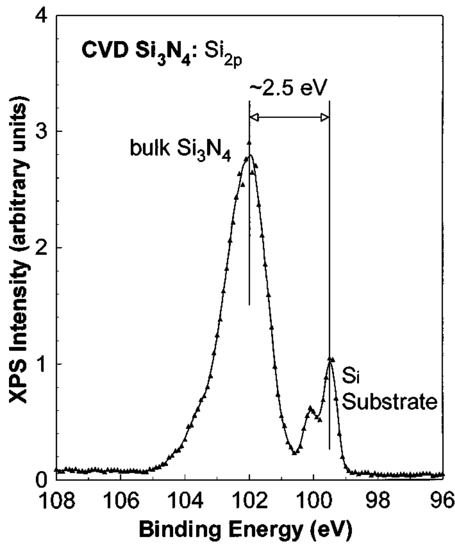

FIG. 13. Core level $Si_{2p\ 1/2}$ XPS spectra from the ~0.9-nm-thick Si_3N_4 deposition on the Si substrate followed by annealing at 900 °C at 0.3 Torr for 30 s in He ambient in on-line RTA.

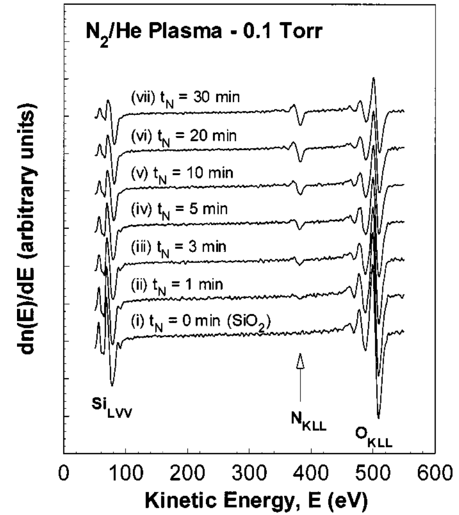

FIG. 14. On-line AES spectra using a 3 keV electron beam from (i) a 4.0-nm-thick SiO_2 surface, followed by (ii)–(vii) N_2/He plasma top surface nitridation for 1–30 minutes. The process pressure was 0.1 Torr.

nitrided interface was increased. Figure 13 shows Si_{2p} XPS spectra from 9-nm-thick Si_3N_4. The binding energy difference between the $Si_{2p\ 3/2}$ and the Si–N peak in the Si_3N_4 layer is about 2.5 eV. This value is very close to the relative binding energy of Si^{3+} (~2.4–2.5 eV). The integrated suboxide XPS response for the nitrided interface is larger than that of the non-nitrided interface; however, after subtraction of the Si–N contribution, the actual suboxide fraction is reduced.

From the combination of XPS studies and electrical measurements, it is, therefore, concluded that the incorporation of the nitrogen at the Si–SiO_2 interface leads to reduced interfacial suboxide bonding, and that this modified interface structure leads to reductions in both FN and direct tunneling. A model based on the XPS data that includes quantitative differences between the suboxide transition regions of nitrided and non-nitrided interfaces has been discussed in Ref. 29. This model tunneling calculation accounts for the reductions in both FN and direct tunneling that have been discussed above.

B. Incorporation of nitrogen on the top surface of an oxide: The "*O–N*" *structure*

Processing for the "*O–N*" *structure* employed steps 1, 3, 4, and 5 of the process sequence in Fig. 2. Figure 14 shows on-line AES data from (i) bulk oxide deposition followed by the 900 °C anneal (oxide thickness, t_{ox}~4.0 nm) and (ii)–(vii) the top surface N_2/He plasma process at 0.1 Torr for exposure times from 1 to 30 min.[30] As the N_2/He plasma exposure time was increased, (i) the N_{KLL} Auger peak at ~379 eV increased and (ii) the Si_{LVV} feature (Si–O, at ~76 eV) and O_{KLL} feature at ~510 eV decreased. This demonstrates that a longer N_2/He plasma exposure time resulted in increased top surface nitrogen incorporation. Based on these AES spectra, we can estimate the atomic concentration of nitrogen [N] using the following equation:

$$[N]=\frac{\frac{I_N}{S_N}}{\frac{I_{Si}}{S_{Si}}+\frac{I_N}{S_N}+\frac{I_O}{S_O}}\times 100\ (\text{at. \%}), \qquad (1)$$

where I_N, I_{Si} and I_O are AES intensities[31] of N, Si, and O, respectively and S_N, S_{Si}, and S_O are relative sensitivity factors for N, Si, and O,[32] respectively.

Figure 15 displays [N] as a function of N_2/He plasma nitridation time, t_N (min). [N] increases with time and tends to saturate with increasing exposure time t_N. The data fit the following *pseudo-first-order* reaction relationship:

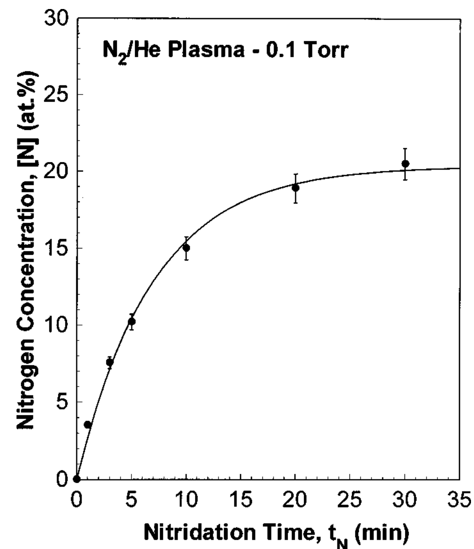

FIG. 15. Nitrogen concentration [N] as a function of N_2/He plasma nitridation time t_N.

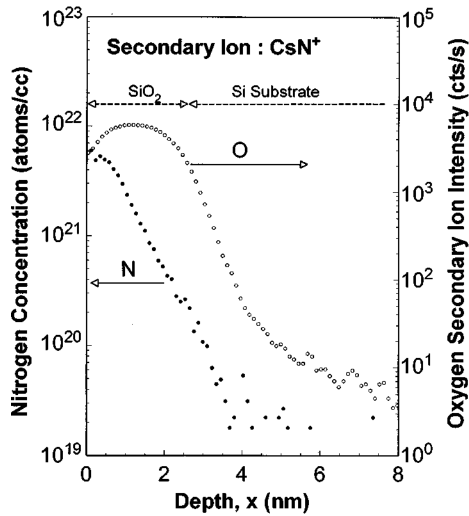

FIG. 16. SIMS depth profiles of top surface nitridation. Nitridation time was 10 min. Total oxide thickness was ~3 nm. The detected secondary ions were CsN^+.

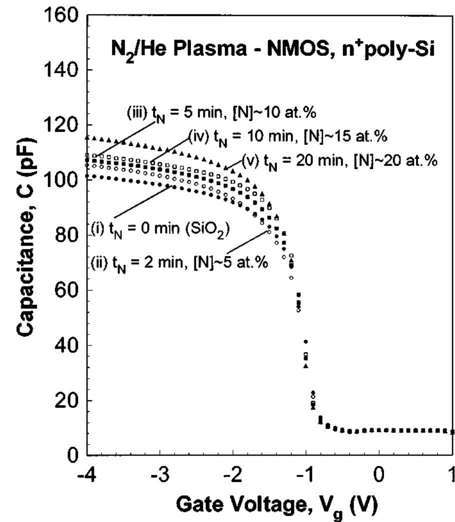

FIG. 17. High-frequency (1 MHz) $C-V$ traces for (i) devices with no nitrogen on top oxide surface, and (ii)–(v) devices with 2–20 min N_2/He nitridation of the top surface of the oxide. Equivalent oxide (electrical) thickness decreased with increasing top nitridation time. The gate electrode was phosphorous-implanted n^+ poly-Si.

$$[\mathrm{N}]=20.4\{1-\exp(-0.14t_{\mathrm{N}})\}\ (\mathrm{at.}\,\%), \tag{2}$$

where 20.4 is the concentration (at. %) at long exposure times, and 0.14 is proportional to the reaction rate (min^{-1}). The saturation value of 20.4 at. % is consistent with the nitrogen being incorporated into a Si_3N_4 layer that is of the order of 2 molecular layers thick, ~0.8 nm, or alternatively, has a nitrogen areal density of $\sim 4-5\times 10^{15}$ atoms cm^{-2}.

The nitrogen confinement on the top surface of the oxide was confirmed using SIMS. Figure 16 displays the SIMS depth profiles for N and O species for the 10 min top surface nitridation of a 3.0-nm-thick RPECVD oxide film. The profile indicates that the nitrogen was confined near the top surface region, and did not penetrate to the Si–SiO_2 interface. This confinement was confirmed by fabricating an *n*-channel metal–oxide–semiconductor (NMOS) capacitor with an n^+ poly-Si gate electrode. A previously published study of top surface nitridation by remote plasma processing used ARXPS to demonstrate confinement of nitrogen to the top surface of the dielectric film.[30]

Figure 17 shows high-frequency (1 MHz) $C-V$ measurements on (i) a device with a control oxide and not subjected to top surface nitridation, and (ii)–(v) devices in which the control oxide was subjected to top surface plasma-assisted nitridation for periods of 2–20 min. The initial oxide thickness before nitridation was approximately 3.3 nm. As shown in Fig. 17, top oxide surface nitridation did not change the flatband voltage. This is consistent with nitrogen being incorporated only at the top surface of the oxide film and not penetrating through to the Si–SiO_2 interface. However, as the N_2/He nitridation time was increased, the capacitance in the accumulation region was increased. This means that the equivalent oxide thickness decreased as the N_2/He plasma exposure time increased. Since the dielectric constant of Si_3N_4 is about two times that of SiO_2, this decrease in equivalent oxide thickness reduction is attributed to the top surface of the oxide layer being converted in a Si_3N_4 layer. The as-deposited oxide physical thickness is 3.3 nm and the equivalent oxide thickness is 3.3 nm as well. If 0.4 nm of the oxide is converted to the ~0.4 nm Si_3N_4 layer, the total equivalent oxide thickness would be reduced ~3.1 nm. Similarly, if the 0.8 nm oxide layer is converted to 0.8 nm of Si_3N_4, the total equivalent oxide thickness would be ~2.9 nm. Note that the physical thickness is not significantly changed by the top surface nitridation process, which effects primarily the electrical thickness determined from the capacitance. These assumptions regarding the conversion of top surface oxide to nitride agree with the experimental $C-V$ data, and are consistent with the SIMS data as well. Approximately one-molecular layer of Si_3N_4 is formed on the oxide after the 10 min nitridation and two-molecular layers of Si_3N_4 are formed on the oxide after the 20 min nitridation.

The heavily nitrided layer on the top surface of the oxide is an effective boron diffusion barrier for PMOS devices with boron-doped p^+ poly-Si gate electrodes. Boron penetration to the Si–SiO_2 interface is easily detected by fabricating PMOS capacitors with boron-doped p^+ poly-Si gate electrodes on *n*-type Si substrates and monitoring the flatband voltage shift via the $C-V$ technique.[33] Boron diffusion from the p^+ poly-Si gate electrode into the Si substrate results in a large *positive* flatband voltage shift, typically ~0.5 V.

Figure 18 shows the flatband voltage for PMOS devices with (i) an oxide gate dielectric as a control sample and (ii)–(v) oxides subjected to 2–20 minute N_2/He plasma top surface nitridation, which correspond to 5–20 at. % of nitrogen incorporation at the top surface of the oxide. The flatband voltages were determined by analysis of high-frequency $C-V$ data. Unlike the NMOS with n^+ poly-Si gate-electrode devices, large flatband voltage shifts are obtained. Compared to the flatband voltage of the oxide subjected to the 20 min nitridation (~20 at. % of nitrogen), which displayed a flatband voltage of 0.74 ± 0.03 V, the flat-

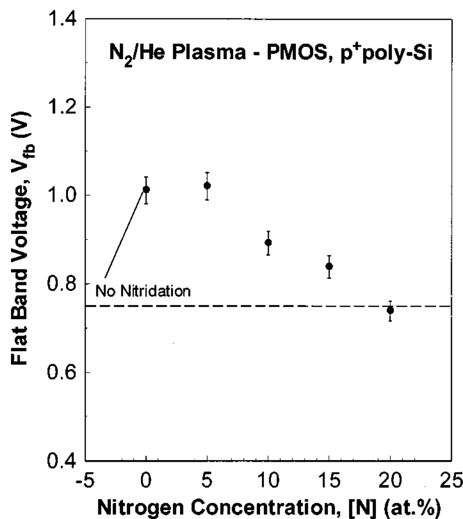

FIG. 18. Flatband voltage shift as a function of nitrogen concentration [N]. The flatband voltage was determined by the high-frequency $C-V$ method. The gate electrode was boron-implanted p^+ poly-Si.

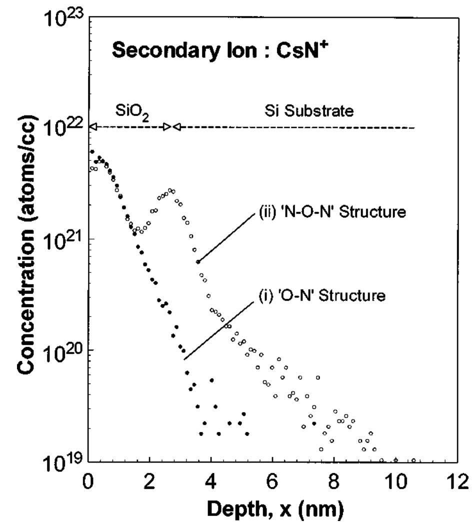

FIG. 19. SIMS depth profiles of (i) the ''*O–N*'' *structure* (10 min top nitridation only) and (ii) ''*N–O–N*'' *structure* (90 s interfacial nitridation and 10 min top nitridation) samples. The total oxide thickness was ~3 nm. The detected secondary ions were CsN^+.

band voltages of the samples with less than 20 at. % of nitrogen at the top surface of the oxide were shifted toward more positive voltages due to boron penetration into the $Si–SiO_2$ interfacial region. This means that less than 20 at. % of nitrogen at the top surface of the oxide did not effectively prevent boron penetration into the interface. The flatband voltage of the device in which the oxide was subjected to a 20 min plasma nitridation was at a voltage consistent with the doping densities of the p^+ poly-Si and the substrate, indicating that 20 at. % nitrogen, or equivalently, ~0.8 nm of Si_3N_4 was effective in completely suppressing the boron transport out of the p^+ poly-Si during the dopant activation anneal. This thickness for effective suppression of boron atom transport is the same as that determined in another series of experiments in which RPECVD nitride layers were deposited onto the top surface of oxide gate dielectrics.[34]

C. Incorporation of nitrogen at the $Si–SiO_2$ interface and at the top surface of an oxide to form an ''*N–O–N*'' *structure*

In this section, it is demonstrated that the combination of interfacial nitridation and top surface nitridation discussed in the previous two sections can be used to fabricate ''*N–O–N*'' *dielectrics* for PMOS devices with p^+ poly-Si gate electrodes. Processing for the ''*N–O–N*'' *structure* is illustrated in Fig. 2. The times were zero (control sample) and 90 s for the interfacial nitridation process, and 20 min for the top surface nitridation. The nitrogen concentration at the $Si–SiO_2$ interface and on the top surface of the oxide were $\sim 7–8\times 10^{14}$ and $\sim 4-5\times 10^{15}$ cm^{-2}, respectively, and corresponding to approximately 1 *monolayer* of nitrogen at the $Si–SiO_2$ interface, and *two-molecular* layers of Si_3N_4 at the top surface of the oxide.

SIMS depth profiling was used to characterize the nitrogen distribution in the thin oxide films. The control sample has an ''*O–N*'' *structure* with nitrogen incorporated only at the top surface via a 10 min N_2/He plasma nitridation. The other sample has a ''*N–O–N*'' *structure*, which is described in Fig. 2. The total thickness of each sample for SIMS was ~3.0 nm. Figure 19 shows the SIMS nitrogen profiles obtained by detection of CsN^+ ions. The sample with the ''*N–O–N*'' *structure* displays two separated and distinct peaks; one is at the $Si–SiO_2$ interface and the other is at the top surface of the oxide, whereas the sample with the ''*O–N*'' *structure* displays only the top surface nitrogen peak. As in the other SIMS profiles, the widths of the nitrogen features are an artifact of the SIMS analysis technique.

These interfacial and top oxide surface nitridation processes have been combined for the fabrication of PMOS capacitors with boron-doped p^+ poly-Si gate electrodes. The equivalent oxide thickness for each device was ~2.5 nm. The dielectric film thickness was determined by the high-frequency $C-V$ method. We used two samples; (i) one in which only top oxide surface nitridation was used to form the ''*O–N*'' dielectric and (ii) a second in which interfacial and top surface nitridation were combined to form the ''*N–O–N*'' dielectric.

The flatband voltages of the devices with ''*O–N*'' and ''*N–O–N*'' *structure* dielectrics were essentially the same, $\sim 0.74\pm 0.02$ V. As we already noted in Sec. III A, interfacial nitrogen does not shift the flatband voltage from the value determined by substrate and poly-Si doping. However, if boron were to diffuse into the Si substrate, the flatband voltage would have been shifted to more positive values. The analysis of the $C-V$ traces indicates both flatband voltages are the same, and with 0.05 V of a flatband voltage calculated from the respective substrate and gate electrode doping. This demonstrates that (i) the top surface nitride layer effectively suppressed boron diffusion in both samples and (ii) the interfacial nitride layer did not effect the flatband voltage shift for the ''*N–O–N*'' *structure* sample.

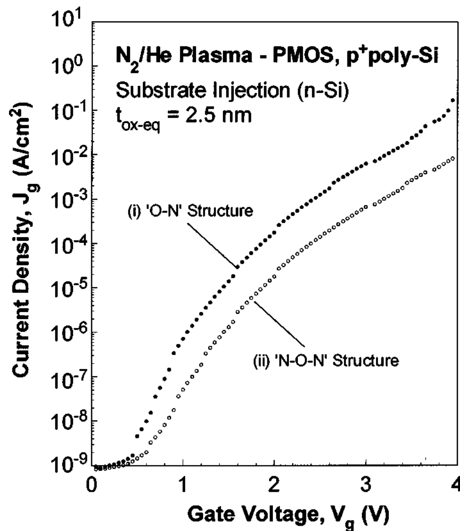

FIG. 20. Substrate injection mode (gate electrode biased positively) $J-V$ traces for devices with a 2.5-nm-thick gate oxide on n-Si(100), demonstrating effects of the monolayer of interfacial nitrogen in reducing tunnel currents in direct tunneling region. The gate electrode was boron-doped p^+ poly-Si.

In Sec. III A, we demonstrated a reduction in tunneling current with interfacial nitridation. This same effect is shown in Fig. 20, i.e., due to the interfacial nitrogen, the tunneling current in the device with the ''$N-O-N$'' *dielectric* is reduced compared with the current in the sample without the interfacial nitrogen in the device with the ''$O-N$'' *dielectric*. The magnitude of the tunneling current reduction in Fig. 20 is about the same as the reductions associated with interface nitridation for p-type substrates and n^+ poly-Si gate electrodes, as shown in Fig. 10. This experiment demonstrates that top surface nitridation suppresses boron diffusion at the top surface of the oxide, and interfacial nitrogen reduces the tunnel current, and that there is no *interference* between these two nitridation processes.

IV. CONCLUSIONS

We have demonstrated that the ''$N-O-N$'' *structure* for ultrathin gate dielectrics has (i) approximately 1 ML of nitrogen atoms at the $Si-SiO_2$ interface and (ii) approximately two molecular layers of silicon nitride at the top surface of the oxide. It is difficult to relate the interfacial nitridation in monolayers, or nitrogen atoms cm^{-2} to a percentage since this requires additional quantification of previously published SIMS data, as for example, in Refs. 9–11. We have fabricated this ''$N-O-N$'' *structure* using a combination of low thermal budget remote plasma and RTA processing, specifically, by employing the interfacial and top surface nitridation processes described above. For the interface formation, we used the two-step interface formation process discussed in Sec. III A, and for the top nitridation, we used the process discussed in Sec. III B. We observed two separate nitrogen peaks at the $Si-SiO_2$ interface and top surface using SIMS analysis. The ''$N-O-N$'' *structure* was incorporated into PMOS devices with p^+ poly-Si gate electrodes that demonstrated: (i) effective suppression of boron diffusion from the degenerately doped p^+ poly-Si gate electrode and (ii) an order of magnitude reduction of the direct tunneling current. This ''$N-O-N$'' *structured* gate dielectric satisfies many of the electrical properties required for aggressively scaled MOSFET devices.

Finally, the quality of electrical quality of the monolayer nitrided interfaces is consistent with the extension of constraint theory to Si–dielectric interfaces, as developed in Ref. 35. The results of Ref. 35 indicate that an average number of bonds/atom in the interfacial region between crystalline Si and the noncrystalline dielectric must be less than about 3, an empirical demarcation level between device quality on the low side of 3, as for $Si-SiO_2$ (~ 2.8), and increasing defective interfaces on the high side, as for $Si-Si_3N_4$ (~ 3.5). In contrast, the average number of bonds/atom at a monolayer nitrided interface of the type described in this article is essentially the same as at a $Si-SiO_2$ interface, ~ 2.8, so that device-quality interfaces are anticipated and indeed observed for monolayer-level interface nitridation.

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