

MONOLITHIC PHASE-LOCKED LOOPS AND CLOCK RECOVERY CIRCUITS

THEORY AND DESIGN

Edited by

Behzad Razavi

AT&T Bell Laboratories



The Institute of Electrical and Electronics Engineers, Inc., New York



A JOHN WILEY & SONS, INC., PUBLICATION

Contents

PREFACE	ix
Design of Monolithic Phase-Locked Loops and Clock Recovery Circuits—A Tutorial B. Razavi (<i>Original Paper</i>).	1
PART 1 BASIC THEORY	41
Theory of AFC Synchronization W. J. Gruen (<i>Proceedings of the IRE</i> , August 1953).	43
Color-Carrier Reference Phase Synchronization Accuracy in NTSC Color Television D. Richman (<i>Proceedings of the IRE</i> , January 1954).	49
Charge-Pump Phase-Locked Loops F. M. Gardner (<i>IEEE Transactions on Communications</i> , November 1980).	77
z-Domain Model for Discrete-Time PLLs J. P. Hein and J. W. Scott (<i>IEEE Transactions on Circuits and Systems</i> , November 1988).	87
Analyze PLLs with Discrete Time Modeling J. Kovacs (<i>Microwaves & RF</i> , May 1991).	94
Properties of Frequency Difference Detectors F. M. Gardner (<i>IEEE Transactions on Communications</i> , February 1985).	99
Frequency Detectors for PLL Acquisition in Timing and Carrier Recovery D. G. Messerschmitt (<i>IEEE Transactions on Communications</i> , September 1979).	107
Analysis of Phase-Locked Timing Extraction Circuits for Pulse Code Transmission E. Roza (<i>IEEE Transactions on Communications</i> , September 1974).	115
Optimization of Phase-Locked Loop Performance in Data Recovery Systems R. S. Co and J. H. Mulligan, Jr. (<i>IEEE Journal of Solid-State Circuits</i> , September 1994).	129
Noise Properties of PLL Systems V. F. Kroupa (<i>IEEE Transactions on Communications</i> , October 1982).	142
PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design B. Kim, T. C. Weigandt, and P. R. Gray (<i>Proceedings of the International Symposium on Circuits and Systems</i> , June 1994).	151
Practical Approach Augurs PLL Noise in RF Synthesizers M. O'Leary (<i>Microwaves & RF</i> , September 1987).	155
The Effects of Noise in Oscillators E. Hafner (<i>Proceedings of the IEEE</i> , February 1966)	160
A Simple Model of Feedback Oscillator Noise Spectrum D. B. Leeson (<i>Proceedings of the IEEE</i> , February 1966).	180
Noise in Relaxation Oscillators A. A. Abidi and R. G. Meyer (<i>IEEE Journal of Solid-State Circuits</i> , December 1983).	182
Analysis of Timing Jitter in CMOS Ring Oscillators T. C. Weigandt, B. Kim, and P. R. Gray (<i>Proceedings of the International Symposium on Circuits and Systems</i> , June 1994).	191
Analysis, Modeling, and Simulation of Phase Noise in Monolithic Voltage-Controlled Oscillators B. Razavi (<i>Proceedings of the Custom Integrated Circuits Conference</i> , May 1995).	195

PART 2	BUILDING BLOCKS	199
Start-up and Frequency Stability in High-Frequency Oscillators	N. M. Nguyen and R. G. Meyer (<i>IEEE Journal of Solid-State Circuits</i> , May 1992).	201
MOS Oscillators with Multi-Decade Tuning Range and Gigahertz Maximum Speed	M. Banu (<i>IEEE Journal of Solid-State Circuits</i> , April 1988).	211
A Bipolar 1 GHz Multi-Decade Monolithic Variable-Frequency Oscillator	J. T. Wu (<i>International Solid-State Circuit Conference Digest of Technical Papers</i> , February 1991).	219
A Digital Phase and Frequency Sensitive Detector	J. I. Brown (<i>Proceedings of the IEEE</i> , April 1971).	222
A 3-State Phase Detector Can Improve Your Next PLL Design	C. A. Sharpe (<i>EDN Magazine</i> , September 1976).	224
GaAs Monolithic Phase/Frequency Discriminator	I. Shahriary et al. (<i>IEEE Gallium Arsenide Integrated Circuits Symposium Digest of Technical Papers</i> , October 1985).	229
A New Phase-Locked Loop Timing Recovery Method for Digital Regenerators	J. A. Bellisio (<i>IEEE International Communications Conference Recording</i> , June 1976).	233
A Phase-Locked Loop with Digital Frequency Comparator for Timing Signal Recovery	J. A. Afonso, A. J. Quiterio, and D. S. Arantes (<i>National Telecommunications Conference Recording</i> , 1979).	237
Clock Recovery from Random Binary Signals	J. D. H. Alexander (<i>Electronics Letters</i> , October 1975).	242
A Si Bipolar Phase and Frequency Detector IC for Clock Extraction up to 8 Gb/s	A. Pottbacker, U. Langmann, and H. U. Schreiber (<i>IEEE Journal of Solid-State Circuits</i> , December 1992).	244
A Self-Correcting Clock Recovery Circuit	C. R. Hogge (<i>IEEE Journal of Lightwave Technology</i> , December 1985).	249
PART 3	MODELING AND SIMULATION	253
An Integrated PLL Clock Generator for 275 MHz Graphic Displays	G. Gutierrez and D. DeSimone (<i>Proceedings of the Custom Integrated Circuits Conference</i> , May 1990).	255
The Macro Modeling of Phase-Locked Loops for the SPICE Simulator	M. Sitkowski (<i>IEEE Circuits and Devices Magazine</i> , March 1991).	259
Modeling and Simulation of an Analog Charge Pump Phase-Locked Loop	S. Can and Y. E. Sahinkaya (<i>Simulation</i> , April 1988).	264
Mixed-Mode Simulation of Phase-Locked Loops	B. A. A. Antao, F. M. El-Turky, and R. H. Leonowich (<i>Proceedings of the Custom Integrated Circuits Conference</i> , May 1993).	270
Behavioral Representation for VCO and Detectors in Phase-Lock Systems	E. Liu and A. L. Sangiovanni-Vincentelli (<i>Proceedings of the Custom Integrated Circuits Conference</i> , May 1992).	274
Behavioral Simulation Techniques for Phase/Delay-Locked Systems	A. Demir, E. Liu, and A. L. Sangiovanni-Vincentelli (<i>Proceedings of the Custom Integrated Circuits Conference</i> , May 1994).	278
PART 4	PHASE-LOCKED LOOPS	283
A Monolithic Phase-Locked Loop with Detection Processor	E. N. Murthi (<i>IEEE Journal of Solid State Circuits</i> , February 1979).	285
A 200-MHz CMOS Phase-Locked Loop with Dual Phase Detectors	K. M. Ware, H.-S. Lee, and C. G. Sodini (<i>IEEE Journal of Solid-State Circuits</i> , December 1989).	292
High-Frequency Phase-Locked Loops in Monolithic Bipolar Technology	M. Soyuer and R. G. Meyer (<i>IEEE Journal of Solid-State Circuits</i> , June 1989).	301
A 6-GHz Integrated Phase-Locked Loop Using AlGaAs/GaAs Heterojunction Bipolar Transistors	A. W. Buchwald, et al. (<i>IEEE Journal of Solid-State Circuits</i> , December 1992).	310

A 6-GHz 60-mW BiCMOS Phase-Locked Loop with 2-V Supply	320
B. Razavi and J. Sung (<i>IEEE Journal of Solid-State Circuits</i> , December 1994).	
Design of PLL-Based Clock Generation Circuits	326
D. K. Jeong, et al. (<i>IEEE Journal of Solid-State Circuits</i> , April 1987).	
A Variable Delay Line PLL for CPU-Coprocessor Synchronization	333
M. G. Johnson and E. L. Hudson (<i>IEEE Journal of Solid-State Circuits</i> , October 1988).	
A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors	339
I. A. Young, J. K. Greason, and K. L. Wong (<i>IEEE Journal of Solid-State Circuits</i> , November 1992).	
A Wide-Bandwidth Low-Voltage PLL for PowerPC Microprocessors	347
J. Alvarez", et al. (<i>IEEE Journal of Solid-State Circuits</i> , April 1995).	
A 30-128 MHz Frequency Synthesizer Standard Cell	355
R. F. Bitting and W. P. Repasky (<i>Proceedings of the Custom Integrated Circuits Conference</i> , May 1992).	
Cell-Based Fully Integrated CMOS Frequency Synthesizers	361
D. Mijuskovic, et al. (<i>IEEE Journal of Solid-State Circuits</i> , March 1994).	
Fully-Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ± 50 psec Jitter	369
I. Novof, et al. (<i>International Solid-State Circuit Conference Digest of Technical Papers</i> , February 1995).	
PLL Design for a 500 MB/s Interface	377
M. Horowitz, et al. (<i>International Solid-State Circuit Conference Digest of Technical Papers</i> , February 1993).	
PART 5 CLOCK AND DATA RECOVERY CIRCUITS	381
An Analog PLL-Based Clock and Data Recovery Circuit with High Input Jitter Tolerance	383
S. Y. Sun (<i>IEEE Journal of Solid-State Circuits</i> , April 1989).	
A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2- μ m CMOS	389
B. Kim, D. N. Helman, and P. R. Gray (<i>IEEE Journal of Solid-State Circuits</i> , December 1990).	
A BiCMOS PLL-Based Data Separator Circuit with High Stability and Accuracy	399
S. Miyazawa, et al. (<i>IEEE Journal of Solid-State Circuits</i> , February 1991).	
A Versatile Clock Recovery Architecture and Monolithic Implementation	405
L. De Vito (<i>Invited Paper</i>).	
A 155-MHz Clock Recovery Delay- and Phase-Locked Loop	421
T. H. Lee and J. F. Bulzacchelli (<i>IEEE Journal of Solid-State Circuits</i> , December 1992).	
A Monolithic 156 Mb/s Clock and Data Recovery PLL Circuit using the Sample-and-Hold Technique	431
N. Ishihara and Y. Akazawa (<i>IEEE Journal of Solid-State Circuits</i> , December 1994).	
A Monolithic 480 Mb/s Parallel AGC/Decision/Clock Recovery Circuit in 1.2- μ m CMOS	437
T. H. Hu and P. R. Gray (<i>IEEE Journal of Solid-State Circuits</i> , December 1993).	
A Monolithic 622 Mb/sec Clock Extraction and Data Retiming Circuit	444
B. Lai and R. C. Walker (<i>International Solid-State Circuit Conference Digest of Technical Papers</i> , February 1991).	
A 660 Mb/s CMOS Clock Recovery Circuit with Instantaneous Locking for NRZ Data and Burst-Mode Transmission	447
M. Banu and A. Dunlop (<i>International Solid-State Circuit Conference Digest of Technical Papers</i> , February 1993).	
A Monolithic 2.3-Gb/s 100-mW Clock and Data Recovery Circuit in Silicon Bipolar Technology	450
M. Soyuer (<i>IEEE Journal of Solid-State Circuits</i> , December 1993).	
A 50 MHz Phase- and Frequency-Locked Loop	454
R. R. Cordell, et al. (<i>IEEE Journal of Solid-State Circuits</i> , December 1979).	
NMOS ICs for Clock and Data Regeneration in Gigabit-per-Second Optical-Fiber Receivers	461
S. K. Enam and A. A. Abidi (<i>IEEE Journal of Solid-State Circuits</i> , December 1992).	
A PLL-Based 2.5-Gb/s Clock and Data Regenerator IC	473
H. Ransijn and P. O'Connor (<i>IEEE Journal of Solid-State Circuits</i> , October 1991).	
A 2.5-Gb/sec 15-mW BiCMOS Clock Recovery Circuit	481
B. Razavi and J. Sung (<i>Symposium on VLSI Circuits Digest of Technical Papers</i> , 1995).	
An 8 GHz Silicon Bipolar Clock Recovery and Data Regenerator IC	483
A. Pottbacker and U. Langmann (<i>IEEE Journal of Solid-State Circuits</i> , December 1994).	

AUTHOR INDEX

SUBJECT INDEX

EDITOR'S BIOGRAPHY